PRELIMINARY | Data Sheet | October 2003 | FN9129

Triple Output Regulator with Single Synchronous Buck and Dual LDO

The ISL6413 is a highly integrated triple output regulator which provides a single chip solution for wireless chipset power management. The device integrates high efficiency synchronous buck regulator with two ultra low noise LDO regulators. The IC accepts an input voltage range of 3.0V to 3.6V and provides three regulated output voltages: 1.8V (PWM), 2.84V (LDO1), and another ultra-clean 2.84V (LDO2).

The Synchronous current mode PWM regulator with integrated N- and P-channel power MOSFET provides pre-set 1.8V for BBP/MAC core supply. Synchronous rectification with internal MOSFETs is used to achieve higher efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on PWM output.

The ISL6413 also has two LDO regulators which use an internal PMOS transistor as the pass device. LDO2 features ultra low noise that does not typically exceed 30µV RMS to aid VCO stability. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6413 also integrates a RESET function, which eliminates the need for additional RESET IC required in WLAN applications. The IC asserts a RESET signal whenever the V_{IN} supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after V_{IN} has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include over current protection for all three outputs and thermal shutdown.

High integration and the thin Quad Flat No-lead (QFN) package makes ISL6413 an ideal choice to power many of today's small form factor industry standard wireless cards such as PCMCIA, mini-PCI and Cardbus-32.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. DWG. #
ISL6413IR	-40 to 85	24 Ld QFN	L24.4x4B

Features

- Fully Integrated Synchronous Buck Regulator + Dual LDO
- High Output Current (For QFN package)
  - PWM, 1.8V 400mA
  - LDO1, 2.84V 300mA
  - LDO2, 2.84V 200mA
- Ultra-Compact DC-DC Converter Design
- Stable with Small Ceramic Output Capacitors
- High conversion efficiency
- Low Shutdown supply current
- Ultra-Low Dropout Voltage for LDOs
  - LDO1, 2.84V . . . . . 125mV (typ.) at 300mA
  - LDO2, 2.84V . . . . . 100mV (typ.) at 200mA
- Ultra-Low Output Voltage Noise
  - <30µV_{RMS} (typ.) for LDO2 (VCO Supply)
- PG_LDO, PG_PWM and $\overline{\text{PG\_PWM}}$ outputs
- Extensive circuit protection and monitoring features
  - Over voltage protection
  - Over current protection
  - Shutdown
  - Thermal Shutdown
- Integrated RESET output for microprocessor reset
- Proven Reference Design for Total WLAN System Solution
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint Improves PCB Efficiency and Is Thinner in Profile

Applications

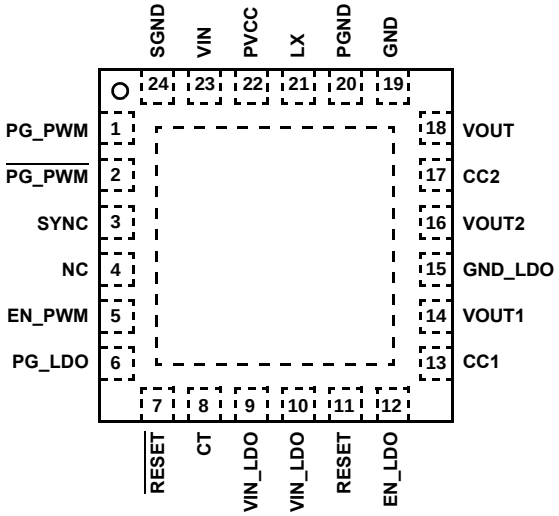
- WLAN Cards
  - PCMCIA, Cardbus32, MiniPCI Cards
  - Compact Flash Cards
- Liberty Chipset
- Hand-Held Instruments

Related Literature

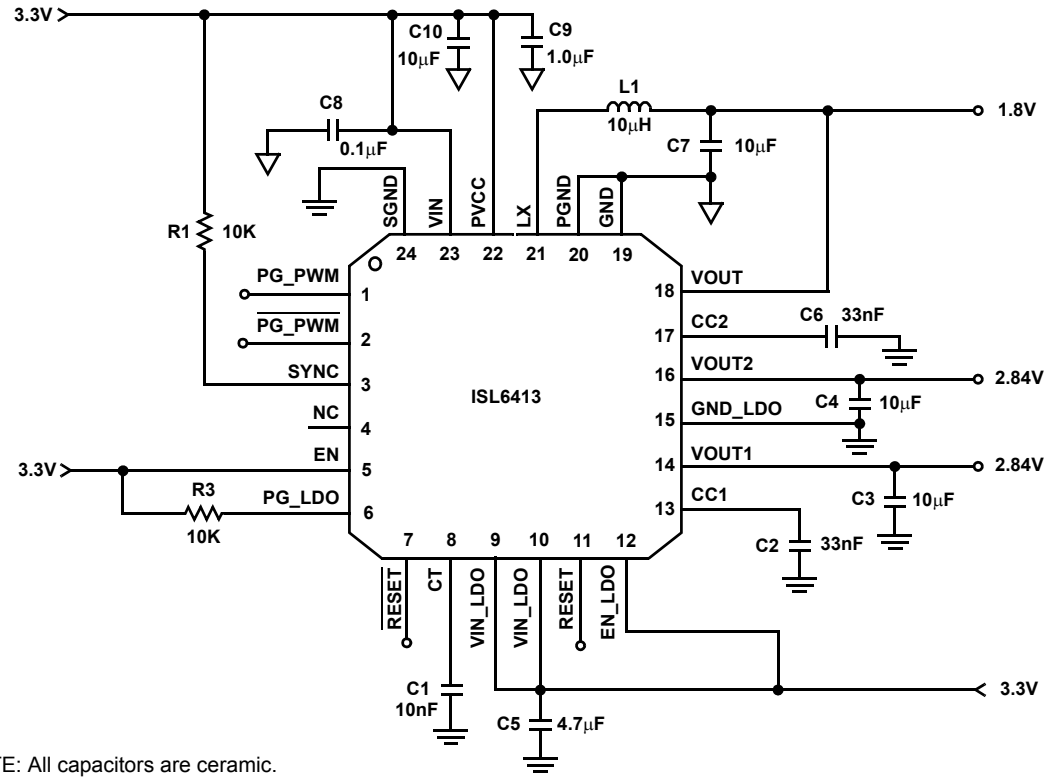
- TB363 - Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)
- TB389 - PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages

Pinout

ISL6413 (QFN)
TOP VIEW

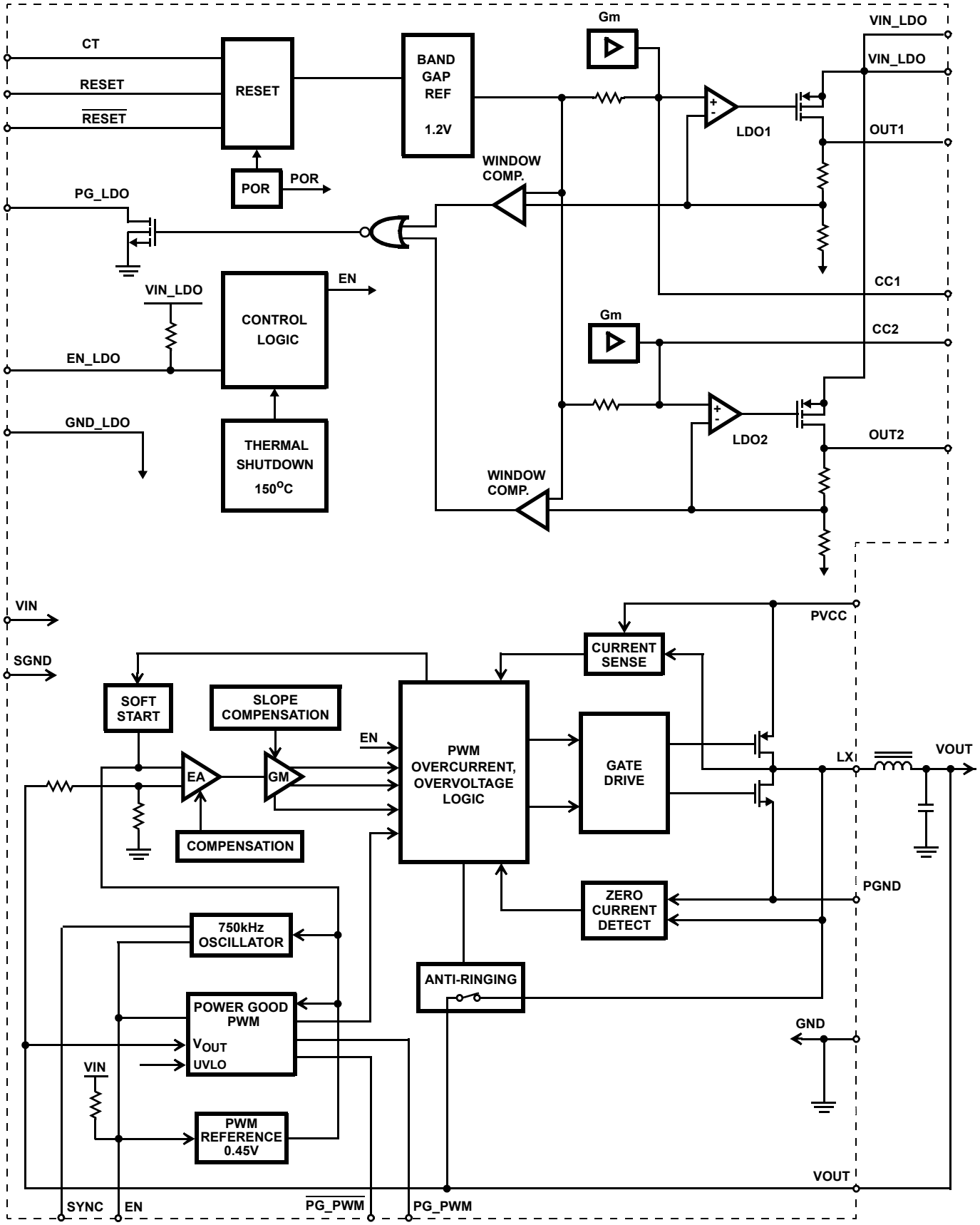


Typical Application Schematic

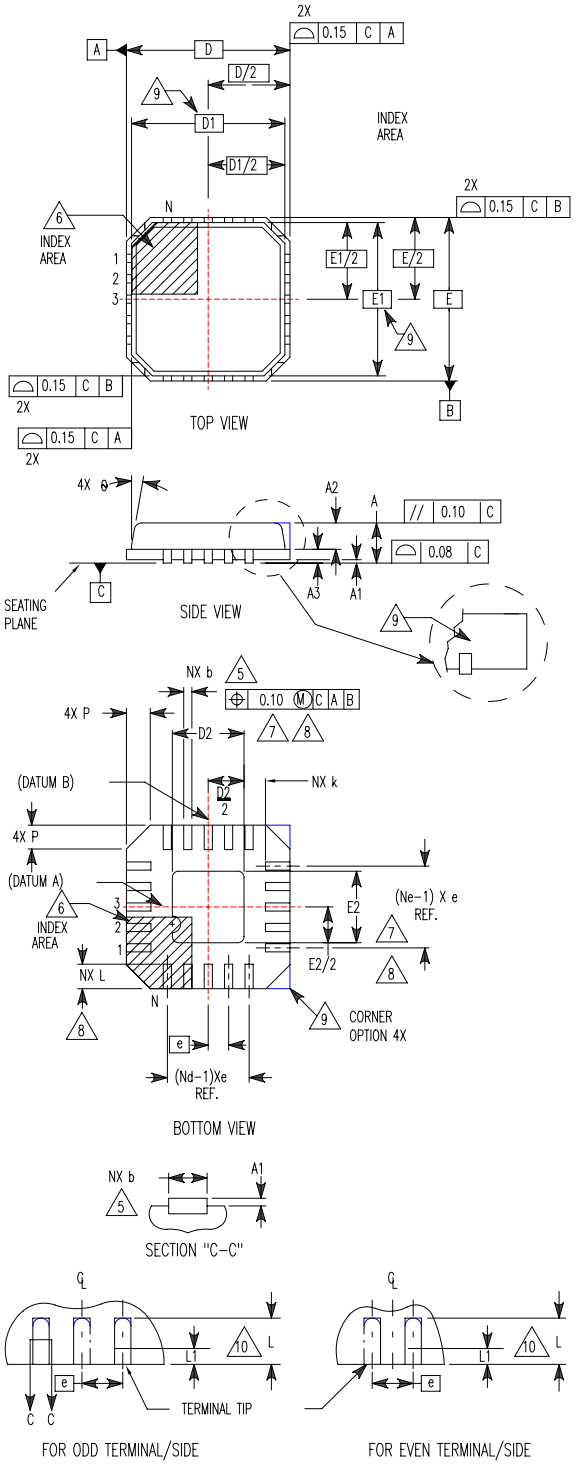


NOTE: All capacitors are ceramic.

Functional Block Diagram



Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L24.4x4B

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.19	2.34	2.49	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.19	2.34	2.49	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		24		2
Nd		6		3
Ne		6		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.