L4949, NCV4949

100 mA, 5.0 V, Low Dropout Voltage Regulator with Reset and Sense

The L4949 is a monolithic integrated 5.0 V voltage regulator with a very low dropout and additional functions such as reset and an uncommitted voltage sense comparator.

It is designed for supplying microcontroller/microprocessor controlled systems particularly in automotive applications.

Features

- Operating DC Supply Voltage Range 5.0 V to 28 V
- Transient Supply Voltage Up to 40 V
- Extremely Low Quiescent Current in Standby Mode
- High Precision Output Voltage 5.0 V ±1%
- Output Current Capability Up to 100 mA
- Very Low Dropout Voltage Less Than 0.4 V
- Reset Circuit Sensing The Output Voltage
- Programmable Reset Pulse Delay
- Voltage Sense Comparator
- Thermal Shutdown and Short Circuit Protections
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These are Pb−Free Devices

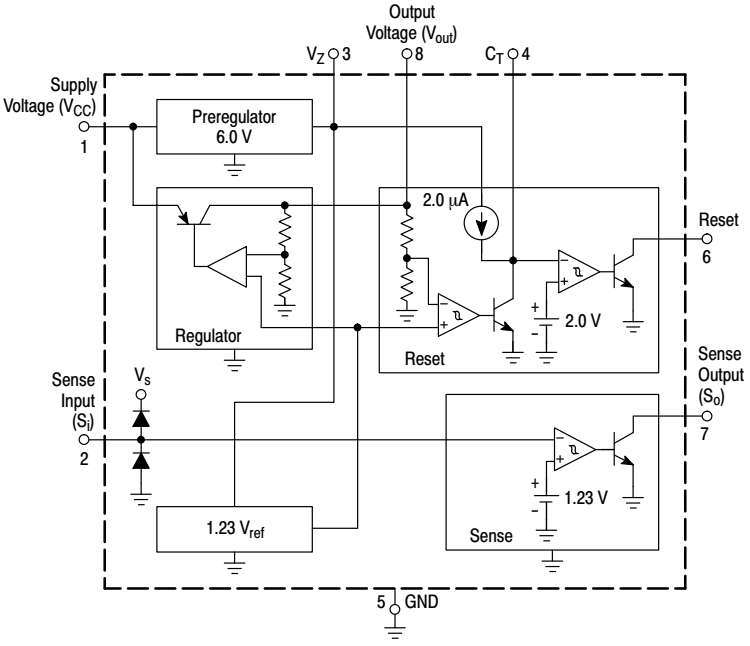

Figure 1. Representative Block Diagram

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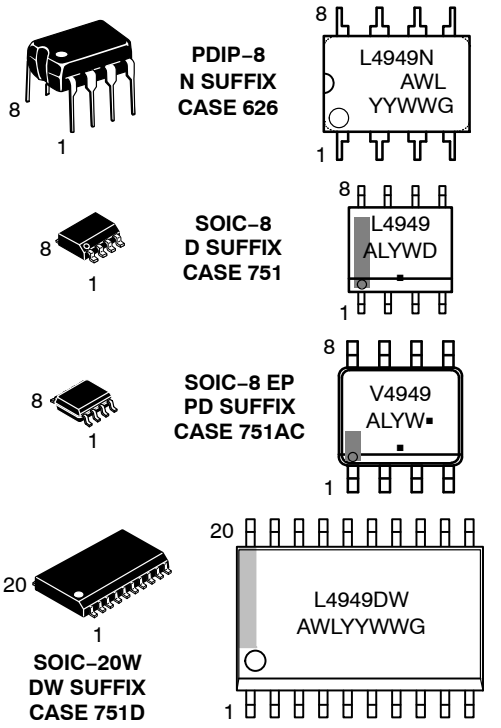
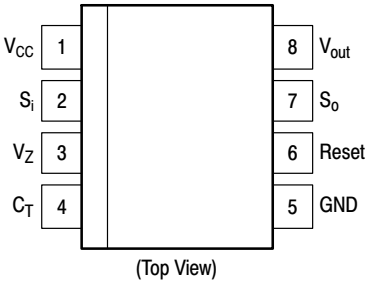
MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Device

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Operating Supply Voltage	V_{CC}	28	V
Transient Supply Voltage (t < 1.0 s)	$V_{CC\ TR}$	40	V
Output Current	I_{out}	Internally Limited	–
Output Voltage	V_{out}	20	V
Sense Input Current	I_{SI}	±1.0	mA
Sense Input Voltage	V_{SI}	V_{CC}	–
Output Voltages Reset Output Sense Output	 V_{Reset} V_{SO}	 20 20	V
Output Currents Reset Output Sense Output	 I_{Reset} I_{SO}	 5.0 5.0	mA
Preregulator Output Voltage	V_Z	7.0	V
Preregulator Output Current	I_Z	5.0	mA
ESD Protection at any pin Human Body Model Machine Model	 – –	 2000 400	V
Thermal Resistance, Junction–to–Air P Suffix, DIP–8 Plastic Package, Case 626 D Suffix, SOIC–8 Plastic Package, Case 751 PD Suffix, SOIC–8 EP Plastic Package, Case 751AC (Note 1) D Suffix, SOIC–20 Plastic Package, Case 751D	$R_{\theta JA}$	 100 200 85 80	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Soldered to a 200 mm^2 1 oz. copper–clad FR–4 board.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, –40°C < T_A < 125°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 1.0 mA)	V_{out}	4.95	5.0	5.05	V
Output Voltage (6.0 V < V_{CC} < 28 V, 1.0 mA < I_{out} < 50 mA)	V_{out}	4.9	5.0	5.1	V
Output Voltage (V_{CC} = 35 V, t < 1.0 s, 1.0 mA < I_{out} < 50 mA)	V_{out}	4.9	5.0	5.1	V
Dropout Voltage I_{out} = 10 mA I_{out} = 50 mA I_{out} = 100 mA	V_{drop}	 – – –	 0.1 0.2 0.3	 0.25 0.40 0.50	V
Input to Output Voltage Difference in Undervoltage Condition (V_{CC} = 4.0 V, I_{out} = 35 mA)	V_{IO}	–	0.2	0.4	V
Line Regulation (6.0 V < V_{CC} < 28 V, I_{out} = 1.0 mA)	Reg_{line}	–	1.0	20	mV
Load Regulation (1.0 mA < I_{out} < 100 mA)	Reg_{load}	–	8.0	30	mV
Current Limit V_{out} = 4.5 V V_{out} = 0 V	I_{Lim}	 105 –	 200 100	 400 –	mA
Quiescent Current (I_{out} = 0.3 mA, T_A < 100°C)	I_{QSE}	–	150	260	μA
Quiescent Current (I_{out} = 100 mA)	I_Q	–	–	5.0	mA

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14 V, −40°C < T_A < 125°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
RESET					
Reset Threshold Voltage	V_{Resth}	–	V_{out} − 0.5	–	V
Reset Threshold Hysteresis @ T_A = 25°C @ T_A = −40 to +125°C	$V_{Resth,hys}$	 50 50	 100 –	 200 300	mV
Reset Pulse Delay (C_T = 100 nF, $t_R \geq$ 100 μs)	t_{ResD}	55	100	180	ms
Reset Reaction Time (C_T = 100 nF)	t_{ResR}	–	5.0	30	μs
Reset Output Low Voltage (R_{Reset} = 10 kΩ to V_{out}, $V_{CC} \geq$ 3.0 V)	V_{ResL}	–	–	0.4	V
Reset Output High Leakage Current (V_{Reset} = 5.0 V)	I_{ResH}	–	–	1.0	μA
Delay Comparator Threshold	V_{CTth}	–	2.0	–	V
Delay Comparator Threshold Hysteresis	$V_{CTth, hys}$	–	100	–	mV
SENSE					
Sense Low Threshold (V_{SI} Decreasing = 1.5 V to 1.0 V)	V_{SOth}	1.16	1.23	1.35	V
Sense Threshold Hysteresis	$V_{SOth,hys}$	20	100	200	mV
Sense Output Low Voltage ($V_{SI} \leq$ 1.16 V, $V_{CC} \geq$ 3.0 V, R_{SO} = 10 kΩ to V_{out})	V_{SOL}	–	–	0.4	V
Sense Output Leakage (V_{SO} = 5.0 V, $V_{SI} \geq$ 1.5 V)	I_{SOH}	–	–	1.0	μA
Sense Input Current	I_{SI}	−1.0	0.1	1.0	μA
PREREGULATOR					
Preregulator Output Voltage (I_Z = 10 μA)	V_Z	–	6.3	–	V

PIN FUNCTION DESCRIPTION

Pin SOIC−8, PDIP−8	Pin SOIC−8 EP	Pin SOIC−20W	Symbol	Description
1	1	19	V_{CC}	Supply Voltage
2	2	20	S_i	Input of Sense Comparator
3	3	1	V_Z	Output of Preregulator
4	4	2	C_T	Reset Delay Capacitor
5	5	4 – 7, 14 – 17	GND	Ground
6	6	10	Reset	Output of Reset Comparator
7	7	11	S_O	Output of Sense Comparator
8	8	12	V_{out}	Main Regulator Output
–	–	3, 8, 9, 13, 18	NC	No Connect
–	EPAD	–	EPAD	Connect to Ground potential or leave unconnected

TYPICAL CHARACTERIZATION CURVES

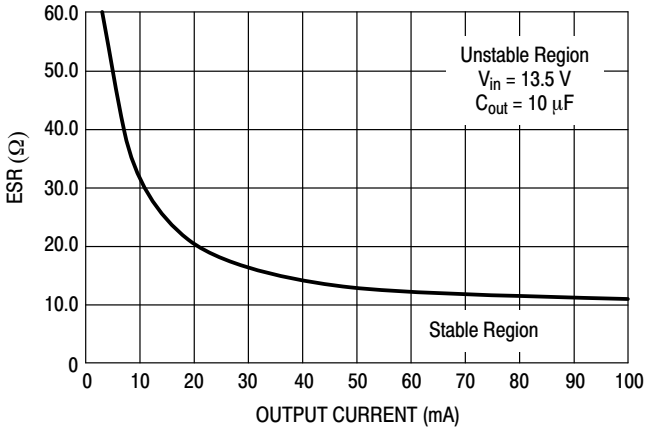


Figure 2. ESR Stability Border Vs. Output Current (Full ESR Range)

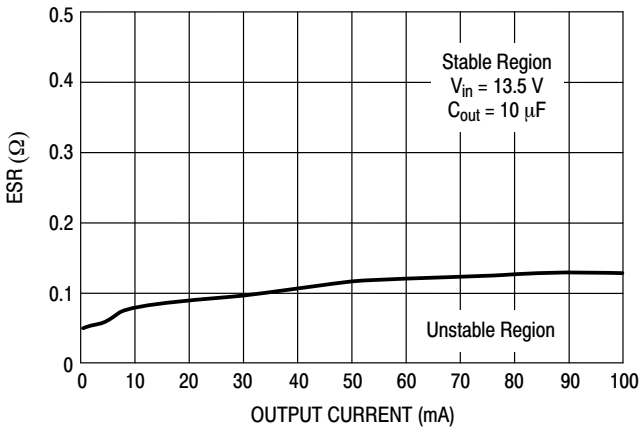


Figure 3. ESR Stability Border Vs. Output Current (Very Low ESR)

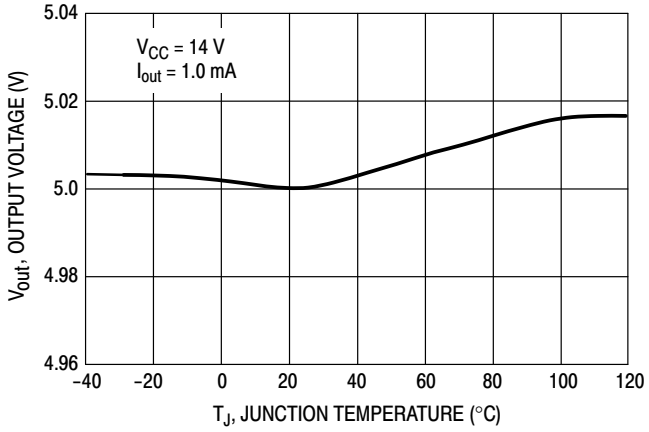


Figure 4. Output Voltage versus Junction Temperature

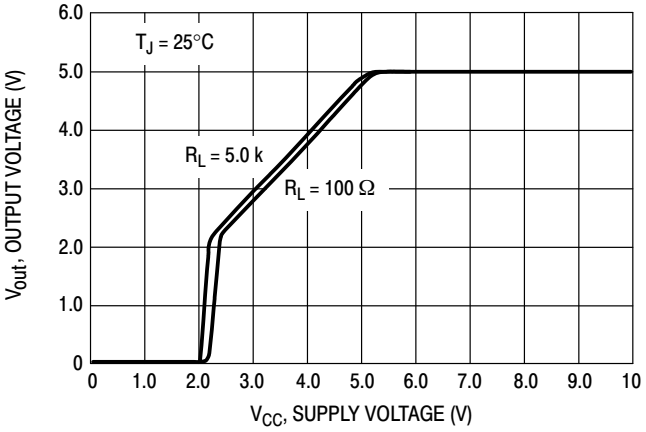


Figure 5. Output Voltage versus Supply Voltage

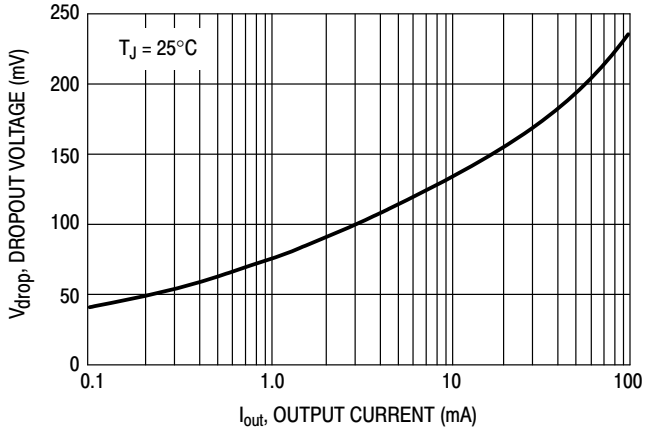


Figure 6. Dropout Voltage versus Output Current

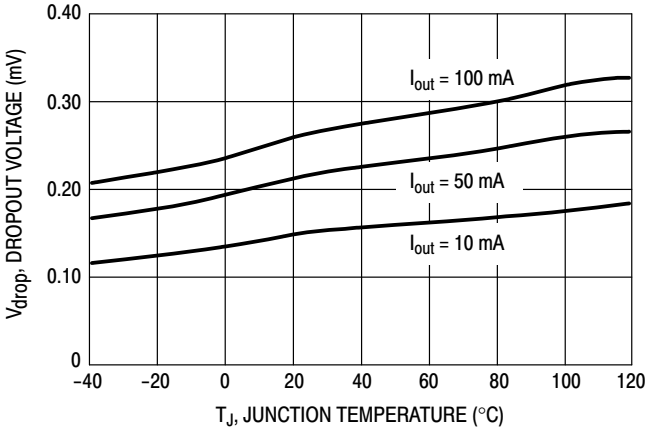


Figure 7. Dropout Voltage versus Junction Temperature

TYPICAL CHARACTERIZATION CURVES (continued)

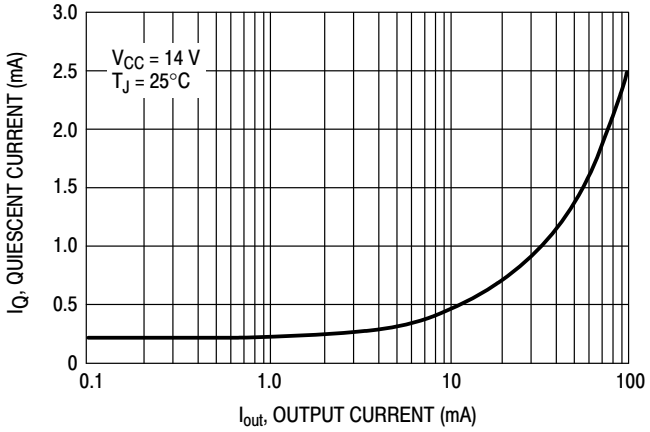


Figure 8. Quiescent Current versus Output Current

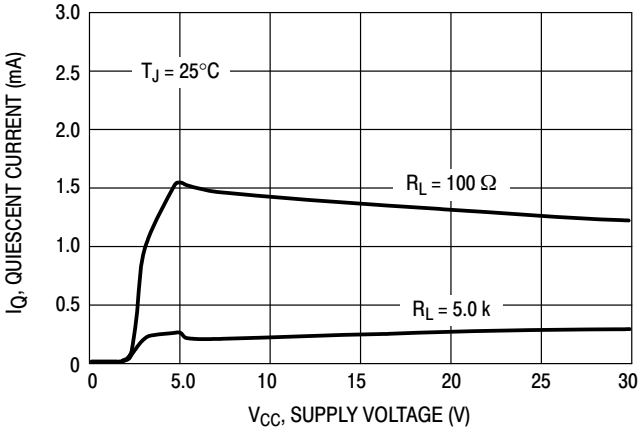


Figure 9. Quiescent Current versus Supply Voltage

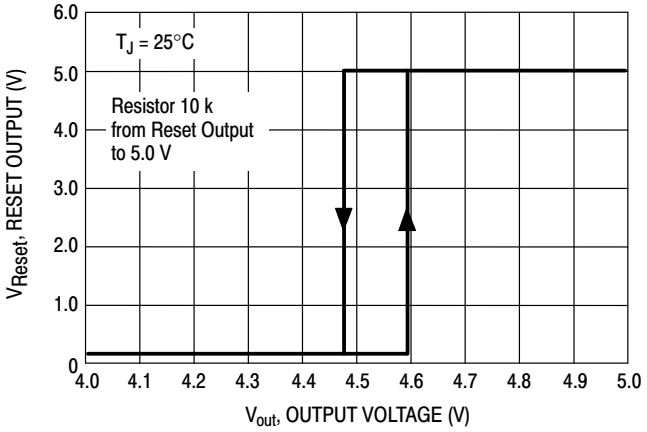


Figure 10. Reset Output versus Regulator Output Voltage

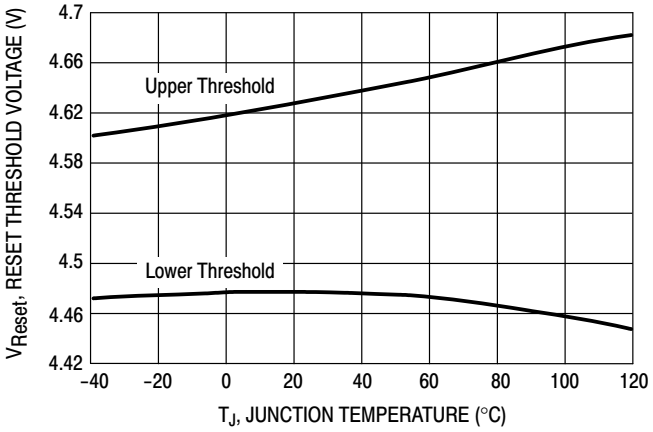


Figure 11. Reset Thresholds versus Junction Temperature

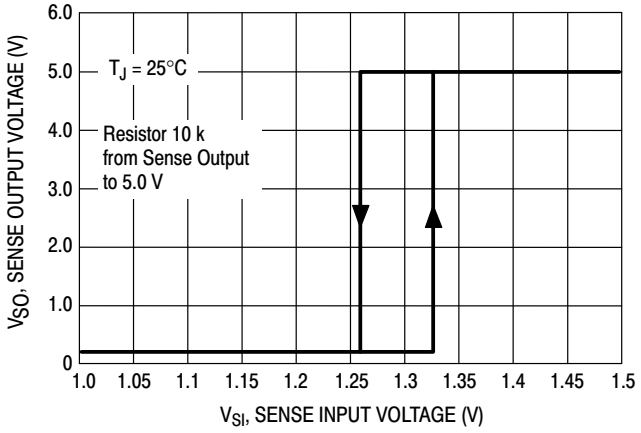


Figure 12. Sense Output versus Sense Input Voltage

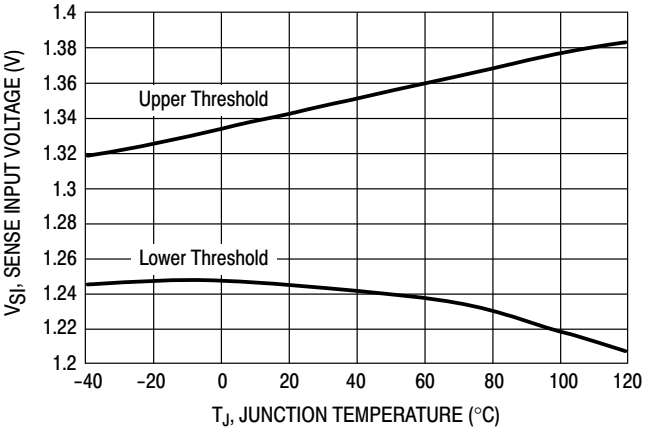
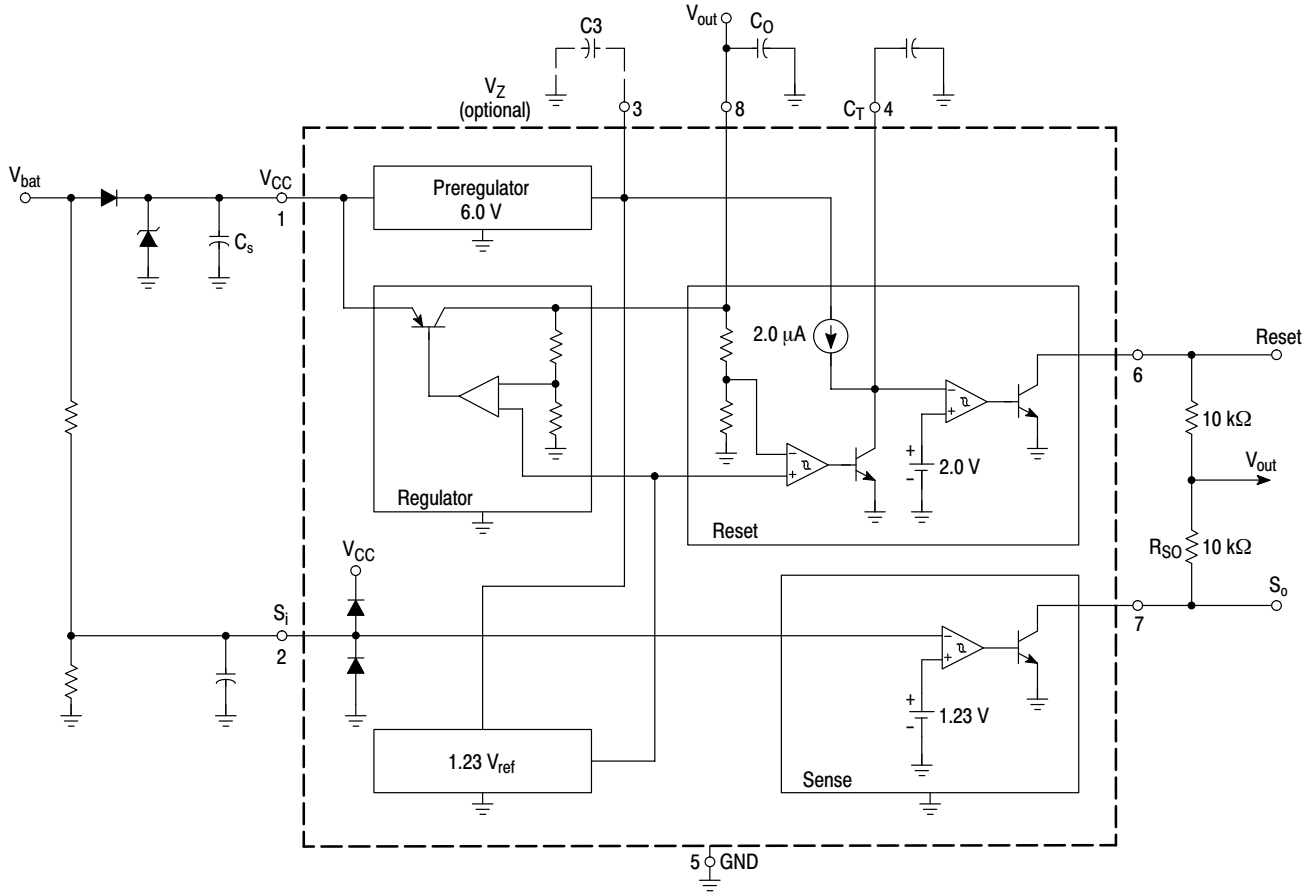


Figure 13. Sense Thresholds versus Junction Temperature

APPLICATION INFORMATION

Supply Voltage Transient

High supply voltage transients can cause a reset output signal perturbation. For supply voltages greater than 8.0 V the circuit shows a high immunity of the reset output against supply transients of more than 100 V/μs. For supply voltages less than 8.0 V supply transients of more than 0.4 V/μs can cause a reset signal perturbation. To improve the transient behavior for supply voltages less than 8.0 V a capacitor at Pin 3 can be used. A capacitor at Pin 3 (C3 ≤ 1.0 μF) also reduces the output noise.



NOTE: 1. For stability: $C_s \geq 1.0$ μF, $C_O \geq 4.7$ μF, ESR < 10 Ω at 10 kHz
2. Recommended for application: $C_s = C_O = 10$ μF

Figure 14. Application Schematic

OPERATING DESCRIPTION

The L4949 is a monolithic integrated low dropout voltage regulator. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. It is also suitable in other applications where the included functions are required. The modular approach of this device allows the use of other features and functions independently when required.

Voltage Regulator

The voltage regulator uses an isolated collector vertical PNP transistor as a regulating element. With this structure, very low dropout voltage at currents up to 100 mA is obtained. The dropout operation of the standby regulator is maintained down to 3.0 V input supply voltage. The output voltage is regulated up to a transient input supply voltage of 35 V.

A typical curve showing the standby output voltage as a function of the input supply voltage is shown in Figure 16.

The current consumption of the device (quiescent current) is less than 200 μA.

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. The quiescent current as a function of the supply input voltage is shown in Figure 17.

Short Circuit Protection:

The maximum output current is internally limited. In case of short circuit, the output current is foldback current limited as described in Figure 15.

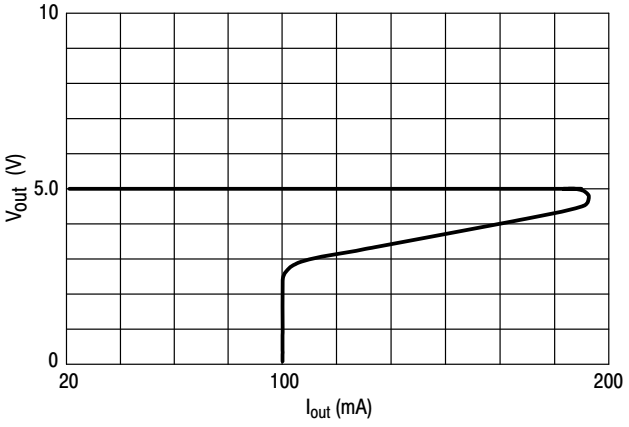


Figure 15. Foldback Characteristic of V_{out}

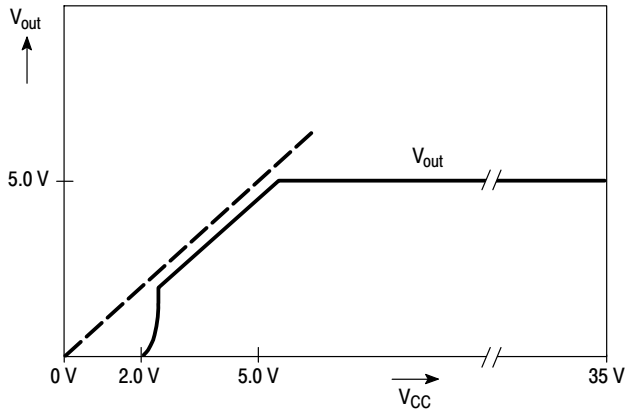


Figure 16. Output Voltage versus Supply Voltage

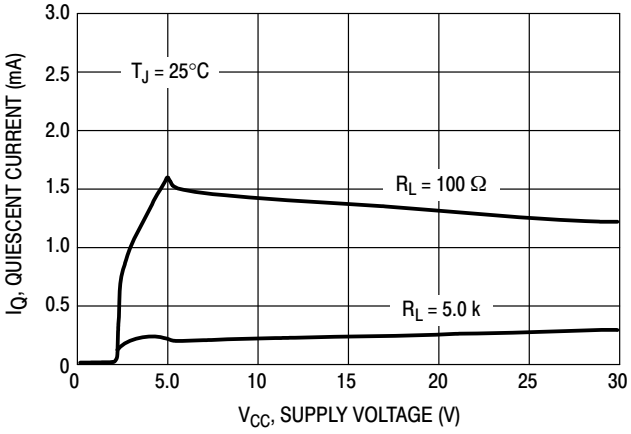


Figure 17. Quiescent Current versus Supply Voltage

Preregulator

To improve transient immunity a preregulator stabilizes the internal supply voltage to 6.0 V. This internal voltage is present at Pin 3 (V_Z). This voltage should not be used as an output because the output capability is very small (≤ 100 μA).

This output may be used to improve transient behavior for supply voltages less than 8.0 V. In this case a capacitor (100 nF – 1.0 μF) must be connected between Pin 3 and GND. If this feature is not used Pin 3 must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in Figure 18.

The reset circuit supervises the output voltage. The reset threshold of 4.5 V is defined by the internal reference voltage and standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T:

$$t_{RD} = \frac{C_T \times 2.0\ V}{2.0\ \mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T. The reaction time of the reset circuit increases the noise immunity.

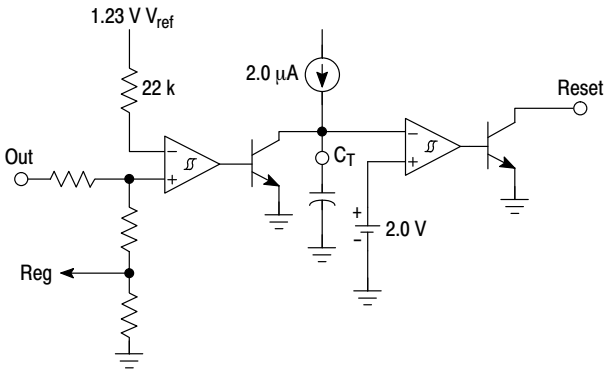


Figure 18. Reset Circuit

Output voltage drops below the reset threshold only marginally longer than the reaction time results in a shorter reset delay time.

The nominal reset delay time will be generated for output voltage drops longer than approximately 50 μs. The typical reset output waveforms are shown in Figure 19.

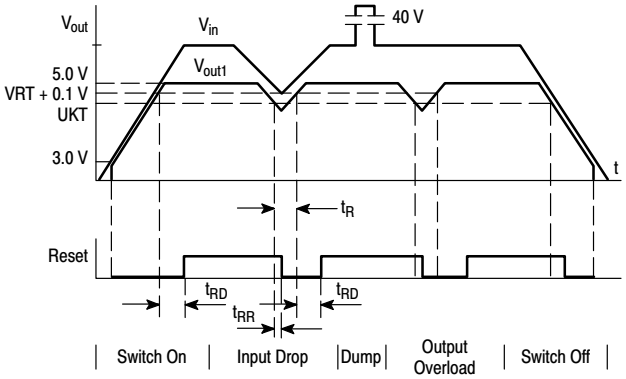


Figure 19. Typical Reset Output Waveforms

Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23 V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after a protection diode and to provide additional information to the microprocessor such as low voltage warnings.

ORDERING INFORMATION

Device	Operating Temperature Range	Package	Shipping†
L4949NG	T_J = −40°C to +125°C	PDIP−8 (Pb−Free)	50 Units / Rail
L4949DG		SOIC−8 (Pb−Free)	98 Units / Rail
L4949DR2G		SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV4949DG*		SOIC−8 (Pb−Free)	98 Units / Rail
NCV4949PDG*		SOIC−8 EP (Pb−Free)	98 Units / Rail
NCV4949DR2G*		SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV4949PDR2G*		SOIC−8 EP (Pb−Free)	2500 Units / Tape & Reel
NCV4949DWR2G*		SOIC−20W (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV4949: T_{low} = −40°C, T_{high} = +125°C. Guaranteed by design.
NCV prefix is for automotive and other applications requiring site and change control.

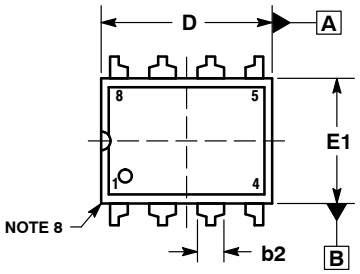
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

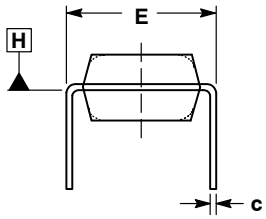
SCALE 1:1

PDIP–8
CASE 626–05
ISSUE P

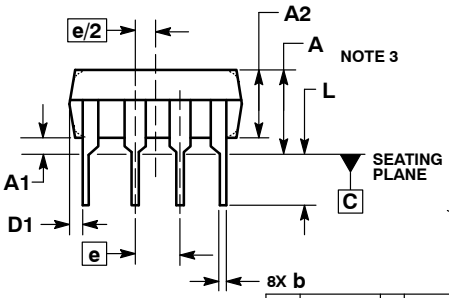
DATE 22 APR 2015



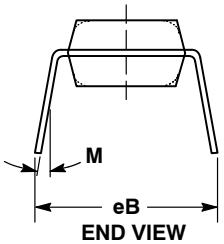
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



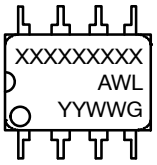
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP–8	PAGE 1 OF 1

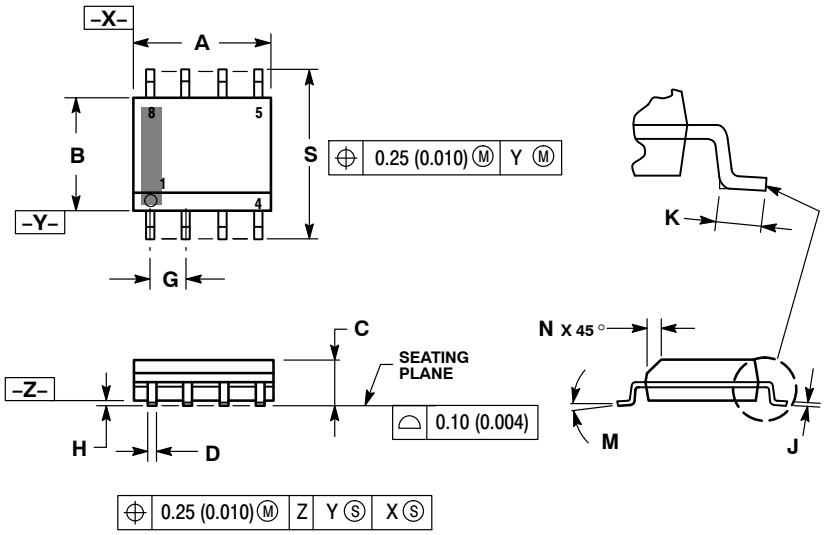
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

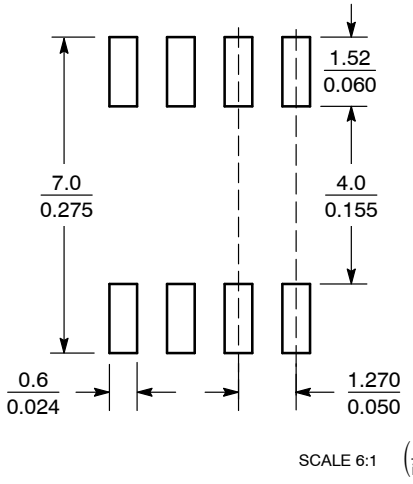
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

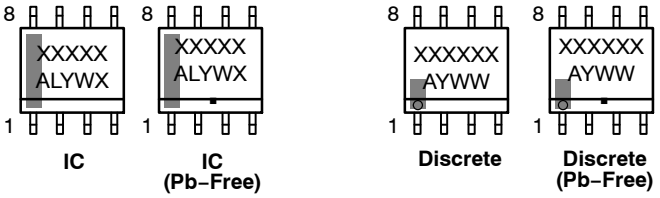
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

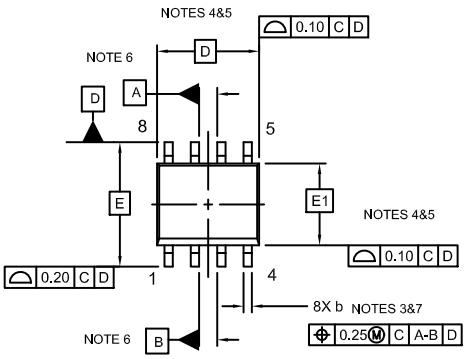
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

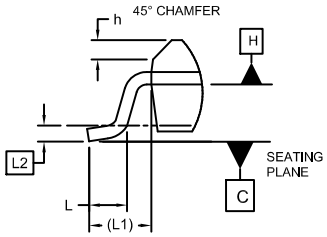
DATE 02 APR 2019

NOTES:

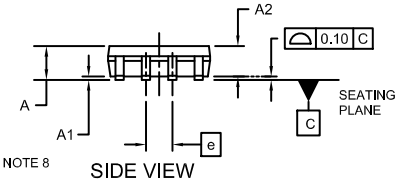
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



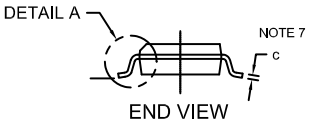
TOP VIEW



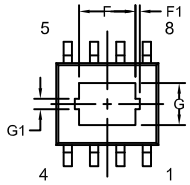
DETAIL A



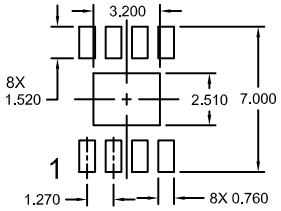
SIDE VIEW



END VIEW



BOTTOM VIEW

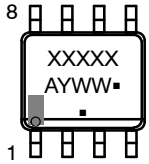


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



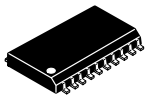
XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON14029D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−8 EP	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

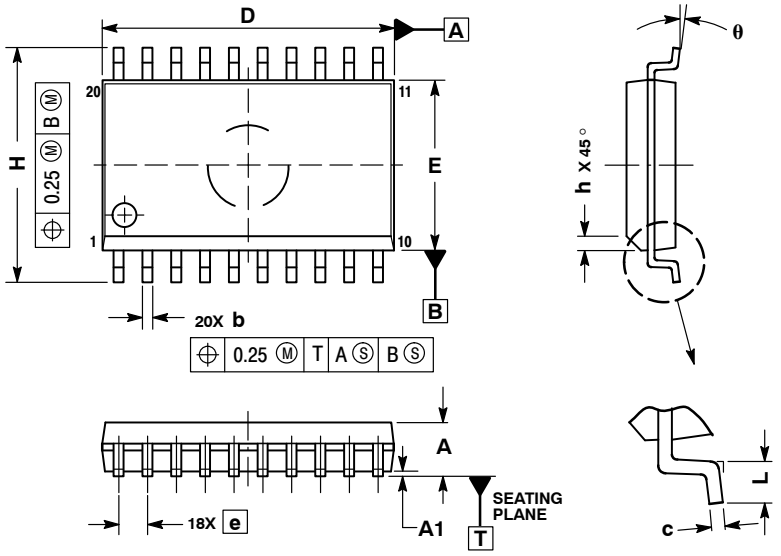
ON Semiconductor®



SCALE 1:1

SOIC–20 WB
CASE 751D–05
ISSUE H

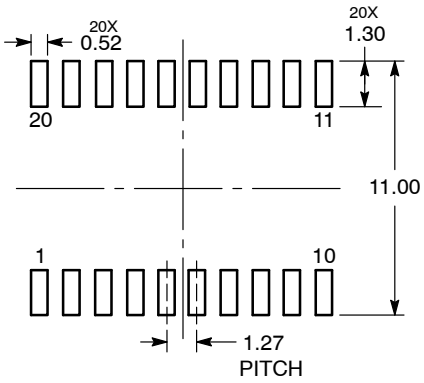
DATE 22 APR 2015



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

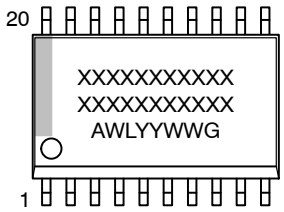
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**SOIC–20 WB**	**PAGE 1 OF 1**

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