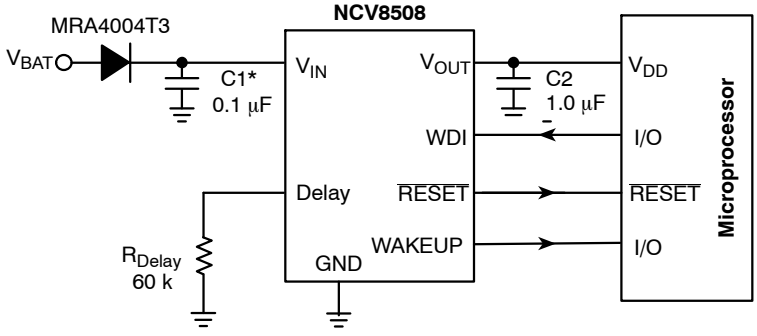
NCV8508

5.0 V, 250 mA LDO with Watchdog and $\overline{\text{RESET}}$

The NCV8508 is a precision micropower Low Dropout (LDO) voltage regulator. The part contains many of the required features for powering microprocessors. Its robustness makes it suitable for severe automotive environments. In addition, the NCV8508 is ideal for use in battery operated, microprocessor controlled equipment because of its extremely low quiescent current.

Features

- Output Voltage: 5.0 V
- ±3.0% Output Voltage
- I_{OUT} Up to 250 mA
- Quiescent Current Independent of Load
- Micropower Compatible Control Functions:
  - Wakeup
  - Watchdog
  - $\overline{\text{RESET}}$
- Low Quiescent Current (100 μA typ)
- Protection Features:
  - Thermal Shutdown
  - Short Circuit
  - 45 V Operation
- Internally Fused Leads in SO−16L Package
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- AEC Qualified
- PPAP Capable
- This is a Pb−Free Device*



*C1 required if regulator is located far from power supply filter.

Figure 1. Application Circuit

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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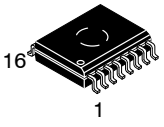
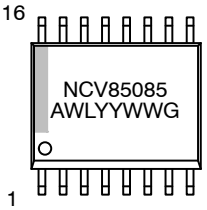
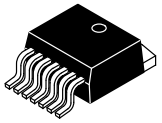
http://onsemi.com

MARKING DIAGRAMS

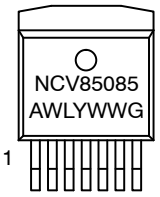


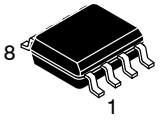
SO−16L
DW SUFFIX
CASE 751G



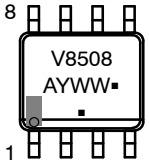


D²PAK−7
DPS SUFFIX
CASE 936AB





SO−8 EP
PD SUFFIX
CASE 751AC

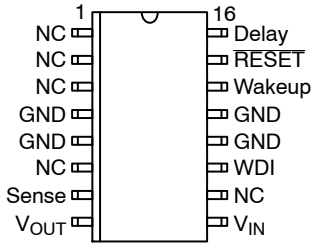


A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G or ▪	= Pb−Free Package

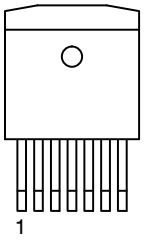
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 23 of this data sheet.

PIN CONNECTIONS

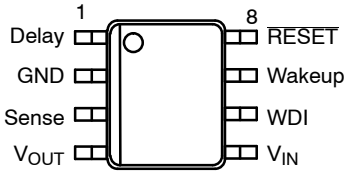


SO−16L



Tab = GND
Lead 1. V_{OUT}
2. V_{IN}
3. WDI
4. GND
5. Wakeup
6. $\overline{RESET}$
7. Delay

D^2PAK−7



SO−8 EP

PACKAGE PIN DESCRIPTION

PACKAGE PIN #			PIN SYMBOL	FUNCTION
D^2PAK−7	SO−16L	SO−8 EP		
1	8	4	V_{OUT}	Regulated output voltage ± 3.0%.
2	9	5	V_{IN}	Supply Voltage to the IC.
3	11	6	WDI	CMOS compatible input lead. The Watchdog function monitors the falling edge of the incoming signal.
4	4, 5, 12, 13	2	GND	Ground connection.
5	14	7	Wakeup	CMOS compatible output consisting of a continuously generated signal used to “wake up” the microprocessor from sleep mode.
6	15	8	$\overline{RESET}$	CMOS compatible output lead $\overline{RESET}$ goes low whenever V_{OUT} drops by more than 7.0% from nominal, or during the absence of a correct Watchdog signal.
7	16	1	Delay	Buffered bandgap voltage used to create timing current for $\overline{RESET}$ and Wakeup from R_{Delay}.
–	1−3, 6, 10	–	NC	No Connection.
–	7	3	Sense	Kelvin connection which allows remote sensing of the output voltage for improved regulation. Connect to V_{OUT} if remote sensing is not required.
–	–	EPAD	EPAD	Connect to Ground potential or leave unconnected.

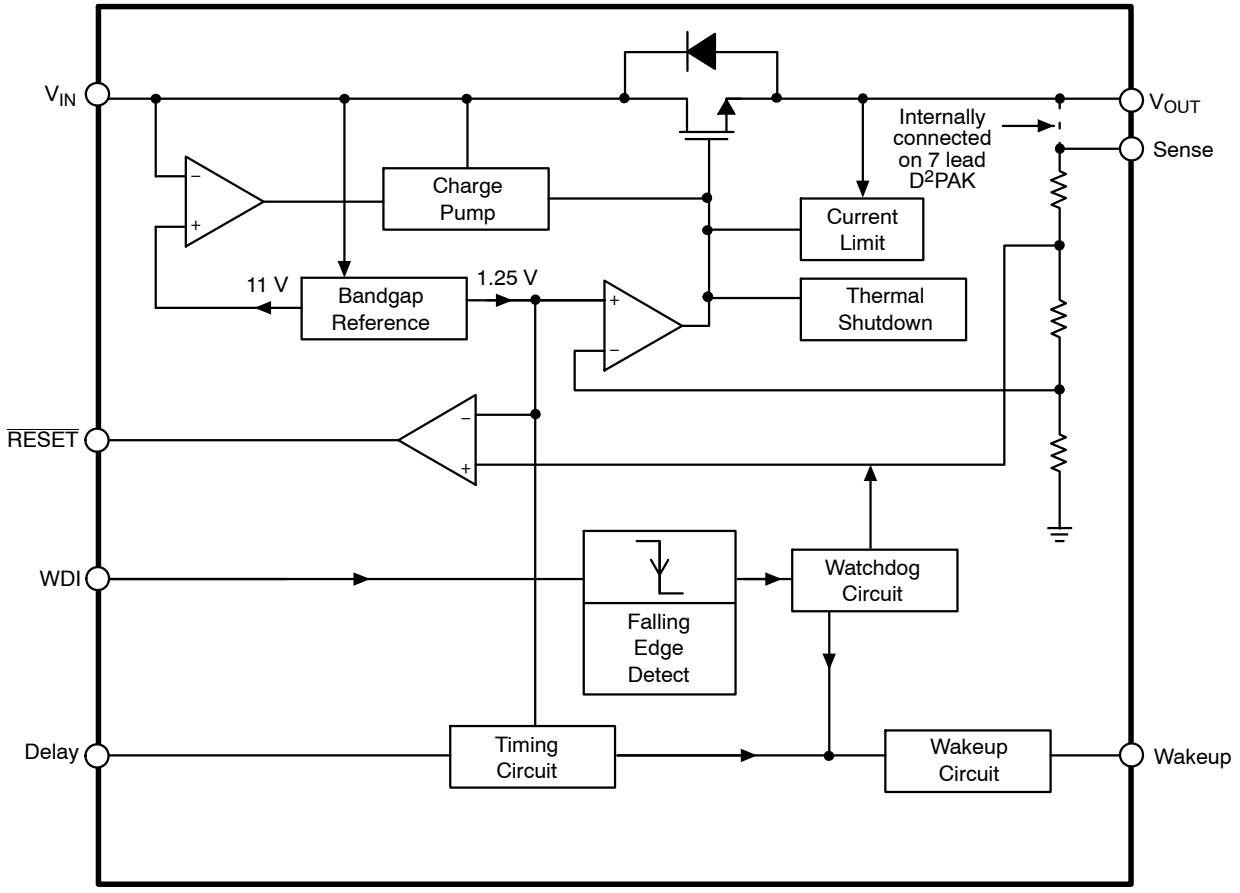


Figure 2. Block Diagram

MAXIMUM RATINGS

Rating	Value	Unit
Input Voltage, V_{IN} (DC)	−0.3 to 45	V
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)	60	V
Output Voltage, V_{OUT}	−0.3 to 18	V
ESD Susceptibility: Human Body Model Machine Model	 2.0 150	 kV V
Logic Inputs/Outputs ($\overline{RESET}$, WDI, Wakeup)	−0.3 to +7.0	V
Operating Junction Temperature, T_J	−40 to150	°C
Storage Temperature Range, T_S	−55 to +150	°C
Peak Reflow Soldering Temperature: Reflow: (Note 1)	240 Peak 260 Peak (Pb−Free) (Note 3)	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.
2. Depending on thermal properties of substrate $R_{\theta JA} = R_{\theta JC} + R_{\theta JCA}$.
3. −5°C/+0°C allowable conditions, applies to both Pb and Pb−Free devices.

THERMAL CHARACTERISTICS

See Package Thermal Data Section (Page 10)

ELECTRICAL CHARACTERISTICS ($-40°C \le T_J \le 125°C$; $6.0\ V \le V_{IN} \le 28\ V$, $100\ \mu A \le I_{OUT} \le 150\ mA$, $C_2 = 1.0\ \mu F$, $R_{Delay} = 60\ k$; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
OUTPUT					
Output Voltage	–	4.85	5.00	5.15	V
Dropout Voltage ($V_{IN} - V_{OUT}$)	I_{OUT} = 150 mA. Note 4	–	450	900	mV
Load Regulation	V_{IN} = 14 V, 100 μA ≤ I_{OUT} ≤ 150 mA	–	5.0	30	mV
Line Regulation	6.0 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 5.0 mA	–	5.0	50	mV
Current Limit	–	250	400	–	mA
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
Quiescent Current	V_{IN} = 12 V, I_{OUT} = 150 mA, (see Figure 6)	–	100	150	μA
$\overline{\text{RESET}}$					
Threshold	–	4.50	4.65	4.80	V
Output Low	R_{LOAD} = 10 k to V_{OUT}, V_{OUT} ≥ 1.0 V R_{LOAD} = 5.1 k to V_{OUT}, V_{OUT} ≥ 1.0 V	–	0.2 0.4	0.4 0.8	V
Output High	R_{LOAD} = 10 k to GND R_{LOAD} = 5.1 k to GND	V_{OUT} – 0.5 V_{OUT} – 1.0	V_{OUT} – 0.25 V_{OUT} – 0.5	–	V
Delay Time	V_{IN} = 14 V, R_{Delay} = 60 k, I_{OUT} = 5.0 mA V_{IN} = 14 V, R_{Delay} = 120 k, I_{OUT} = 5.0 mA	2.0 –	3.0 6.0	4.0 –	ms ms
WATCHDOG INPUT					
Threshold High	–	70	–	–	%V_{OUT}
Threshold Low	–	–	–	30	%V_{OUT}
Hysteresis	–	–	100	–	mV
Input Current	WDI = 6.0 V	–	0.1	+10	μA
Pulse Width	50% WDI falling edge to 50% WDI rising edge and 50% WDI rising edge to 50% WDI falling edge, (see Figure 5)	5.0	–	–	μs
WAKEUP OUTPUT (V_{IN} = 14 V, I_{OUT} = 5.0 mA)					
Wakeup Period	See Figures 4 and 5, R_{DELAY} = 60 k See Figures 4 and 5, R_{DELAY} = 120 k	18 –	25 50	32 –	ms ms
Wakeup Duty Cycle Nominal	See Figure 3	45	50	55	%
$\overline{\text{RESET}}$ HIGH to Wakeup Rising Delay Time	R_{DELAY} = 60 k 50% $\overline{\text{RESET}}$ rising edge to 50% Wakeup edge, R_{DELAY} = 120 k (see Figures 3 and 4)	9.0 –	12.5 25	16 –	ms ms
Wakeup Response to Watchdog Input	50% WDI falling edge to 50% Wakeup falling edge	–	0.1	5.0	μs
Wakeup Response to $\overline{\text{RESET}}$	50% $\overline{\text{RESET}}$ falling edge to 50% Wakeup falling edge. V_{OUT} = 5.0 V→ 4.5 V	–	0.1	5.0	μs
Output Low	R_{LOAD} = 10 k to V_{OUT}, V_{OUT} ≥ 1.0 V R_{LOAD} = 5.1 k to V_{OUT}, V_{OUT} ≥ 1.0 V	–	0.2 0.4	0.4 0.8	V
Output High	R_{LOAD} = 10 k to GND R_{LOAD} = 5.1 k to GND	V_{OUT} – 0.5 V_{OUT} – 1.0	V_{OUT} – 0.25 V_{OUT} – 0.5	–	V
DELAY					
Output Voltage	I_{DELAY} = 50 μA. Note 5	–	1.25	–	V

4. Measured when the output voltage has dropped 100 mV from the nominal value. (see Figure 12)
5. Current drain on the Delay pin directly affects the Delay Time, Wakeup Period, and the $\overline{\text{RESET}}$ to Wakeup Delay Time.

TIMING DIAGRAMS

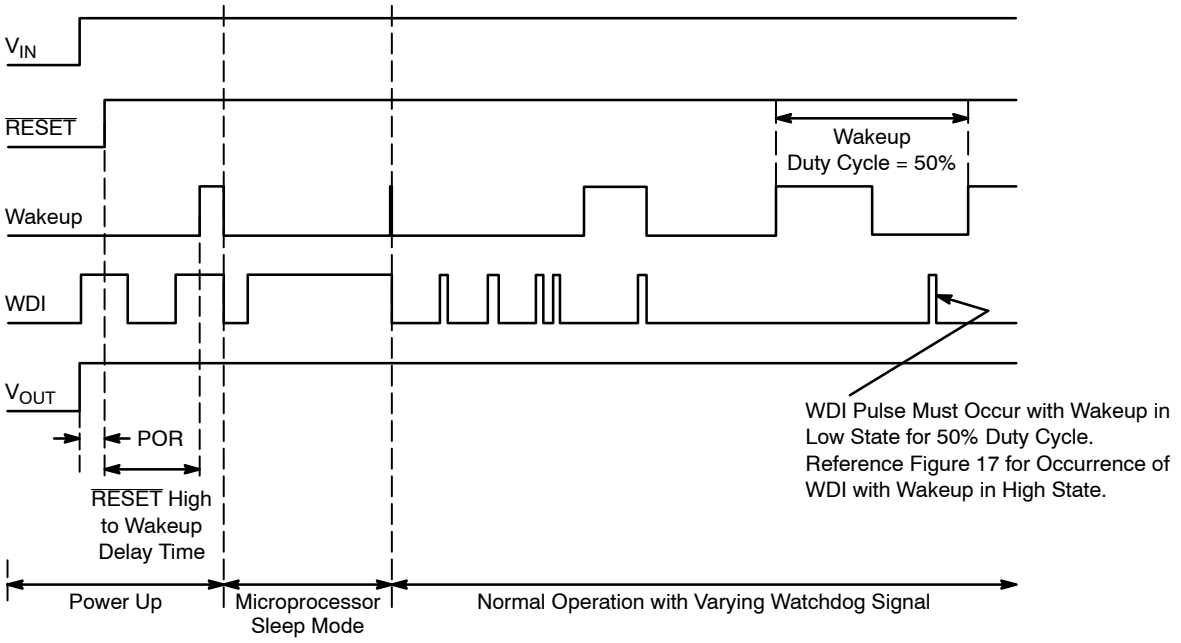


Figure 3. Power Up, Sleep Mode and Normal Operation

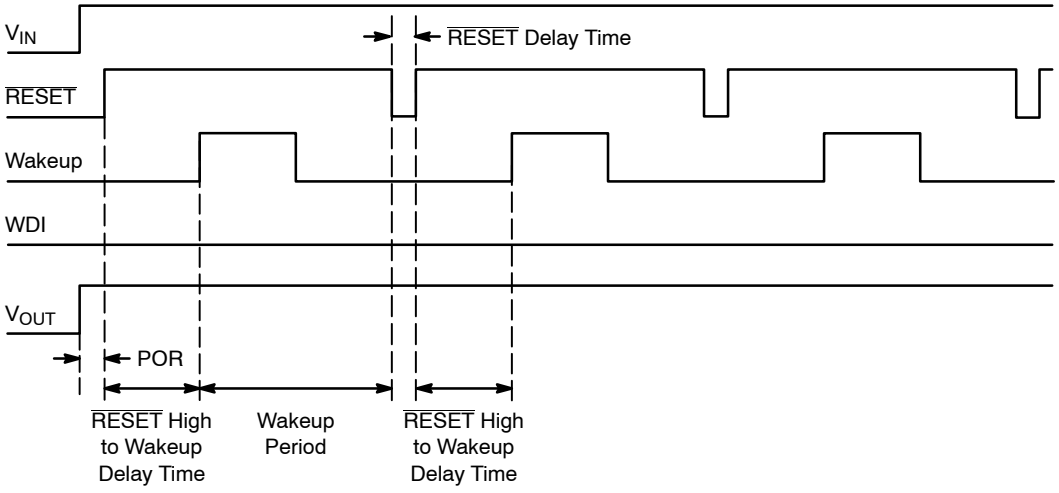


Figure 4. Error Condition: Watchdog Remains Low and a RESET Is Issued

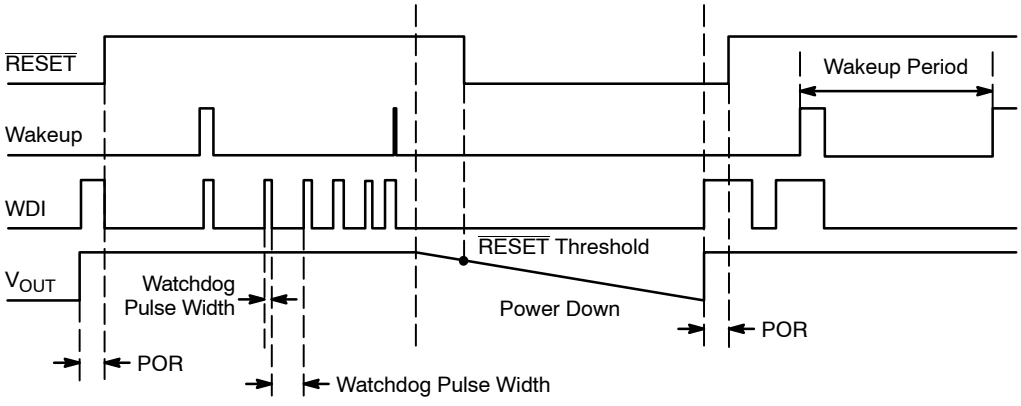


Figure 5. Power Down and Restart Sequence

TYPICAL PERFORMANCE CHARACTERISTICS

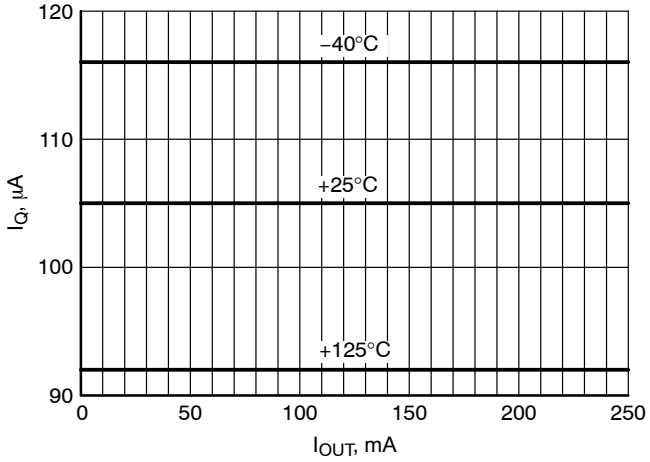


Figure 6. Quiescent Current vs Output Current

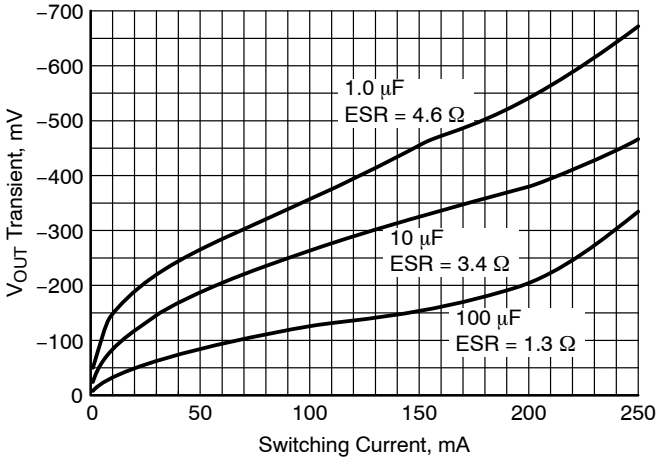


Figure 7. Load Transient Response

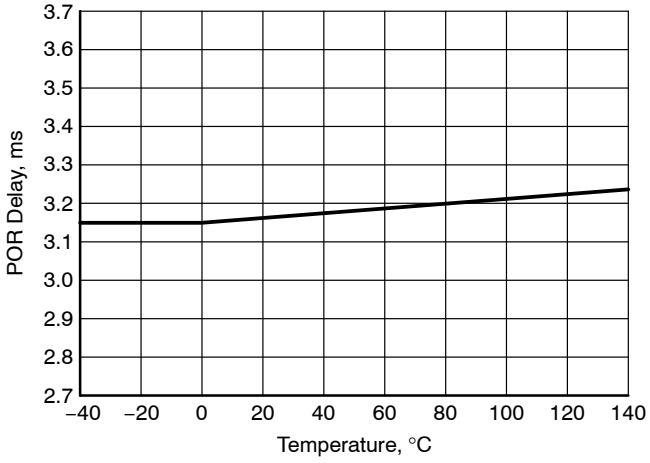


Figure 8. POR Delay vs Temp, R_{DELAY} = 60 kΩ

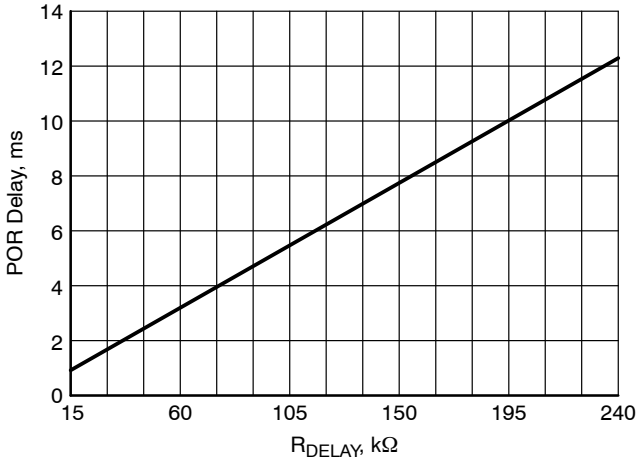


Figure 9. POR Delay vs R_{DELAY}

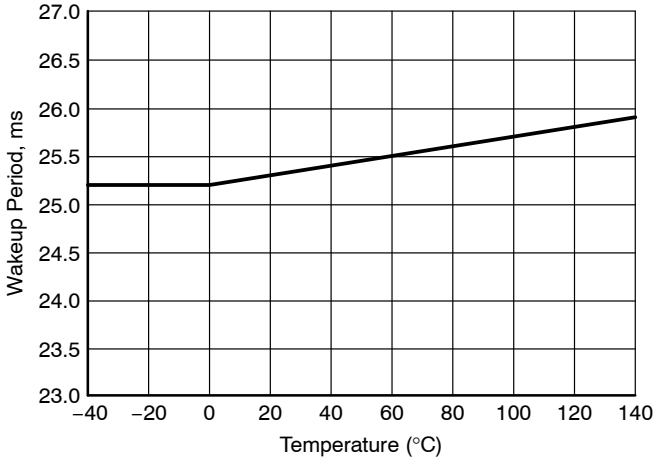


Figure 10. Wakeup Period vs Temp, R_{DELAY} = 60 kΩ

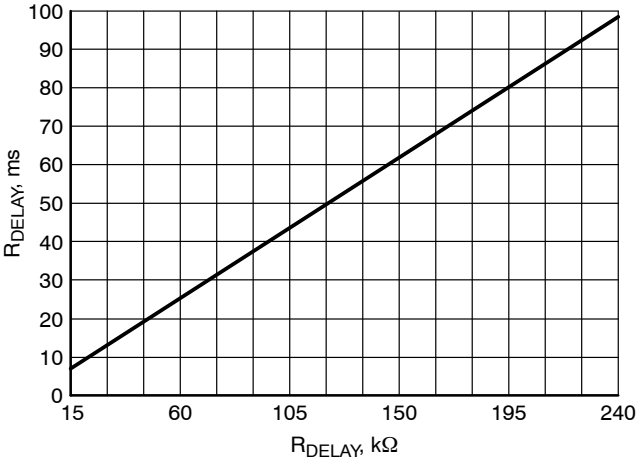


Figure 11. Wakeup Period vs R_{DELAY}

TYPICAL PERFORMANCE CHARACTERISTICS

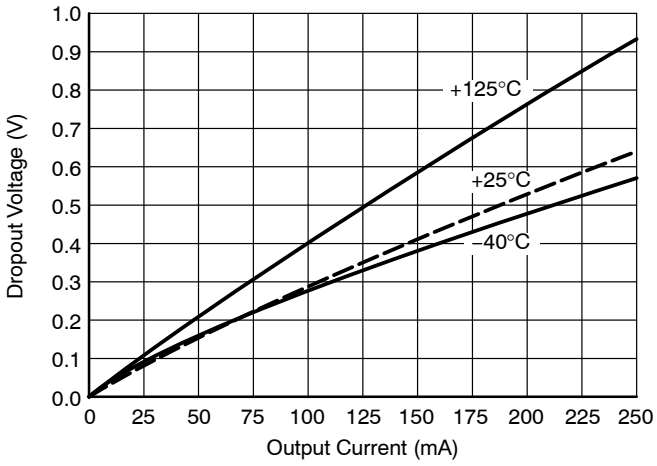


Figure 12. Dropout Voltage vs Output Current

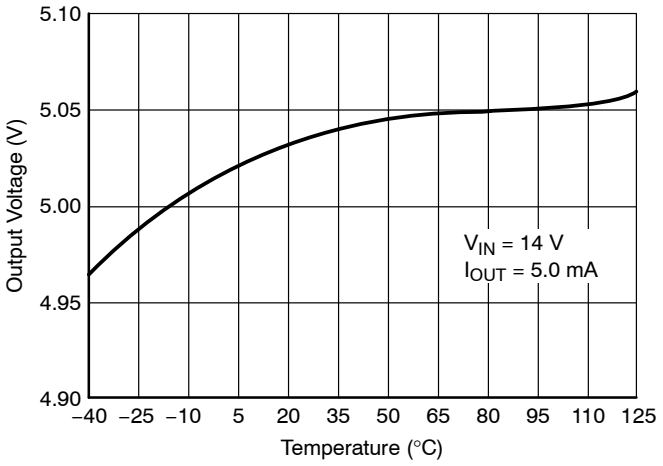


Figure 13. Output Voltage vs Temperature

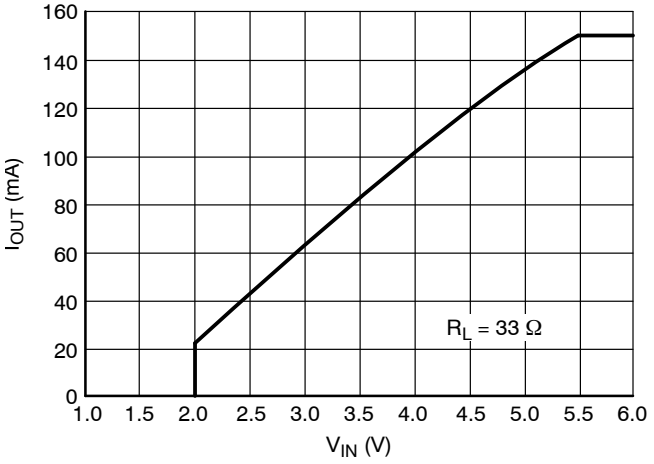


Figure 14. Output Current vs Input Voltage

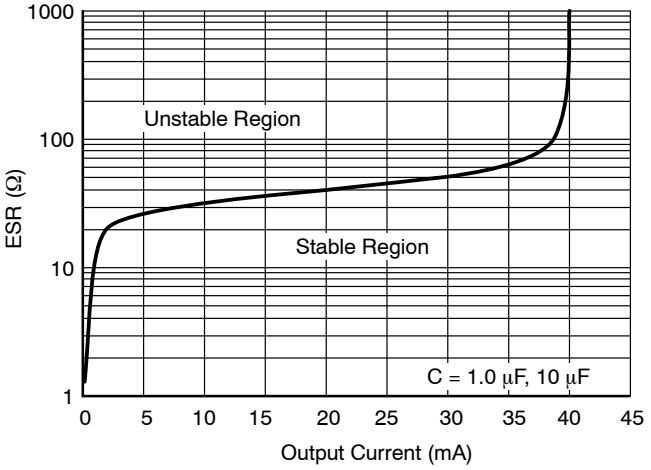


Figure 15. Output Capacitor ESR

DEFINITION OF TERMS

Dropout Voltage: The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

DETAILED OPERATING DESCRIPTION

The NCV8508 is a precision micropower voltage regulator with very low quiescent current (100 μA typical at 250 mA load). A typical dropout voltage is 450 mV at 150 mA. Microprocessor control logic includes Watchdog, Wakeup and $\overline{\text{RESET}}$. This unique combination of extremely low quiescent current and full microprocessor control makes the NCV8508 ideal for use in battery operated, microprocessor controlled equipment in addition to being a good fit in the automotive environment.

The NCV8508 Wakeup function brings the microprocessor out of Sleep mode. The microprocessor in turn signals its Wakeup status back to the NCV8508 by issuing a Watchdog signal.

The Watchdog logic function monitors an input signal (WDI) from the microprocessor. The NCV8508 responds to the falling edge of the Watchdog signal which it expects at least once during each Wakeup period. When the correct Watchdog signal is received, a falling edge is issued on the Wakeup signal line.

$\overline{\text{RESET}}$ is independent of V_{IN} and operates correctly to an output voltage as low as 1.0 V. A signal is issued in any of three situations. During power up, the $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. Finally, a $\overline{\text{RESET}}$ signal is issued if the regulator does not receive a Watchdog signal within the Wakeup period.

The $\overline{\text{RESET}}$ pulse width, Wakeup signal frequency, and Wakeup delay time are all set by one external resistor, R_{Delay}.

The Delay pin is a buffered bandgap voltage (1.25 V). It can be used as a reference for an external tracking regulator as shown in Figure 16.

The regulator is protected against short circuit and thermal runaway conditions. The device runs through 45 volt transients, making it suitable for use in automotive environments.

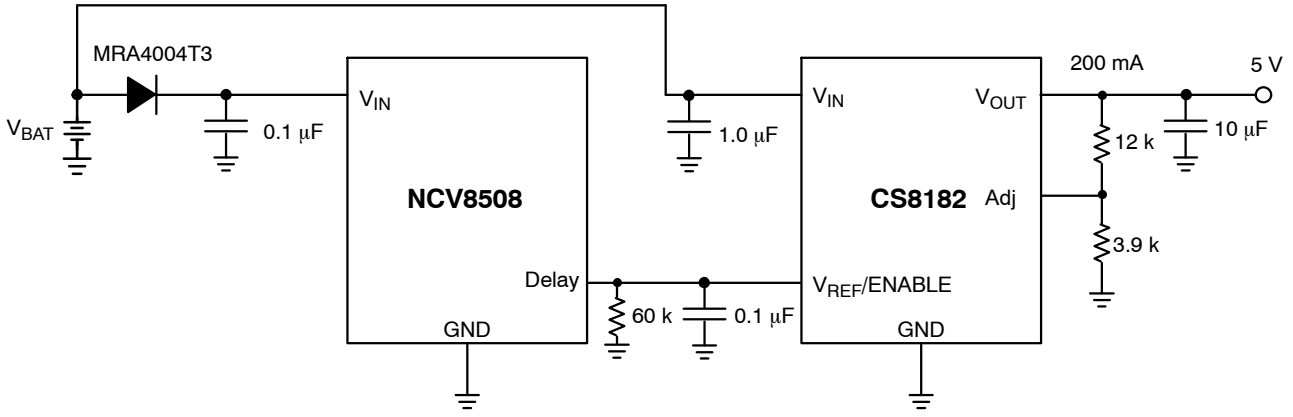


Figure 16. Application Circuit

CIRCUIT DESCRIPTION

Functional Description

To reduce the drain on the battery, a system can go into a low current consumption mode whenever it is not performing a main routine. The Wakeup signal is generated continuously and is used to interrupt a microcontroller that is in sleep mode. The nominal output is a 5.0 volt square wave (voltage generated from V_{OUT}) with a duty cycle of 50% at a frequency that is determined by a timing resistor, R_{Delay}.

When the microprocessor receives a rising edge from the Wakeup output, it must issue a Watchdog pulse and check its inputs to decide if it should resume normal operations or remain in the sleep mode.

The first falling edge of the Watchdog signal causes the Wakeup to go low within 2.0 μs (typ) and remain low until the next Wakeup cycle (see Figure 17). Other Watchdog pulses received within the same cycle are ignored (Figure 3).

During power up, $\overline{\text{RESET}}$ is held low until the output voltage is in regulation. During operation, if the output voltage shifts below the regulation limits, the $\overline{\text{RESET}}$ toggles low and remains low until proper output voltage regulation is restored. After the $\overline{\text{RESET}}$ delay, $\overline{\text{RESET}}$ returns high.

The Watchdog circuitry continuously monitors the input Watchdog signal (WDI) from the microprocessor. The absence of a falling edge on the Watchdog input during one Wakeup cycle will cause a $\overline{\text{RESET}}$ pulse to occur at the end of the Wakeup cycle. (see Figure 4).

The Wakeup output is pulled low during a $\overline{\text{RESET}}$ regardless of the cause of the $\overline{\text{RESET}}$. After the $\overline{\text{RESET}}$ returns high, the Wakeup cycle begins again (see Figure 4).

The $\overline{\text{RESET}}$ Delay Time, Wakeup signal frequency and $\overline{\text{RESET}}$ high to Wakeup delay time are all set by one external resistor R_{Delay}.

Wakeup Period = $(4.17 \times 10^{-7})R_{Delay}$

$\overline{\text{RESET}}$ Delay Time = $(5.21 \times 10^{-8})R_{Delay}$

$\overline{\text{RESET}}$ HIGH to Wakeup Delay Time = $(2.08 \times 10^{-7})R_{Delay}$

Resistor temperature coefficient and tolerance as well as the tolerance of the NCV8508 must be taken into account in order to get the correct system tolerance for each parameter.

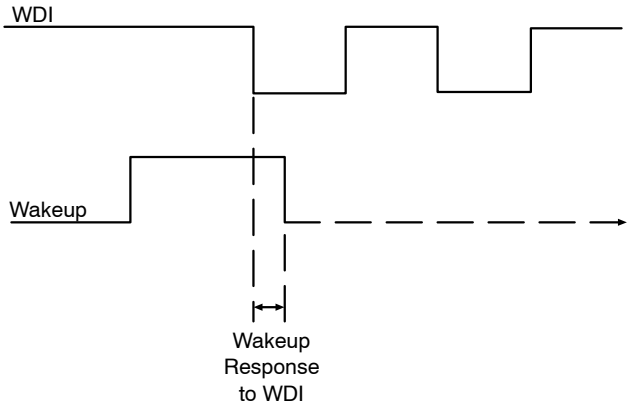


Figure 17. Wakeup Response to WDI

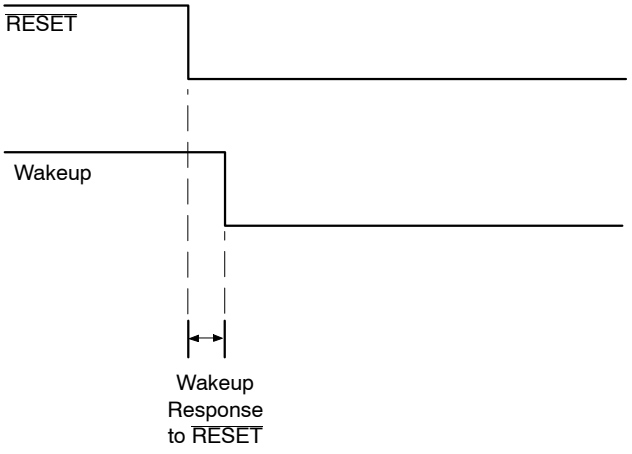


Figure 18. Wakeup Response to $\overline{\text{RESET}}$ (Low Voltage)

THERMAL DATA

Recommend Thermal Data for SOIC−16 Package

Parameter	Test Conditions Typical Value		Units
	min−pad board (Note 6)	**1”−pad board** (Note 7)	
Junction−to−Lead (psi−JL, Ψ_{JL})	20	15	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	100	83	°C/W

6. 1 oz. copper, 94 mm^2 copper area, 0.062” thick FR4.
7. 1 oz. copper, 767 mm^2 copper area, 0.062” thick FR4.

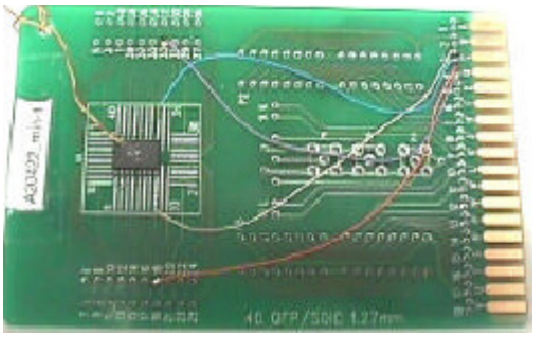


Figure 19. Min Pad PCB Layout

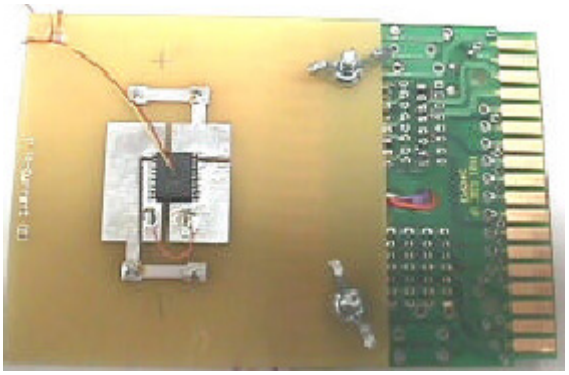


Figure 20. Min Pad PCB Layout

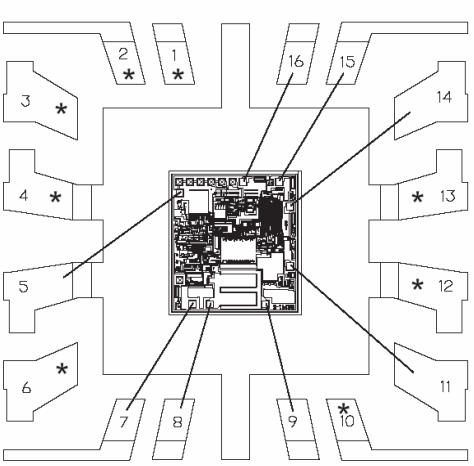


Figure 21. Internal Construction of the Package (notice pins 4, 5 and 12, 13 are connected to flag)

Table 1. SOIC 16−Lead Thermal RC Network Models

	96 mm²	767 mm²		96 mm²	767 mm²	Cu Area
	Cauer network			Foster network		
	C's	C's	Units	Tau	Tau	units
1	**1.84E−06**	**1.84E−06**	W−s/C	2.99E−07	2.99E−07	sec
2	**8.69E−06**	**8.69E−06**	W−s/C	4.40E−06	4.40E−06	sec
3	**2.61E−05**	**2.61E−05**	W−s/C	4.62E−05	4.62E−05	sec
4	**8.98E−05**	**8.98E−05**	W−s/C	5.08E−04	5.08E−04	sec
5	**2.30E−03**	**2.30E−03**	W−s/C	8.93E−03	8.95E−03	sec
6	**2.99E−02**	**3.07E−02**	W−s/C	2.04E−01	2.19E−01	sec
7	1.79E−01	1.90E−01	W−s/C	3.26E+00	2.75E+00	sec
8	7.79E−01	9.94E−01	W−s/C	3.21E+01	2.19E+01	sec
9	5.34E+00	3.98E+00	W−s/C	1.24E+02	1.20E+02	sec
	R's	R's		R's	R's	
1	**0.199**	**0.199**	C/W	**0.123**	**0.123**	C/W
2	**0.598**	**0.598**	C/W	**0.349**	**0.349**	C/W
3	**1.795**	**1.795**	C/W	**1.057**	**1.057**	C/W
4	**4.085**	**4.085**	C/W	4.61	4.61	C/W
5	**3.977**	**3.977**	C/W	3.87	3.89	C/W
6	**7.509**	**7.833**	C/W	5.77	5.99	C/W
7	19.886	15.247	C/W	13.17	11.38	C/W
8	40.307	24.781	C/W	28.85	15.52	C/W
9	18.193	21.446	C/W	38.75	37.05	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 225 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

θJA vs Copper Spreader Area

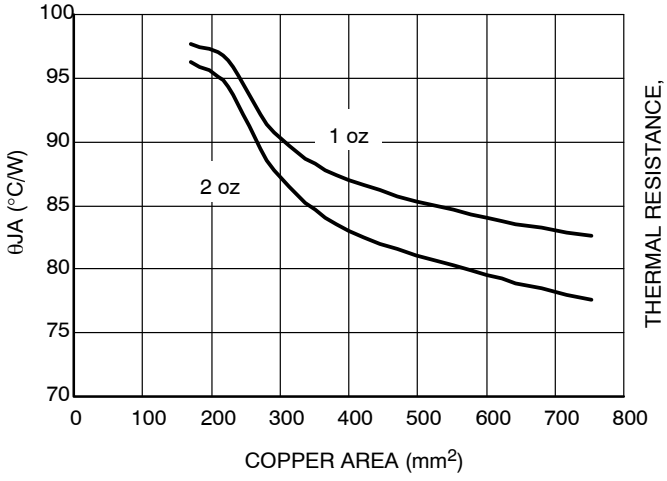


Figure 22. SOIC 16−Lead θJA as a Function of the Pad Copper Area Including Traces, Board Material

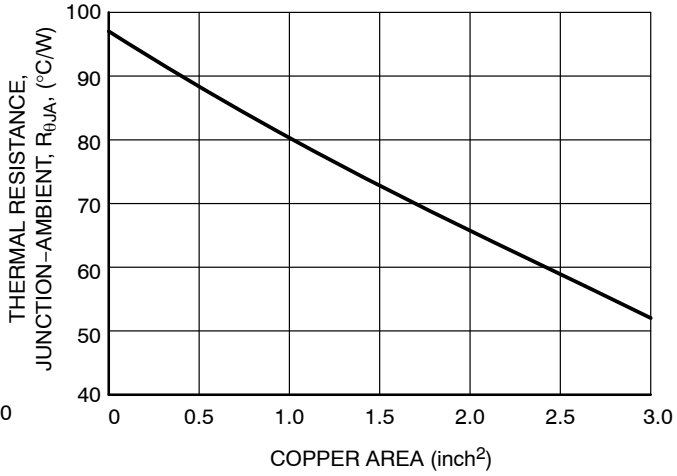


Figure 23. 16 Lead SOW (4 Leads Fused), θJA as a Function of the Pad Copper Area (2 oz. Cu Thickness), Board Material = 0.0625″ G−10/R−4

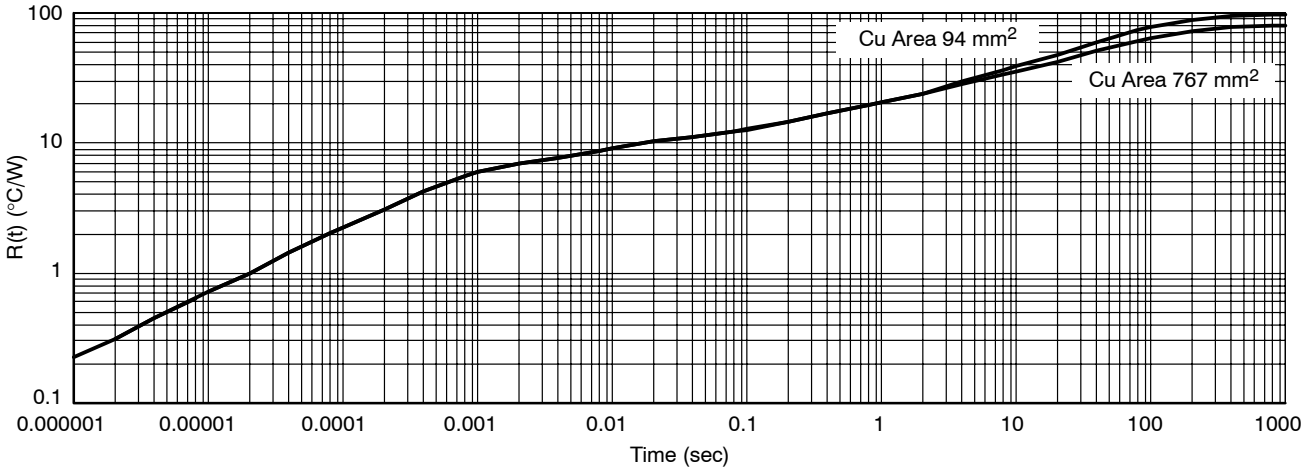


Figure 24. SOIC 16−Lead Single Pulse Heating Curve

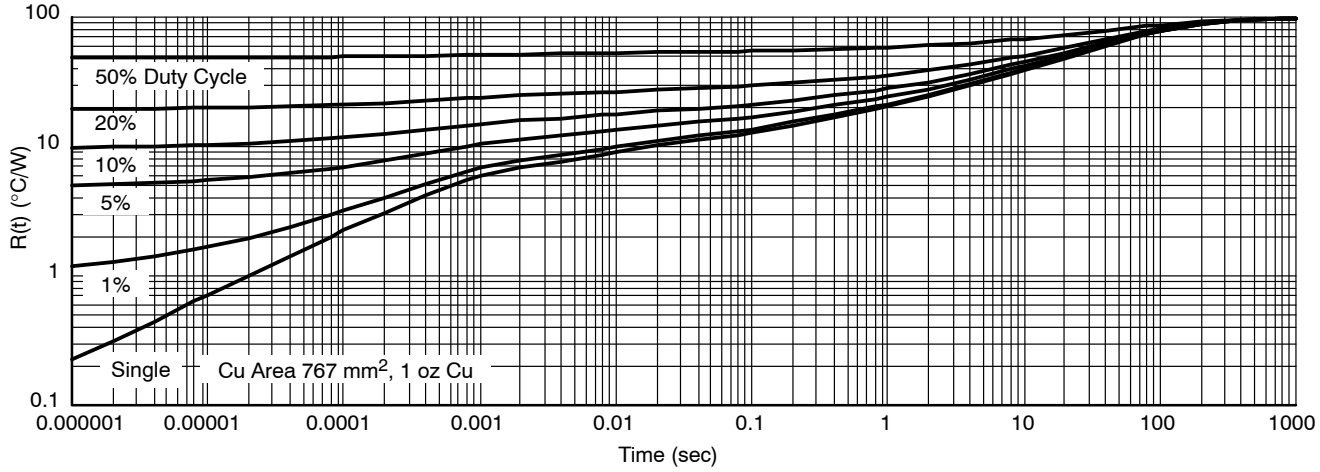


Figure 25. SOIC 16−Lead Thermal Duty Cycle Curves on 1” Spreader Test Board

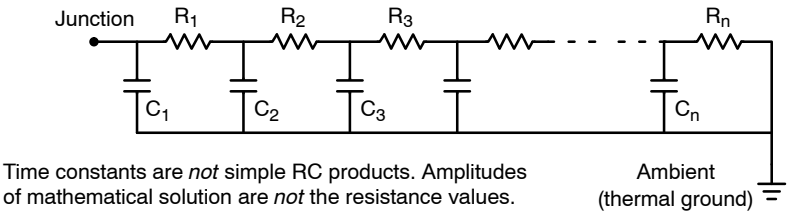


Figure 26. Grounded Capacitor Thermal Network (“Cauer” Ladder)

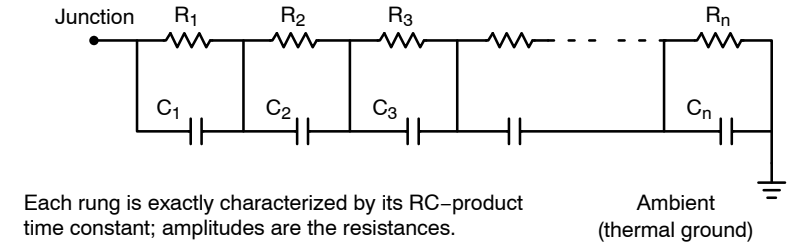


Figure 27. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

Recommend Thermal Data for D²PAK−7 Package

Parameter	Test Conditions Typical Value		Units
	min−pad board (Note 8)	**1”−pad board** (Note 9)	
Junction−to−Lead (psi−JL, Ψ_{JL})	6.0	6.0	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	78	44	°C/W

8. 1 oz. copper, 118 mm² copper area, 0.062” thick FR4.
9. 1 oz. copper, 626 mm² copper area, 0.062” thick FR4.

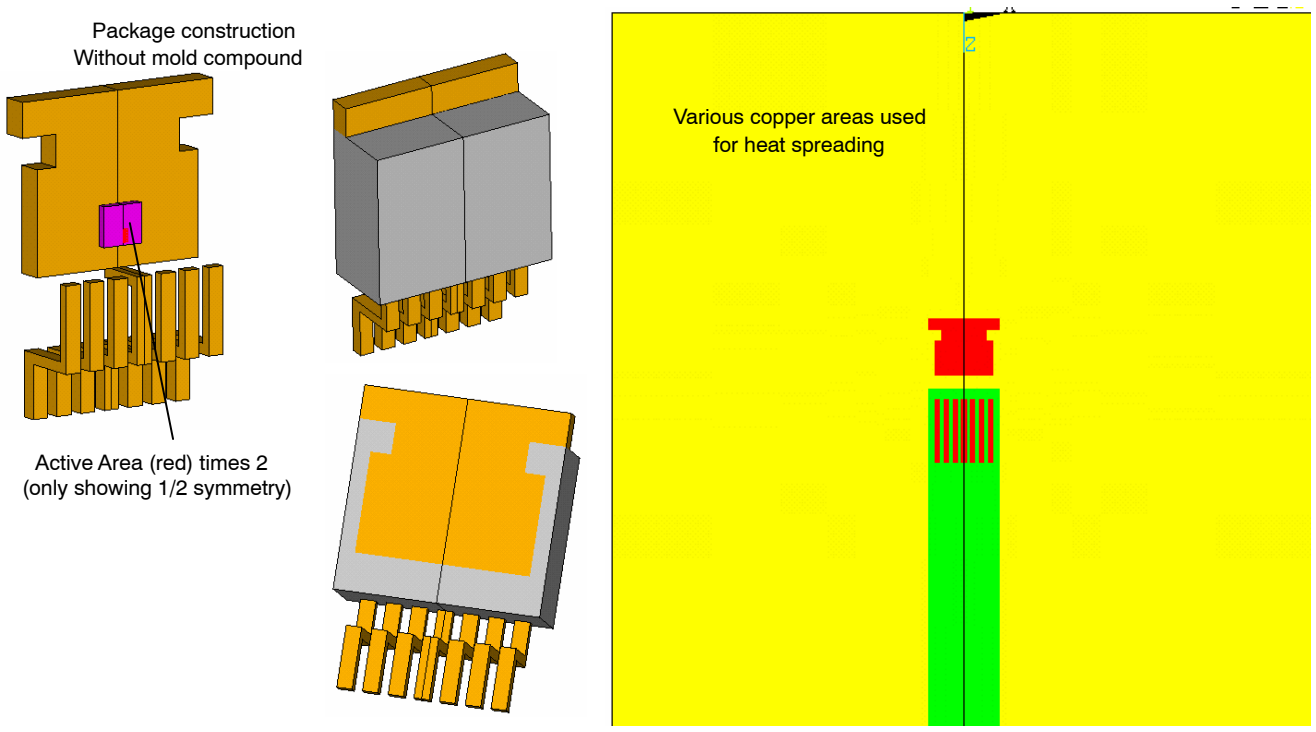


Figure 28. PCB Layout and Package Construction for Simulation

Table 2. D²PAK 7−Lead Thermal RC Network Models

	118 mm²	626 mm²		118 mm²	626 mm²	Cu Area
	Cauer Network			Foster Network		
	C's	C's	Units	Tau	Tau	units
1	**1.45E−06**	**1.45E−06**	W−s/C	**1.00E−07**	**1.00E−07**	sec
2	**5.55E−06**	**5.58E−06**	W−s/C	**1.00E−06**	**1.00E−06**	sec
3	**1.57E−05**	**1.59E−05**	W−s/C	**1.00E−05**	**1.00E−05**	sec
4	**5.11E−05**	**5.22E−05**	W−s/C	0.000	0.000	sec
5	**3.48E−04**	**5.94E−04**	W−s/C	0.001	0.002	sec
6	1.07E−02	6.62E−02	W−s/C	0.006	0.029	sec
7	2.65E−02	1.55E−01	W−s/C	0.020	0.080	sec
8	0.524	0.413	W−s/C	1.43	2.63	sec
9	0.490	2.441	W−s/C	6.52	3.6	sec
10	0.843	0.410	W−s/C	104.512	95.974	sec
	R's	R's		R's	R's	
1	**0.089**	**0.089**	C/W	**5.25E−02**	**5.25E−02**	C/W
2	**0.210**	**0.208**	C/W	**1.14E−01**	**1.14E−01**	C/W
3	**0.637**	**0.624**	C/W	**3.59E−01**	**3.59E−01**	C/W
4	**1.899**	**2.107**	C/W	1.5	1.9	C/W
5	**1.883**	**2.454**	C/W	2.6	3.0	C/W
6	1.398	0.952	C/W	0.1	0.1	C/W
7	0.315	0.360	C/W	1.7	0.9	C/W
8	14.348	7.042	C/W	0.1	0.1	C/W
9	5.621	20.823	C/W	7.2	4.6	C/W
10	51.986	9.649	C/W	64.8	33.3	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 166 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

θJA vs Copper Spreader Area

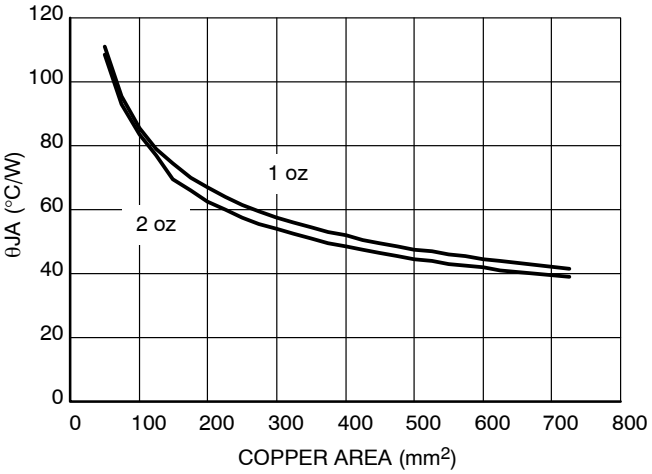


Figure 29. D²PAK 7−lead θJA as a Function of the Pad Copper Area Including Traces, Board Material

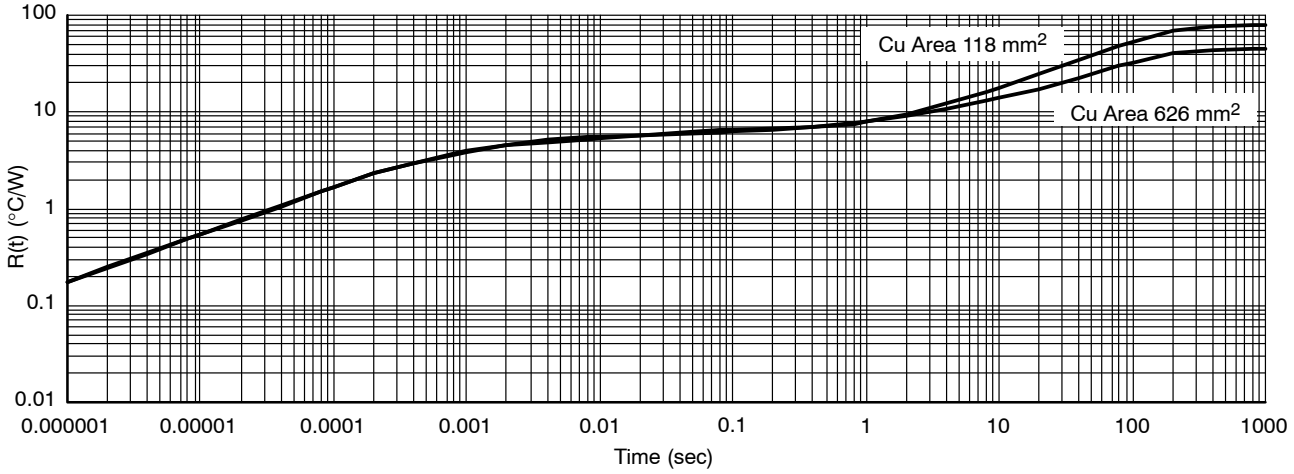


Figure 30. D²PAK 7−Lead Single Pulse Heating Curve

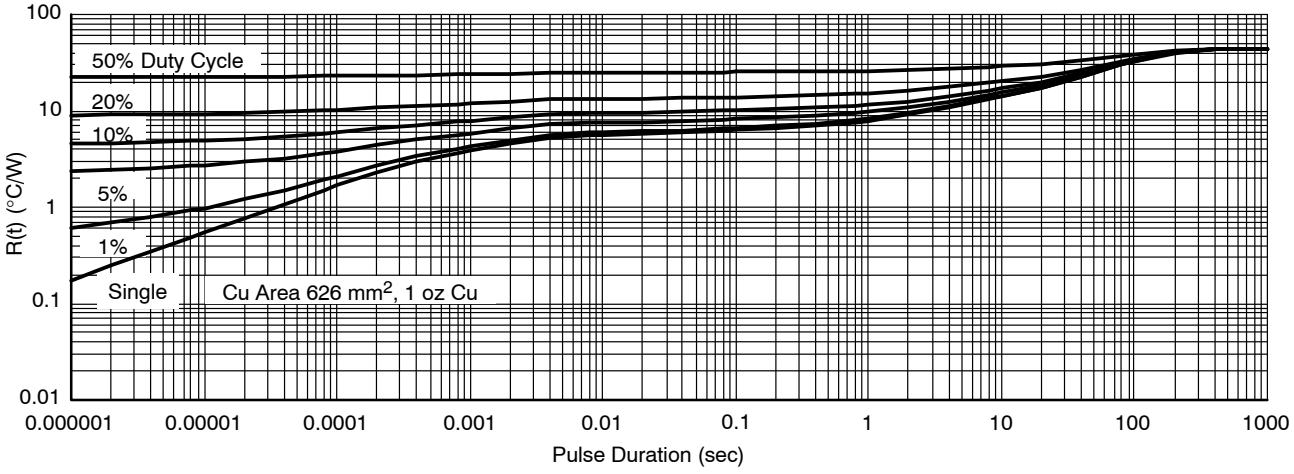


Figure 31. D²PAK 7−Lead Thermal Duty Cycle Curves on 1” Spreader Test Board

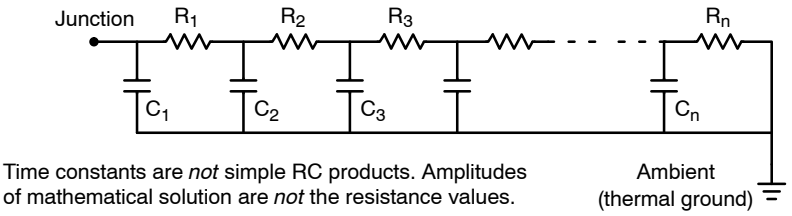


Figure 32. Grounded Capacitor Thermal Network (“Cauer” Ladder)

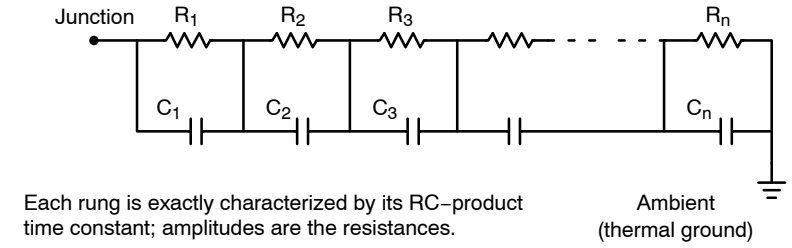


Figure 33. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

Recommend Thermal Data for SOIC−8 EP Package

Parameter	Test Conditions Typical Value		Units
Pad is soldered to PCB copper	**min−pad board** (Note 10)	**1”−pad board** (Note 11)	
Junction−to−Lead (psi−JL, Ψ_{JL})	64	54	°C/W
Junction−to−Lead (psi−JPad, Ψ_{Jp})	14	11	°C/W
Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	122	84	°C/W

10. 1 oz. copper, 54 mm^2 copper area, 0.062” thick FR4.
11. 1 oz. copper, 717 mm^2 copper area, 0.062” thick FR4.

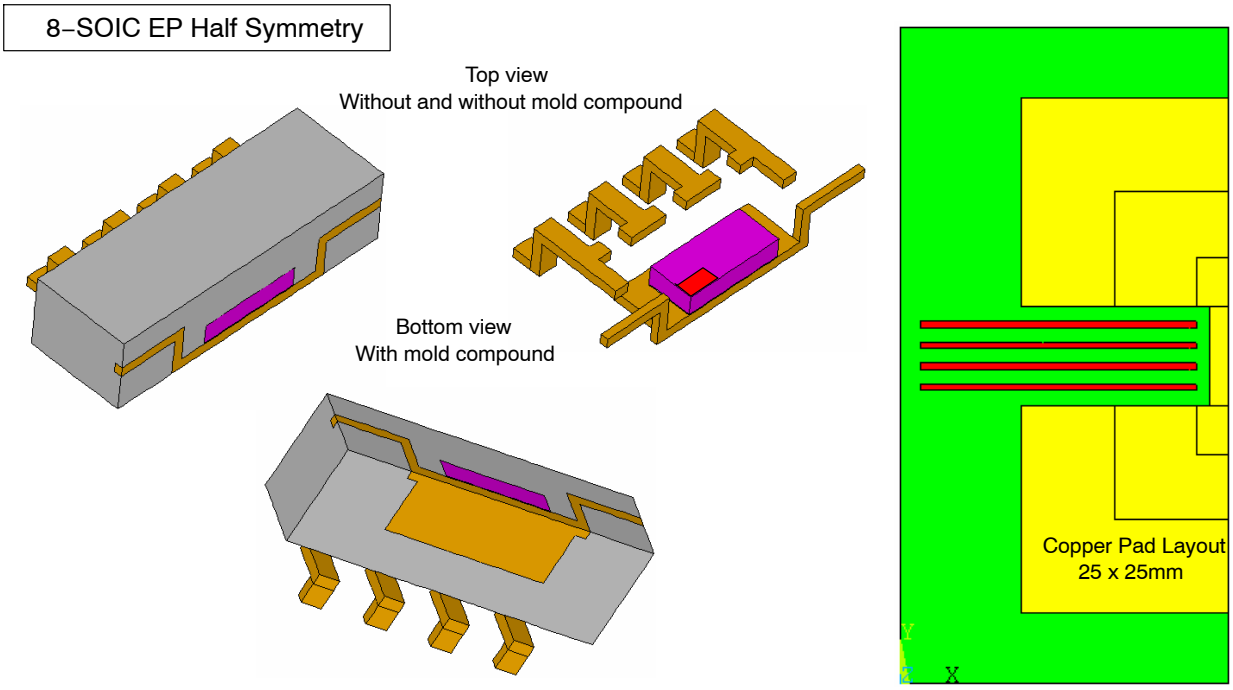


Figure 34. Internal Construction of the Package and PCB Layout for Multiple Pad Area

Table 3. SOIC 8−Lead EP Thermal RC Network Models

	54 mm²	717 mm²		54 mm²	717 mm²	Cu Area
	Cauer Network			Foster Network		
	C's	C's	Units	Tau	Tau	units
1	**2.28E−06**	**2.28E−06**	W−s/C	2.99E−07	2.99E−07	sec
2	**1.08E−05**	**1.08E−05**	W−s/C	4.40E−06	4.40E−06	sec
3	**3.24E−05**	**3.24E−05**	W−s/C	4.36E−05	4.36E−05	sec
4	**9.71E−05**	**9.71E−05**	W−s/C	3.59E−04	3.74E−04	sec
5	**6.28E−04**	**7.55E−04**	W−s/C	3.17E−03	4.59E−03	sec
6	**7.13E−03**	**1.49E−02**	W−s/C	0.030	0.162	sec
7	1.54E−02	9.28E−02	W−s/C	0.341	0.473	sec
8	6.16E−02	1.72E−01	W−s/C	2.909	1.653	sec
9	1.94E−01	3.83E−01	W−s/C	16.126	8.488	sec
10	1.52E+00	2.41E+00	W−s/C	54.334	71.562	sec
	R's	R's		R's	R's	
1	**0.161**	**0.161**	C/W	**0.11**	**0.11**	C/W
2	**0.482**	**0.482**	C/W	**0.26**	**0.26**	C/W
3	**1.445**	**1.445**	C/W	**0.73**	**0.73**	C/W
4	**3.00**	**3.00**	C/W	2.60	2.83	C/W
5	**4.47**	**5.34**	C/W	4.80	5.82	C/W
6	**5.92**	**12.21**	C/W	2.98	8.95	C/W
7	20.11	16.03	C/W	12.20	0.61	C/W
8	51.85	4.89	C/W	26.10	12.91	C/W
9	68.87	15.34	C/W	62.22	16.96	C/W
10	27.52	22.36	C/W	71.83	32.09	C/W

NOTE: Bold face items in the Cauer network above, represent the package without the external thermal system. The Bold face items in the Foster network are computed by the square root of time constant R(t) = 225 * sqrt(time(sec)). The constant is derived based on the active area of the device with silicon and epoxy at the interface of the heat generation.

The Cauer networks generally have physical significance and may be divided between nodes to separate thermal behavior due to one portion of the network from another. The Foster networks, though when sorted by time constant (as above) bear a rough correlation with the Cauer networks, are really only convenient mathematical models. Cauer networks can be easily implemented using circuit simulating tools, whereas Foster networks may be more easily implemented using mathematical tools (for instance, in a spreadsheet program), according to the following formula:

$$R(t) = \sum_{i=1}^{n} R_i \left(1 - e^{-t/tau_i}\right)$$

θJA vs Copper Spreader Area

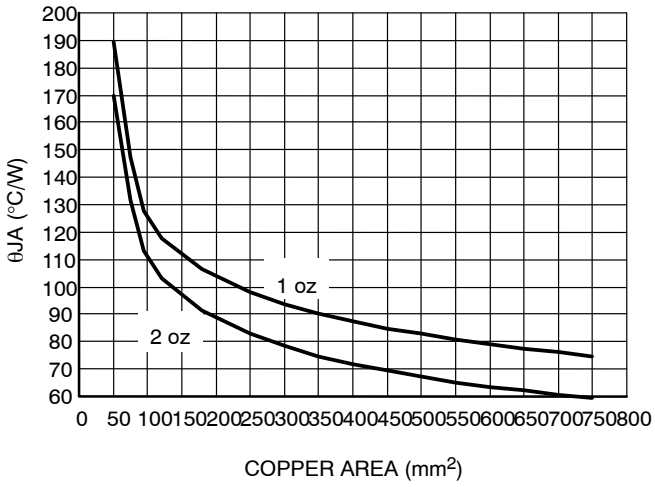


Figure 35. SOIC 8−Lead EP θJA as a Function of the Pad Copper Area Including Traces, Board Material

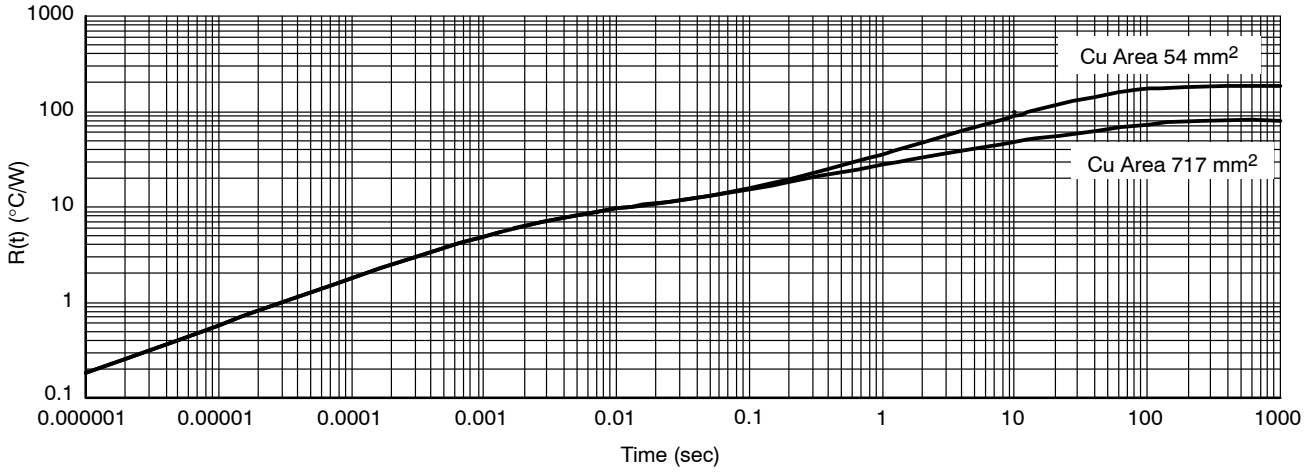


Figure 36. SOIC 8−Lead EP Single Pulse Heating Curve

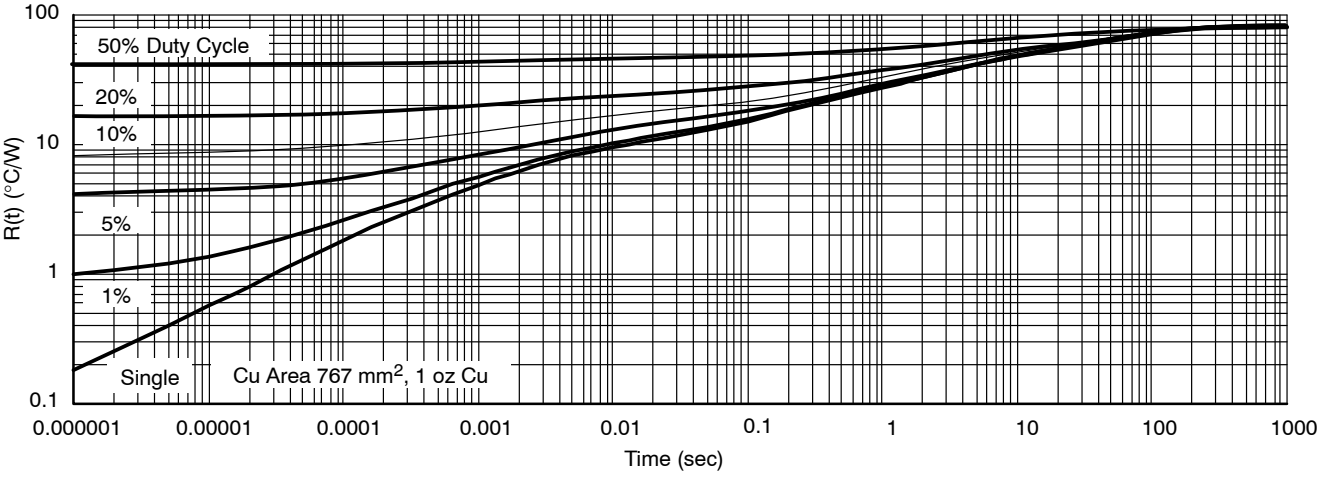


Figure 37. SOIC 8−Lead Thermal Duty Cycle Curves on 1” Spreader Test Board

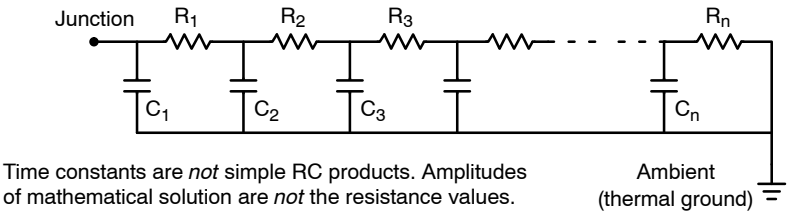


Figure 38. Grounded Capacitor Thermal Network (“Cauer” Ladder)

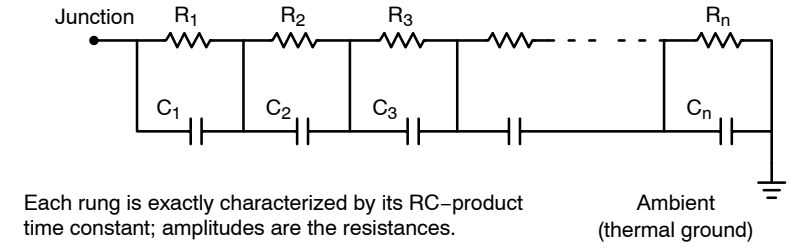


Figure 39. Non−Grounded Capacitor Thermal Ladder (“Foster” Ladder)

APPLICATION NOTES

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 40) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

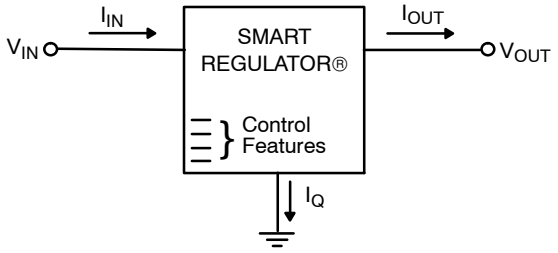


Figure 40. Single Output Regulator with Key Performance Parameters Labeled

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$s less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV8508DW50G	5.0 V	SO−16L (Pb−Free)	47 Units / Rail
NCV8508DW50R2G	5.0 V	SO−16L (Pb−Free)	1000 / Tape & Reel
NCV8508D2T50G	5.0 V	D^2PAK−7 (Pb−Free)	50 Units / Rail
NCV8508D2T50R4G	5.0 V	D^2PAK−7 (Pb−Free)	750 / Tape & Reel
NCV8508PD50G	5.0 V	SO−8 EP (Pb−Free)	98 Units / Rail
NCV8508PD50R2G	5.0 V	SO−8 EP (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

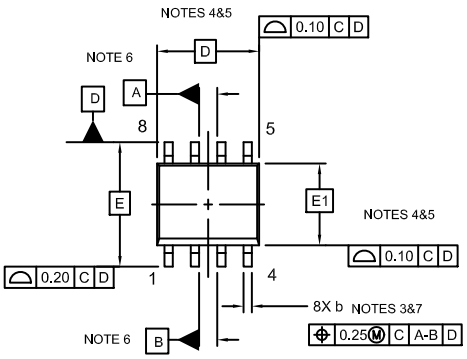
SCALE 1:1

SOIC−8 EP
CASE 751AC
ISSUE D

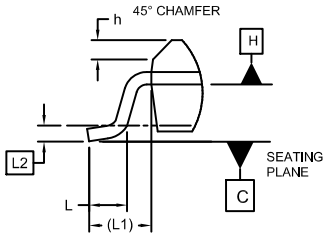
DATE 02 APR 2019

NOTES:

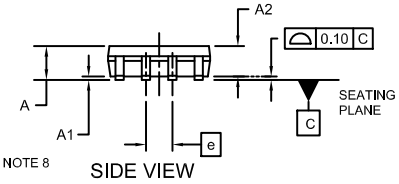
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



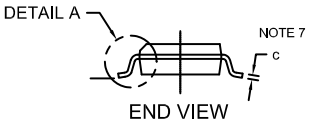
TOP VIEW



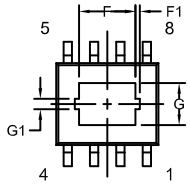
DETAIL A



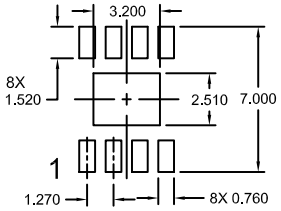
SIDE VIEW



END VIEW



BOTTOM VIEW

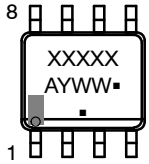


RECOMMENDED
MOUNTING FOOTPRINT*

DIM	MILLIMETERS		
	MIN.	NOM..	MAX.
A	1.35	1.55	1.75
A1	−−−	0.05	0.10
A2	1.35	1.50	1.65
b	0.31	0.41	0.51
c	0.17	0.21	0.23
D	4.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
F	2.24	2.72	3.20
F1	0.15	0.20	0.25
G	1.55	2.03	2.51
G1	0.41	0.46	0.51
h	0.25	0.38	0.50
L	0.40	0.84	1.27
L1	1.04 REF		
L2	0.25 REF		
Ø	0°	4°	8°

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D."

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present and may be in either location. Some products may not follow the Generic Marking.

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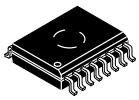
DESCRIPTION:	SOIC−8 EP	PAGE 1 OF 1

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021



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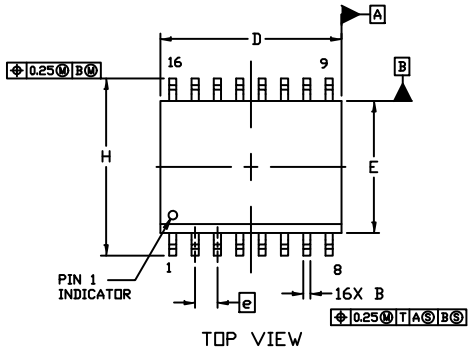
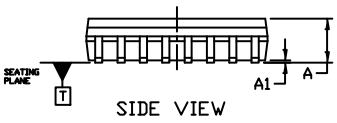
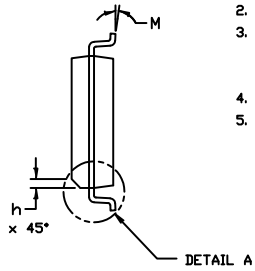
SCALE 1:1



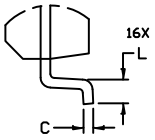
TOP VIEW



SIDE VIEW



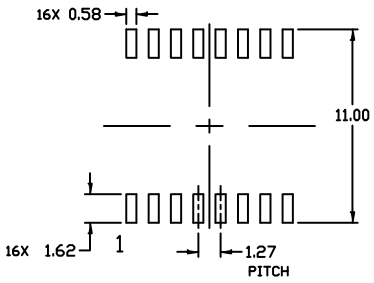
END VIEW



DETAIL A
2X SCALE

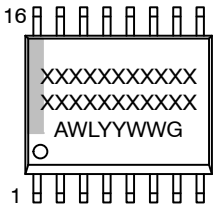
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

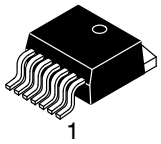
DOCUMENT NUMBER:	**98ASB42567B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

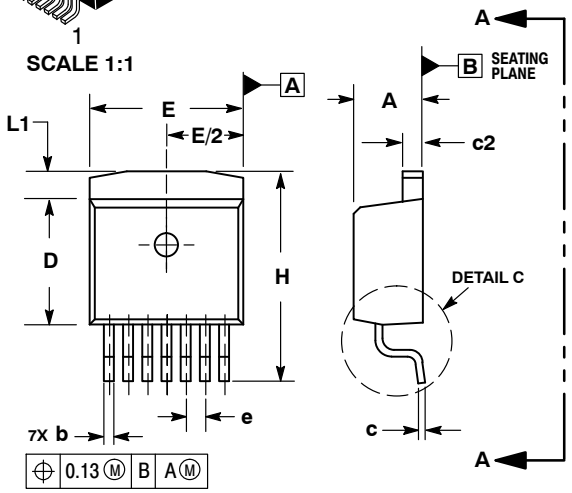
ON Semiconductor®

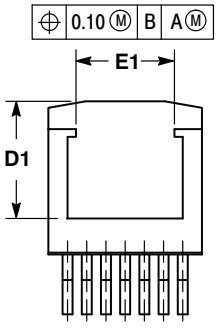
D²PAK–7 (SHORT LEAD)
CASE 936AB–01
ISSUE B

DATE 08 SEP 2009

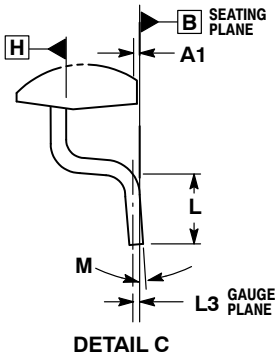


SCALE 1:1





VIEW A–A

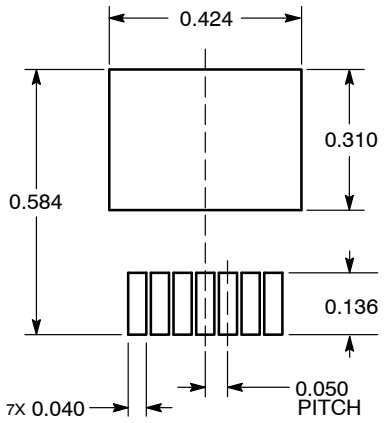


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	---	6.86	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

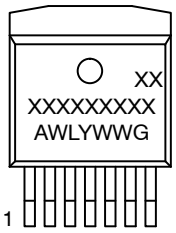
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb–Free Package

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DESCRIPTION:	D²PAK–7 (SHORT LEAD)	PAGE 1 OF 1

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