Linear Voltage Regulator - Fast Transient Response, Enable
500 mA

NCP177

The NCP177 is CMOS LDO regulator featuring 500 mA output current. The input voltage is as low as 1.6 V and the output voltage can be set from 0.7 V.

Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Output Voltage Range: 0.7 V to 3.6 V
- Quiescent Current typ. 60 μA
- Low Dropout: 200 mV Typ. at 500 mA, $V_{OUT-NOM}$ = 1.8 V
- High Output Voltage Accuracy ±0.8%
- Stable with Small 1 μF Ceramic Capacitors
- Over−current Protection
- Thermal Shutdown Protection: 175°C
- With (NCP177A) and Without (NCP177B) Output Discharge Function
- Available in XDFN4 1 mm x 1 mm x 0.4 mm Package
- This is a Pb−Free Device

Typical Applications

- Battery Powered Equipment
- Portable Communication Equipment
- Cameras, Image Sensors and Camcorders

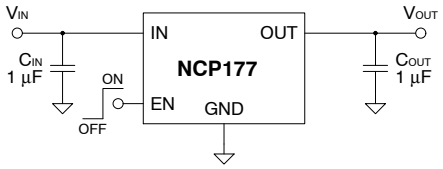

Figure 1. Typical Application Schematic

ON Semiconductor®

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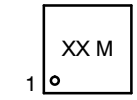
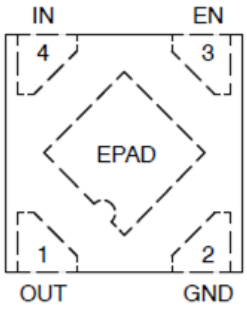
XDFN4
CASE 711AJ

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

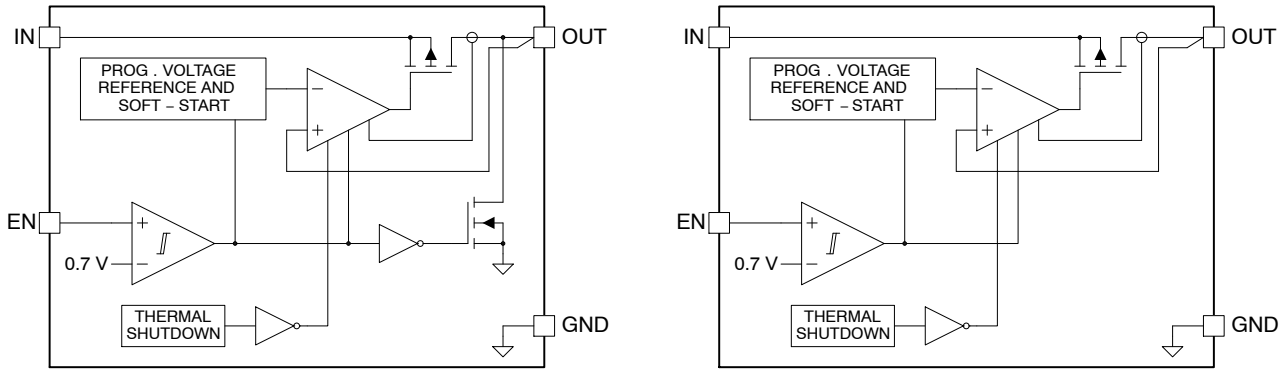
PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.



NCP177A (with output active discharge) NCP177B (without output active discharge)

Figure 2. Internal Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin
2	GND	Power supply ground pin
3	EN	Enable pin (active “H”)
4	IN	Power supply input voltage pin
–	EPAD	Exposed pad should be tied to ground plane for better power dissipation

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	IN	−0.3 to 6.0	V
Output Voltage	OUT	−0.3 to V_{IN} + 0.3	V
Chip Enable Input	EN	−0.3 to 6.0	V
Output Current	I_{OUT}	Internally Limited	mA
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114
   ESD Machine Model tested per JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 (Note 3) Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	223	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C
The specifications in bold are guaranteed at −40°C ≤ T_J ≤ 85°C. (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Input Voltage			V_{IN}	1.6		5.5	V
Output Voltage	V_{OUT_NOM} ≥ 1.8 V	T_J = +25°C	V_{OUT}	−0.8		0.8	%
		−40°C ≤ T_J ≤ 85°C		−2.0		1.0	
	V_{OUT_NOM} < 1.8 V	T_J = +25°C		−1.2		1.2	
		−40°C ≤ T_J ≤ 85°C		−2.5		1.5	
Line Regulation	V_{IN} = $V_{OUT-NOM}$ + 0.5 V to 5.25 V V_{IN} ≥ 1.6 V		LineReg		0.02	**0.1**	%/V
Load Regulation	1 mA ≤ I_{OUT} ≤ 500 mA, V_{IN} ≥ 1.75 V		LoadReg		1	**10**	mV
Dropout Voltage (Note 5)	I_{OUT} = 500 mA	1.4 V ≤ V_{OUT} < 1.8 V	V_{DO}		295	**380**	mV
		1.8 V ≤ V_{OUT} < 2.1 V			200	**285**	
		2.1 V ≤ V_{OUT} < 2.5 V			160	**240**	
		2.5 V ≤ V_{OUT} < 3.0 V			130	**200**	
		3.0 V ≤ V_{OUT} < 3.6 V			110	**175**	
Quiescent Current	I_{OUT} = 0 mA		I_Q		60	**90**	μA
Standby Current	V_{EN} = 0 V		I_{STBY}		0.1	**1**	μA
Output Current Limit	V_{OUT} = $V_{OUT-NOM}$ − 100 mV, V_{IN} ≥ 1.75 V		I_{OUT}	**510**	800		mA
	V_{OUT} = $V_{OUT-NOM}$ − 100 mV, V_{IN} ≥ 1.6 V			**300**	600		
Short Circuit Current	V_{OUT} = 0 V, V_{IN} ≥ 1.75 V		I_{SC}	**510**	800		mA
EN Pin Threshold Voltage	EN Input Voltage “H”		V_{ENH}	**1.0**			V
	EN Input Voltage “L”		V_{ENL}			**0.4**	
Enable Input Current	V_{EN} = V_{IN} = 5.5 V		I_{EN}		0.15	**0.6**	μA
Power Supply Rejection Ratio	f = 1 kHz, Ripple 0.2 Vp−p, V_{IN} = $V_{OUT-NOM}$ + 1.0 V, I_{OUT} = 30 mA (V_{OUT} ≤ 2.0 V, V_{IN} = 3.0 V)		PSRR		75		dB
Output Noise	f = 10 Hz to 100 kHz				54		μV_{RMS}
Output Discharge Resistance (NCP177A option only)	V_{IN} = 4.0 V, V_{EN} = 0 V, V_{OUT} = $V_{OUT-NOM}$		R_{ACTDIS}		60		Ω
Thermal Shutdown Temperature	Temperature rising from 25°C		T_{SD_TEMP}		175		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD_TEMP}		T_{SD_HYST}		20		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Measured when the output voltage falls 3% below the nominal output voltage (the voltage measured under the condition V_{IN} = $V_{OUT-NOM}$ + 0.5 V).

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C

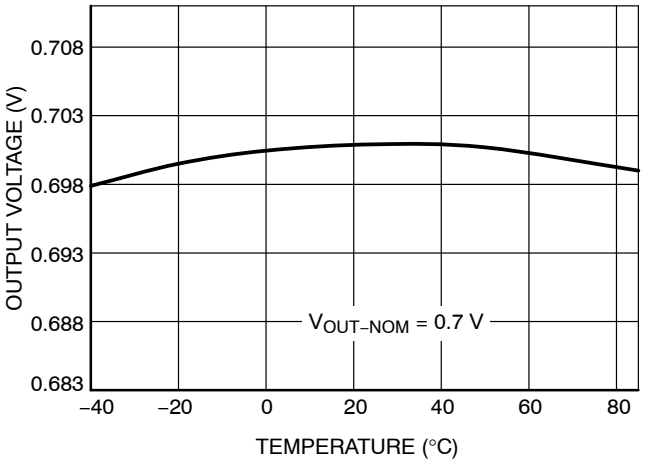


Figure 3. Output Voltage vs. Temperature

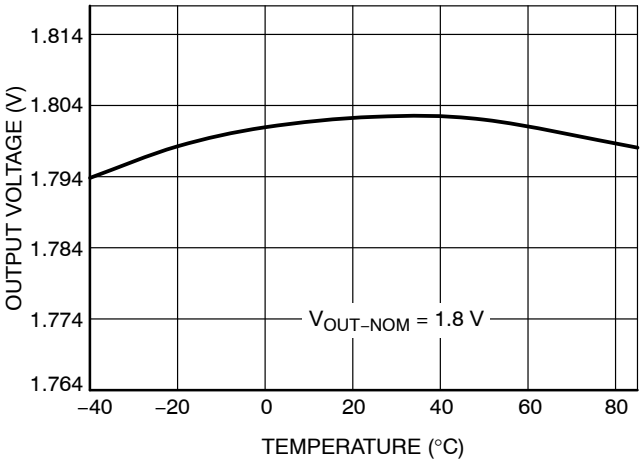


Figure 4. Output Voltage vs. Temperature

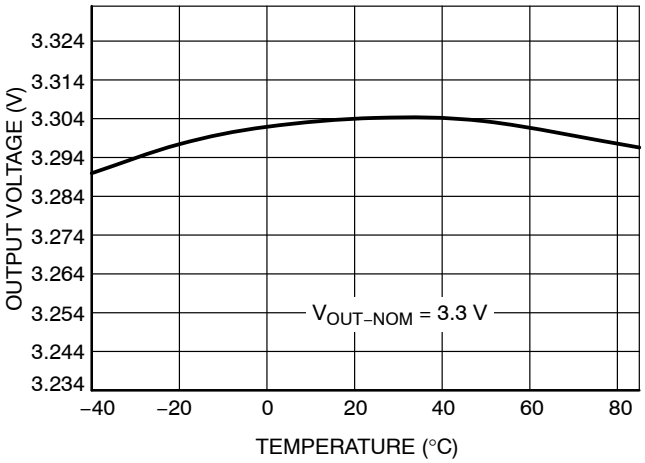


Figure 5. Output Voltage vs. Temperature

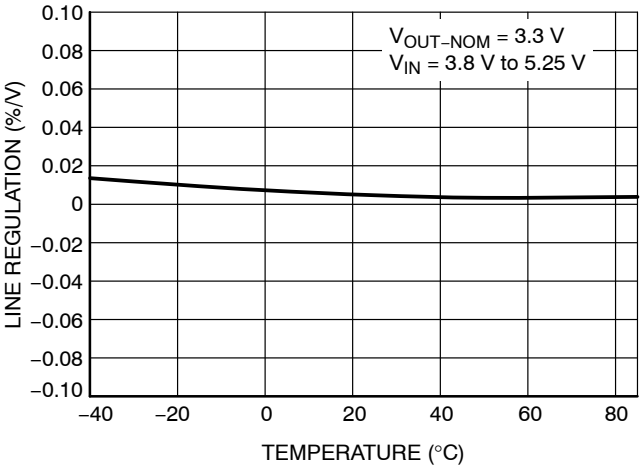


Figure 6. Line Regulation vs. Temperature

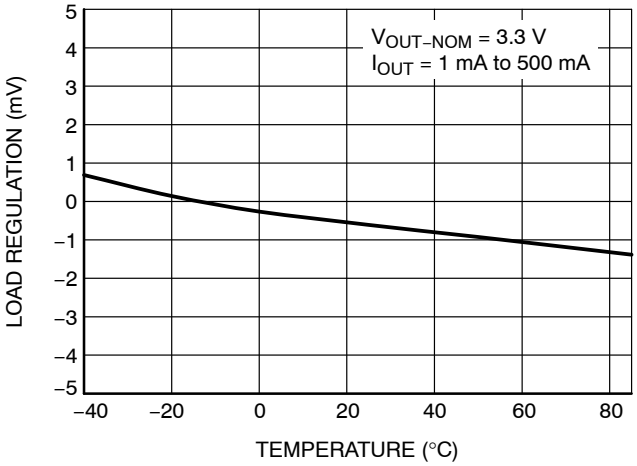


Figure 7. Load Regulation vs. Temperature

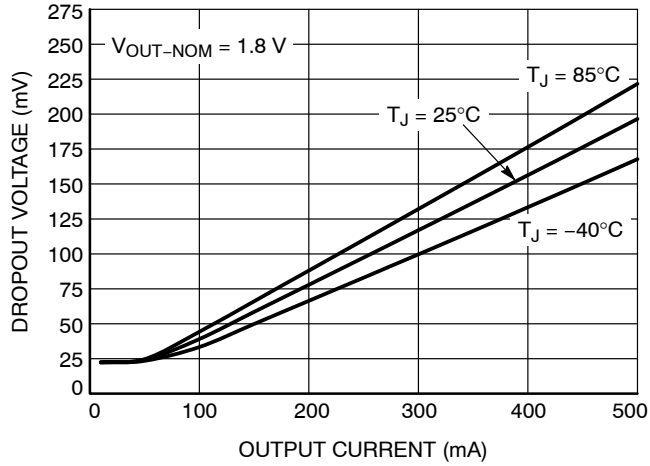


Figure 8. Dropout Voltage vs. Output Current

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C

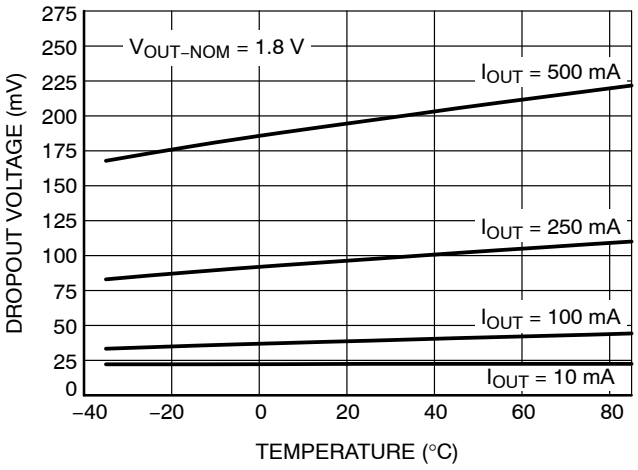


Figure 9. Dropout Voltage vs. Temperature

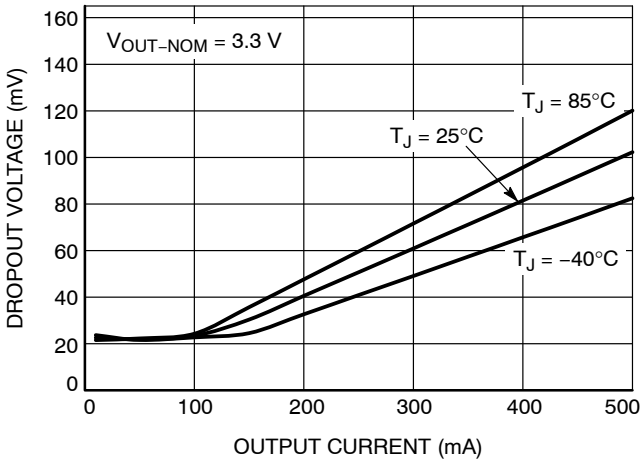


Figure 10. Dropout Voltage vs. Output Current

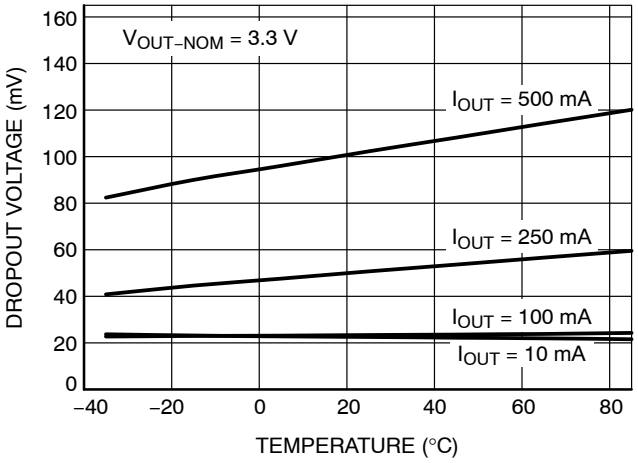


Figure 11. Dropout Voltage vs. Temperature

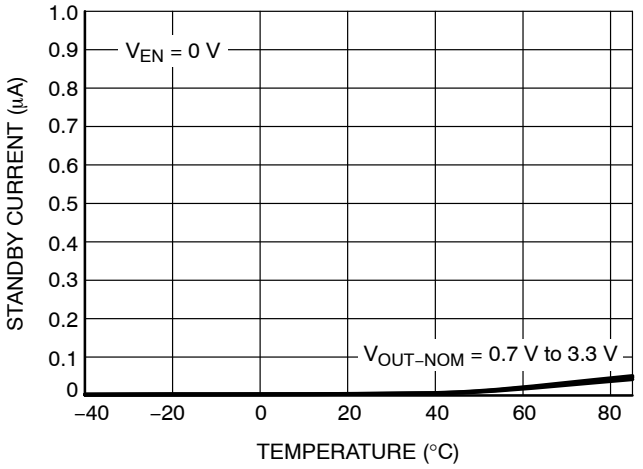


Figure 12. Standby Current vs. Temperature

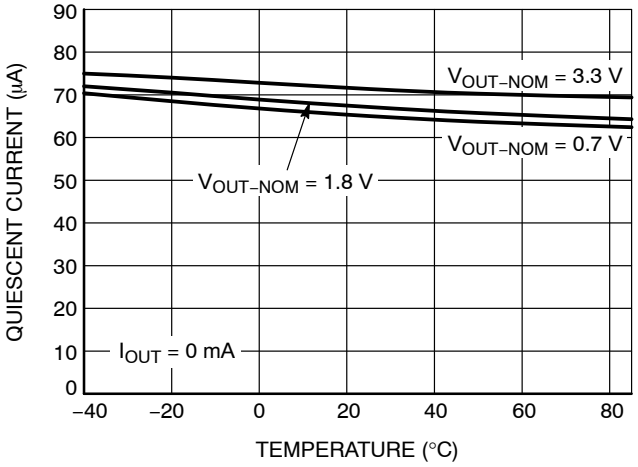


Figure 13. Quiescent Current vs. Temperature

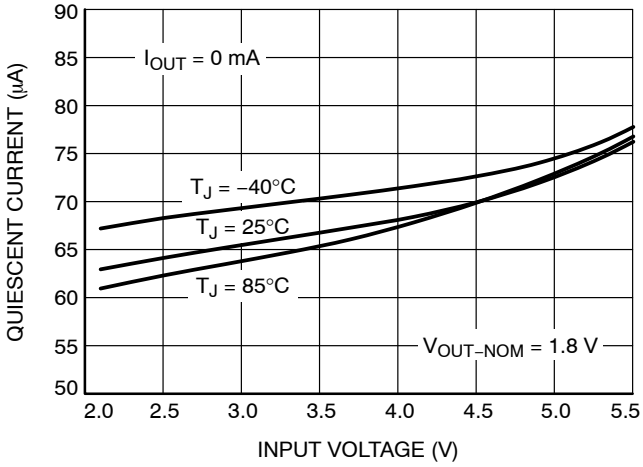


Figure 14. Quiescent Current vs. Input Voltage

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C

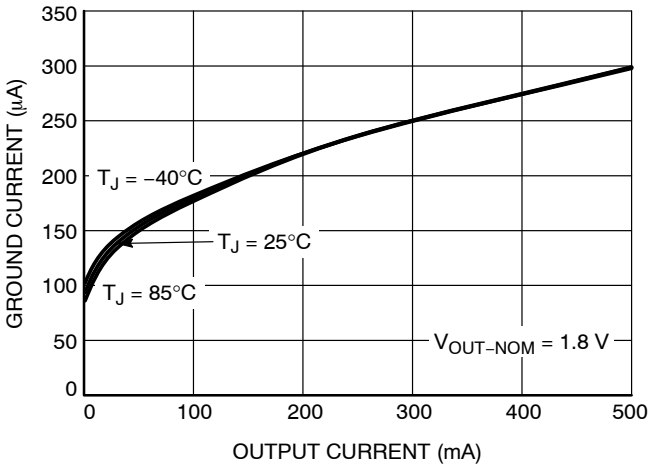


Figure 15. Ground Current vs. Output Current

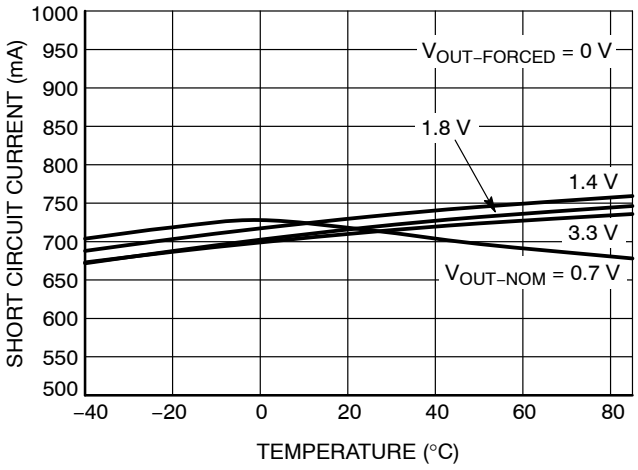


Figure 16. Short Circuit Current vs. Temperature

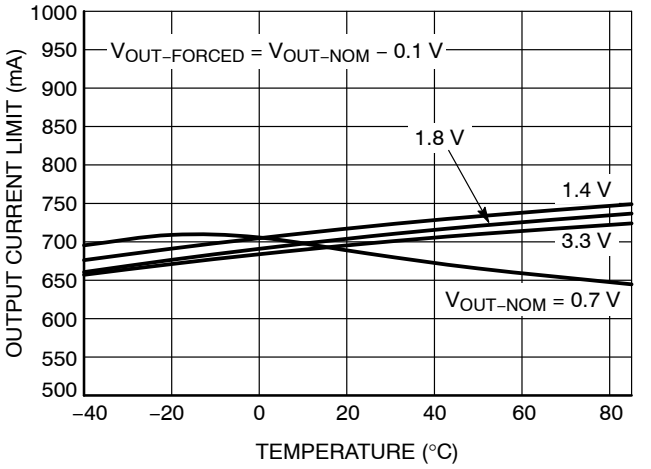


Figure 17. Output Current Limit vs. Temperature

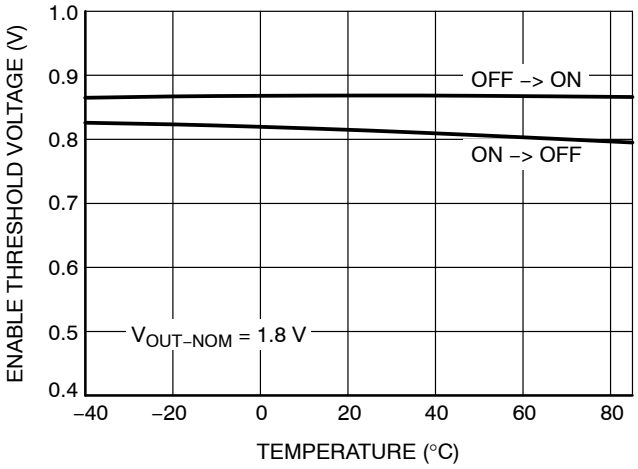


Figure 18. Enable Threshold Voltage vs. Temperature

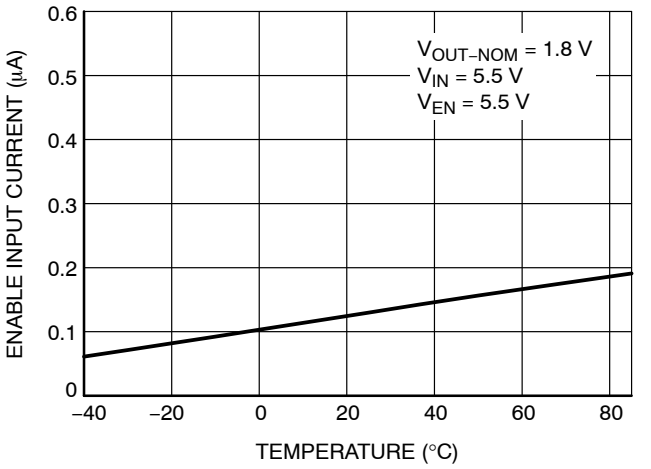


Figure 19. Enable Input Current vs. Temperature

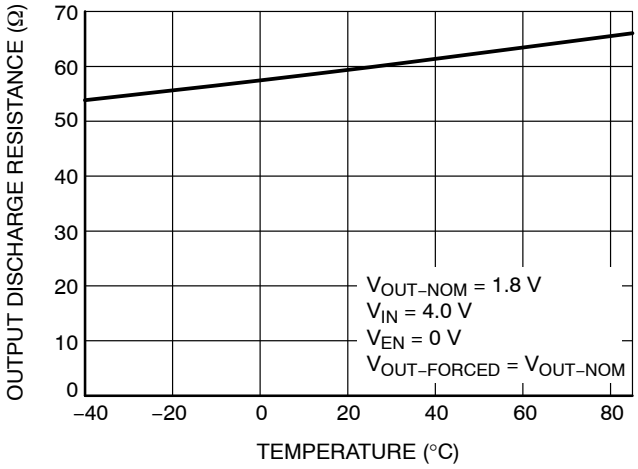


Figure 20. Output Discharge Resistance vs. Temperature (NCP177A option only)

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C

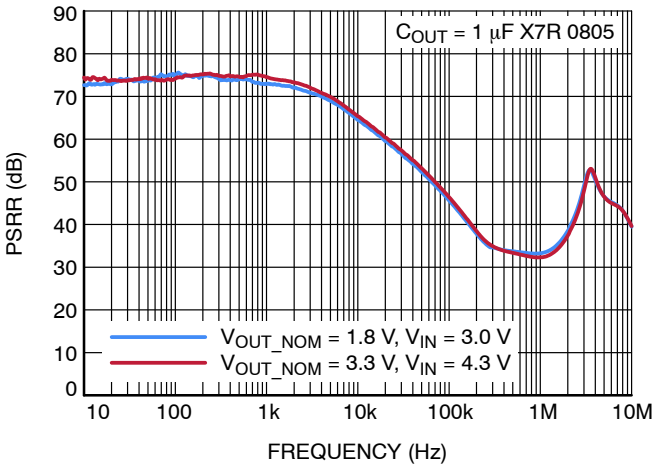


Figure 21. Power Supply Rejection Ratio

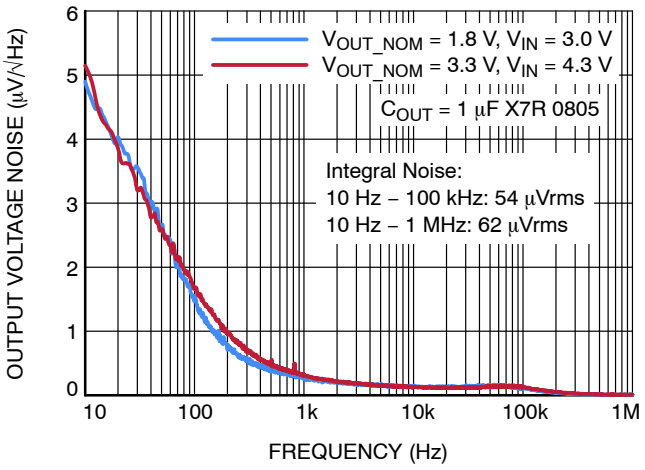


Figure 22. Output Voltage Noise Spectral Density

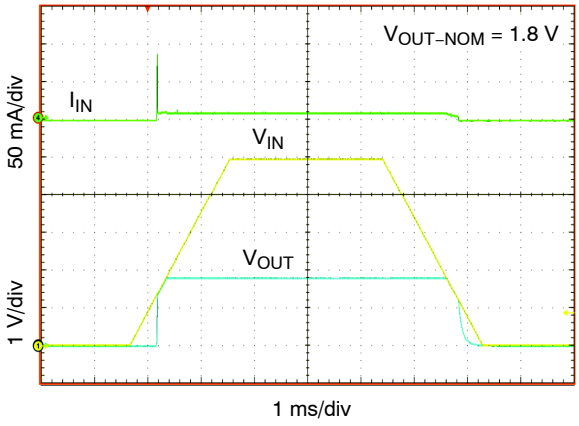


Figure 23. Turn−ON/OFF − VIN Driven (slow)

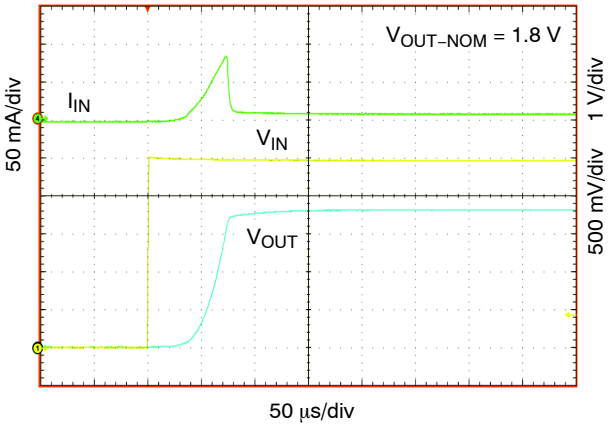


Figure 24. Turn−ON − VIN Driven (fast)

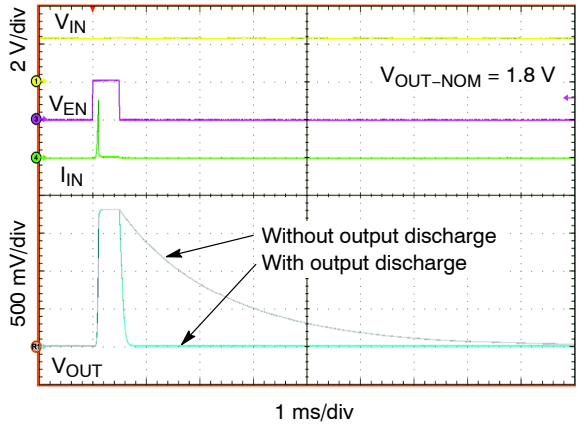


Figure 25. Turn−ON/OFF − EN Driven

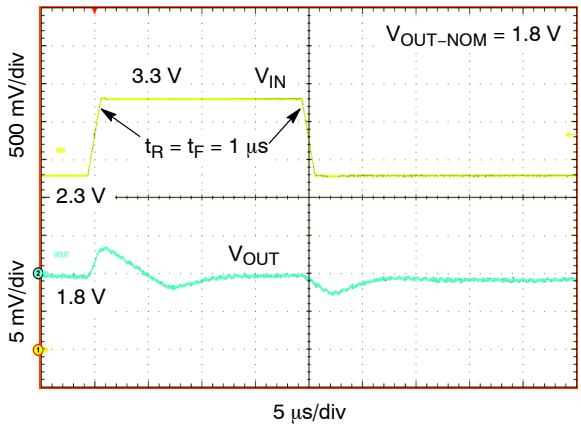


Figure 26. Line Transient Response

TYPICAL CHARACTERISTICS

V_{IN} = $V_{OUT-NOM}$ + 0.5 V or V_{IN} = 1.6 V (whichever is higher), V_{EN} = 1.2 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF, T_J = 25°C

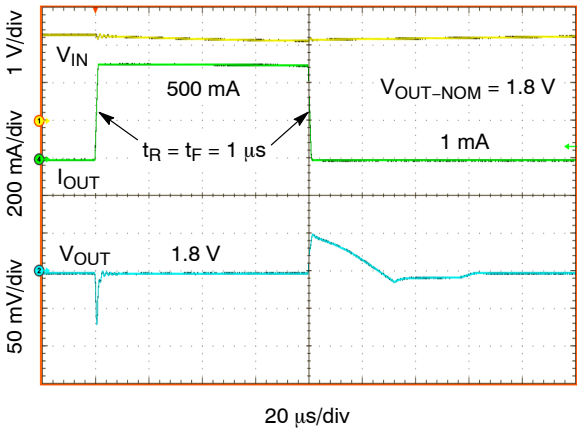


Figure 27. Load Transient Response

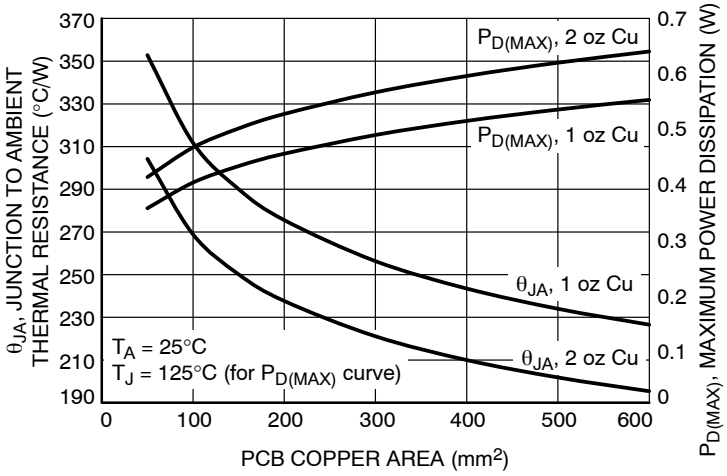


Figure 28. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area

APPLICATIONS INFORMATION

General

The NCP177 is a high performance 500 mA low dropout linear regulator (LDO) delivering excellent noise and dynamic performance. Thanks to its adaptive ground current behavior the device consumes only 60 μA of quiescent current (no−load condition).

The regulator features low noise of 48 μV_{RMS}, PSRR of 75 dB at 1 kHz and very good line/load transient performance. Such excellent dynamic parameters, small dropout voltage and small package size make the device an ideal choice for powering the precision noise sensitive circuitry in portable applications.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as 100 nA typ. from the IN pin.

The device is fully protected in case of output overload, output short circuit condition or overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater for the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto the input voltage.

There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitor for its low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during load current changes.

Output Capacitor Selection (C_{OUT})

The LDO requires an output capacitor connected as close as possible to the output and ground pins. The recommended capacitor value is 1 μF, ceramic X7R or X5R type due to its low capacitance variations over the specified temperature range. The LDO is designed to remain stable with minimum effective capacitance of 0.8 μF. When selecting the capacitor the changes with temperature, DC bias and package size needs to be taken into account. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias voltage (refer the capacitor's datasheet for details).

There is no requirement for the minimum value of equivalent series resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 0.5 Ω. Larger capacitance and lower ESR improves the load transient response and high frequency PSRR. Only ceramic capacitors are recommended, the other types like tantalum capacitors not due to their large ESR.

Enable Operation

The LDO uses the EN pin to enable/disable its operation and to deactivate/activate the output discharge function (A−version only).

If the EN pin voltage is < 0.4 V the device is disabled and the pass transistor is turned off so there is no current flow between the IN and OUT pins. On A−version the active discharge transistor is active so the output voltage is pulled to GND through 60 Ω (typ.) resistor.

If the EN pin voltage is > 1.0 V the device is enabled and regulates the output voltage. The active discharge transistor is turned off.

The EN pin has internal pull−down current source with value of 300 nA typ. which assures the device is turned off when the EN pin is unconnected. In case when the EN function isn't required the EN pin should be tied directly to IN pin.

Output Current Limit

Output current is internally limited to a 750 mA typ. The LDO will source this current when the output voltage drops down from the nominal output voltage (test condition is $V_{OUT-NOM}$ − 100 mV). If the output voltage is shorted to ground, the short circuit protection will limit the output current to 700 mA typ. The current limit and short circuit protection will work properly over the whole temperature and input voltage ranges. There is no limitation for the short circuit duration.

Thermal Shutdown

When the LDO's die temperature exceeds the thermal shutdown threshold value the device is internally disabled. The IC will remain in this state until the die temperature decreases by value called thermal shutdown hysteresis. Once the IC temperature falls this way the LDO is back enabled. The thermal shutdown feature provides the protection against overheating due to some application failure and it is not intended to be used as a normal working function.

Power Dissipation

Power dissipation caused by voltage drop across the LDO and by the output current flowing through the device needs to be dissipated out from the chip. The maximum power dissipation is dependent on the PCB layout, number of used Cu layers, Cu layers thickness and the ambient temperature. The maximum power dissipation can be computed by following equation:

$$P_{D(MAX)} = \frac{T_J - T_A}{\theta_{JA}} = \frac{125 - T_A}{\theta_{JA}} \text{ [W]} \qquad \text{(eq. 1)}$$

Where: $(T_J - T_A)$ is the temperature difference between the junction and ambient temperatures and θ_{JA} is the thermal resistance (dependent on the PCB as mentioned above).

For reliable operation junction temperature should be limited do +125°C.

The power dissipated by the LDO for given application conditions can be calculated by the next equation:

$$P_D = V_{IN} \cdot I_{GND} + \left(V_{IN} - V_{OUT}\right) \cdot I_{OUT} \text{ [W]} \qquad \text{(eq. 2)}$$

Where: I_{GND} is the LDO's ground current, dependent on the output load current.

Connecting the exposed pad and N/C pin to a large ground planes helps to dissipate the heat from the chip.

The relation of θ_{JA} and $P_{D(MAX)}$ to PCB copper area and Cu layer thickness could be seen on the Figure 26.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case when $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Power Supply Rejection Ratio

The LDO features very high power supply rejection ratio. The PSRR at higher frequencies (in the range above 100 kHz) can be tuned by the selection of C_{OUT} capacitor and proper PCB layout. A simple LC filter could be added to the LDO's IN pin for further PSRR improvement.

Enable Turn−On Time

The enable turn−on time is defined as the time from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT-NOM}$, C_{OUT} and T_A.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors as close as possible to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors size with appropriate effective capacitance.

Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Power Dissipation section). Exposed pad and N/C pin should be tied to the ground plane for good power dissipation.

ORDERING INFORMATION

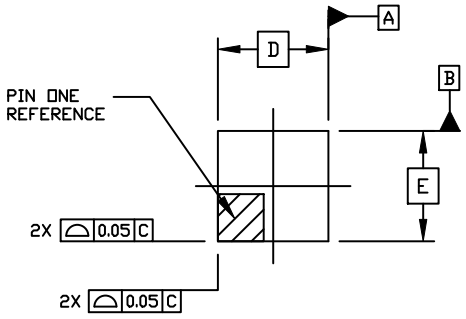
Part Number	Voltage Option	Option	Marking	Package	Shipping†
NCP177AMX070TCG	0.70 V	With output discharge	JA	XDFN−4 (Pb−Free)	3000 / Tape & Reel
NCP177AMX090TCG	0.90 V		JM		
NCP177AMX100TCG	1.00 V		JC		
NCP177AMX110TCG	1.10 V		JD		
NCP177AMX120TCG	1.20 V		JE		
NCP177AMX125TCG	1.25 V		JK		
NCP177AMX135TCG	1.35 V		JF		
NCP177AMX150TCG	1.50 V		JG		
NCP177AMX180TCG	1.80 V		JH		
NCP177AMX330TCG	3.30 V		JJ		
NCP177BMX070TCG	0.70 V	Without output discharge	HA		
NCP177BMX100TCG	1.00 V		HC		
NCP177BMX110TCG	1.10 V		HD		
NCP177BMX120TCG	1.20 V		HE		
NCP177BMX125TCG	1.25 V		HL		
NCP177BMX135TCG	1.35 V		HF		
NCP177BMX150TCG	1.50 V		HG		
NCP177BMX180TCG	1.80 V		HH		
NCP177BMX330TCG	3.30 V		HJ		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

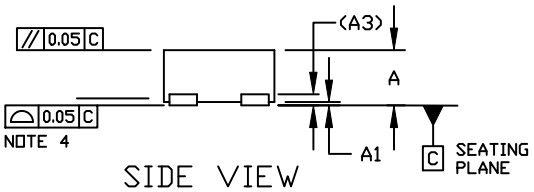
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

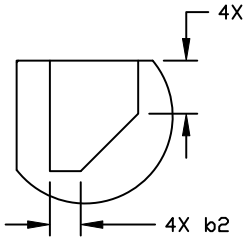
DATE 08 MAR 2022



TOP VIEW



SIDE VIEW

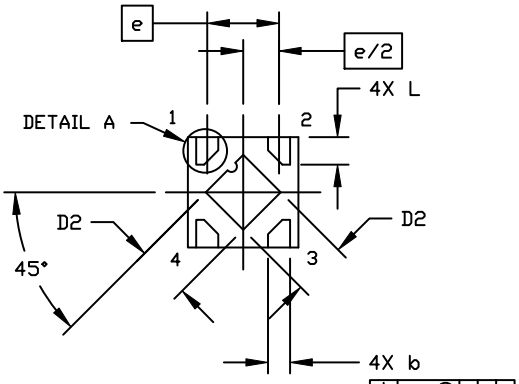


DETAIL A

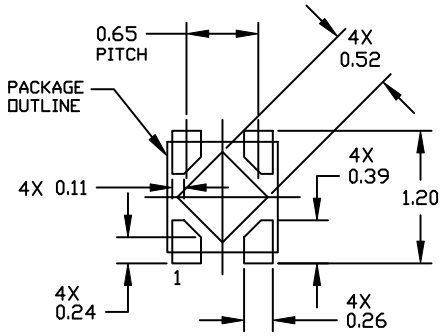
NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.33	0.38	0.43
A1	0.00	---	0.05
A3		0.10 REF	
b	0.15	0.20	0.25
b2	0.02	0.07	0.12
D	0.90	1.00	1.10
D2	0.43	0.48	0.53
E	0.90	1.00	1.10
e		0.65 BSC	
L	0.20		0.30
L2	0.07		0.17



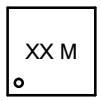
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**XDFN4, 1.0X1.0, 0.65P**	**PAGE 1 OF 1**

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