# LDO Regulator for RF and Analog Circuits - Ultra-Low Noise and High PSRR

## 250 mA

# NCP160

The NCP160 is a linear regulator capable of supplying 250 mA output current. Designed to meet the requirements of RF and analog circuits, the NCP160 device provides low noise, high PSRR, low quiescent current, and very good load/line transients. The device is designed to work with a 1 μF input and a 1 μF output ceramic capacitor. It is available in two thickness ultra−small 0.35P, 0.64 mm x 0.64 mm Chip Scale Package (CSP) and XDFN−4 0.65P, 1 mm x 1 mm.

### Features

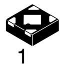
- Operating Input Voltage Range: 1.9 V to 5.5 V
- Available in Fixed Voltage Option: 1.8 V to 5.14 V
- ±2% Accuracy Over Load/Temperature
- Ultra Low Quiescent Current Typ. 18 μA
- Standby Current: Typ. 0.1 μA
- Very Low Dropout: 80 mV at 250 mA
- Ultra High PSRR: Typ. 98 dB at 20 mA, f = 1 kHz
- Ultra Low Noise: 10 $\mu V_{RMS}$
- Stable with a 1 μF Small Case Size Ceramic Capacitors
- Available in −WLCSP4 0.64 mm x 0.64 mm x 0.4 mm
  −WLCSP4 0.64 mm x 0.64 mm x 0.33 mm
  −XDFN4 1 mm x 1 mm x 0.4 mm
- These Devices are Pb−Free and are RoHS Compliant

### Typical Applications

- Battery−powered Equipment
- Wireless LAN Devices
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

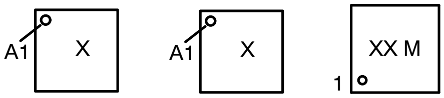
**WLCSP4**
**CASE 567JZ**

**WLCSP4**
**CASE 567KA**



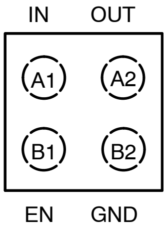
**XDFN4**
**CASE 711AJ**

### MARKING DIAGRAMS

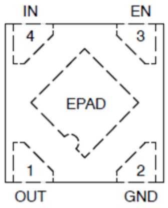


X or XX = Specific Device Code
M = Date Code

### PIN CONNECTIONS



(Top View)



(Top View)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page NO TAG of this data sheet.

**November, 2021 − Rev. 18**

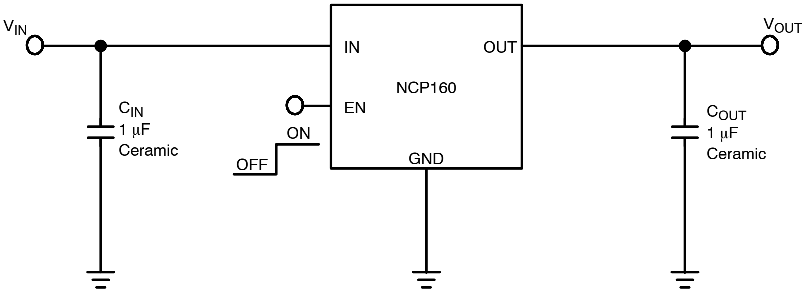


Figure 1. Typical Application Schematics

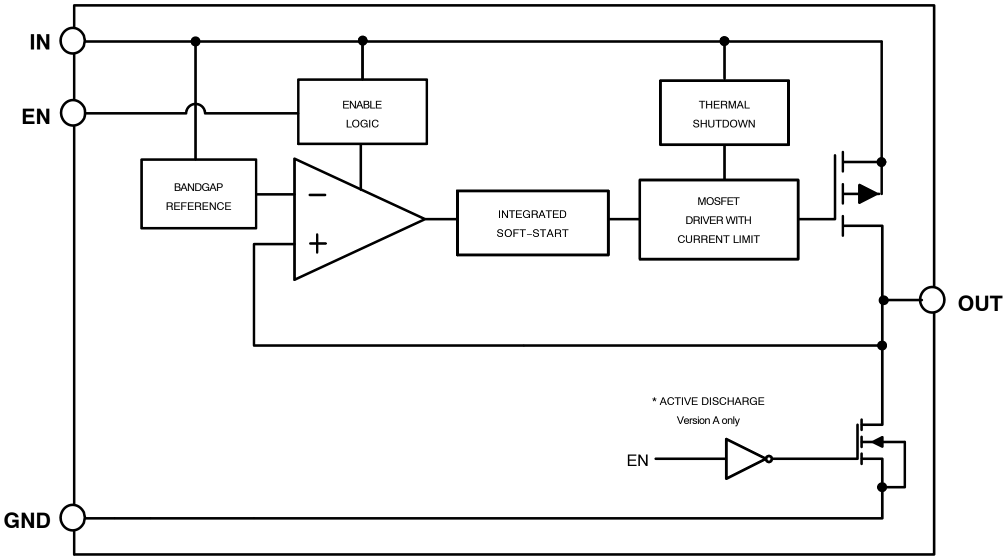


Figure 2. Simplified Schematic Block Diagram

## PIN FUNCTION DESCRIPTION

| Pin No. CSP4 | Pin No. XDFN4 | Pin Name | Description |
|---|---|---|---|
| A1 | 4 | IN | Input voltage supply pin |
| A2 | 1 | OUT | Regulated output voltage. The output should be bypassed with small 1 μF ceramic capacitor. |
| B1 | 3 | EN | Chip enable: Applying $V_{EN}$ < 0.4 V disables the regulator, Pulling $V_{EN}$ > 1.2 V enables the LDO. |
| B2 | 2 | GND | Common ground connection |
| – | EPAD | EPAD | Expose pad can be tied to ground plane for better power dissipation |

### ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (Note 1) | $V_{IN}$ | −0.3 V to 6 | V |
| Output Voltage | $V_{OUT}$ | −0.3 to $V_{IN}$ + 0.3, max. 6 | V |
| Chip Enable Input | $V_{CE}$ | −0.3 V to 6 | V |
| Output Short Circuit Duration | $t_{SC}$ | unlimited | s |
| Maximum Junction Temperature | $T_J$ | 150 | °C |
| Storage Temperature | $T_{STG}$ | −55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2000 | V |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

### THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, CSP4 (Note 3)<br>Thermal Resistance, Junction−to−Air | $R_{\theta JA}$ | 108 | °C/W |
| Thermal Characteristics, XDFN4 (Note 3)<br>Thermal Resistance, Junction−to−Air | | 198.1 | |

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

**ELECTRICAL CHARACTERISTICS** $-40°C \le T_J \le 125°C$; $V_{IN} = V_{OUT(NOM)} + 1$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT} = 1$ µF, unless otherwise noted. $V_{EN} = 1.2$ V. Typical values are at $T_J = +25°C$ (Note 4).

| Parameter | Test Conditions | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Input Voltage | | | $V_{IN}$ | 1.9 | | 5.5 | V |
| Output Voltage Accuracy | $V_{IN} = V_{OUT(NOM)} + 1$ V<br>$0 \text{ mA} \le I_{OUT} \le 250$ mA | | $V_{OUT}$ | −2 | | +2 | % |
| Line Regulation | $V_{OUT(NOM)} + 1 \text{ V} \le V_{IN} \le 5.5$ V | | $Line_{Reg}$ | | 0.02 | | %/V |
| Load Regulation | $I_{OUT} = 1$ mA to 250 mA | | $Load_{Reg}$ | | 0.001 | | %/mA |
| Dropout Voltage (Note 5) | $I_{OUT} = 250$ mA | $V_{OUT(NOM)} = 1.8$ V | $V_{DO}$ | | 180 | 250 | mV |
| | | $V_{OUT(NOM)} = 2.5$ V | | | 110 | 175 | |
| | | $V_{OUT(NOM)} = 2.8$ V | | | 95 | 160 | |
| | | $V_{OUT(NOM)} = 2.85$ V | | | 95 | 160 | |
| | | $V_{OUT(NOM)} = 3.0$ V | | | 90 | 155 | |
| | | $V_{OUT(NOM)} = 3.2$ V | | | 85 | 149 | |
| | | $V_{OUT(NOM)} = 3.3$ V | | | 80 | 145 | |
| | | $V_{OUT(NOM)} = 3.5$ V | | | 75 | 140 | |
| | | $V_{OUT(NOM)} = 4.5$ V | | | 65 | 120 | |
| | | $V_{OUT(NOM)} = 5.0$ V | | | 75 | 105 | |
| | | $V_{OUT(NOM)} = 5.14$ V | | | 60 | 105 | |
| Output Current Limit | $V_{OUT} = 90\%\ V_{OUT(NOM)}$ | | $I_{CL}$ | 250 | 700 | | mA |
| Short Circuit Current | $V_{OUT} = 0$ V | | $I_{SC}$ | | 690 | | |
| Quiescent Current | $I_{OUT} = 0$ mA | | $I_Q$ | | 18 | 23 | µA |
| Shutdown Current | $V_{EN} \le 0.4$ V, $V_{IN} = 4.8$ V | | $I_{DIS}$ | | 0.01 | 1 | µA |
| EN Pin Threshold Voltage | EN Input Voltage “H” | | $V_{ENH}$ | 1.2 | | | V |
| | EN Input Voltage “L” | | $V_{ENL}$ | | | 0.4 | |
| EN Pull Down Current | $V_{EN} = 4.8$ V | | $I_{EN}$ | | 0.2 | 0.5 | µA |
| Turn−On Time | $C_{OUT} = 1$ µF, From assertion of $V_{EN}$ to $V_{OUT} = 95\%\ V_{OUT(NOM)}$ | | | | 120 | | µs |
| Power Supply Rejection Ratio | $I_{OUT} = 20$ mA | f = 100 Hz | PSRR | | 91 | | dB |
| | | f = 1 kHz | | | 98 | | |
| | | f = 10 kHz | | | 82 | | |
| | | f = 100 kHz | | | 48 | | |
| Output Voltage Noise | f = 10 Hz to 100 kHz | $I_{OUT} = 1$ mA | $V_N$ | | 14 | | $µV_{RMS}$ |
| | | $I_{OUT} = 250$ mA | | | 10 | | |
| Thermal Shutdown Threshold | Temperature rising | | $T_{SDH}$ | | 160 | | °C |
| | Temperature falling | | $T_{SDL}$ | | 140 | | °C |
| Active Output Discharge Resistance | $V_{EN} < 0.4$ V, Version A only | | $R_{DIS}$ | | 280 | | Ω |
| Line Transient (Note 6) | $V_{IN} = (V_{OUT(NOM)} + 1\text{ V})$ to $(V_{OUT(NOM)} + 1.6\text{ V})$ in 30 µs, $I_{OUT} = 1$ mA | | $Tran_{LINE}$ | −1 | | | mV |
| | $V_{IN} = (V_{OUT(NOM)} + 1.6\text{ V})$ to $(V_{OUT(NOM)} + 1\text{ V})$ in 30 µs, $I_{OUT} = 1$ mA | | | | | +1 | |
| Load Transient (Note 6) | $I_{OUT} = 1$ mA to 200 mA in 10 µs | | $Tran_{LOAD}$ | −40 | | | mV |
| | $I_{OUT} = 200$ mA to 1mA in 10 µs | | | | | +40 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when $V_{OUT}$ falls 100 mV below $V_{OUT(NOM)}$.
6. Guaranteed by design.

## TYPICAL CHARACTERISTICS

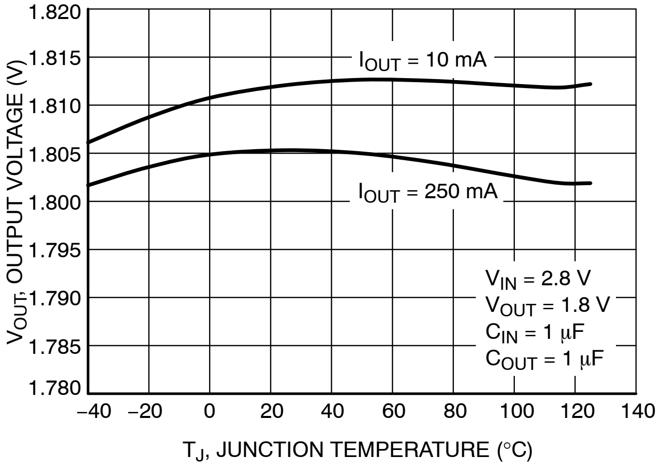


**Figure 3. Output Voltage vs. Temperature – $V_{OUT}$ = 1.8 V – XDFN Package**

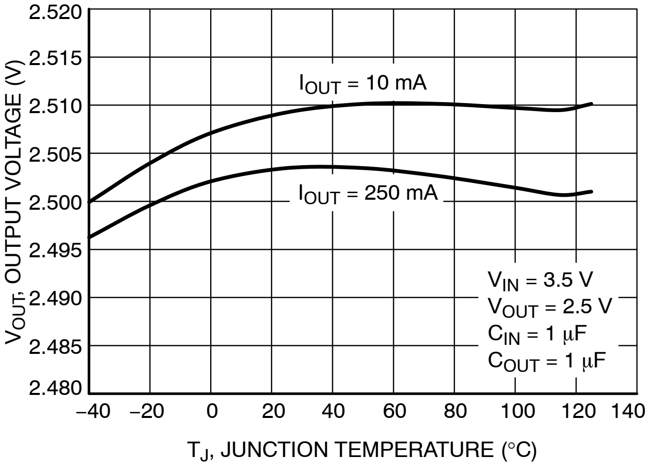


**Figure 4. Output Voltage vs. Temperature – $V_{OUT}$ = 2.5 V – XDFN Package**

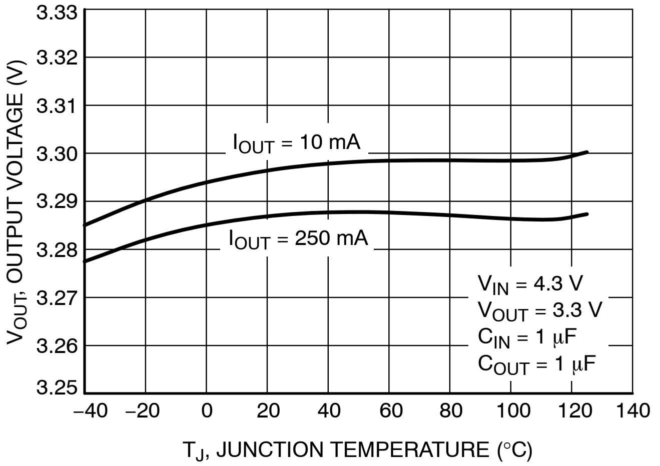


**Figure 5. Output Voltage vs. Temperature – $V_{OUT}$ = 3.3 V – XDFN Package**

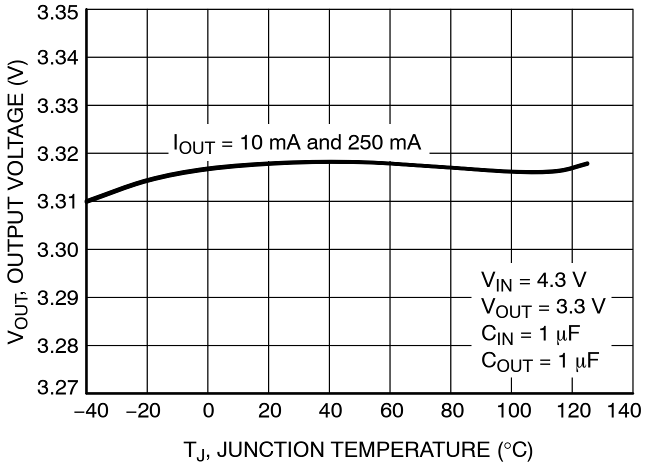


**Figure 6. Output Voltage vs. Temperature – $V_{OUT}$ = 3.3 V – CSP Package**

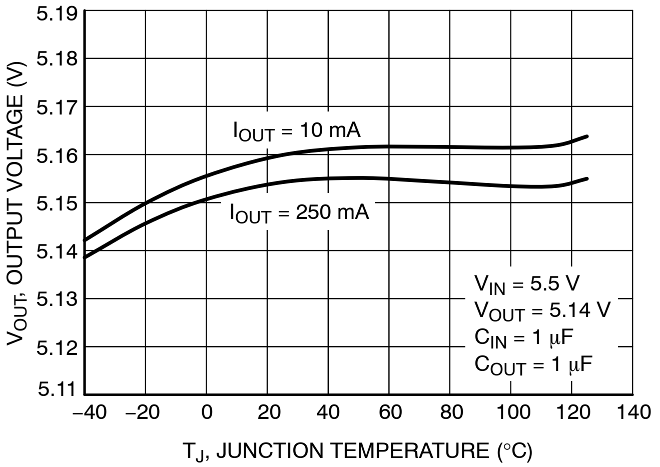


**Figure 7. Output Voltage vs. Temperature – $V_{OUT}$ = 5.14 V – XDFN Package**

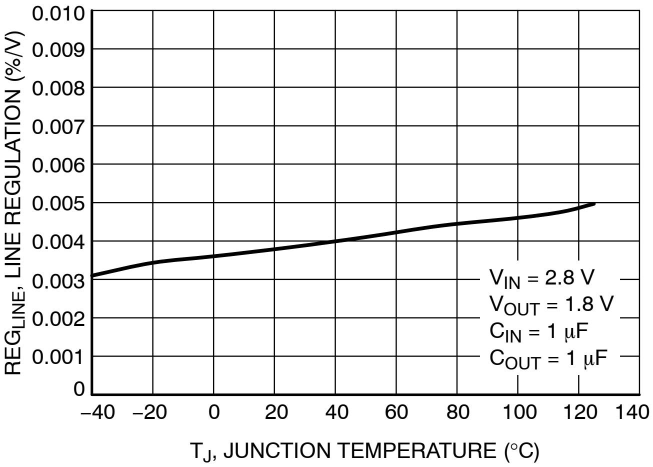


**Figure 8. Line Regulation vs. Temperature – $V_{OUT}$ = 1.8 V**

## TYPICAL CHARACTERISTICS

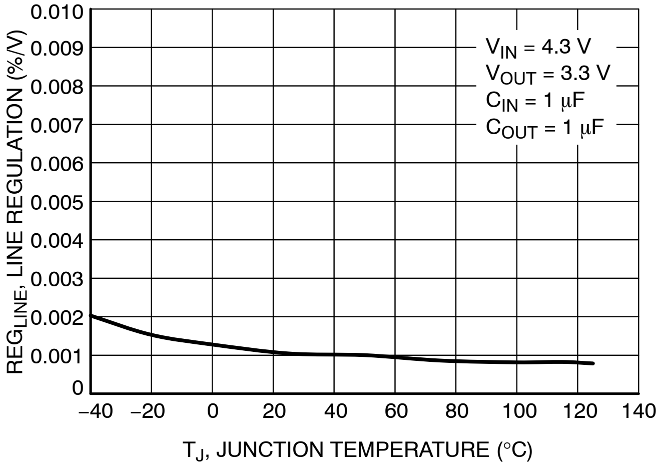


**Figure 9. Line Regulation vs. Temperature – $V_{OUT}$ = 3.3 V**

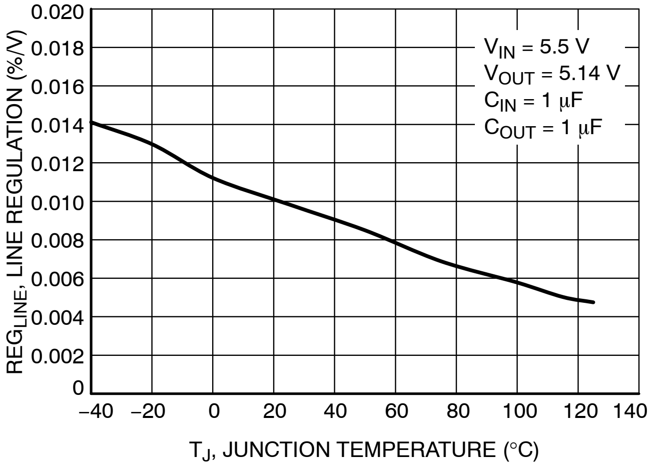


**Figure 10. Line Regulation vs. Temperature – $V_{OUT}$ = 5.14 V**

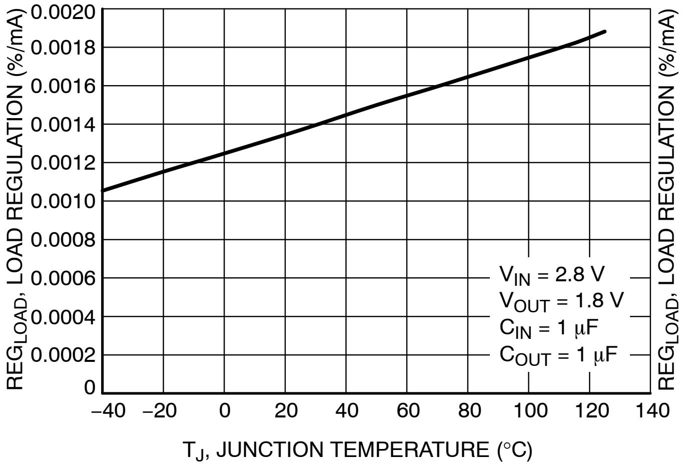


**Figure 11. Load Regulation vs. Temperature – $V_{OUT}$ = 1.8 V**

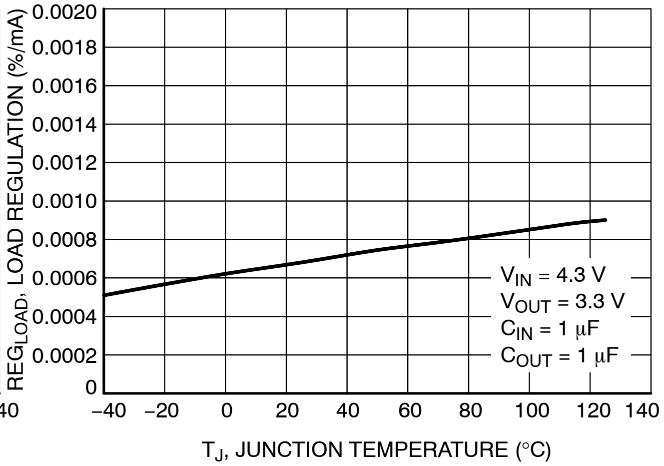


**Figure 12. Load Regulation vs. Temperature – $V_{OUT}$ = 3.3 V**

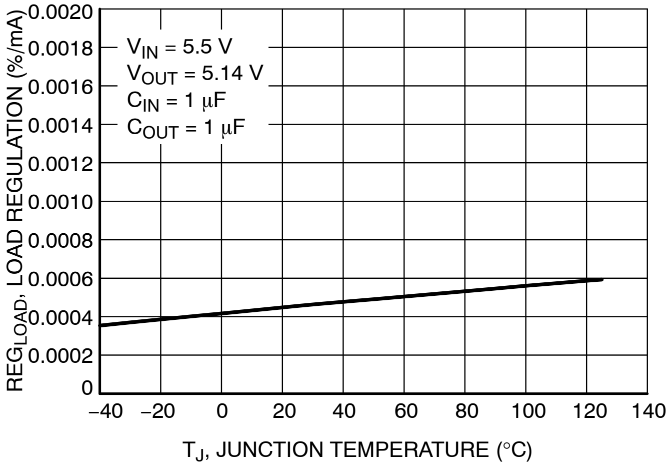


**Figure 13. Load Regulation vs. Temperature – $V_{OUT}$ = 5.14 V**

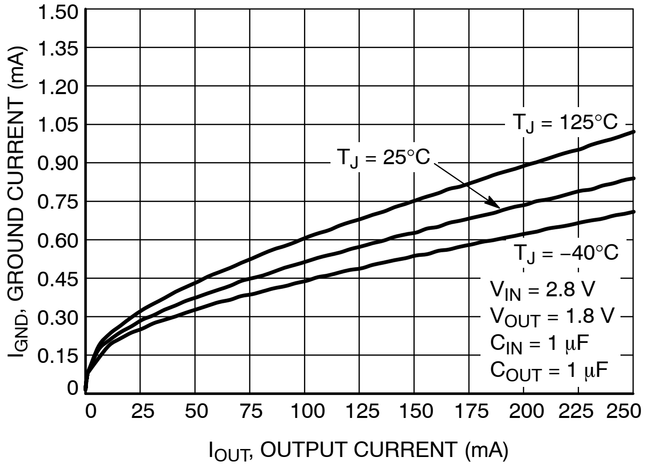


**Figure 14. Ground Current vs. Load Current – $V_{OUT}$ = 1.8 V**

## TYPICAL CHARACTERISTICS

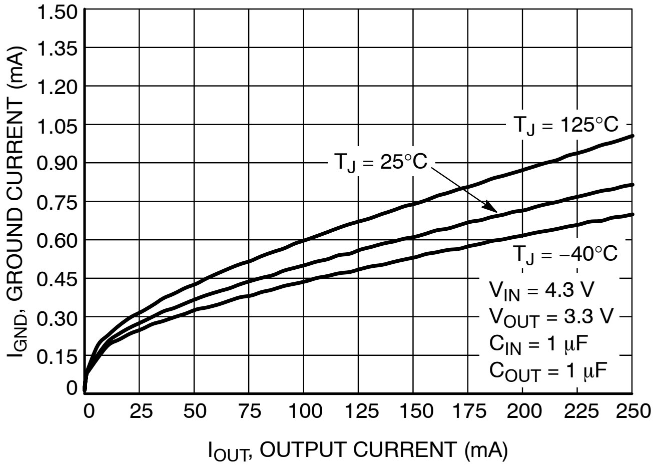


**Figure 15. Ground Current vs. Load Current – $V_{OUT}$ = 3.3 V**

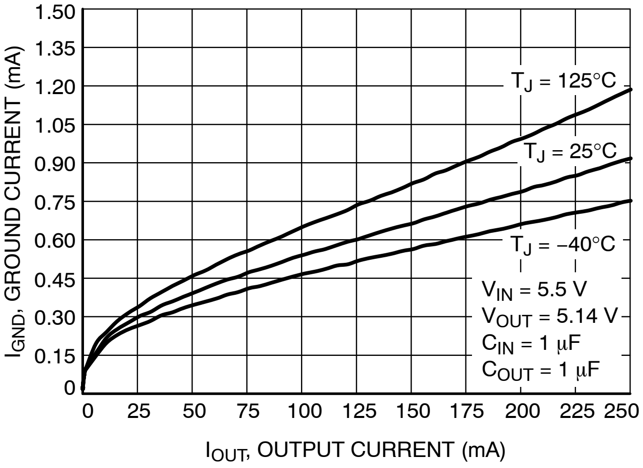


**Figure 16. Ground Current vs. Load Current – $V_{OUT}$ = 5.14 V**

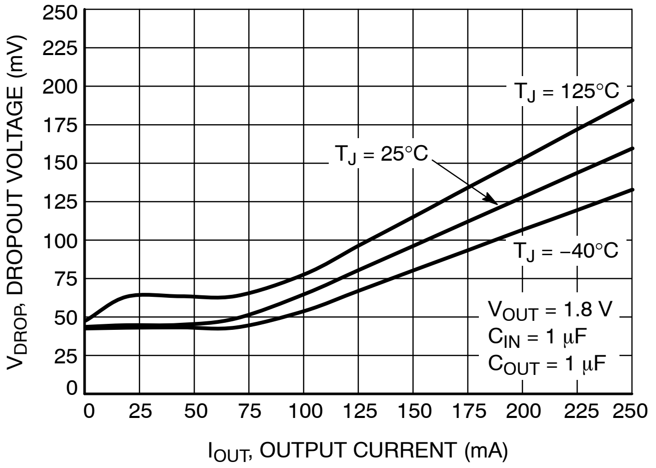


**Figure 17. Dropout Voltage vs. Load Current – $V_{OUT}$ = 1.8 V**

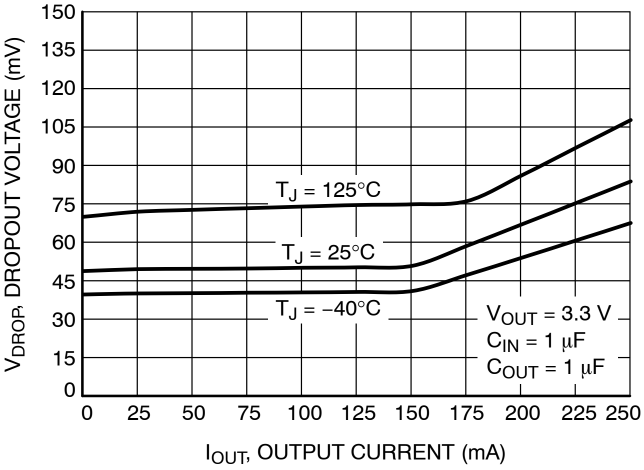


**Figure 18. Dropout Voltage vs. Load Current – $V_{OUT}$ = 3.3 V**

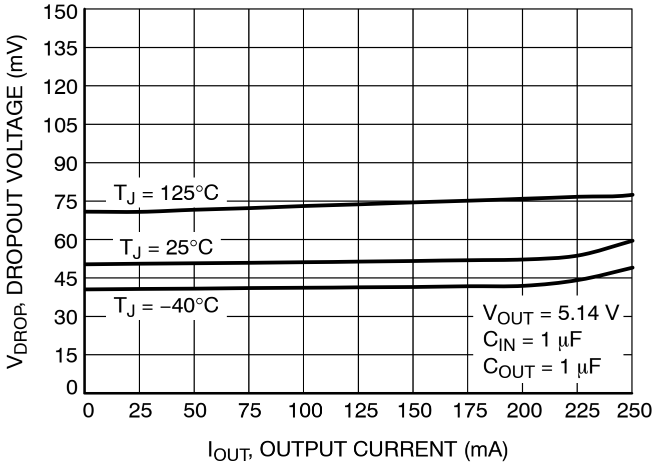


**Figure 19. Dropout Voltage vs. Load Current – $V_{OUT}$ = 5.14 V**

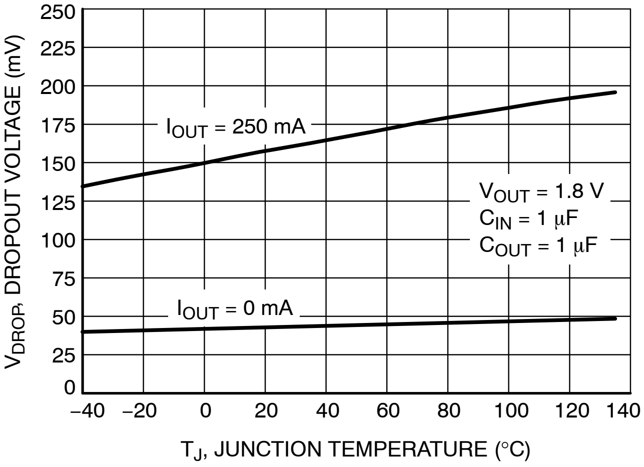


**Figure 20. Dropout Voltage vs. Temperature– $V_{OUT}$ = 1.8 V**

## TYPICAL CHARACTERISTICS

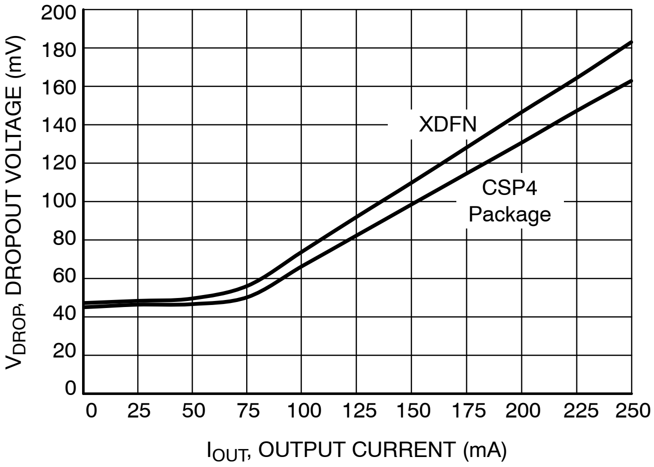


Figure 21. Comparison Dropout for XDFN and CSP – 1.8 V

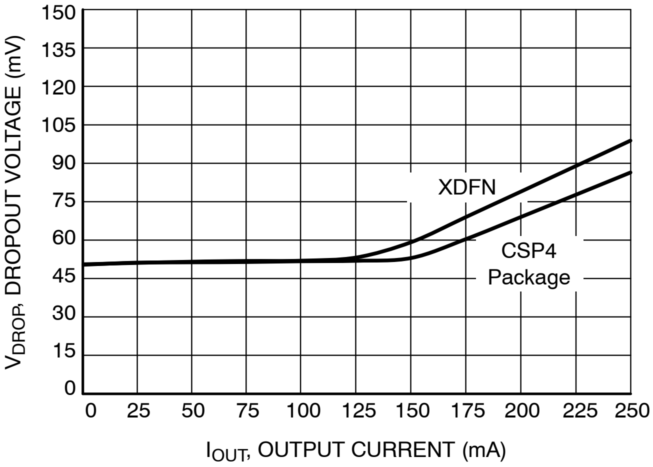


Figure 22. Comparison Dropout for XDFN and CSP – 3.3 V

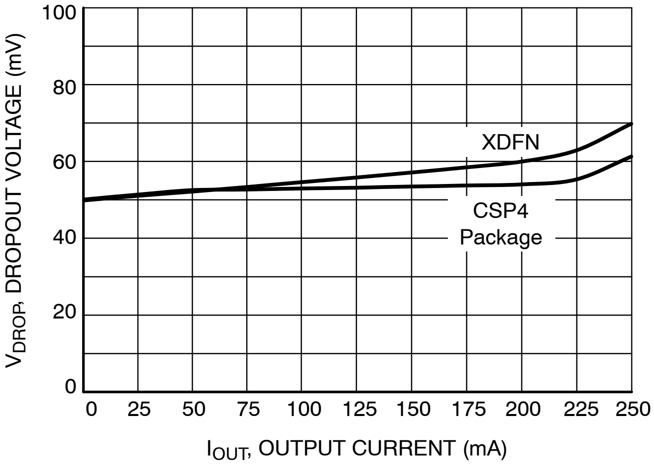


Figure 23. Comparison Dropout for XDFN and CSP – 5.14 V

## TYPICAL CHARACTERISTICS

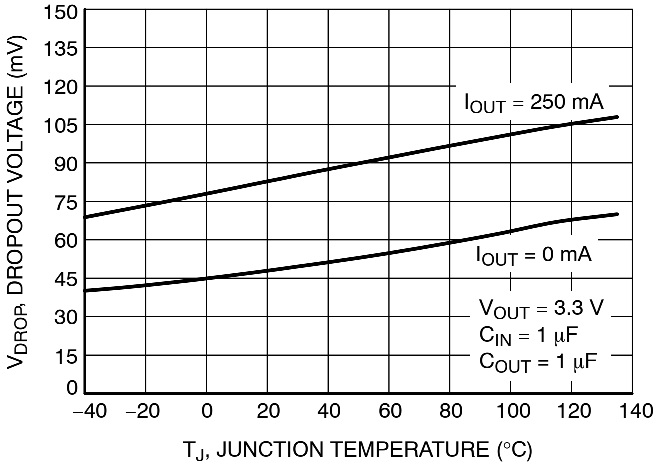


**Figure 24. Dropout Voltage vs. Temperature– $V_{OUT}$ = 3.3 V**

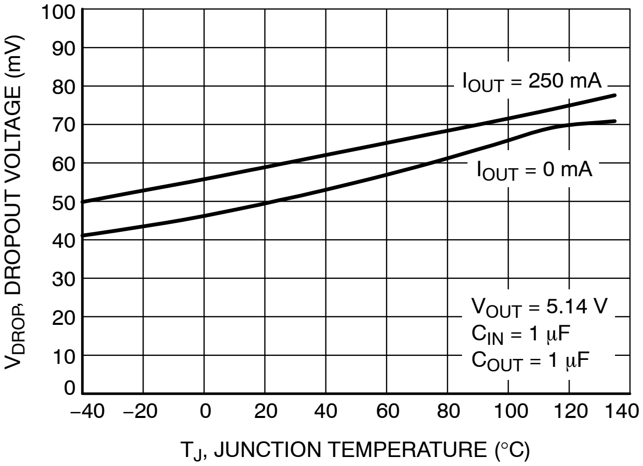


**Figure 25. Dropout Voltage vs. Temperature– $V_{OUT}$ = 5.14 V**

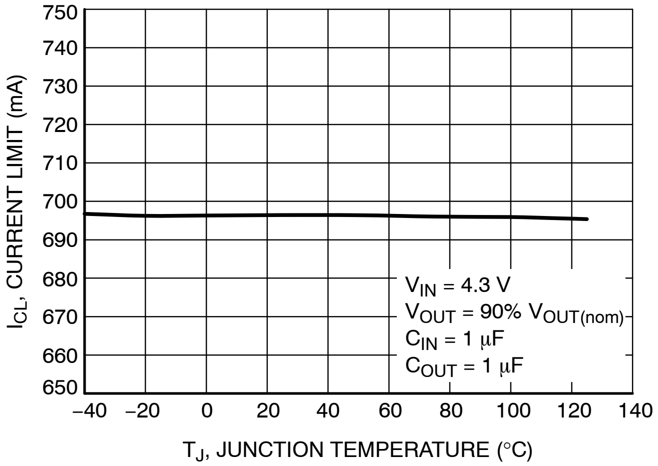


**Figure 26. Current Limit vs. Temperature**

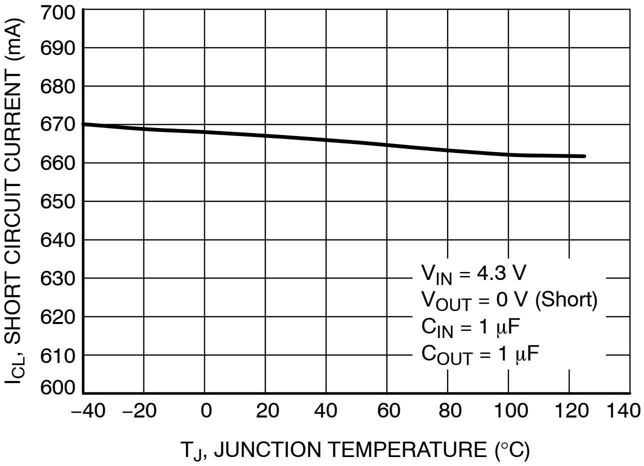


**Figure 27. Short Circuit Current vs. Temperature**

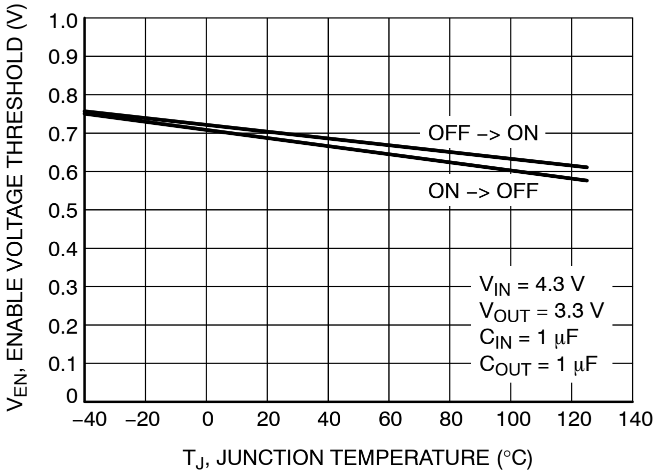


**Figure 28. Enable Threshold Voltage vs. Temperature**

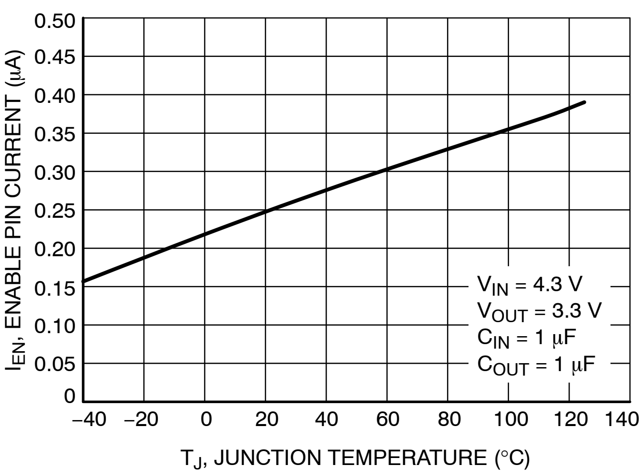


**Figure 29. Enable Current Temperature**

## TYPICAL CHARACTERISTICS

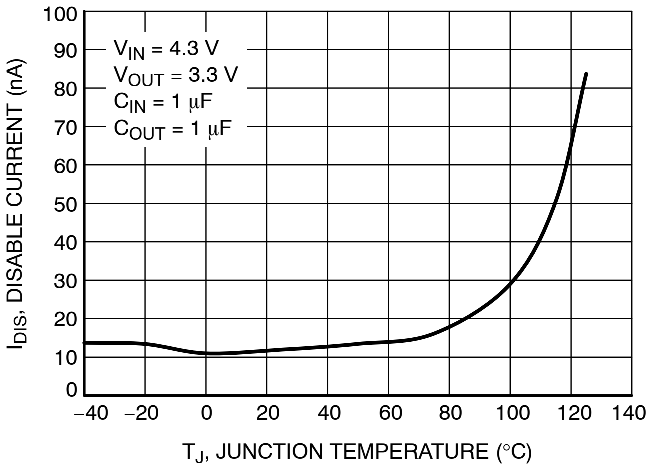


**Figure 30. Disable Current vs. Temperature**

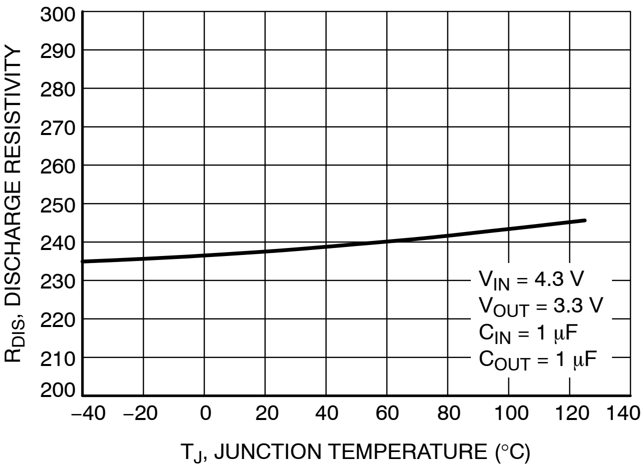
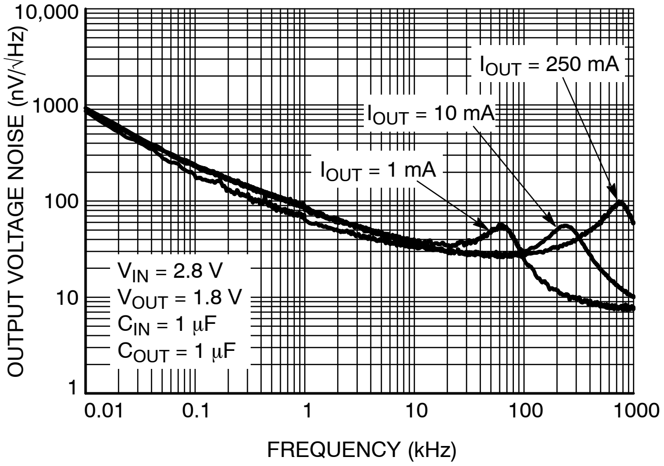
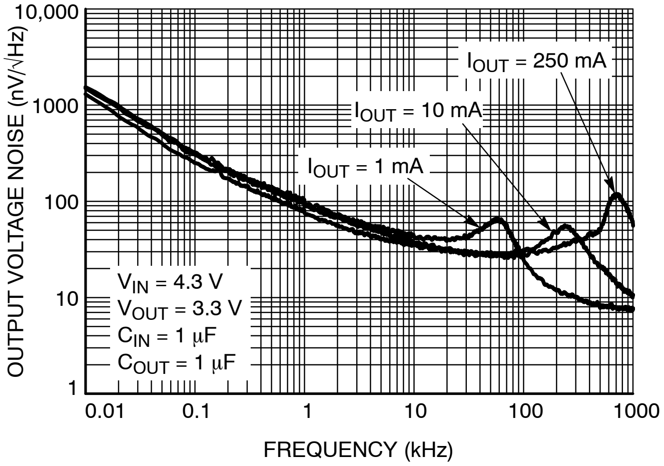


**Figure 31. Discharge Resistivity vs. Temperature**



| $I_{OUT}$ | RMS Output Noise (μV) | |
|---|---|---|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 14.62 | 14.10 |
| 10 mA | 11.12 | 10.48 |
| 250 mA | 10.37 | 9.82 |

**Figure 32. Output Voltage Noise Spectral Density – $V_{OUT}$ = 1.8 V**



| $I_{OUT}$ | RMS Output Noise (μV) | |
|---|---|---|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 16.9 | 15.79 |
| 10 mA | 12.64 | 11.13 |
| 250 mA | 11.96 | 10.64 |

**Figure 33. Output Voltage Noise Spectral Density – $V_{OUT}$ = 3.3 V**

## TYPICAL CHARACTERISTICS

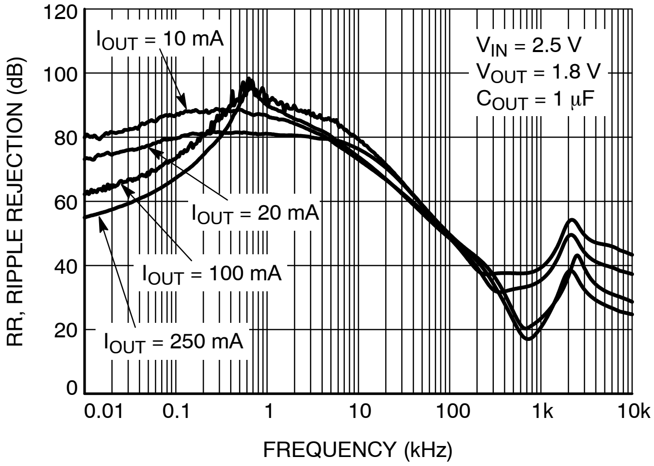


**Figure 34. Power Supply Rejection Ratio, $V_{OUT}$ = 1.8 V**

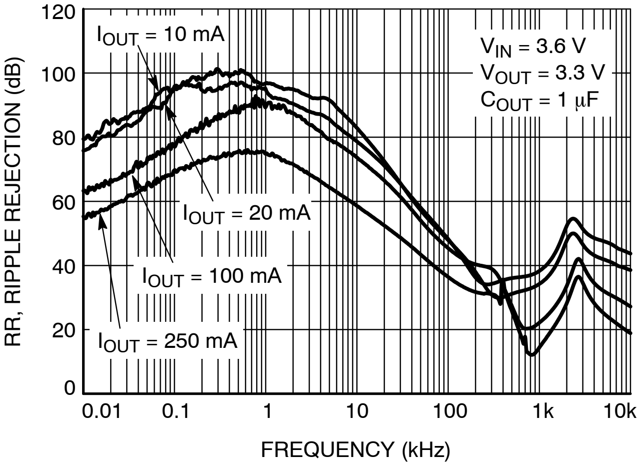


**Figure 35. Power Supply Rejection Ratio, $V_{OUT}$ = 3.3 V**

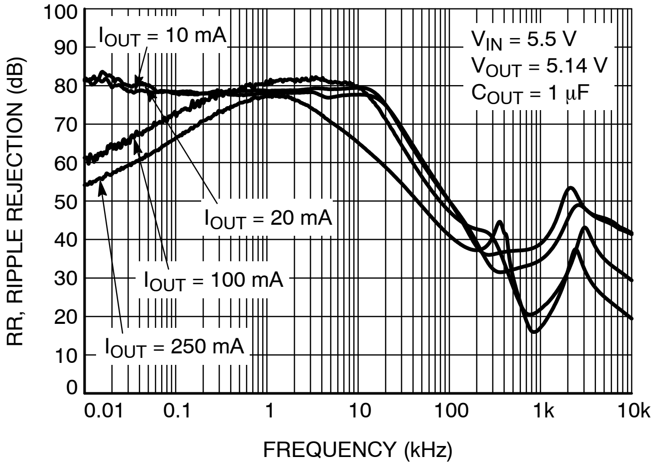


**Figure 36. Power Supply Rejection Ratio, $V_{OUT}$ = 5.14 V**

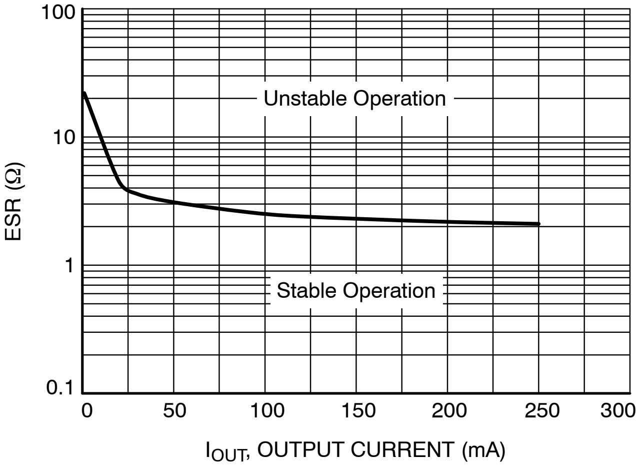


**Figure 37. Stability vs. ESR**

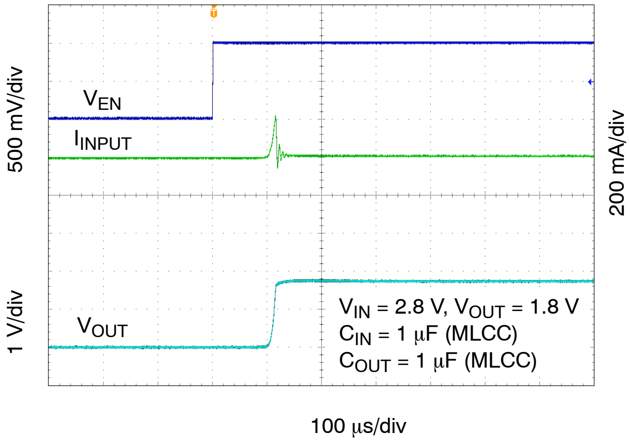


**Figure 38. Enable Turn−on Response − $C_{OUT}$ = 1 μF, $I_{OUT}$ = 10 mA**

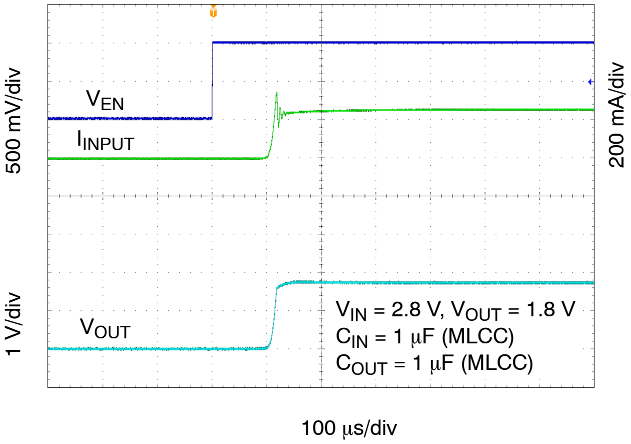


**Figure 39. Enable Turn−on Response − $C_{OUT}$ = 1 μF, $I_{OUT}$ = 250 mA**

## TYPICAL CHARACTERISTICS

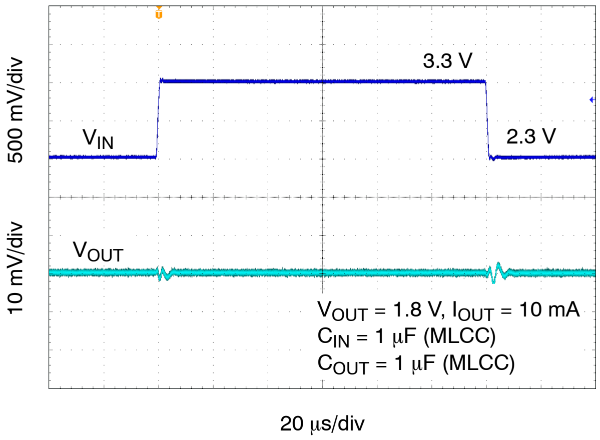


**Figure 40. Line Transient Response – $V_{OUT}$ = 1.8 V**

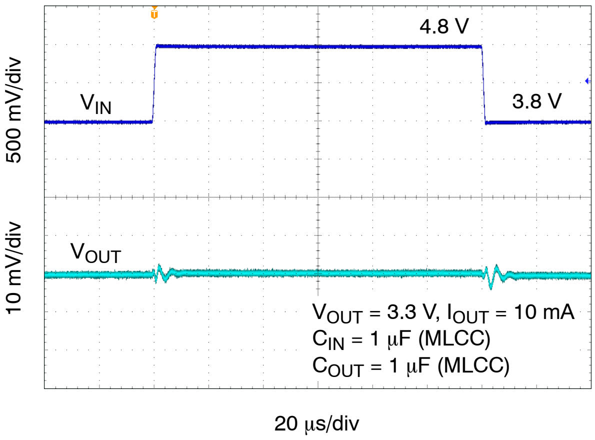


**Figure 41. Line Transient Response – $V_{OUT}$ = 3.3 V**

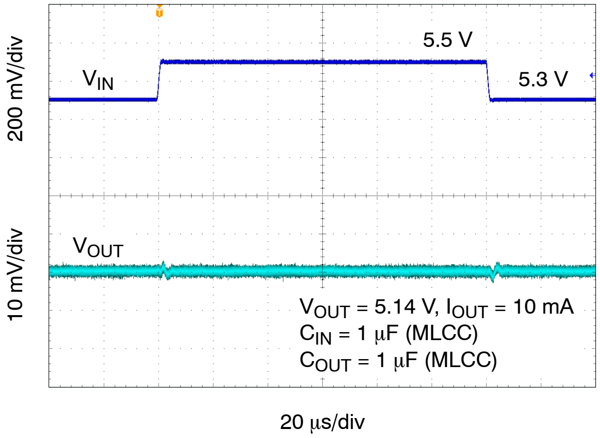


**Figure 42. Line Transient Response – $V_{OUT}$ = 5.14 V**

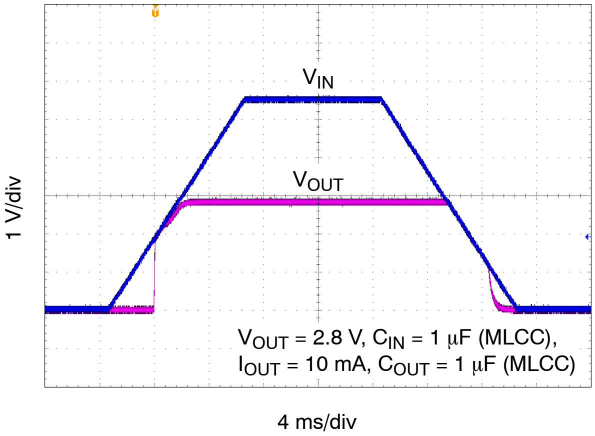


**Figure 43. Turn–on/off – Slow Rising $V_{IN}$**

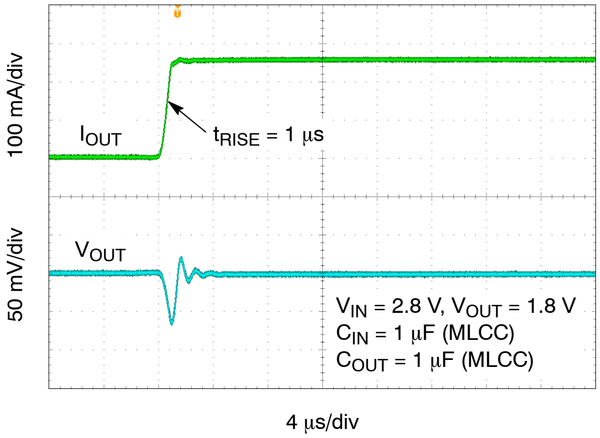


**Figure 44. Load Transient Response – 1 mA to 250 mA – $V_{OUT}$ = 1.8 V**

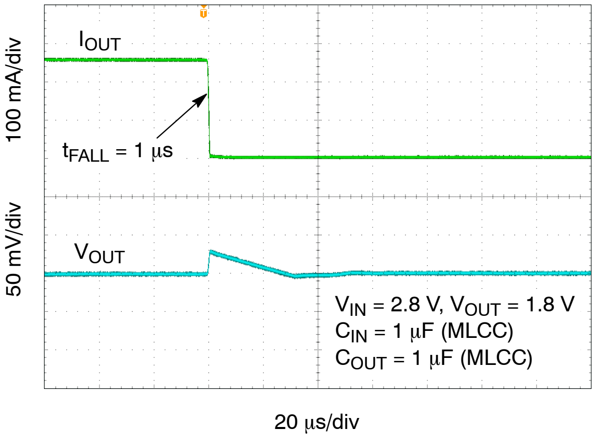


**Figure 45. Load Transient Response – 250 mA to 1 mA – $V_{OUT}$ = 1.8 V**

## TYPICAL CHARACTERISTICS

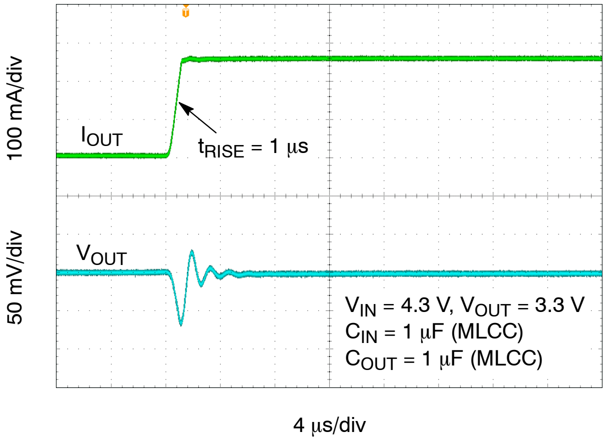


Figure 46. Load Transient Response – 1 mA to 250 mA – $V_{OUT}$ = 3.3 V

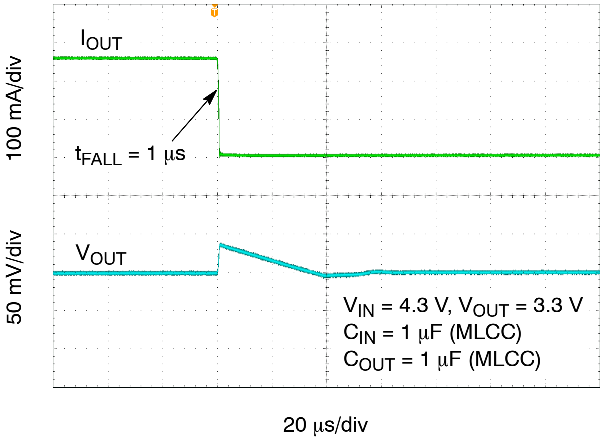


Figure 47. Load Transient Response – 250 mA to 1 mA – $V_{OUT}$ = 3.3 V

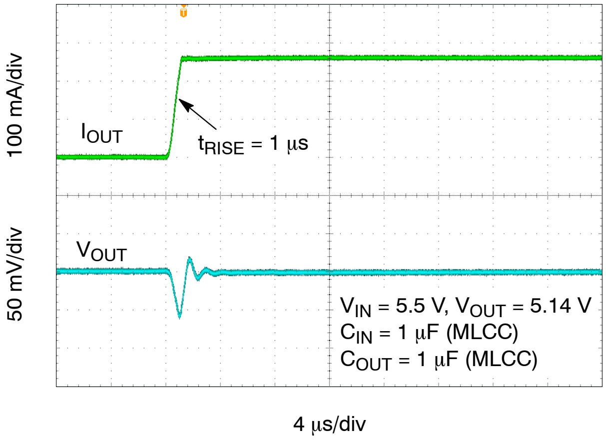


Figure 48. Load Transient Response – 1 mA to 250 mA – $V_{OUT}$ = 5.14 V

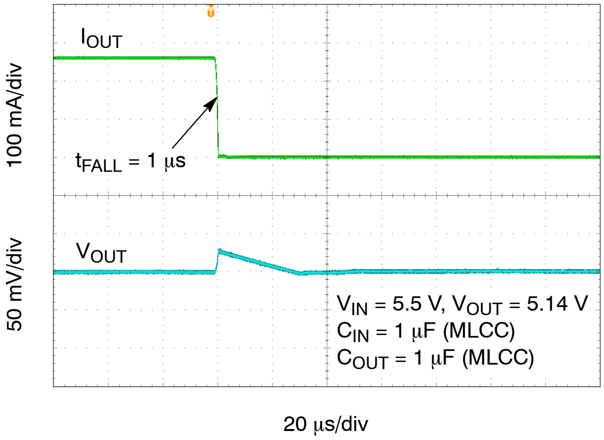


Figure 49. Load Transient Response – 250 mA to 1 mA – $V_{OUT}$ = 5.14 V

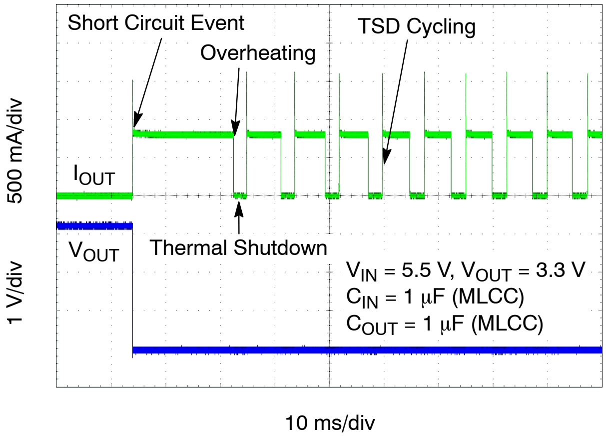


Figure 50. Short Circuit and Thermal Shutdown

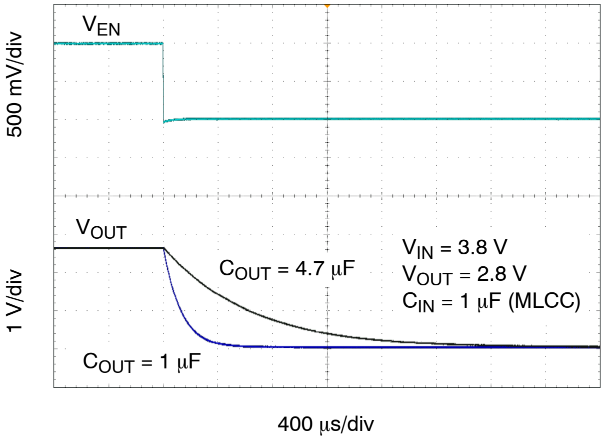


Figure 51. Enable Turn−off

## APPLICATIONS INFORMATION

### General

The NCP160 is an ultra−low noise 250 mA low dropout regulator designed to meet the requirements of RF applications and high performance analog circuits. The NCP160 device provides very high PSRR and excellent dynamic response. In connection with low quiescent current this device is well suitable for battery powered application such as cell phones, tablets and other. The NCP160 is fully protected in case of current overload, output short circuit and overheating.

### Input Capacitor Selection ($C_{IN}$)

Input capacitor connected as close as possible is necessary for ensure device stability. The X7R or X5R capacitor should be used for reliable performance over temperature range. The value of the input capacitor should be 1 μF or greater to ensure the best dynamic performance. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

### Output Decoupling ($C_{OUT}$)

The NCP160 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP160 is designed to remain stable with minimum effective capacitance of 0.7 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0201 the effective capacitance drops rapidly with the applied DC bias. Please refer Figure 52.

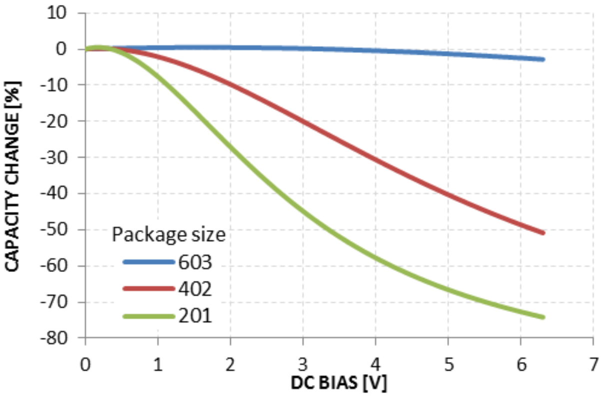


**Figure 52. Capacity vs DC Bias Voltage**

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the $C_{OUT}$ but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

### Enable Operation

The NCP160 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage $V_{OUT}$ is pulled to GND through a 280 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the $V_{IN}$.

If the EN pin voltage >1.2 V the device is guaranteed to be enabled. The NCP160 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 200 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

### Output Current Limit

Output Current is internally limited within the IC to a typical 700 mA. The NCP60 will source this amount of current measured with a voltage drops on the 90% of the nominal $V_{OUT}$. If the Output Voltage is directly shorted to ground ($V_{OUT} = 0$ V), the short circuit protection will limit the output current to 690 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

### Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ($T_{SD}$ − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ($T_{SDU}$ − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

### Power Dissipation

As power dissipated in the NCP160 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP160 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125^{\circ}C - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP160 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN} \cdot I_{GND} + I_{OUT}\left(V_{IN} - V_{OUT}\right) \qquad \text{(eq. 2)}$$

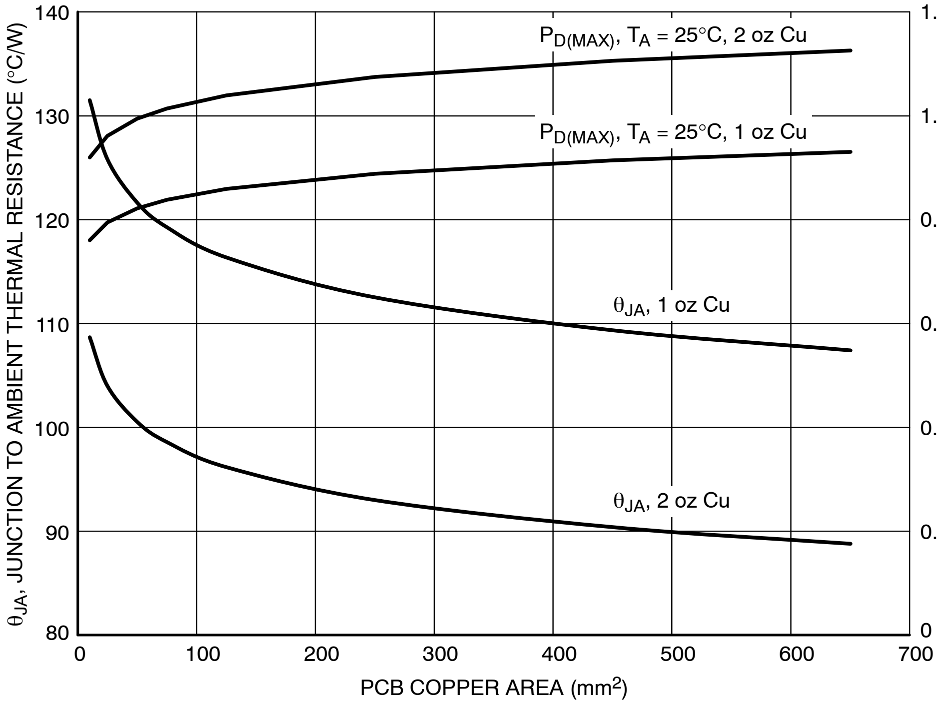


**Figure 53. $\theta_{JA}$ and $P_{D\,(MAX)}$ vs. Copper Area (CSP4)**

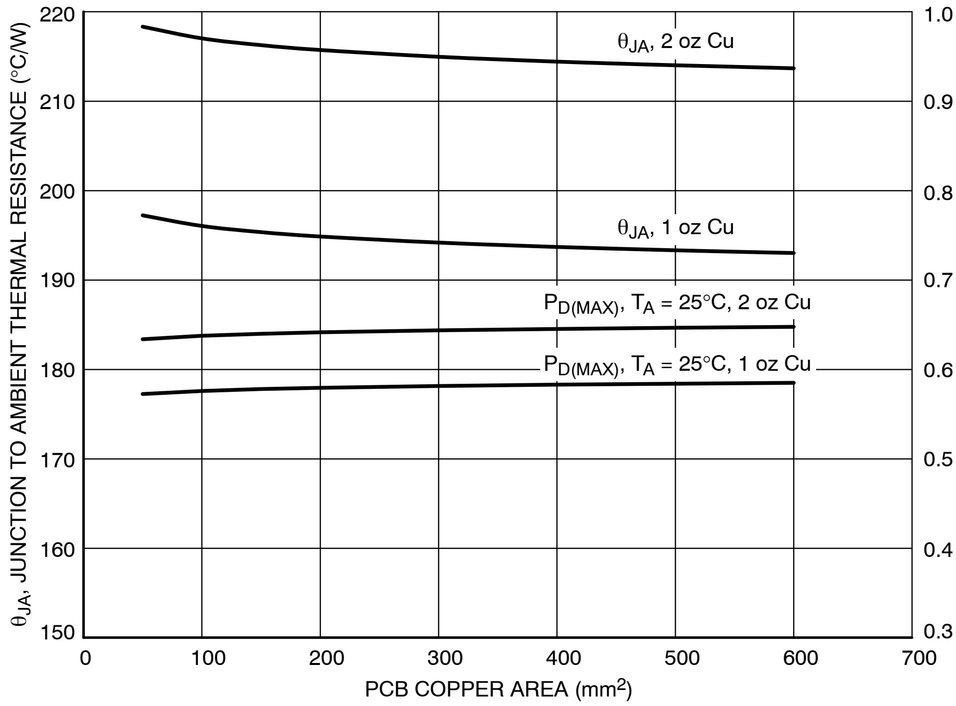


**Figure 54. $\theta_{JA}$ and $P_{D\,(MAX)}$ vs. Copper Area (XDFN4)**

### Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

### Power Supply Rejection Ratio

The NCP160 features very high Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of $C_{OUT}$ capacitor and proper PCB layout.

### Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which $V_{OUT}$ will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, $C_{OUT}$, $T_A$.

### PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place $C_{IN}$ and $C_{OUT}$ capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 or 0201 capacitors with appropriate capacity. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad can be tied to the GND pin for improvement power dissipation and lower device temperature.

## ORDERING INFORMATION

| Device | Nominal Output Voltage | Description | Marking | Rotation | Package | Shipping† |
|---|---|---|---|---|---|---|
| NCP160AFCS180T2G | 1.8 V | 250 mA, Active Discharge | A | 0° | WLCSP4<br>CASE 567KA<br>(Pb-Free) | 5000 / Tape & Reel |
| NCP160AFCS250T2G | 2.5 V | | D | 0° | | |
| NCP160AFCS270T2G | 2.7 V | | 4 | 0° | | |
| NCP160AFCS280T2G | 2.8 V | | E | 0° | | |
| NCP160AFCSC280T2G | 2.8 V | 250 mA, Active Discharge, Backside Coating | E | 0° | | |
| NCP160AFCS285T2G | 2.85 V | 250 mA, Active Discharge | F | 0° | | |
| NCP160AFCS2925T2G | 2.925 V | | T | 0° | | |
| NCP160AFCS300T2G | 3.0 V | | J | 0° | | |
| NCP160AFCS320T2G | 3.2 V | | V | 0° | | |
| NCP160AFCS330T2G | 3.3 V | | K | 0° | | |
| NCP160AFCS350T2G | 3.5 V | | L | 0° | | |
| NCP160AFCS370T2G | 3.7 V | | Y | 0° | | |
| NCP160AFCS450T2G | 4.5 V | | P | 0° | | |
| NCP160AFCS500T2G | 5.0 V | | R | 0° | | |
| NCP160AFCS514T2G | 5.14 V | | Q | 0° | | |
| NCP160BFCS180T2G | 1.8 V | 250 mA, Non-Active Discharge | A | 90° | | |
| NCP160BFCS250T2G | 2.5 V | | D | 90° | | |
| NCP160BFCS280T2G | 2.8 V | | E | 90° | | |
| NCP160BFCS285T2G | 2.85 V | | F | 90° | | |
| NCP160BFCS2925T2G | 2.925 V | | T | 90° | | |
| NCP160BFCS300T2G | 3.0 V | | J | 90° | | |
| NCP160BFCS330T2G | 3.3 V | | K | 90° | | |
| NCP160BFCS350T2G | 3.5 V | | L | 90° | | |
| NCP160BFCS450T2G | 4.5 V | | P | 90° | | |
| NCP160BFCS500T2G | 5.0 V | | R | 90° | | |
| NCP160BFCS514T2G | 5.14 V | | Q | 90° | | |

**ORDERING INFORMATION** (continued)

| Device | Nominal Output Voltage | Description | Marking | Rotation | Package | Shipping† |
|---|---|---|---|---|---|---|
| NCP160AFCT180T2G | 1.8 V | 250 mA, Active Discharge | A | 0° | WLCSP4<br>CASE 567JZ<br>(Pb-Free) | 5000 / Tape & Reel |
| NCP160AFCT250T2G | 2.5 V | | D | 0° | | |
| NCP160AFCT270T2G | 2.7 V | | T | 0° | | |
| NCP160AFCT280T2G | 2.8 V | | E | 0° | | |
| NCP160AFCT285T2G | 2.85 V | | F | 0° | | |
| NCP160AFCT300T2G | 3.0 V | | J | 0° | | |
| NCP160AFCT330T2G | 3.3 V | | K | 0° | | |
| NCP160AFCTC330T2G | 3.3 V | 250 mA, Active Discharge, Backside Coating | K | 0° | | |
| NCP160AFCT350T2G | 3.5 V | 250 mA, Active Discharge | L | 0° | | |
| NCP160AFCT450T2G | 4.5 V | | P | 0° | | |
| NCP160AFCT500T2G | 5.0 V | | R | 0° | | |
| NCP160AFCT514T2G | 5.14 V | | Q | 0° | | |
| NCP160AFCTC180T2G | 1.8 V | 250 mA, Active Discharge, Backside Coating | A | 0° | | |
| NCP160BFCT180T2G | 1.8 V | 250 mA, Non-Active Discharge | A | 90° | | |
| NCP160BFCT210T2G | 2.1 V | | T | 90° | | |
| NCP160BFCT250T2G | 2.5 V | | D | 90° | | |
| NCP160BFCT280T2G | 2.8 V | | E | 90° | | |
| NCP160BFCT285T2G | 2.85 V | | F | 90° | | |
| NCP160BFCT300T2G | 3.0 V | | J | 90° | | |
| NCP160BFCT330T2G | 3.3 V | | K | 90° | | |
| NCP160BFCT350T2G | 3.5 V | | L | 90° | | |
| NCP160BFCT450T2G | 4.5 V | | P | 90° | | |
| NCP160BFCT500T2G | 5.0 V | | R | 90° | | |
| NCP160BFCT514T2G | 5.14 V | | Q | 90° | | |

**ORDERING INFORMATION** (continued)

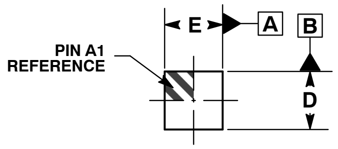
| Device | Nominal Output Voltage | Description | Marking | Package | Shipping† |
|---|---|---|---|---|---|
| NCP160AMX180TBG | 1.8 V | 250 mA, Active Discharge | DF | XDFN4 (Pb-Free) | 3000 / Tape & Reel |
| NCP160AMX1825TBG | 1.825 V | | D7 | | |
| NCP160AMX250TBG | 2.5 V | | DG | | |
| NCP160AMX270TBG | 2.7 V | | D6 | | |
| NCP160AMX275TBG | 2.75 V | | D2 | | |
| NCP160AMX280TBG | 2.8 V | | DH | | |
| NCP160AMX285TBG | 2.85 V | | DJ | | |
| NCP160AMX290TBG | 2.9 V | | D4 | | |
| NCP160AMX300TBG | 3.0 V | | DK | | |
| NCP160AMX320TBG | 3.2 V | | DY | | |
| NCP160AMX310TBG | 3.1 V | | D3 | | |
| NCP160AMX330TBG | 3.3 V | | DA | | |
| NCP160AMX350TBG | 3.5 V | | DL | | |
| NCP160AMX450TBG | 4.5 V | | DM | | |
| NCP160AMX500TBG | 5.0 V | | DW | | |
| NCP160AMX514TBG | 5.14 V | | DC | | |
| NCP160BMX180TBG | 1.8 V | 250 mA, Non-Active Discharge | EF | | |
| NCP160BMX1825TBG | 1.825 V | | E7 | | |
| NCP160BMX250TBG | 2.5 V | | EG | | |
| NCP160BMX275TBG | 2.75 V | | E2 | | |
| NCP160BMX280TBG | 2.8 V | | EH | | |
| NCP160BMX285TBG | 2.85 V | | EJ | | |
| NCP160BMX300TBG | 3.0 V | | EK | | |
| NCP160BMX330TBG | 3.3 V | | EA | | |
| NCP160BMX350TBG | 3.5 V | | EL | | |
| NCP160BMX450TBG | 4.5 V | | EM | | |
| NCP160BMX500TBG | 5.0 V | | EW | | |
| NCP160BMX514TBG | 5.14 V | | EC | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

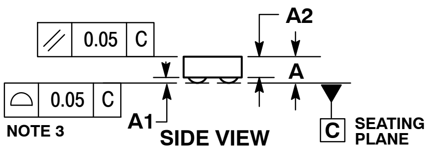
**SCALE 4:1**

**WLCSP4, 0.64x0.64**
CASE 567JZ
ISSUE A

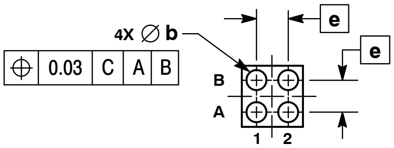
DATE 03 AUG 2016



**TOP VIEW**



**SIDE VIEW**

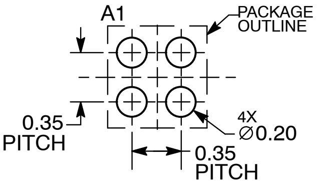


**BOTTOM VIEW**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | --- | --- | 0.33 |
| A1 | 0.04 | 0.06 | 0.08 |
| A2 | 0.23 REF | | |
| b | 0.195 | 0.210 | 0.225 |
| D | 0.610 | 0.640 | 0.670 |
| E | 0.610 | 0.640 | 0.670 |
| e | 0.35 BSC | | |

## RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| **DOCUMENT NUMBER:** | **98AON85781F** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| **DESCRIPTION:** | **WLCSP4, 0.64X0.64** | **PAGE 1 OF 1** |

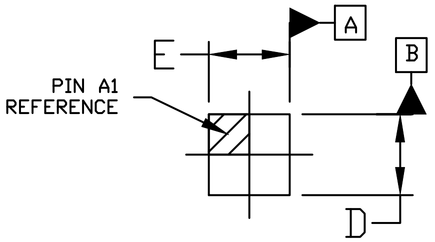
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**ON Semiconductor**®

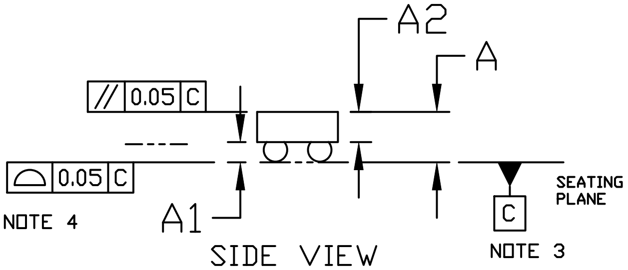
**SCALE 4:1**

**WLCSP4, 0.64x0.64**
CASE 567KA
ISSUE B

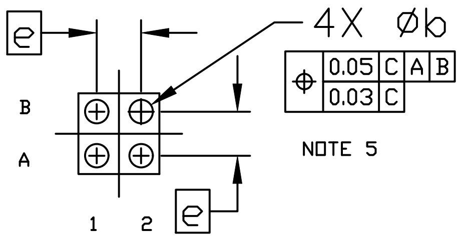
DATE 24 MAR 2020



TOP VIEW

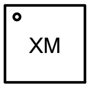


SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM*



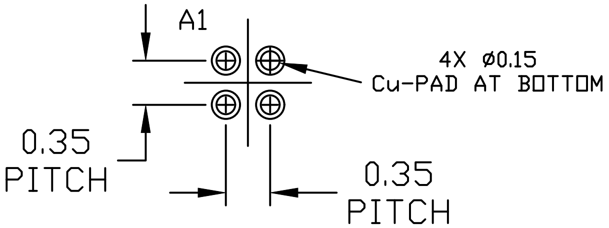
X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.355 | 0.405 | 0.455 |
| A1 | 0.13 | 0.15 | 0.17 |
| A2 | 0.255 REF | | |
| b | 0.167 | 0.187 | 0.207 |
| D | 0.610 | 0.640 | 0.670 |
| E | 0.610 | 0.640 | 0.670 |
| e | 0.35 BSC | | |



RECOMMENDED
MOUNTING FOOTPRINT*
(NSMD PAD TYPE)

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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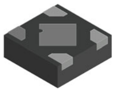
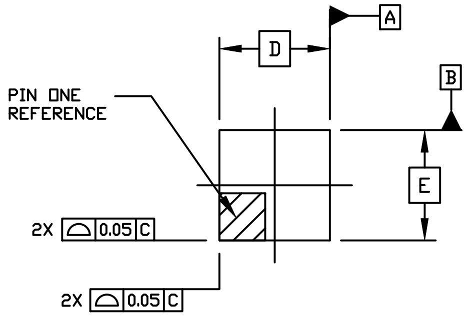
| **DESCRIPTION:** | **WLCSP4, 0.64X0.64** | **PAGE 1 OF 1** |

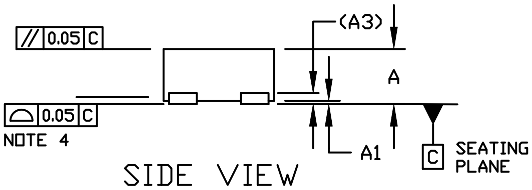


**XDFN4 1.0x1.0, 0.65P**
CASE 711AJ
ISSUE C

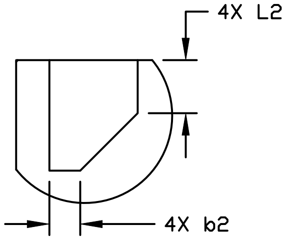
DATE 08 MAR 2022



TOP VIEW



SIDE VIEW

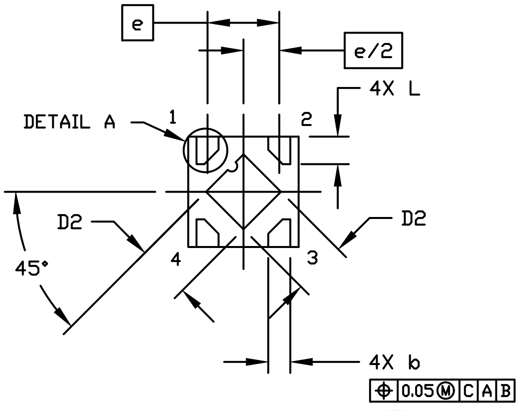


DETAIL A

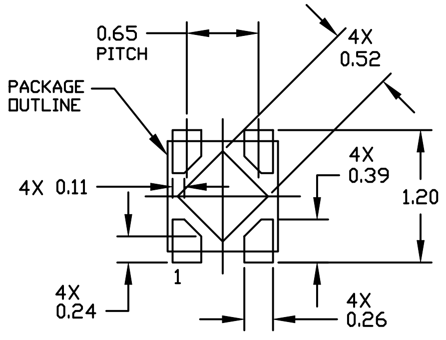
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.33 | 0.38 | 0.43 |
| A1 | 0.00 | --- | 0.05 |
| A3 | 0.10 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| b2 | 0.02 | 0.07 | 0.12 |
| D | 0.90 | 1.00 | 1.10 |
| D2 | 0.43 | 0.48 | 0.53 |
| E | 0.90 | 1.00 | 1.10 |
| e | 0.65 BSC | | |
| L | 0.20 | | 0.30 |
| L2 | 0.07 | | 0.17 |



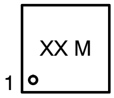
BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT

* FOR ADDITIONAL INFORMATION ON OUR Pb-FRE
STRATEGY AND SOLDERING DETAILS, PLEASE
DOWNLOAD THE ONSEMI SOLDERING AND MOUNT
TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

**GENERIC**
**MARKING DIAGRAM***



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
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| **DESCRIPTION:** | **XDFN4, 1.0X1.0, 0.65P** | **PAGE 1 OF 1** |

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