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LM5010A/LM5010AQ
High Voltage 1A Step Down Switching Regulator

General Description

The LM5010A Step Down Switching Regulator is an enhanced version of the LM5010 with the input operating range extended to 6V minimum. The LM5010A features all the functions needed to implement a low cost, efficient, buck regulator capable of supplying in excess of 1A load current. This high voltage regulator integrates an N-Channel Buck Switch, and is available in thermally enhanced LLP-10 and TSSOP-14EP packages. The constant on-time regulation scheme requires no loop compensation resulting in fast load transient response and simplified circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection is set at 1.25A. Additional features include: VCC under-voltage lock-out, thermal shutdown, gate drive under-voltage lock-out, and maximum duty cycle limiter.

Features

- Wide 6V to 75V Input Voltage Range
- Valley Current Limiting At 1.25A
- Programmable Switching Frequency Up To 1 MHz
- Integrated 80V N-Channel Buck Switch
- Integrated High Voltage Bias Regulator
- No Loop Compensation Required
- Ultra-Fast Transient Response
- Nearly Constant Operating Frequency With Line and Load Variations
- Adjustable Output Voltage
- 2.5V, ±2% Feedback Reference
- Programmable Soft-Start
- Thermal shutdown
- LM5010AQ is AEC-Q100 Grade 1 & 0 qualified

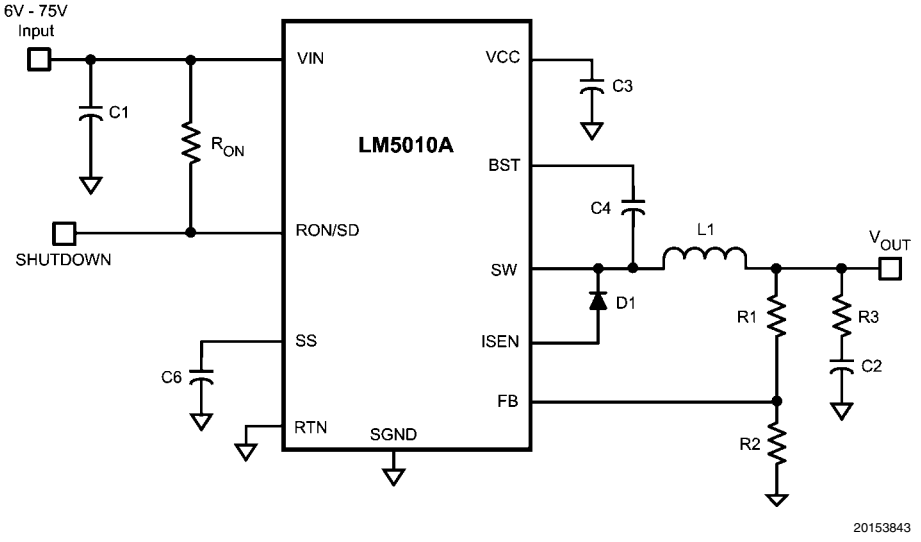
Typical Applications

- Non-Isolated Telecommunications Regulator
- Secondary Side Post Regulator
- Automotive Electronics

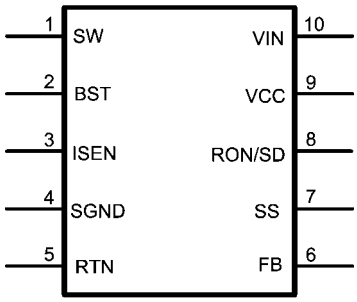
Package

- LLP-10 (4 mm x 4 mm)
- TSSOP-14EP
- Both Packages Have Exposed Thermal Pad For Improved Heat Dissipation

Basic Step Down Regulator



Connection Diagrams



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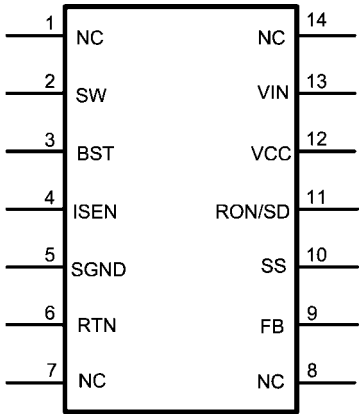

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Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As	Automotive Grade*
LM5010ASD	LLP-10 (4x4)	SDC10A	1000 Units on Tape and Reel	No
LM5010ASDX	LLP-10 (4x4)	SDC10A	4500 Units on Tape and Reel	No
LM5010AMH	TSSOP-14EP	MXA14A	94 Units in Rail	No
LM5010AMHE	TSSOP-14EP	MXA14A	250 Units on Tape and Reel	No
LM5010AMHX	TSSOP-14EP	MXA14A	2500 Units on Tape and Reel	No
LM5010AQ1MH	TSSOP-14EP	MXA14A	94 Units in Rail	Grade 1
LM5010AQ1MHX	TSSOP-14EP	MXA14A	2500 Units on Tape and Reel	Grade 1
LM5010AQ0MH	TSSOP-14EP	MXA14A	94 Units in Rail	Grade 0
LM5010AQ0MHX	TSSOP-14EP	MXA14A	2500 Units on Tape and Reel	Grade 0

*Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard. Automotive grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

Pin Descriptions

Pin Number		Name	Description	Application Information
LLP-10	TSSOP-14			
1	2	SW	Switching Node	Internally connected to the buck switch source. Connect to the inductor, free-wheeling diode, and bootstrap capacitor.
2	3	BST	Boost pin for bootstrap capacitor	Connect a capacitor from SW to the BST pin. The capacitor is charged from VCC via an internal diode during the buck switch off-time.
3	4	ISEN	Current sense	During the buck switch off-time, the inductor current flows through the internal sense resistor, and out of the ISEN pin to the free-wheeling diode. The current limit comparator keeps the buck switch off if the ISEN current exceeds 1.25A (typical).
4	5	SGND	Current Sense Ground	Re-circulating current flows into this pin to the current sense resistor.
5	6	RTN	Circuit Ground	Ground return for all internal circuitry other than the current sense resistor.
6	9	FB	Voltage feedback input from the regulated output	Input to both the regulation and over-voltage comparators. The FB pin regulation level is 2.5V.
7	10	SS	Softstart	An internal 11.5 µA current source charges the SS pin capacitor to 2.5V to soft-start the reference input of the regulation comparator.
8	11	RON/SD	On-time control and shutdown	An external resistor from VIN to the RON/SD pin sets the buck switch on-time. Grounding this pin shuts down the regulator.
9	12	VCC	Output of the bias regulator	The voltage at VCC is nominally equal to V_{IN} for V_{IN} < 8.9V, and regulated at 7V for V_{IN} > 8.9V. Connect a 0.47 µF, or larger capacitor from VCC to ground, as close as possible to the pins. An external voltage can be applied to this pin to reduce internal dissipation if V_{IN} is greater than 8.9V. MOSFET body diodes clamp VCC to VIN if $V_{CC} > V_{IN}$.
10	13	VIN	Input supply voltage	Nominal input range is 6V to 75V. Input bypass capacitors should be located as close as possible to the VIN pin and RTN pins.
	1,7,8,14	NC	No connection.	No internal connection. Can be connected to ground plane to improve heat dissipation.
		EP	Exposed Pad	Exposed metal pad on the underside of the device. It is recommended to connect this pad to the PC board ground plane to aid in heat dissipation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN to RTN	-0.3V to 76V
BST to RTN	-0.3V to 90V
SW to RTN (Steady State)	-1.5V
BST to VCC	76V
BST to SW	14V
VCC to RTN	-0.3V to 14V
SGND to RTN	-0.3V to +0.3V
SS to RTN	-0.3V to 4V
VIN to SW	76V
All Other Inputs to RTN	-0.3V to 7V
ESD Rating (Note 2)	
Human Body Model	2kV
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 4 sec) (Note 4)	260°C

Operating Ratings (Note 1)

VIN Voltage	6.0V to 75V
Junction Temperature	
LM5010A/LM5010AQ1	–40°C to + 125°C
LM5010AQ0	–40°C to + 150°C

Electrical Charateristics

Specifications with standard type are for T_J = 25°C only; limits in boldface type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 48V, R_{ON} = 200kΩ. See (Note 5).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} Regulator						
V_{CC}Reg	V_{CC} regulated output		**6.6**	7	**7.4**	Volts
	V_{IN} - V_{CC}	I_{CC} = 0 mA, F_S < 200 kHz, 6.0V ≤ V_{IN} ≤ 8.5V		100		mV
	V_{CC} Bypass Threshold	V_{IN} Increasing		8.9		V
	V_{CC} Bypass Hysteresis	V_{IN} Decreasing		260		mV
	V_{CC} output impedance	V_{IN} = 6.0V		55		Ω
	(0 mA ≤ I_{CC} ≤ 5 mA)	V_{IN} = 8.0V		50		
		V_{IN} = 48V		0.21		
	V_{CC} current limit (Note 3)	V_{IN} = 48V, V_{CC} = 0V		15		mA
UVLOVcc	V_{CC} under-voltage lock-out threshold	V_{CC} Increasing		5.25		V
	$UVLO_{VCC}$ hysteresis	V_{CC} Decreasing		180		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		3		µs
	I_{IN} operating current	Non-switching, FB = 3V		675	**950**	µA
	I_{IN} shutdown current	RON/SD = 0V		100	**200**	µA
Switch Characteristics						
$R_{DS(on)}$	Buck Switch $R_{DS(on)}$ @ I_{SW} = 200 mA	T_J ≤ 125°C T_J ≤ 150°C		0.35	**0.80** **0.85**	Ω
$UVLO_{GD}$	Gate Drive UVLO	V_{BST} - V_{SW} Increasing	**1.7**	3.0	**4.0**	V
	$UVLO_{GD}$ hysteresis			400		mV
SOFT-START Pin						
I_{SS}	Internal current source		**8.0**	11.5	**15**	µA
Current Limit						
I_{LIM}	Threshold	Current out of I_{SEN}	**1**	1.25	**1.5**	A
	Resistance from ISEN to SGND			130		mΩ
	Response time			150		ns
On Timer, RON/SD Pin						
t_{ON} - 1	On-time	V_{IN} = 10V, R_{ON} = 200 kΩ	**2.1**	2.75	**3.4**	µs
t_{ON} - 2	On-time	V_{IN} = 75V, R_{ON} = 200 kΩ	**290**	390	**496**	ns
	Shutdown threshold	Voltage at RON/SD rising	**0.30**	0.7	**1.05**	V
	Threshold hysteresis			40		mV

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Timer						
t_{OFF}	Minimum Off-time			260		ns
Regulation and Over-Voltage Comparators (FB Pin)						
V_{REF}	FB regulation threshold	$T_J \leq 125°C$ $T_J \leq 150°C$	**2.445** **2.435**	2.50	**2.550**	V
	FB over-voltage threshold			2.9		V
	FB bias current			1		nA
Thermal Shutdown						
T_{SD}	Thermal shutdown temperature			175		°C
	Thermal shutdown hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient, 0 LFPM Air Flow	SDC Package MXA Package		40 40		°C/W
θ_{JC}	Junction to Case	SDC Package MXA Package		5.2 5.2		°C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

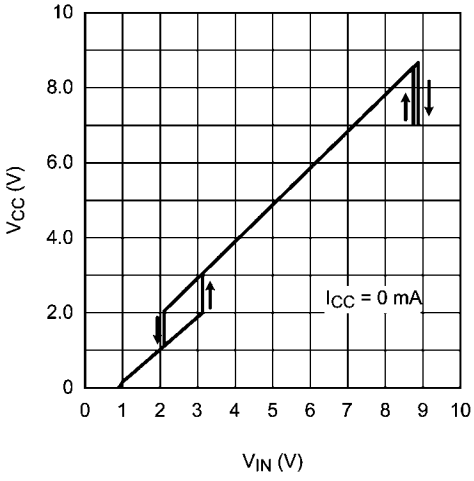
Note 3: V_{CC} provides bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Note 4: For detailed information on soldering plastic TSSOP and LLP packages refer to the Packaging Data Book available from National Semiconductor Corporation.

Note 5: Typical specifications represent the most likely parametric norm at 25°C operation.

Typical Performance Characteristics

V_{CC} vs V_{IN}



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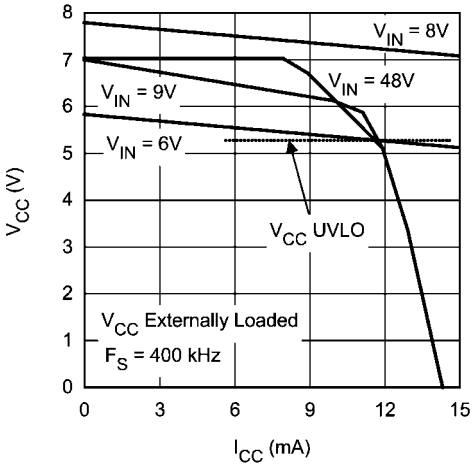
V_{CC} vs I_{CC}



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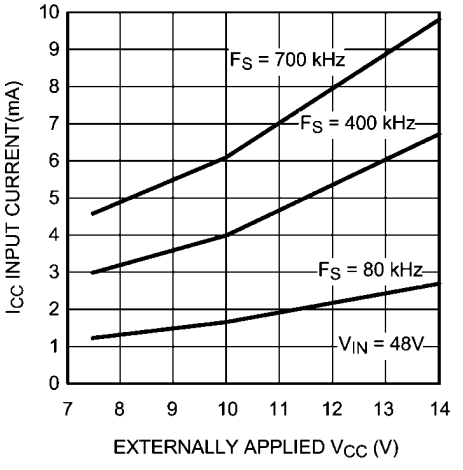
I_{CC} vs Externally Applied V_{CC}



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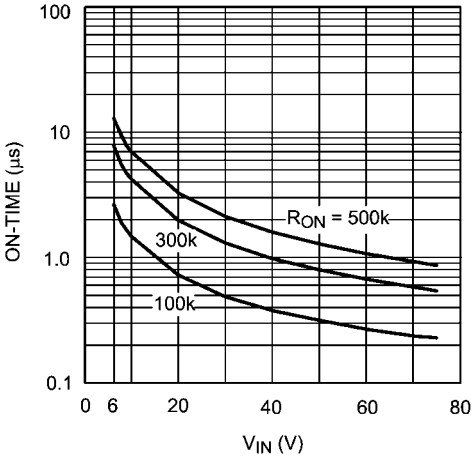
On-Time vs V_{IN} and R_{ON}



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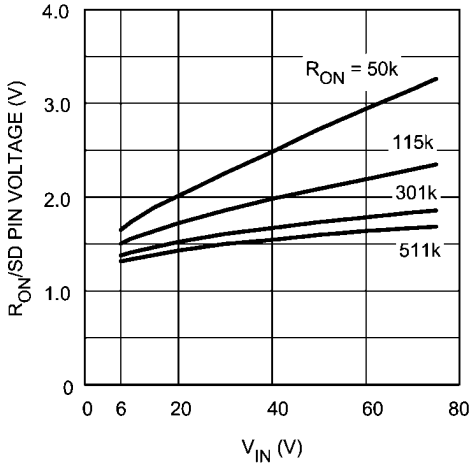
Voltage at RON/SD Pin



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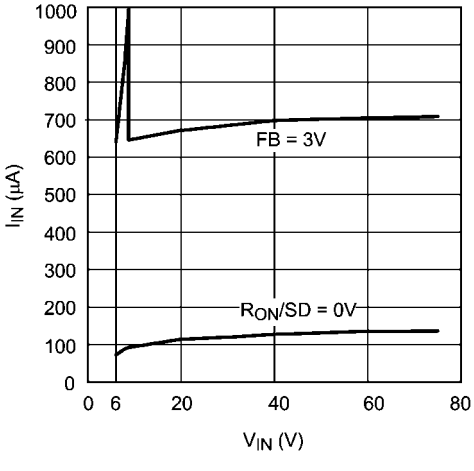
I_{IN} vs V_{IN}



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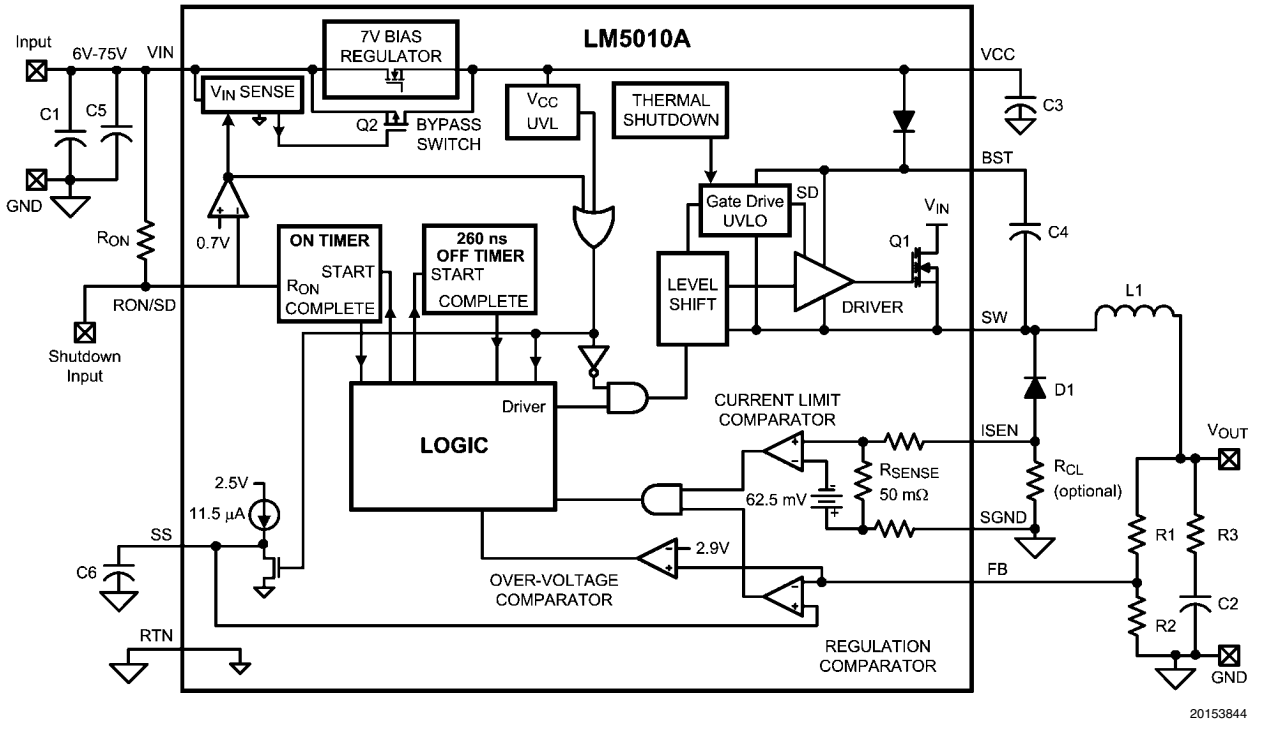
Block Diagram



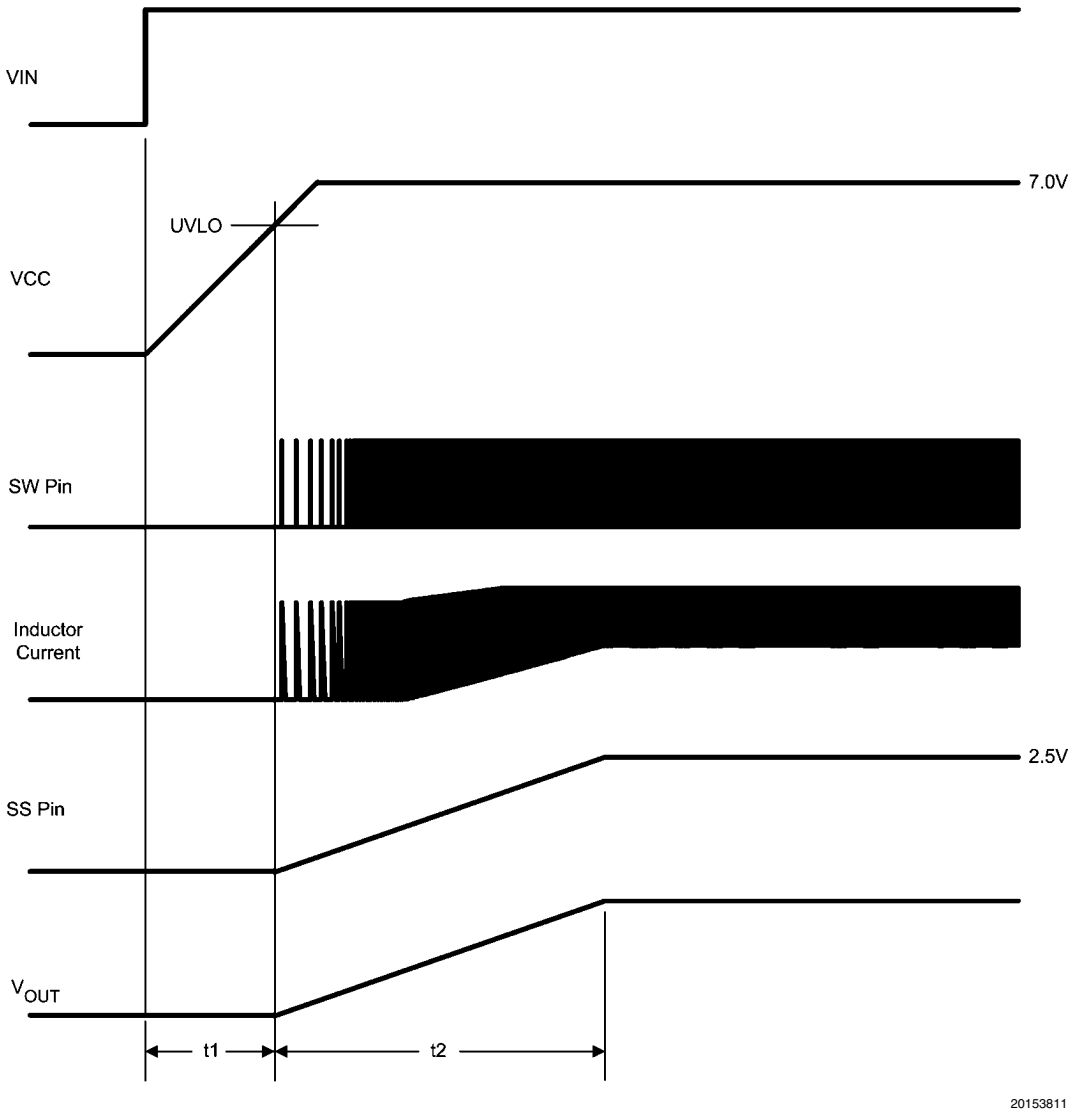


FIGURE 1. Startup Sequence

Functional Description

The LM5010A Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck DC-DC converter capable of supplying in excess of 1A to the load. This high voltage regulator integrates an 80V N-Channel buck switch, with an easy to implement constant on-time controller. It is available in the thermally enhanced LLP-10 and TSSOP-14EP packages. The regulator compares the feedback voltage to a 2.5V reference to control the buck switch, and provides a switch on-time which varies inversely with VIN. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The switching frequency can range from less than 100 kHz to 1.0 MHz. The regulator requires no loop compensation resulting in very fast load transient response. The valley current limit circuit holds the buck switch off until the free-wheeling inductor current falls below the current limit threshold, nominally set at 1.25A.

The LM5010A can be applied in numerous applications to efficiently step down higher DC voltages. This regulator is well suited for 48V telecom applications, as well as the 42V automotive power bus. Features include: Thermal shutdown, VCC under-voltage lock-out, gate drive under-voltage lock-out, and maximum duty cycle limit.

Control Circuit Overview

The LM5010A employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB voltage is below the reference the buck switch is turned on for a time period determined by the input voltage and a programming resistor (R_{ON}). Following the on-time the switch remains off for a fixed 260 ns off-time, or until the FB voltage falls below the reference, whichever is longer. The buck switch then turns on for another on-time period. Referring to the Block Diagram, the output voltage is set by R1 and R2. The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.5V \times (R1 + R2) / R2 \quad (1)$$

The LM5010A requires a minimum of 25 mV of ripple voltage at the FB pin for stable fixed-frequency operation. If the output

capacitor's ESR is insufficient additional series resistance may be required (R3 in the Block Diagram).

The LM5010A operates in continuous conduction mode at heavy load currents, and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never decaying to zero during the off-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The operating frequency in the continuous conduction mode is calculated as follows:

$$F_S = \frac{V_{OUT} \times (V_{IN} - 1.4V)}{1.18 \times 10^{-10} \times (R_{ON} + 1.4\ k\Omega) \times V_{IN}} \quad (2)$$

The buck switch duty cycle is equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = t_{ON} \times F_S = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Under light load conditions, the LM5010A operates in discontinuous conduction mode, with zero current flowing through the inductor for a portion of the off-time. The operating frequency is always lower than that of the continuous conduction mode, and the switching frequency varies with load current. Conversion efficiency is maintained at a relatively high level at light loads since the switching losses diminish as the power delivered to the load is reduced. The discontinuous mode operating frequency is approximately:

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.4 \times 10^{20}}{R_L \times R_{ON}^2} \quad (4)$$

where R_L = the load resistance.

Start-Up Bias Regulator (V_{CC})

A high voltage bias regulator is integrated within the LM5010A. The input pin (VIN) can be connected directly to line voltages between 6V and 75V. Referring to the block diagram and the graph of V_{CC} vs. V_{IN}, when V_{IN} is between 6V and the bypass threshold (nominally 8.9V), the bypass switch (Q2) is on, and V_{CC} tracks V_{IN} within 100 mV to 150 mV. The bypass switch on-resistance is approximately 50Ω, with inherent current limiting at approximately 100 mA. When VIN is above the bypass threshold, Q2 is turned off, and V_{CC} is regulated at 7V. The V_{CC} regulator output current is limited at approximately 15 mA. When the LM5010A is shutdown using the RON/SD pin, the V_{CC} bypass switch is shut off, regardless of the voltage at VIN.

When V_{IN} exceeds the bypass threshold, the time required for Q2 to shut off is approximately 2 - 3 µs. The capacitor at VCC (C3) must be a minimum of 0.47 µF to prevent the voltage at VCC from rising above its absolute maximum rating in response to a step input applied at VIN. C3 must be located as close as possible to the LM5010A pins.

In applications with a relatively high input voltage, power dissipation in the bias regulator is a concern. An auxiliary voltage of between 7.5V and 14V can be diode connected to the VCC pin (D2 in *Figure 2*) to shut off the VCC regulator, reducing internal power dissipation. The current required into the VCC pin is shown in the Typical Performance Characteristics. Internally a diode connects VCC to VIN requiring that the auxiliary voltage be less than V_{IN}.

The turn-on sequence is shown in *Figure 1*. When VCC exceeds the under-voltage lock-out threshold (UVLO) of 5.25V (t1 in *Figure 1*), the buck switch is enabled, and the SS pin is released to allow the soft-start capacitor (C6) to charge up. The output voltage V_{OUT} is regulated at a reduced level which increases to the desired value as the soft-start voltage increases (t2 in *Figure 1*).

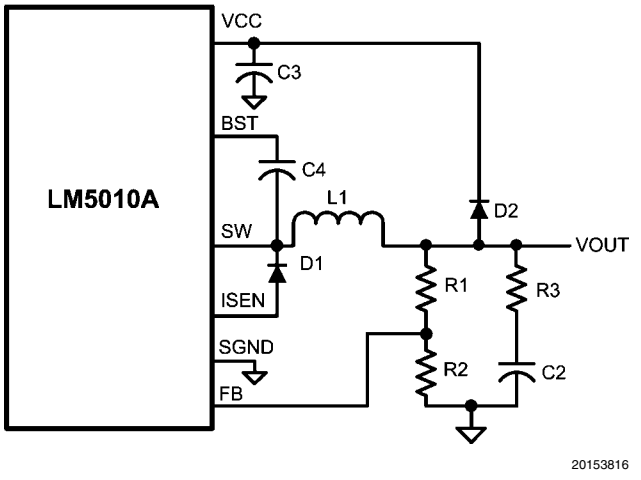


FIGURE 2. Self Biased Configuration

Regulation Comparator

The feedback voltage at the FB pin is compared to the voltage at the SS pin (2.5V, ±2%). In normal operation an on-time period is initiated when the voltage at FB falls below 2.5V. The buck switch conducts for the on-time programmed by R_{ON}, causing the FB voltage to rise above 2.5V. After the on-time period the buck switch remains off until the FB voltage falls below 2.5V. Input bias current at the FB pin is less than 5 nA over temperature.

Over-Voltage Comparator

The feedback voltage at FB is compared to an internal 2.9V reference. If the voltage at FB rises above 2.9V the on-time is immediately terminated. This condition can occur if the in-

put voltage, or the output load, changes suddenly. The buck switch remains off until the voltage at FB falls below 2.5V.

ON-Time Control

The on-time of the internal buck switch is determined by the R_{ON} resistor and the input voltage (V_{IN}), and is calculated as follows:

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R_{ON} + 1.4k)}{(V_{IN} - 1.4V)} + 67\ ns \quad (5)$$

The R_{ON} resistor can be determined from the desired on-time by re-arranging Equation 5 to the following:

$$R_{ON} = \frac{(t_{ON} - 67\ ns) \times (V_{IN} - 1.4V)}{1.18 \times 10^{-10}} - 1.4\ k\Omega \quad (6)$$

To set a specific continuous conduction mode switching frequency (Fs), the R_{ON} resistor is determined from the following:

$$R_{ON} = \frac{V_{OUT} \times (V_{IN} - 1.4V)}{V_{IN} \times F_S \times 1.18 \times 10^{-10}} - 1.4\ k\Omega \quad (7)$$

In high frequency applications the minimum value for t_{ON} is limited by the maximum duty cycle required for regulation and the minimum off-time of the LM5010A (260 ns, ±15%). The fixed off-time limits the maximum duty cycle achievable with a low voltage at VIN. The minimum allowed on-time to regulate the desired V_{OUT} at the minimum V_{IN} is determined from the following:

$$t_{ON(min)} = \frac{V_{OUT} \times 300\ ns}{(V_{IN(min)} - V_{OUT})} \quad (8)$$

Shutdown

The LM5010A can be remotely shut down by forcing the RON/SD pin below 0.7V with a switch or open drain device. See *Figure 3*. In the shutdown mode the SS pin is internally grounded, the on-time one-shot is disabled, the input current at VIN is reduced, and the V_{CC} bypass switch is turned off. The V_{CC} regulator is not disabled in the shutdown mode. Releasing the RON/SD pin allows normal operation to resume. The nominal voltage at RON/SD is shown in the Typical Performance Characteristics. When switching the RON/SD pin, the transition time should be faster than one to two cycles of the regulator's nominal switching frequency.

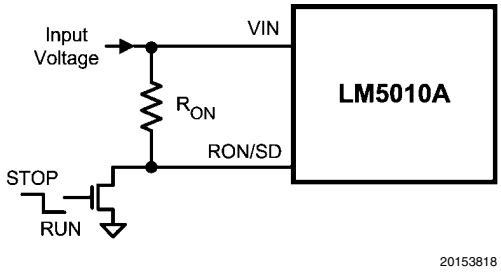


FIGURE 3. Shutdown Implementation

Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating current through the internal current sense resistor (R_{SENSE}). The detection threshold is 1.25A, ±0.25A. Referring to the Block Diagram, if the current into SGND during the off-time exceeds the threshold level the current limit comparator delays the start of the next on-time period. The next on-time starts when the current into SGND is below the threshold **and** the voltage at FB is below 2.5V. *Figure 4* illustrates the inductor current waveform during normal operation and during current limit. The output current I_O is the average of the inductor ripple current waveform. The Low Load Current waveform illustrates continuous conduction mode operation with peak and valley inductor currents below the current limit threshold. When the load current is increased (High Load Current), the ripple waveform maintains the same amplitude and frequency since the current falls below the current limit threshold at the valley of the ripple waveform. Note the average current in the High Load Current portion of *Figure 4* is above the current limit threshold. Since the current reduces below the threshold in the normal off-time each cycle, the start of each on-time is not delayed, and the circuit's output voltage is regulated at the correct value. When the load current is further increased such that the lower peak would be above the threshold, the off-time is lengthened to allow the current to decrease to the threshold before the next on-time begins (Current Limited portion of *Figure 4*). Both V_{OUT} and the switching frequency are reduced as the circuit operates in a constant current mode. The load current (I_{OCL}) is equal to the current limit threshold plus half the ripple current (ΔI/2). The ripple amplitude (ΔI) is calculated from:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L1} \quad (9)$$

The current limit threshold can be increased by connecting an external resistor (R_{CL}) between SGND and ISEN. R_{CL} typically is less than 1Ω, and the calculation of its value is explained in the Applications Information section. If the current limit threshold is increased by adding R_{CL}, the maximum continuous load current should not exceed 1.5A, and the peak current out of the SW pin should not exceed 2A.

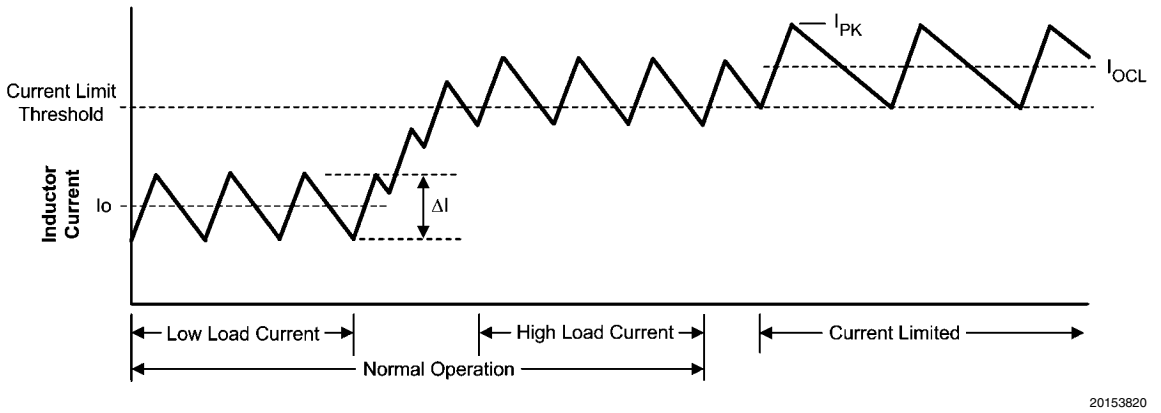


FIGURE 4. Inductor Current - Current Limit Operation

N - Channel Buck Switch and Driver

The LM5010A integrates an N-Channel buck switch and associated floating high voltage gate driver. The peak current through the buck switch should not exceed 2A, and the load current should not exceed 1.5A. The gate driver circuit is powered by the external bootstrap capacitor between BST and SW (C4), which is recharged each off-time from V_{CC} through the internal high voltage diode. The minimum off-time, nominally 260 ns, ensures sufficient time during each cycle to recharge the bootstrap capacitor. A 0.022 µF ceramic capacitor is recommended for C4.

Soft-start

The soft-start feature allows the regulator to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. At turn-on, while V_{CC} is below the under-voltage threshold (t1 in *Figure 1*), the SS pin is internally grounded, and V_{OUT} is held at 0V. When V_{CC} exceeds the under-voltage threshold (UVLO) an internal 11.5 µA current source charges the external capacitor (C6) at the SS pin to 2.5V (t2 in *Figure 1*). The increasing SS voltage at the non-inverting input of the regulation comparator gradually increases the output voltage from zero to the desired value. The soft-start feature keeps the load inductor current from reaching the current limit threshold during start-up, thereby reducing inrush currents.

An internal switch grounds the SS pin if V_{CC} is below the under-voltage lock-out threshold, or if the circuit is shutdown using the RON/SD pin.

Thermal Shutdown

The LM5010A should be operated below the Maximum Operating Junction Temperature rating. If the junction temperature increases during a fault or abnormal operating condition, the internal Thermal Shutdown circuit activates typically at 175°C. The Thermal Shutdown circuit reduces power dissipation by disabling the buck switch and the on-timer. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below approximately 155°C (20°C typical hysteresis), normal operation resumes.

Applications Information

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with a design example. Referring to the Block Diagram, the circuit is to be configured for the following specifications:

- V_{OUT} = 5V
- V_{IN} = 6V to 60V
- F_S = 175 kHz
- Minimum load current = 200 mA
- Maximum load current = 1.0A
- Softstart time = 5 ms.

R1 and R2: These resistors set the output voltage, and their ratio is calculated from:

$$R1/R2 = (V_{OUT}/2.5V) - 1 \quad (10)$$

R1/R2 calculates to 1.0. The resistors should be chosen from standard value resistors in the range of 1.0 kΩ - 10 kΩ. A value of 1.0 kΩ will be used for R1 and for R2.

R_{ON}, F_S: R_{ON} can be chosen using Equation 7 to set the nominal frequency, or from Equation 6 if the on-time at a particular V_{IN} is important. A higher frequency generally means a smaller inductor and capacitors (value, size and cost), but higher switching losses. A lower frequency means a higher efficiency, but with larger components. Generally, if PC board space is tight, a higher frequency is better. The resulting on-time and frequency have a ±25% tolerance. Using equation 7 at a nominal V_{IN} of 8V,

$$R_{ON} = \frac{5V \times (8V - 1.4V)}{8V \times 175\ kHz \times 1.18 \times 10^{-10}} - 1.4\ k\Omega = 198\ k\Omega$$

A value of 200 kΩ will be used for R_{ON}, yielding a nominal frequency of 161 kHz at V_{IN} = 6V, and 205 kHz at V_{IN} = 60V.

L1: The guideline for choosing the inductor value in this example is that it must keep the circuit's operation in continuous conduction mode at minimum load current. This is not a strict requirement since the LM5010A regulates correctly when in discontinuous conduction mode, although at a lower frequency. However, to provide an initial value for L1 the above guideline will be used.

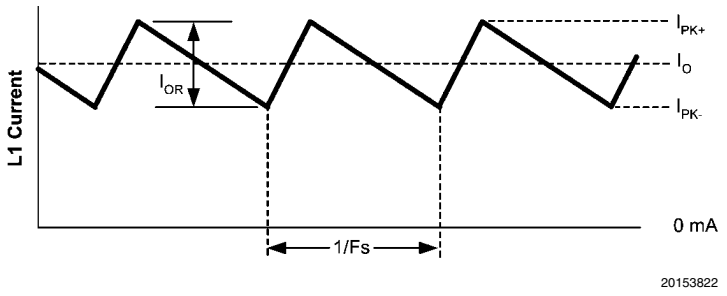


FIGURE 5. Inductor Current

To keep the circuit in continuous conduction mode, the maximum allowed ripple current is twice the minimum load current, or 400 mAp-p. Using this value of ripple current, the inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{I_{OR} \times F_{S(min)} \times V_{IN(max)}} \quad (11)$$

where $F_{S(min)}$ is the minimum frequency of 154 kHz (205 kHz - 25%) at $V_{IN(max)}$.

$$L1 = \frac{5V \times (60V - 5V)}{0.40A \times 154\ kHz \times 60V} = 74.4\ \mu H$$

This provides a minimum value for L1 - the next higher standard value (100 µH) will be used. To prevent saturation, and possible destructive current levels, L1 must be rated for the peak current which occurs if the current limit and maximum ripple current are reached simultaneously (I_{PK} in *Figure 4*). The maximum ripple amplitude is calculated by re-arranging Equation 11 using $V_{IN(max)}$, $F_{S(min)}$, and the minimum inductor value, based on the manufacturer's tolerance. Assume, for this exercise, the inductor's tolerance is ±20%.

$$I_{OR(max)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{L1_{min} \times F_{S(min)} \times V_{IN(max)}} \quad (12)$$

$$I_{OR(max)} = \frac{5V \times (60V - 5V)}{80\ \mu H \times 154\ kHz \times 60V} = 372\ mAp\text{-}p$$

$$I_{PK} = I_{LIM} + I_{OR(max)} = 1.5A + 0.372A = 1.872A$$

where I_{LIM} is the maximum guaranteed current limit threshold. At the nominal maximum load current of 1.0A, the peak inductor current is 1.186A.

R_{CL}: Since it is obvious that the lower peak of the inductor current waveform does not exceed 1.0A at maximum load current (see *Figure 5*), it is not necessary to increase the current limit threshold. Therefore R_{CL} is not needed for this exercise. For applications where the lower peak exceeds 1.0A, see the section entitled Increasing The Current Limit Threshold.

C1: This capacitor limits the ripple voltage at VIN resulting from the source impedance of the supply feeding this circuit, and the on/off nature of the switch current into VIN. At maximum load current, when the buck switch turns on, the current into VIN steps up from zero to the lower peak of the inductor current waveform (I_{PK-} in *Figure 5*), ramps up to the peak value (I_{PK+}), then drops to zero at turn-off. The average current into VIN during this on-time is the load current. For a worst case calculation, C1 must supply this average current during the maximum on-time. The maximum on-time is calculated at V_{IN} = 6V using Equation 5, with a 25% tolerance added:

$$t_{ON(max)} = \left[\frac{1.18 \times 10^{-10} \times (200k + 1.4k)}{6V - 1.4V} + 67\ ns\right] \times 1.25 = 6.5\ \mu s$$

The voltage at VIN should not be allowed to drop below 5.5V in order to maintain V_{CC} above its UVLO.

$$C1 = \frac{I_O \times t_{ON}}{\Delta V} = \frac{1.0A \times 6.5\ \mu s}{0.5V} = 13\ \mu F$$

Normally a lower value can be used for C1 since the above calculation is a worst case calculation which assumes the power source has a high source impedance. A quality ceramic capacitor with a low ESR should be used for C1.

C2 and R3: Since the LM5010A requires a minimum of 25 mVp-p of ripple at the FB pin for proper operation, the required ripple at V_{OUT} is increased by R1 and R2, and is equal to:

$$V_{RIPPLE} = 25\ mVp\text{-}p \times (R1 + R2)/R2 = 50\ mVp\text{-}p$$

This necessary ripple voltage is created by the inductor ripple current acting on C2's ESR + R3. First, the minimum ripple current, which occurs at minimum VIN, maximum inductor value, and maximum frequency, is determined.

$$I_{OR(min)} = \frac{V_{OUT} \times (V_{IN(min)} - V_{OUT})}{L1_{max} \times F_{S(max)} \times V_{IN(min)}}$$

$$= \frac{5V \times (6V - 5V)}{120\ \mu H \times 201\ kHz \times 6V} = 34.5\ mAp\text{-}p \quad (13)$$

The minimum ESR for C2 is then equal to:

$$ESR_{(min)} = \frac{50\ mV}{34.5\ mA} = 1.45\Omega$$

If the capacitor used for C2 does not have sufficient ESR, R3 is added in series as shown in the Block Diagram. The value chosen for C2 is application dependent, and it is recommended that it be no smaller than 3.3 µF. C2 affects the ripple at V_{OUT}, and transient response. Experimentation is usually necessary to determine the optimum value for C2.

C3: The capacitor at the VCC pin provides noise filtering and stability, prevents false triggering of the V_{CC} UVLO at the buck switch on/off transitions, and limits the peak voltage at V_{CC} when a high voltage with a short rise time is initially applied at V_{IN}. C3 should be no smaller than 0.47 µF, and should be a good quality, low ESR, ceramic capacitor, physically close to the IC pins.

C4: The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at each turn-on. A low ESR also ensures a complete recharge during each off-time.

C5: This capacitor suppresses transients and ringing due to lead inductance at VIN. A low ESR, 0.1 µF ceramic chip capacitor is recommended, located physically close to the LM5010A.

C6: The capacitor at the SS pin determines the soft-start time, i.e. the time for the reference voltage at the regulation comparator, and the output voltage, to reach their final value. The capacitor value is determined from the following:

$$C6 = \frac{t_{SS} \times 11.5\ \mu A}{2.5V}$$

For a 5 ms softstart time, C6 calculates to 0.022 µF.

D1: A Schottky diode is recommended. Ultra-fast recovery diodes are not recommended as the high speed transitions at the SW pin may inadvertently affect the IC's operation through external or internal EMI. The diode should be rated for the maximum V_{IN} (60V), the maximum load current (1A), and the peak current which occurs when current limit and maximum ripple current are reached simultaneously (I_{PK} in *Figure 4*), previously calculated to be 1.87A. The diode's forward voltage drop affects efficiency due to the power dissipated during the off-time. The average power dissipation in D1 is calculated from:

$$P_{D1} = V_F \times I_O \times (1 - D)$$

where I_O is the load current, and D is the duty cycle.

FINAL CIRCUIT

The final circuit is shown in *Figure 6*, and its performance is shown in Figures 7 & 8. Current limit measured approximately 1.3A.

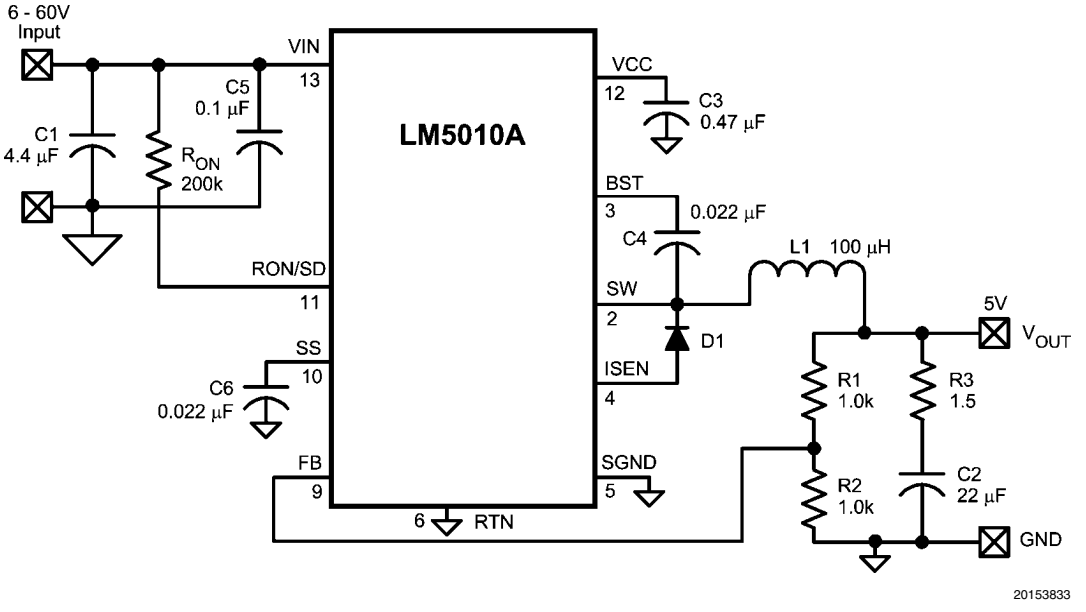


FIGURE 6. Example Circuit

Item	Description	Value
C1	Ceramic Capacitor	(2) 2.2 µF, 100V
C2	Ceramic Capacitor	22 µF, 16V
C3	Ceramic Capacitor	0.47 µF, 16V
C4, C6	Ceramic Capacitor	0.022 µF, 16V
C5	Ceramic Capacitor	0.1 µF, 100V
D1	Schottky Diode	100V, 6A
L1	Inductor	100 µH
R1	Resistor	1.0 kΩ
R2	Resistor	1.0 kΩ
R3	Resistor	1.5 Ω
R_{ON}	Resistor	200 kΩ
U1	National Semi LM5010A	

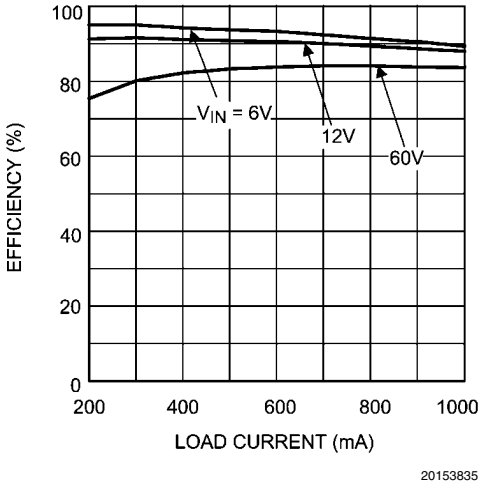


FIGURE 7. Efficiency vs Load Current and V_{IN} Circuit of *Figure 6*

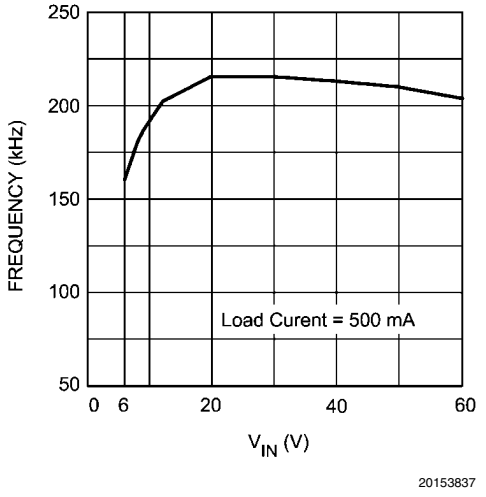


FIGURE 8. Frequency vs V_{IN} Circuit of *Figure 6*

MINIMUM LOAD CURRENT

The LM5010A requires a minimum load current of 500 µA. If the load current falls below that level, the bootstrap capacitor (C4) may discharge during the long off-time, and the circuit will either shutdown, or cycle on and off at a low frequency. If the load current is expected to drop below 500 µA in the application, R1 and R2 should be chosen low enough in value so they provide the minimum required current at nominal V_{OUT}.

LOW OUTPUT RIPPLE CONFIGURATIONS

For applications where low output voltage ripple is required the output can be taken directly from the low ESR output capacitor (C2) as shown in *Figure 9*. However, R3 slightly degrades the load regulation. The specific component values, and the application determine if this is suitable.

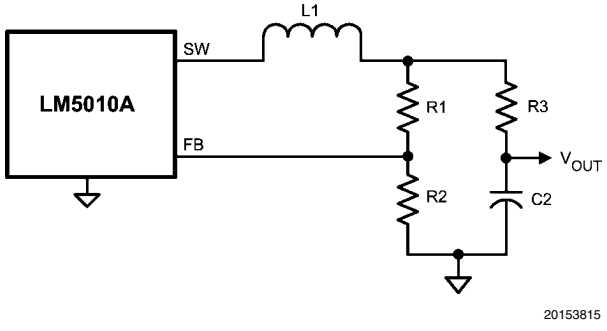


FIGURE 9. Low Ripple Output

Where the circuit of *Figure 9* is not suitable, the circuits of *Figure 10* or *Figure 11* can be used.

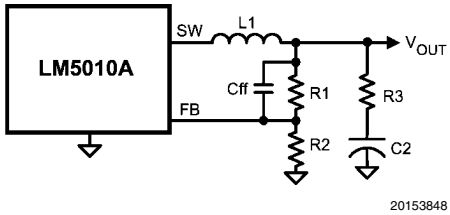


FIGURE 10. Low Output Ripple Using a Feedforward Capacitor

In *Figure 10*, Cff is added across R1 to AC-couple the ripple at V_{OUT} directly to the FB pin. This allows the ripple at V_{OUT} to be reduced, in some cases considerably, by reducing R3. In the circuit of *Figure 6*, the ripple at V_{OUT} ranged from 50 mVp-p at V_{IN} = 6V to 320 mVp-p at V_{IN} = 60V. By adding a

1000 pF capacitor at Cff and reducing R3 to 0.75Ω, the V_{OUT} ripple was reduced by 50%, ranging from 25 mVp-p to 160 mVp-p.

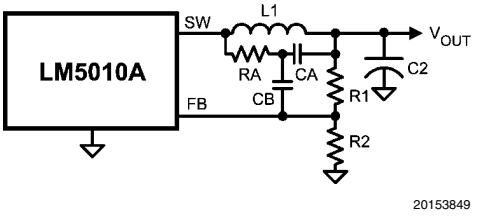


FIGURE 11. Low Output Ripple Using Ripple Injection

To reduce V_{OUT} ripple further, the circuit of *Figure 11* can be used. R3 has been removed, and the output ripple amplitude is determined by C2's ESR and the inductor ripple current. RA and CA are chosen to generate a 40-50 mVp-p sawtooth at their junction, and that voltage is AC-coupled to the FB pin via CB. In selecting RA and CA, V_{OUT} is considered a virtual ground as the SW pin switches between V_{IN} and -1V. Since the on-time at SW varies inversely with V_{IN}, the waveform amplitude at the RA/CA junction is relatively constant. R1 and R2 must typically be increased to more than 10k each to not significantly attenuate the signal provided to FB through CB. Typical values for the additional components are RA = 200k, CA = 680 pF, and CB = 0.01 µF.

INCREASING THE CURRENT LIMIT THRESHOLD

The current limit threshold is nominally 1.25A, with a minimum guaranteed value of 1.0A. If, at maximum load current, the lower peak of the inductor current (I_{PK-} in *Figure 5*) exceeds 1.0A, resistor R_{CL} must be added between S_{GND} and I_{SEN} to increase the current limit threshold to equal or exceed that lower peak current. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator. I_{PK-} is calculated from:

$$I_{PK-} = I_{O(max)} - \frac{I_{OR(min)}}{2} \quad (14)$$

where $I_{O(max)}$ is the maximum load current, and $I_{OR(min)}$ is the minimum ripple current calculated using Equation 13. R_{CL} is calculated from:

$$R_{CL} = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A} \quad (15)$$

where 0.11Ω is the minimum value of the internal resistance from SGND to ISEN. The next smaller standard value resistor should be used for R_{CL}. With the addition of R_{CL}, and when the circuit is in current limit, the upper peak current out of the SW pin (I_{PK} in *Figure 4*) can be as high as:

$$I_{PK} = \frac{1.5A \times (150\ m\Omega + R_{CL})}{R_{CL}} + I_{OR(MAX)}$$

where $I_{OR(max)}$ is calculated using Equation 12. The inductor L1 and diode D1 must be rated for this current. If I_{PK} exceeds 2A , the inductor value must be increased to reduce the ripple amplitude. This will necessitate recalculation of $I_{OR(min)}$, I_{PK-}, and R_{CL}.

Increasing the circuit's current limit will increase power dissipation and the junction temperature within the LM5010A. See the next section for guidelines on this issue.

PC BOARD LAYOUT and THERMAL CONSIDERATIONS

The LM5010A regulation, over-voltage, and current limit comparators are very fast, and will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all the components must be as close as possible to their associated pins. The two major current loops have currents which switch very fast, and so the loops should be as small as possible to minimize conducted and radiated EMI. The first loop is that formed by C1, through the VIN to SW pins, L1, C2, and back to C1. The second loop is that formed by D1, L1, C2, and the SGND and ISEN pins. The ground connection from C2 to C1 should be as short and direct as possible, preferably without going through vias. Directly connect the SGND and RTN pin to each other, and they should be connected as directly as possible to the C1/C2 ground line without going through vias. The power dissipation within the IC can be approximated by determining the total conversion loss (P_{IN} - P_{OUT}), and then subtracting the power losses in the free-wheeling diode and the inductor. The power loss in the diode is approximately:

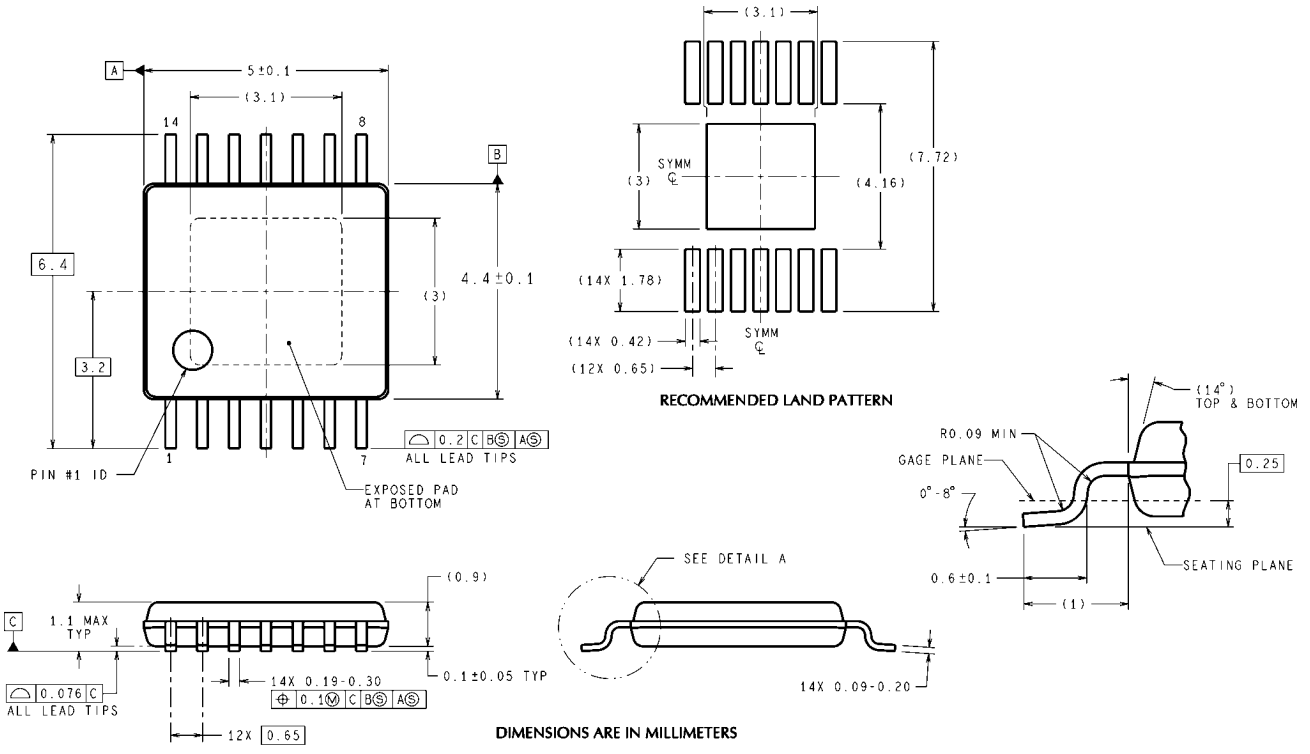
$$P_{D1} = I_O \times V_F \times (1\text{-}D)$$

where Io is the load current, V_F is the diode's forward voltage drop, and D is the duty cycle. The power loss in the inductor is approximately:

$$P_{L1} = I_O^2 \times R_L \times 1.1$$

where R_L is the inductor's DC resistance, and the 1.1 factor is an approximation for the AC losses. If it is expected that the internal dissipation of the LM5010A will produce high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the IC package bottom should be soldered to a ground plane, and that plane should both extend from beneath the IC, and be connected to exposed ground plane on the board's other side using as many vias as possible. The exposed pad is internally connected to the IC substrate. The use of wide PC board traces at the pins, where possible, can help conduct heat away from the IC. The four No Connect pins on the TSSOP package are not electrically connected to any part of the IC, and may be connected to ground plane to help dissipate heat from the package. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead TSSOP Package
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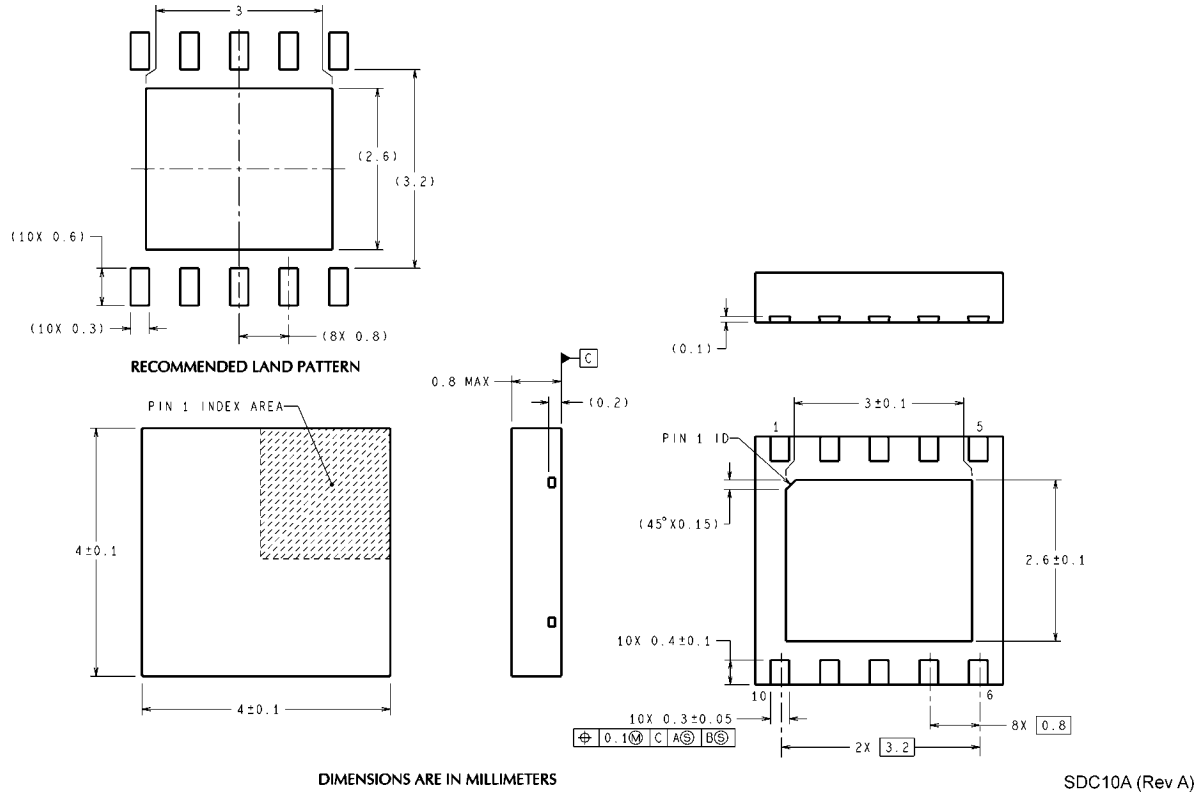

10-Lead LLP Package
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Notes

Notes

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Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
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