ISL91301A, ISL91301B

Triple/Quad Output Power Management IC

FN8966
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The ISL91301A is a 4-phase, three output programmable Power Management IC (PMIC) and the ISL91301B is a 4-phase, four output programmable PMIC. They are optimized with highly efficient, synchronous buck converters capable of multiphase and single-phase operations. The devices can deliver 4A per phase continuous output current for 2.8V to 5.5V supply voltages or 3A per phase current for wider 2.5V to 5.5V supply voltages. It features four buck controllers and can reconfigure its power stages to these controllers. This flexibility allows seamless design-in for a wide range of applications that require high output power and small solution size.

The ISL91301A and ISL91301B integrate low ON-resistance MOSFETs and programmable PWM frequency, allowing the use of very small external inductors and capacitors. They feature automatic Diode Emulation and Pulse Skipping modes under light-load conditions to further improve efficiency and maximize battery life. The ISL91301A and ISL91301B feature a controller based on the proprietary Renesas R5 technology which provides tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and requires no external compensation.

In addition to the standard interrupt, chip enable, and watchdog reset functions, the ISL91301A and ISL91301B also feature four MPIOs and two GPIOs capable of supporting SPI, I^2C communication protocol, and various other pin mode functions.

Features

- Triple output 2+1+1 phases (ISL91301A) or quad output single phase (ISL91301B)
- 4A per phase for the 2.8V to 5.5V supply voltage, VIN_SEL = AVIN
- 3A per phase for the 2.5V to 5.5V supply voltage, VIN_SEL = GND
- Small solution size
- High efficiency (93% for $3.8V_{IN}/1.8V_{OUT}$)
- Low IQ in low power mode
- Proprietary control scheme reduces output capacitor and supports fast load transient (such as 50A/µs per phase)
- ±0.7% system accuracy, remote voltage sensing
- Programmable PWM frequency from 2MHz to 6MHz
- I^2C programmable output from 0.3V to 2V
- Independent Dynamic Voltage Scaling (DVS) for each output
- Soft-start and fault detection (UV, OV, OC, OT), short-circuit protection
- 2.570mmx2.919mm 42 ball WLCSP with 0.4mm pitch

Applications

- Smartphones, AR/VR glasses, drones
- Optical transceiver modules
- Artificial Intelligence (AI) processors
- Client/enterprise/data center SSD, NAS

Related Literature

For a full list of related documents, visit our website

- ISL91301A, ISL91301B device pages

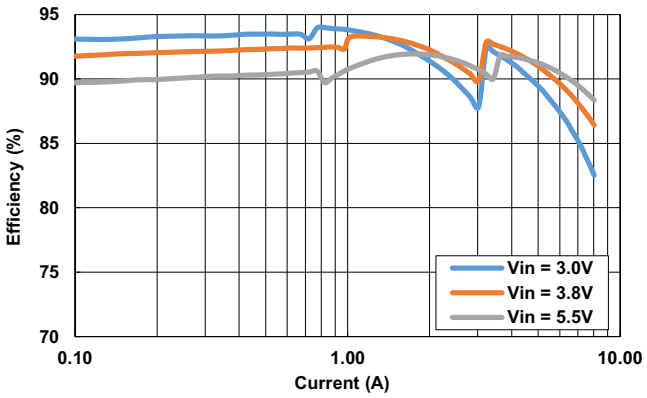


Figure 1. Dual Phase Efficiency (V_{OUT} = 1.8V), Load Sweep (0.1A to 8A)

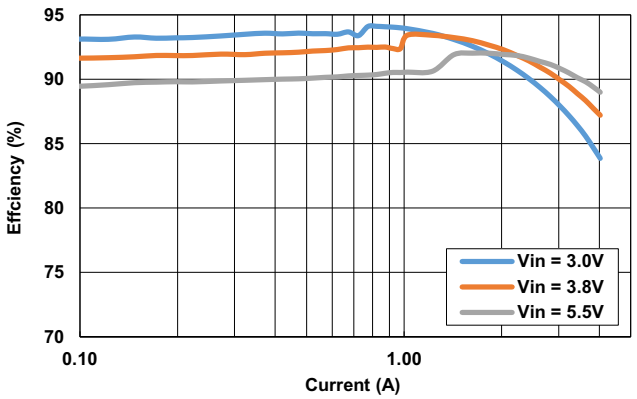


Figure 2. Single Phase Efficiency (V_{OUT} = 1.8V), Load Sweep (0.1A to 4A)

Contents

1. Overview

1.1 Block Diagram

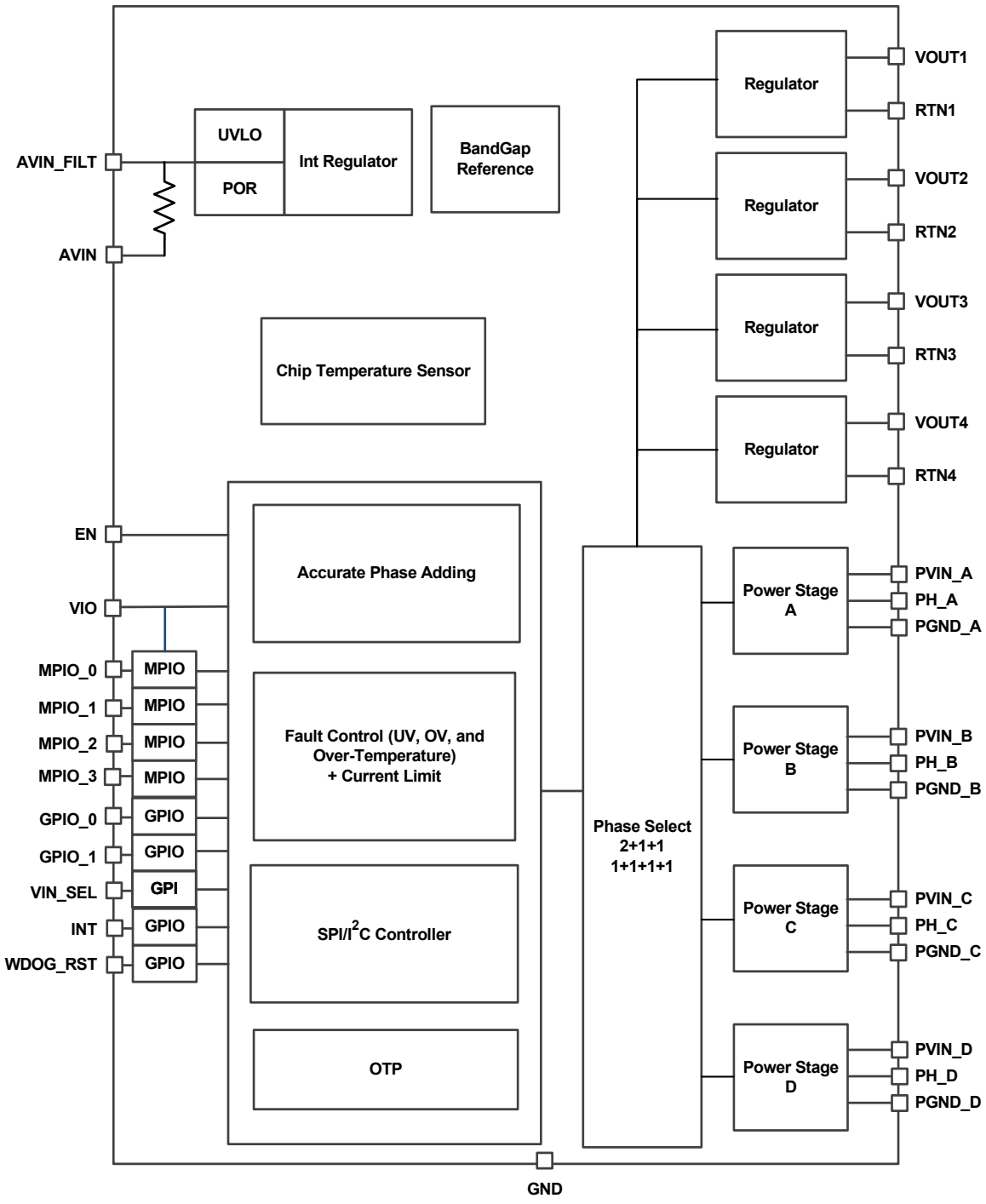


Figure 3. Block Diagram

1.2 Typical Application Diagrams

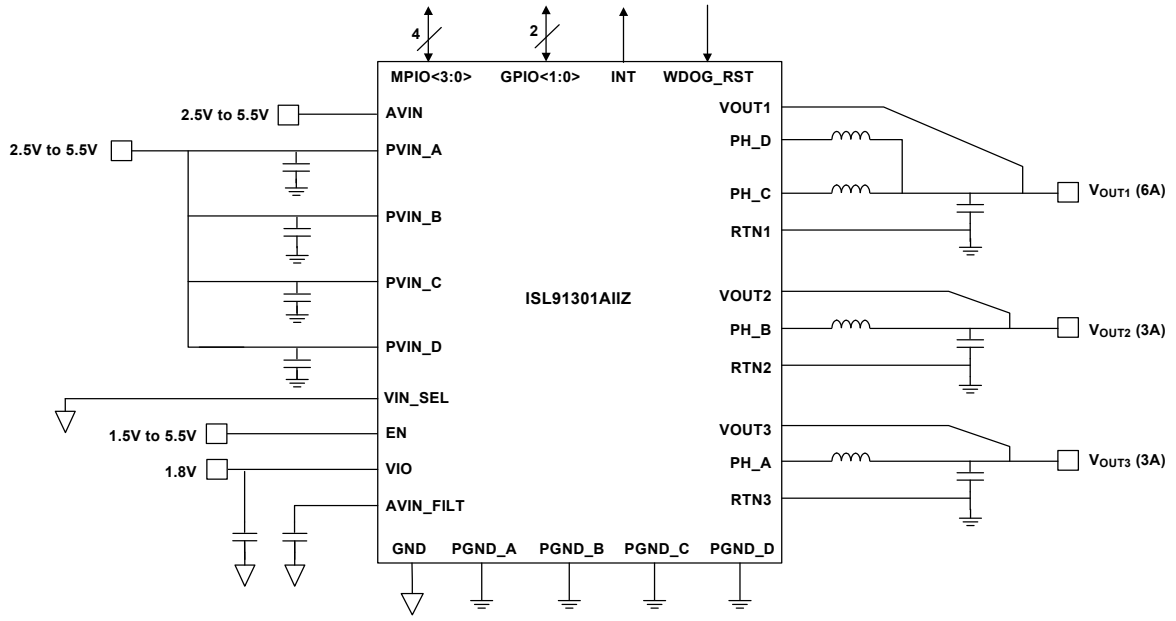


Figure 4. 2 Phase + 1 Phase + 1 Phase (3A/Phase, VIN_min = 2.5V)

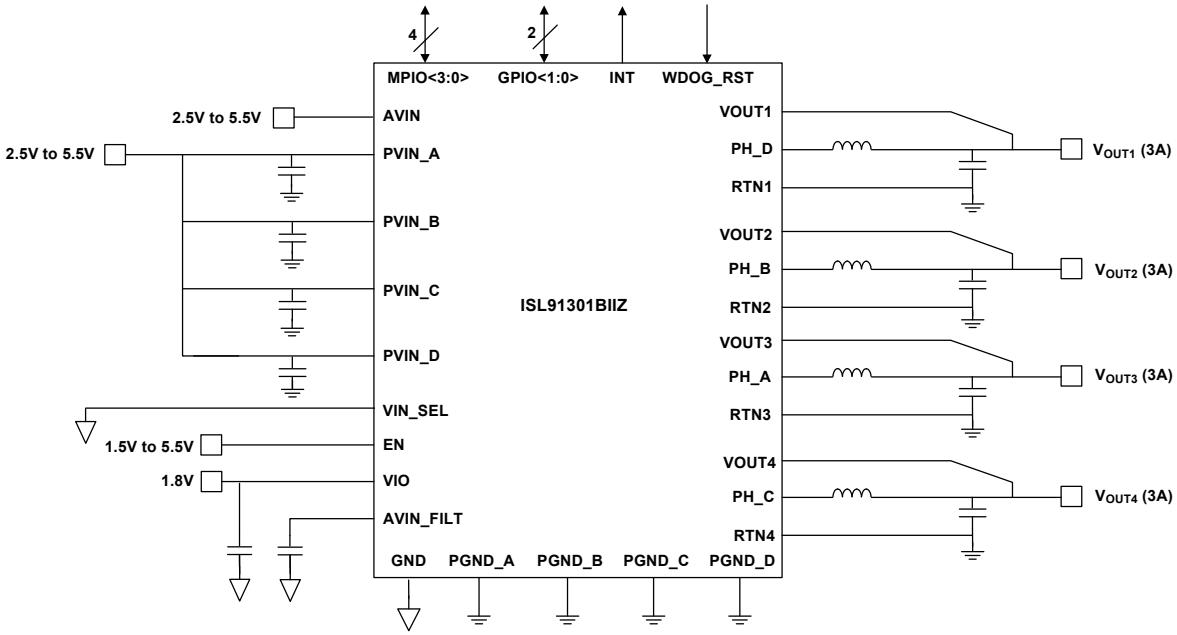


Figure 5. 1 Phase + 1 Phase + 1 Phase + 1 Phase (3A/Phase, VIN_min = 2.5V)

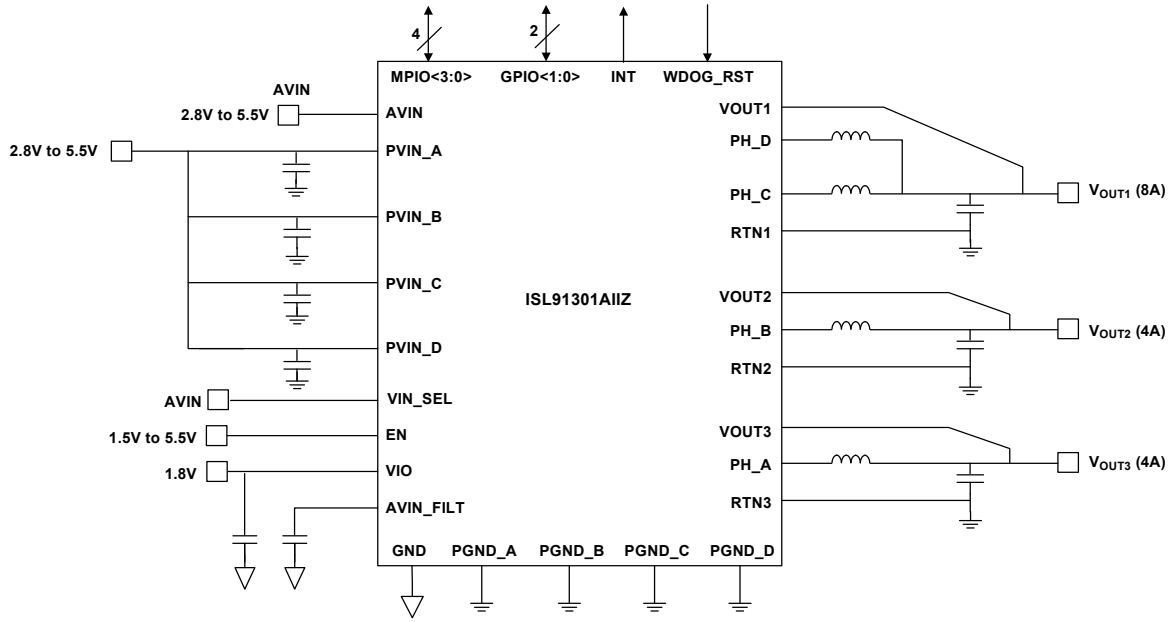


Figure 6. 2 Phase + 1 Phase + 1 Phase (4A/Phase, VIN_min = 2.8V)

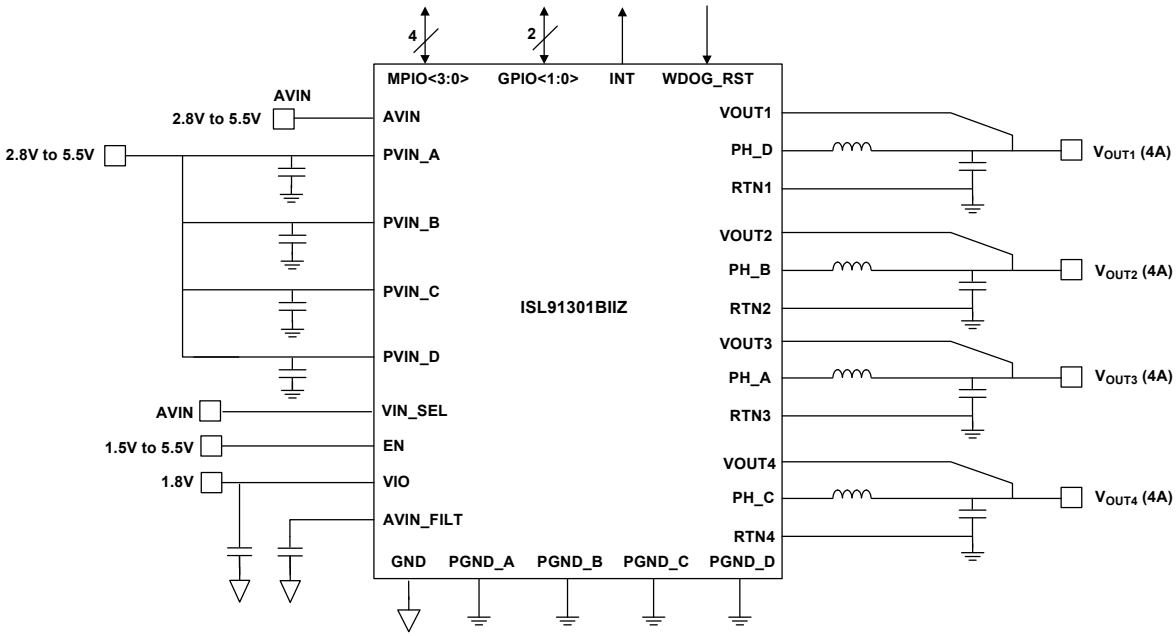


Figure 7. 1 Phase + 1 Phase + 1 Phase + 1 Phase (4A/Phase, VIN_min = 2.8V)

1.3 Ordering Information

Part Number (Notes 3, 4)	Part Marking	Temperature Range (°C)	Tape and Reel (Units) (Note 2)	Package (RoHS Compliant)	Pkg. Dwg #
ISL91301AIIZ-T	301A	-40 to +85	3k	2.570mmx2.919mm, 42 Ball WLCSP	W6x7.42B
ISL91301BIIZ-T	301B	-40 to +85	3k	2.570mmx2.919mm, 42 Ball WLCSP	W6x7.42B
ISL91301AII-H-EV1Z	Evaluation Board (VIN_SEL pin = AVIN, support 4A/phase, Supply Voltage range: 2.8V ~ 5.5V)				
ISL91301AII-L-EV1Z	Evaluation Board (VIN_SEL pin = GND, support 3A/phase, Supply voltage range: 2.5V ~ 5.5V)				
ISL91301BII-H-EV1Z	Evaluation Board (VIN_SEL pin = AVIN, support 4A/phase, Supply Voltage range: 2.8V ~ 5.5V)				
ISL91301BII-L-EV1Z	Evaluation Board (VIN_SEL pin = GND, support 3A/phase, Supply voltage range: 2.5V ~ 5.5V)				

Notes:

1. For additional part options contact your local sales office.
2. See TB347 for details about reel specifications.
3. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
4. For Moisture Sensitivity Level (MSL), see the ISL91301A and ISL91301B device pages. For more information about MSL, see TB363.

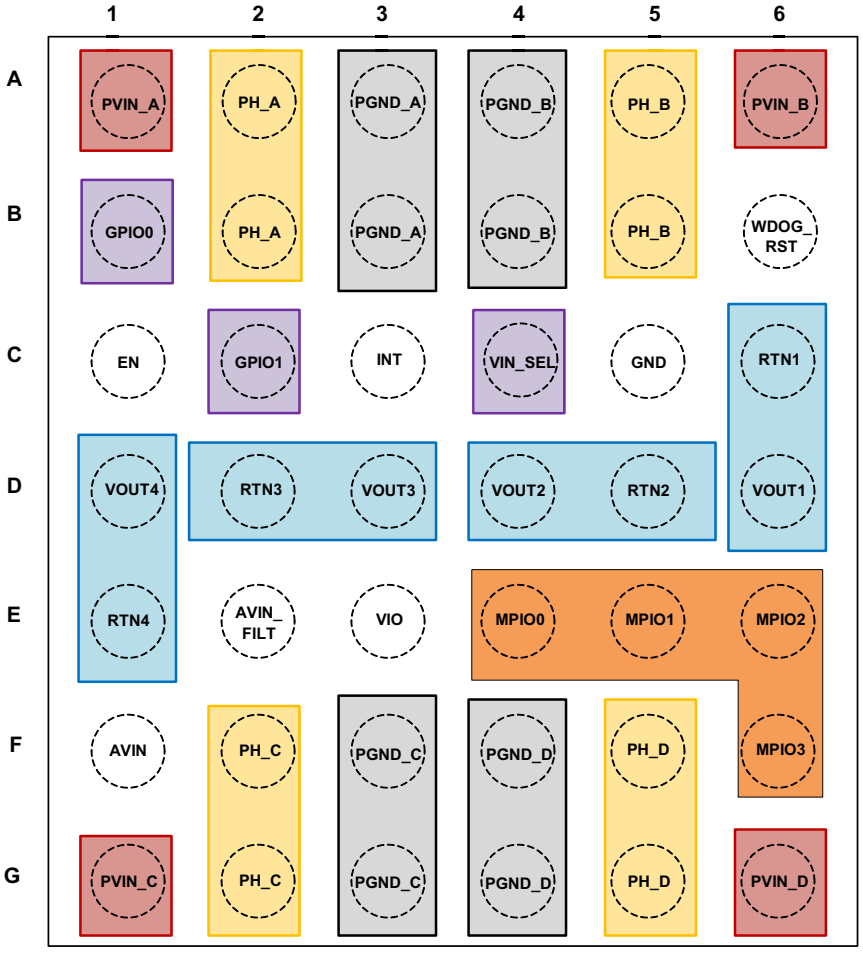
Table 1. Key Differences Between Family of Parts

Part Number	Pin Configuration	Pitch	Output Configuration	Load Per Phase
ISL91302B	54 Ball 6x9 WLCSP	0.4mm	Single Output (4 + 0 Phase)	5A
	54 Ball 6x9 WLCSP	0.4mm	Dual Output (3 + 1 Phase)	5A
	54 Ball 6x9 WLCSP	0.4mm	Dual Output (2 + 2 Phase)	5A
ISL91301A	42 Ball 6x7 WLCSP	0.4mm	Triple Output (2+1+1 Phase)	4A
ISL91301B	42 Ball 6x7 WLCSP	0.4mm	Quad Output (1+1+1+1 Phase)	4A
ISL91211A	54 Ball 6x9 WLCSP	0.4mm	Triple Output (2+1+1 Phase)	5A
ISL91211B	54 Ball 6x9 WLCSP	0.4mm	Quad Output (1+1+1+1 Phase)	5A
ISL91212A	54 Ball 6x9 WLCSP	0.4mm	Triple Output (2+1+1 Phase)	5A
ISL91212B	54 Ball 6x9 WLCSP	0.4mm	Quad Output (1+1+1+1 Phase)	5A

1.4 Pin Configuration

ISL91301A, ISL91301B
42 Ball 6x7 WLCSP
Top View

Jedec Standard:
Balls Down, A1 Top Left Corner



1.5 Pin Descriptions

Pin Location	Pin Name	Type	Description
A1	PVIN_A	Input	Power supply for Power Stage A
A2, B2	PH_A	Output	Switching node for Power Stage A
A3, B3	PGND_A	Input	Ground connection for Power Stage A
A4, B4	PGND_B	Input	Ground connection for Power Stage A
A5, B5	PH_B	Output	Switching node for Power Stage B
A6	PVIN_B	Input	Power supply for Power Stage B
B1	GPIO0	Input/Output	I^2C clock
B6	WDOG_RST	Input	Digital input, resets bucks to default output voltage
C1	EN	Input	Master chip enable input, NMOS logic threshold
C2	GPIO1	Input/Output	I^2C data
C3	INT	Output	Interrupt line
C4	VIN_SEL	Input	For 2.8V~5.5V V_{IN} range, 4A per phase I_{OUT} capability: Tie to AVIN For 2.5V ~ 5.5V V_{IN} range, 3A per phase I_{OUT} capability: Tie to GND
D1	VOUT4	Input	Output voltage sense for Buck4
E1	RTN4	Input	Remote ground sense for Buck4
C5	GND	Input	Analog chip ground
C6	RTN1	Input	Remote ground sense for Buck1
D2	RTN3	Input	Remote ground sense for Buck3
D3	VOUT3	Input	Output voltage sense for Buck3
D4	VOUT2	Input	Output voltage sense for Buck2
D5	RTN2	Input	Remote ground sense for Buck2
D6	VOUT1	Input	Remote output voltage sense for Buck1
E2	AVIN_FILT	Output	Filtered analog supply voltage, 2.5V to 5.5V (VIN_SEL tied to GND); 2.8V to 5.5V (VIN_SEL tied to AVIN) Place a decoupling capacitor close to the IC
E3	VIO	Input	Supply voltage for digital communications. Nominally connected to 1.8V supply, can be tied to AVIN.
E4	MPIO0	Input/Output	SPI clock
E5	MPIO1	Input/Output	SPI/I^2C selector. Low = SPI, High = I^2C. For more information, see "Serial Communication Interface".
E6	MPIO2	Input/Output	SPI master out, slave in
F1	AVIN	Input	Analog supply voltage, 2.5V to 5.5V (VIN_SEL tied to GND); 2.8V to 5.5V (VIN_SEL tied to AVIN)
F2, G2	PH_C	Output	Switching node for Power Stage C
F3, G3	PGND_C	Input	Ground connection for Power Stage C
F4, G4	PGND_D	Input	Ground connection for Power Stage D
F5, G5	PH_D	Output	Switching node for Power Stage D
F6	MPIO3	Input/Output	SPI master in, slave out
G1	PVIN_C	Input	Power supply connection for Power Stage C
G6	PVIN_D	Input	Power supply connection for Power Stage D

1.6 I/O Pin Configuration

The ISL91301A and ISL91301B feature two general purpose pins and four multipurpose I/O pins. MPIO 0-3 are used for SPI and GPIO 0-1 are used for I^2C communications in pin mode 0x0. Additional pin modes are available upon request. For more information, contact your local Renesas sales office.

Table 2. I/O Pin Mode

Pin Mode	MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1	Description
0x0	SCK	SS_B	MOSI	MISO	SCL	SDA	I^2C/SPI both available
0x1	SCK	SS_B	MOSI	MISO	EN_A	EN_B	SPI mode with hardware enables for Bucks 1-4
0x2	PGOOD1	PGOOD2	PGOOD3	PGOOD4	SCL	SDA	I^2C with individual PGOODs for Bucks 1-4
0x3	SCK	SS_B	MOSI	MISO	DVS_PIN_A	DVS_PIN_B	SPI with hardware DVS pins
0x4	DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	SCL	SDA	I^2C with global DVS mode with PGOOD1 and PGOOD2
0x5	DVS1_0	DVS1_1	DVS2_0	DVS2_1	SCL	SDA	I^2C with full pin controlled DVS for BUCK1/BUCK2
0x6	DVS1_0	DVS1_1	DVS2_0	DVS3_0	SCL	SDA	I^2C with full pin controlled DVS for BUCK1 and 1-pin DVS for BUCK2/BUCK3
0x7	DVS1_0	DVS2_0	DVS3_0	DVS4_0	SCL	SDA	I^2C with 1-pin DVS for each buck
0xC	MPIO_ DATA<0>	MPIO_ DATA<1>	MPIO_ DATA<2>	MPIO_ DATA<3>	SCL	SDA	I^2C with parallel controllable data lines.

Table 3. Pin Mode Description

Name	Definition
SCK	SPI Clock
SS_B	SPI/I^2C selector. Low = SPI, High = I^2C.
MOSI	SPI Master out, slave in
MISO	SPI Master in, slave out
I2C_CLK	I^2C Clock
I2C_SDA	I^2C Data
PGOOD1, PGOOD2, PGOOD3, PGOOD4	Four power-good out pins (one per buck)
EN_A, EN_B	Two buck enable input pins. A single buck enable pin can enable/disable up to four bucks. A buck's enable/disable can be controlled from only one enable pin (EN_A, EN_B)
DVS_A, DVS_B	Two DVS input pins. A single DVS pin can control the DVS voltage for up to four bucks. A buck's DVS voltage can be controlled from only one DVS pin (DVS_A or DVS_B)
DVS_PIN1, DVS_PIN0	DVS look-up table to allow two pin to control up to four buck.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
PVIN and AVIN Pins to GND	-0.3	+6	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x00)	-0.3	+2.0	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x01)	-0.3	+2.4	V
VOUT Pin (BUCKx_VOUTFBDIV[1:0] = 0x02)	-0.3	+3.0	V
PH to PGND	-0.3	+0.3 + PVIN	V
VIO, EN Pins to GND	-0.3	+0.3 + AVIN	V
RTN, GND to PGND	-0.3	+0.3	V
INT, MPIO, GPIO Pins to GND	-0.3	+0.3 + VIO	V
ESD Rating (Note 5)	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

5. ESD ratings apply to external pins only.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
42 Ball WLCSP Package Notes 6, 7	42	0.5

Notes:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
7. For θ_{JC}, the “case temp” location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Junction Temperature	-40	+125	°C
Supply Voltage			
AVIN to GND	2.5	5.5	V
PVIN to PGND	2.5	5.5	V
VIO Voltage (VIO to GND)	1.7	AVIN	V
INT, MPIO, GPIO pin to GND	0	VIO	V

2.4 Analog Specifications

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, frequency = 4MHz, VIO = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted**.

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Input Supply						
Supply Voltage	AVIN/PVIN	VIN_SEL = AVIN	**2.8**		**5.5**	V
	AVIN/PVIN	VIN_SEL = PGND	**2.5**		**5.5**	V
AVIN Supply Current	I_Q	EN = 0V		0.1	**1**	µA
AVIN + PVINx Supply Current		EN = 0V		<1	**6**	µA
AVIN + PVINx Supply Current EN = AVIN = PVINx = 3.7V		All BUCKx_EN[0] = 0x0		17		µA
		BUCK1_EN[0] = 0x1, all other BUCKx_EN[0] = 0x0, not switching DCM operation		82		µA
		BUCK2, 3 or 4_EN[0] = 0x1, all other BUCKx_EN[0] = 0x0, not switching DCM operation		62		µA
		BUCK1_EN[0] = 0x1, all other BUCKx_EN[0] = 0x0, not switching, forced CCM operation		1.2		mA
		BUCK2, 3 or 4_EN[0] = 0x1, all other BUCKx_EN[0] = 0x0, not switching, forced CCM operation		1		mA
AVIN UVLO Rising Threshold	VUVLOR	VIN_SEL = AVIN	**2.80**	2.86	**2.95**	V
AVIN UVLO Falling Threshold	VUVLOF	VIN_SEL = AVIN	**2.65**	2.71	**2.80**	V
AVIN UVLO Rising Threshold	VUVLOR	VIN_SEL = PGND	**2.50**	2.58	**2.65**	V
AVIN UVLO Falling Threshold	VUVLOF	VIN_SEL = PGND	**2.30**	2.34	**2.45**	V
Buck Regulation						
Buck Output Voltage Range (Each Output)	V_{OUT}	BUCKx_VOUTFBDIV[1:0] = 0x00	**0.300**		**1.2**	V
		BUCKx_VOUTFBDIV[1:0] = 0x01	**0.375**		**1.5**	V
		BUCKx_VOUTFBDIV[1:0] = 0x02	**0.5**		**2.0**	V
Output Voltage Step Size	V_{STEP}	10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x00		1.2		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x01		1.5		mV
		10-bit control, BUCKx_VOUTFBDIV[1:0] = 0x02		2.0		mV
Output Voltage Accuracy (Note 9)	V_{ACC}	CCM, V_{OUT} > 0.6V	-0.3		0.3	%
		CCM, V_{OUT} > 0.6V T_A = -10°C to +85°C	-0.7		0.7	%
		CCM, V_{OUT} < 0.6V	-4		4	mV
		CCM, V_{OUT} < 0.6V T_A = -10°C to +85°C	-5.5		5.5	mV
Current Matching	I_{MATCH}	I_{OUT} = 4A per phase in the ISL91301A		10		%
Dynamic Response						
Boot-Up Time	V_{BT}	Delay time from when PVIN, AVIN, and EN are asserted to Buck1 PWM switching. This time includes internal reference startup, OTP load, and Buck controller calibration time.		1.4		ms

AVIN/PVIN = 3.7V, V_{OUT} = 1V, L = 220nH, frequency = 4MHz, VIO = 1.8V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +85°C unless otherwise noted. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Dynamic Voltage Scaling (Output Slew Rate)	V_{DVS}	2.5V < V_{IN} < 5.5V, 3mV/µs	**-15**		**15**	%
Frequency						
Switching Frequency (CCM)	f_{SW}			4		MHz
CCM Frequency Tolerance	f_{SW_TOL}		**-15**		**15**	%
Power Stage						
Buck Output Current (Each Phase)		2.8V < V_{IN} < 5.5V, VIN_SEL = AVIN			**4**	A
		2.5V < V_{IN} < 5.5V, VIN_SEL = GND			**3**	A
High-Side Switch ON-Resistance	$r_{DS(ON)}$	Conditions: PVIN = 3.7V, current = 300mA		55		mΩ
Low-Side Switch ON-Resistance	$r_{DS(ON)}$	Conditions: PVIN = 3.7V, current = 300mA		14		mΩ
MPIO/GPIO						
MPIO/GPIO Operating Conditions						
Allowable Range of Supply for Operation	VIO		**1.7**	1.8	**AVIN**	V
Chip Enable Logic Threshold Level						
Low-Level Input Voltage Range	V_{IL}				**0.5**	V
High-Level Input Voltage	V_{IH}		**1.35**			V
MPIO/GPIO Logic Threshold Levels						
Low-Level Input Voltage Range	V_{IL}				**0.25 * V_{IO}**	V
High-Level Input Voltage	V_{IH}		**0.75 * V_{IO}**			V
Hysteresis On Input	V_{HYS}		**0.1 * V_{IO}**			V
Low-Level Output	V_{OL}	1mA			**0.4**	V
High-Level Output	V_{OH}	1mA (250µA for 20% drive configuration)	**V_{IO} - 0.4**			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}				**3.4**	MHz
SPI Frequency Capability	f_{SPI}			26		MHz
Protection						
HSD Current Limit	I_{LIMIT}	2.5V < V_{IN} < 5.5V ISL91301A Phase D, OC = 10A	**-10**		**10**	%
		2.5V < V_{IN} < 5.5V ISL91301A Phase A, B, OC = 6A	**-10**		**10**	%
		2.5V < V_{IN} < 5.5V ISL91301B Phase A, B, C, D, OC = 6A	**-10**		**10**	%
Output UVP Threshold Accuracy	V_{UVP}	Thresholds: -250mV	**-35**		**35**	mV
Output OVP Threshold Accuracy	V_{OVP}	Thresholds: +250mV	**-35**		**35**	mV
Thermal Shutdown Threshold	T_{SPS}	2.5V < V_{IN} < 5.5V	**143**		**162**	°C
		Hysteresis		55		°C

Notes:

8. Parameters with MIN and/or MAX limits established by test, characterization, and/or design.
9. V_{OUT} feedback divider ratio equals 1 (BUCKx_VOUTFBDIV[1:0] = 0x00).

3. Output Configurations

Table 4. Output Configuration

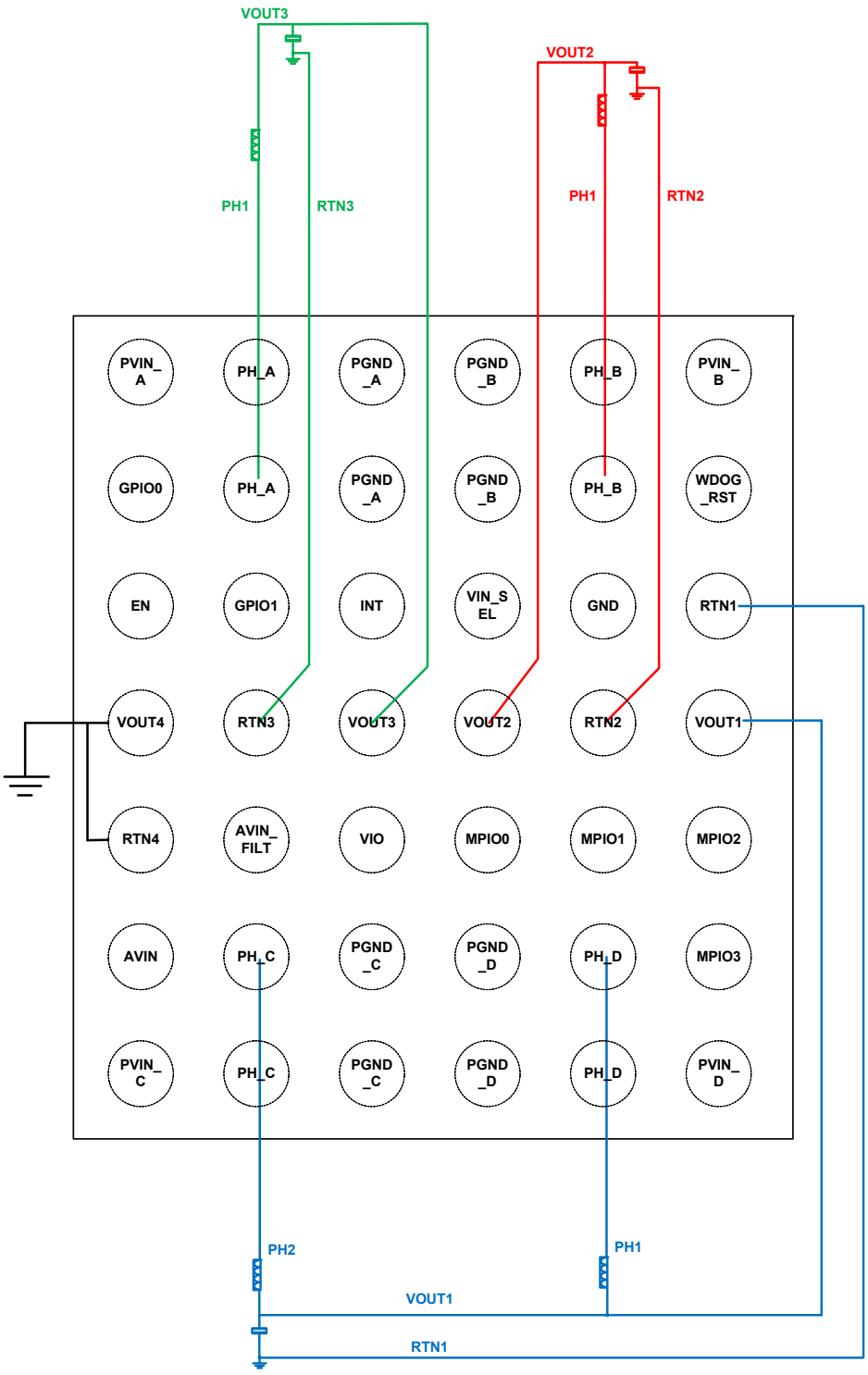
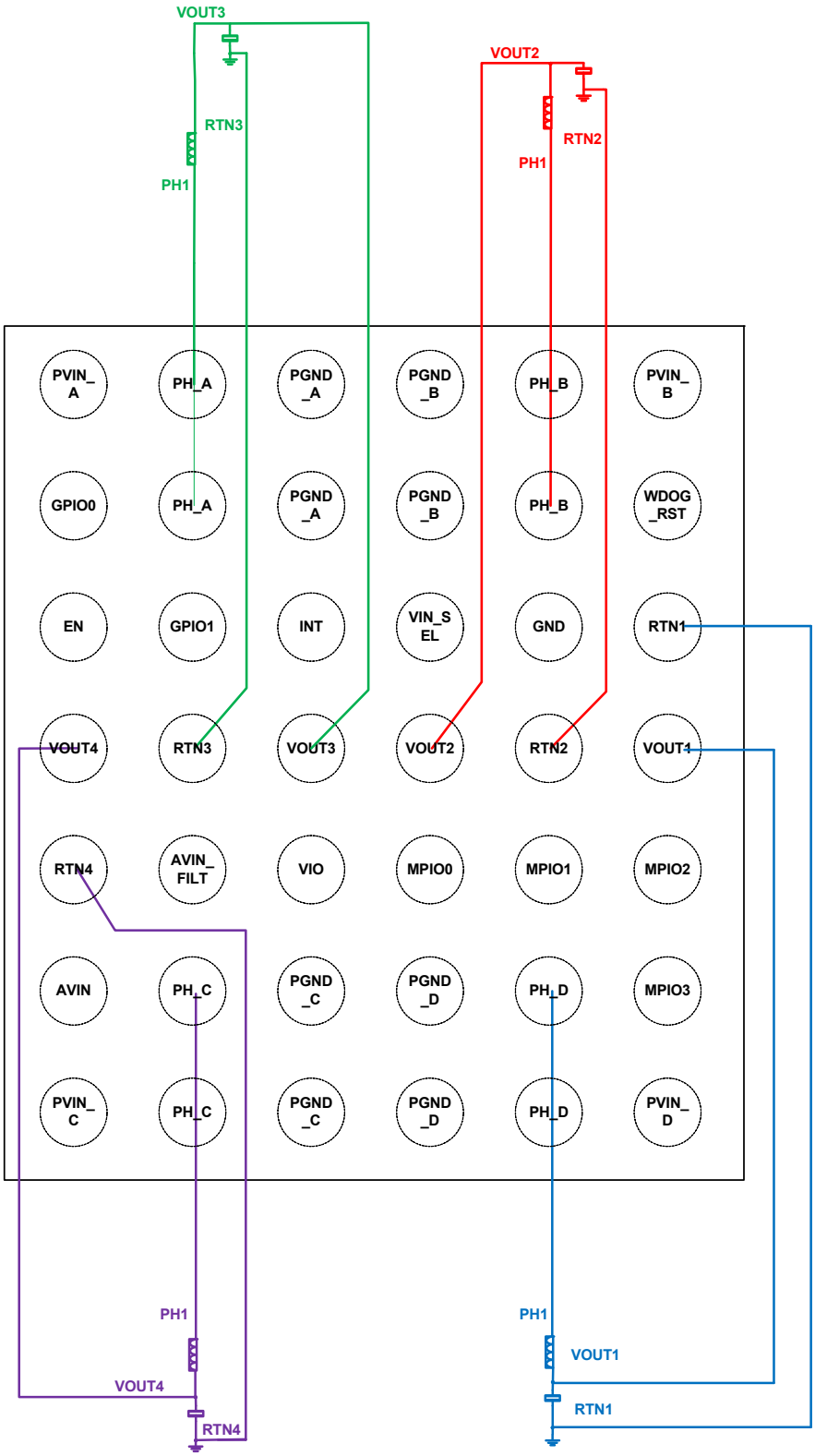
Output Configuration	Power Stage Assignment	Diagram
2-phase + 1-phase + 1-phase Connect: VOUT4/RTN4 to PGND Plane	2-phase: Controller #1 (VOUT1) • Ph1: PH_D • Ph2: PH_C 1-phase: Controller #2 (VOUT2) • Ph1: PH_B 1-phase: Controller #3 (VOUT3) • Ph1: PH_A	ISL91301A Configuration 

Table 4. Output Configuration (Continued)

Output Configuration	Power Stage Assignment	Diagram
1-phase + 1-phase + 1-phase + 1-phase	1-phase: Controller #1 (VOUT1) • Ph1: PH_D 1-phase: Controller #2 (VOUT2) • Ph1: PH_B 1-phase: Controller #3 (VOUT3) • Ph1: PH_A 1-phase: Controller #4 (VOUT4) • Ph1: PH_C	ISL91301B Configuration 

4. Typical Performance Curves

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF.

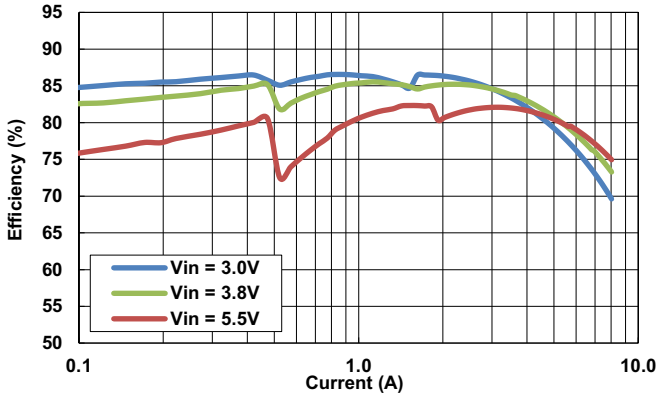


Figure 8. Dual-Phase Efficiency (V_{OUT} = 0.6V), Continuous Load Sweep (0.1A to 8A)

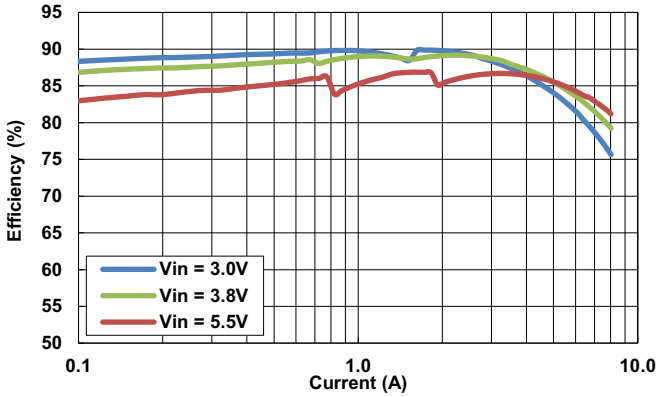


Figure 9. Dual-Phase Efficiency (V_{OUT} = 0.9V), Continuous Load Sweep (0.1A to 8A)

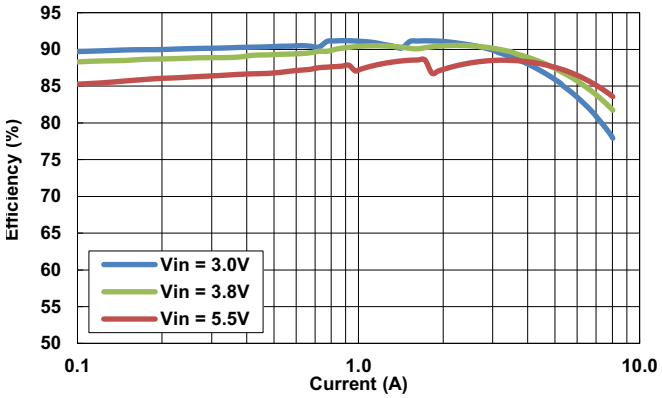


Figure 10. Dual-Phase Efficiency (V_{OUT} = 1.1V), Continuous Load Sweep (0.1A to 8A)

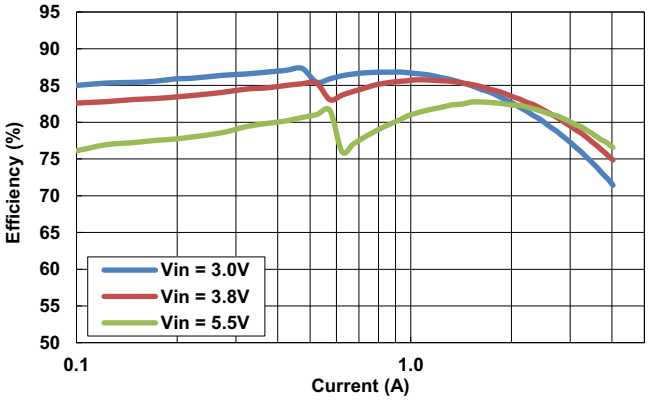


Figure 11. Single-Phase Efficiency (V_{OUT} = 0.6V), Continuous Load Sweep (0.1A to 4A)

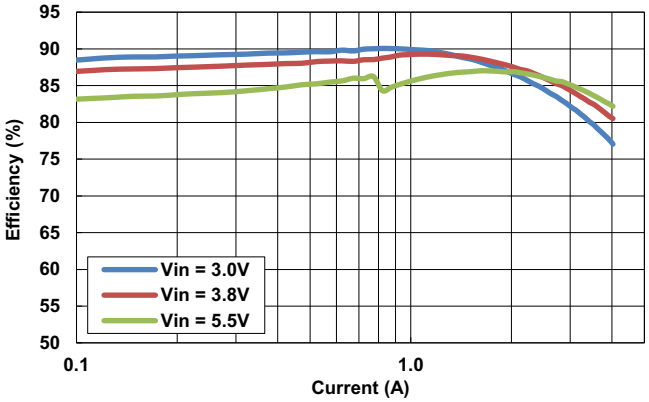


Figure 12. Single-Phase Efficiency (V_{OUT} = 0.9V), Continuous Load Sweep (0.1A to 4A)

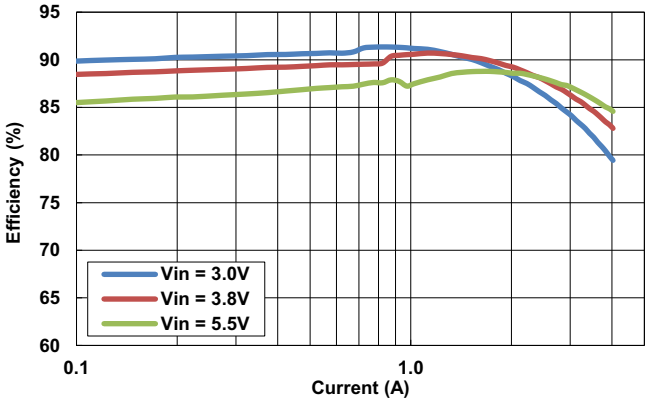
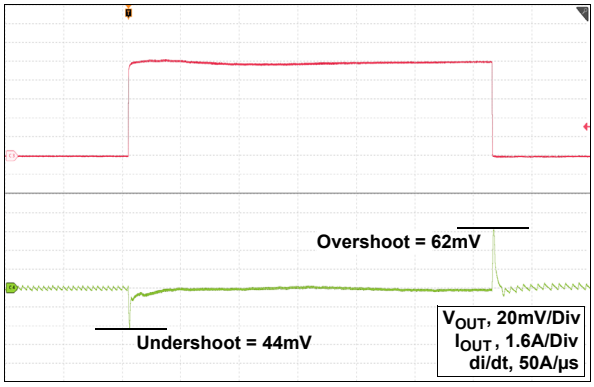


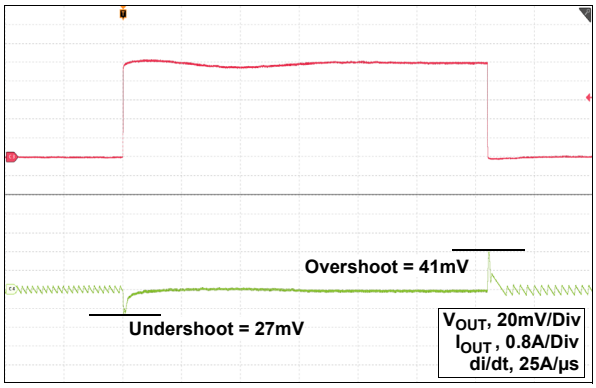
Figure 13. Single-Phase Efficiency (V_{OUT} = 1.1V), Continuous Load Sweep (0.1A to 4A)

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**



Load Step Slew Rate: 50A/µs, 0.1A to 8A
220nH Inductor (Cyntec PIFE25201T-R22MS)
4x22µF Capacitor (0603 6.3V Murata)
2x4.3µF Capacitor (0402 Low ESL Murata)
4x1µF Capacitor (0204 Taiyo Yuden)

Figure 14. Dual-Phase Load Transient (8A/160ns)



Load Step Slew Rate: 25A/µs, 0.1A to 4A
220nH Inductor (Cyntec PIFE25201T-R22MS)
2x22µF Capacitor (0603 6.3V Murata)
2x4.3µF Capacitor (0402 Low ESL Murata)

Figure 15. Single-Phase Transient (4A/160ns)

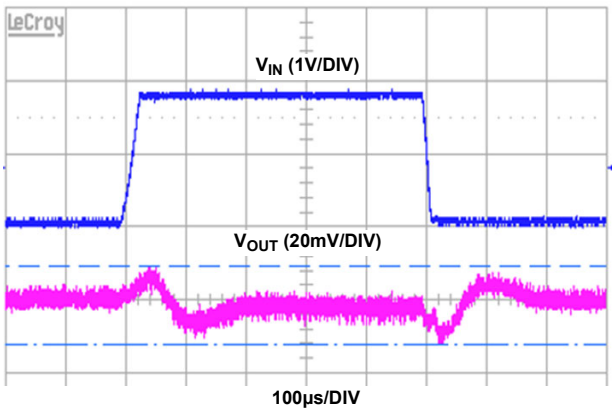


Figure 16. Dual-Phase Line Transient, V_{OUT} = 1V, V_{IN} = 3.1V to 4.8V, Load = 8A, TR and TF = 15µs

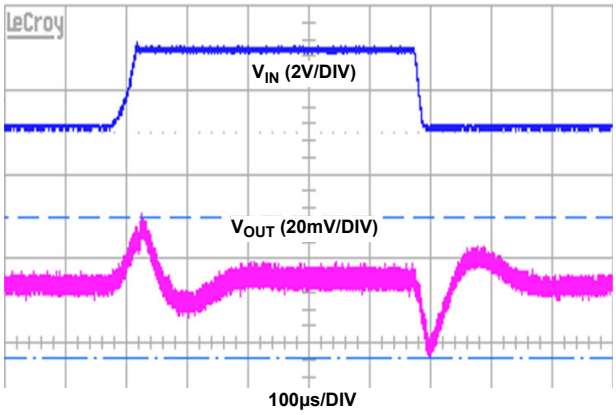


Figure 17. Single-Phase Line Transient, V_{OUT} = 1V, V_{IN} = 3.1 to 4.8V, Load = 4A, TR and TF = 15µs

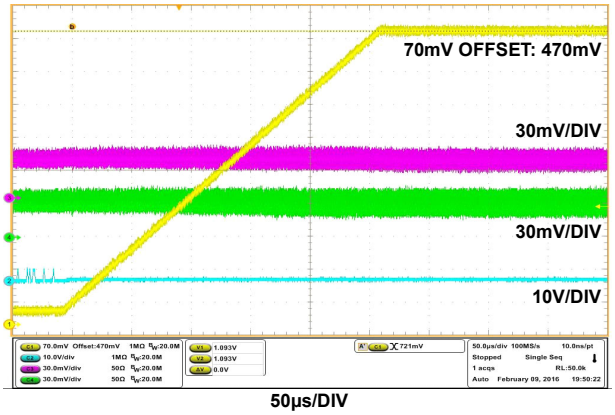


Figure 18. 0.5V to 1.1V DVS (A), Load = 4A, Slew Rate = 3mV/µs, C1 - V_{OUT}, C2 - I_{LX1}, C3 - I_{LX2}, C4 - DVS Command

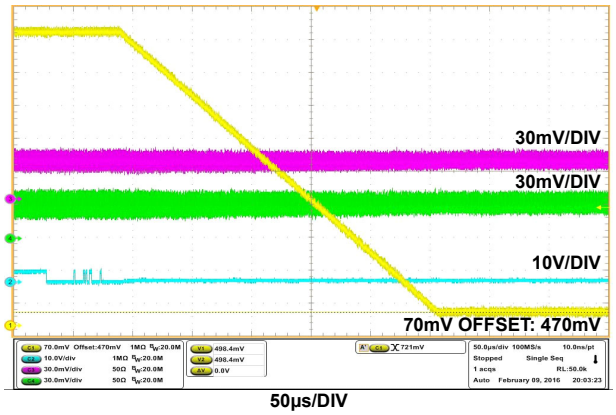


Figure 19. 0.5V to 1.1V DVS (B), LOAD = 4A, Slew Rate = 3mV/µs, C1 - V_{OUT}, C2 - I_{LX1}, C3 - I_{LX2}, C4 - DVS Command

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

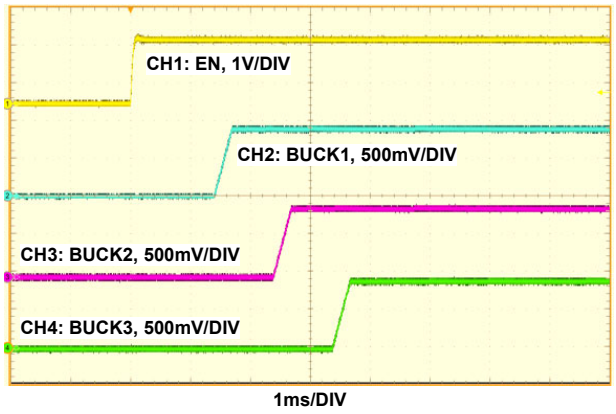


Figure 20. ISL91301A Startup by EN, VOUT1, 2, 3 = 0.9V

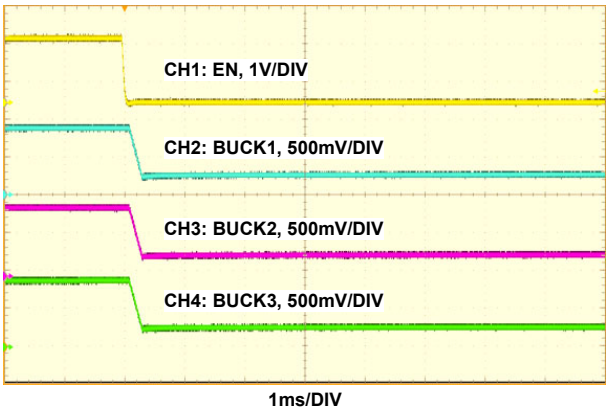


Figure 21. ISL91301A Shutdown by EN, VOUT1, 2, 3 = 0.9V

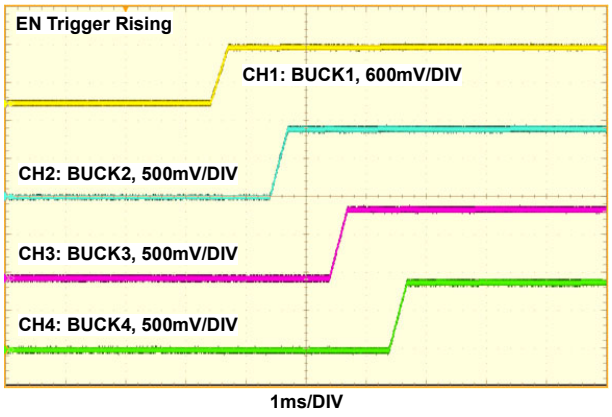


Figure 22. ISL91301B Startup by EN, VOUT1, 2, 3, 4 = 0.9V

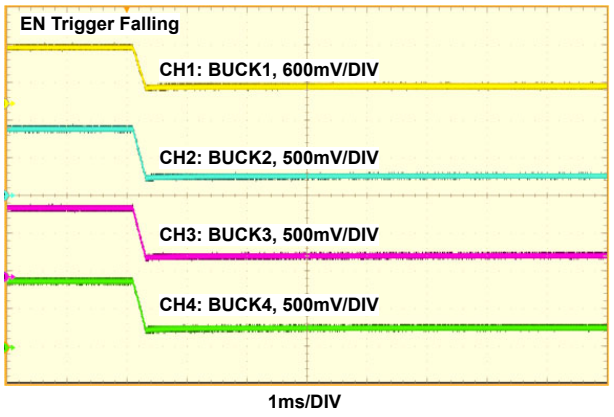


Figure 23. ISL91301B Shutdown by EN, VOUT1, 2, 3, 4 = 0.9V

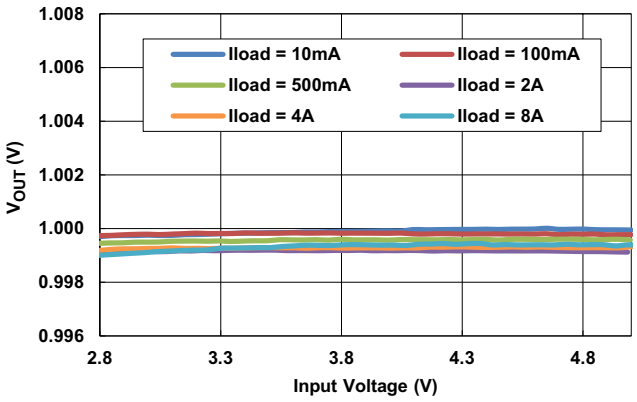


Figure 24. Dual-Phase, V_{OUT} vs V_{IN} (10mA to 8A)

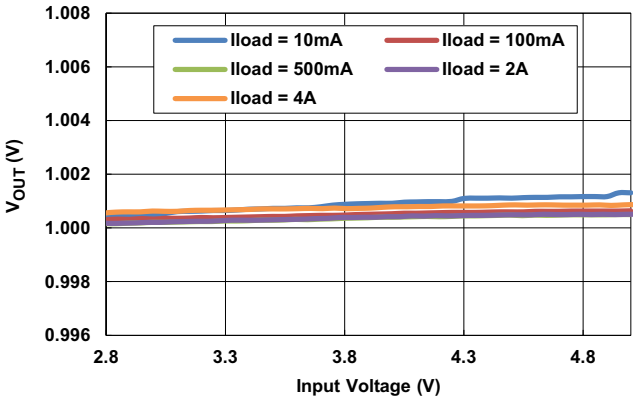


Figure 25. Single-Phase, V_{OUT} vs V_{IN} (10mA to 4A)

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

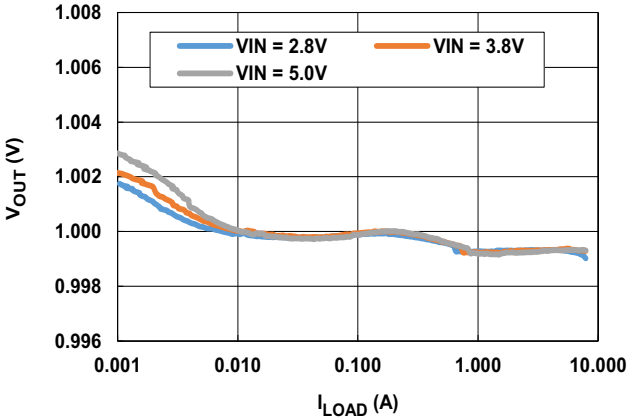


Figure 26. Dual-Phase, V_{OUT} vs Load (1mA to 8A)

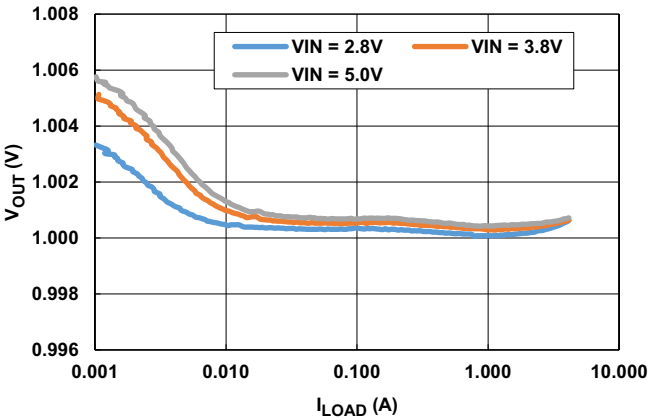


Figure 27. Single-Phase, V_{OUT} vs Load (1mA to 4A)

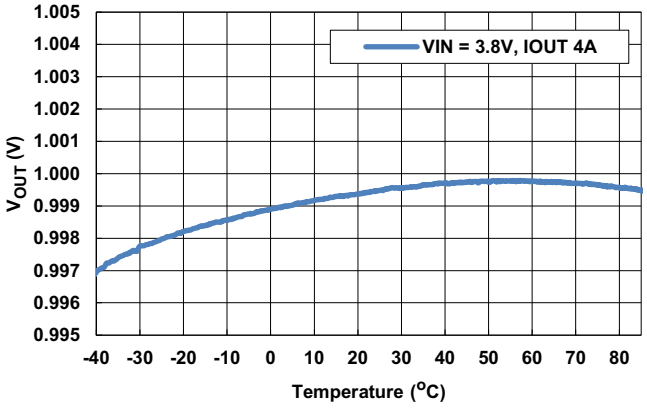


Figure 28. Dual-Phase Forced CCM, V_{OUT} vs Temperature (-40°C to +85°C)

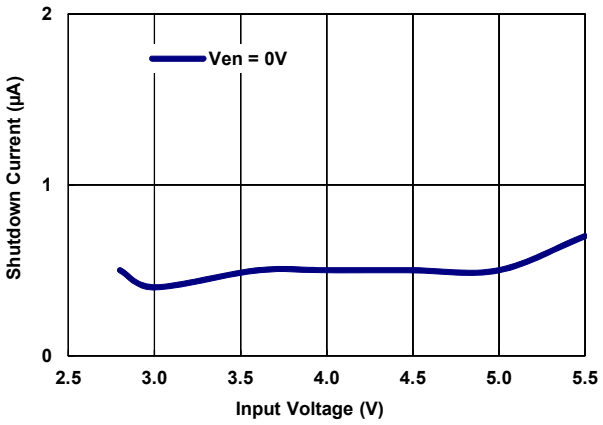


Figure 29. Shutdown Current vs V_{IN}

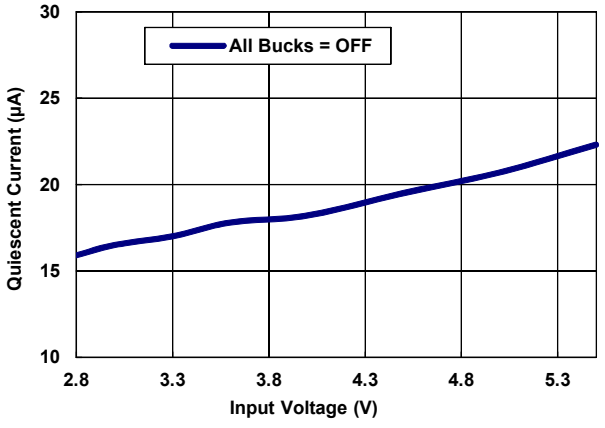


Figure 30. Quiescent Current (All Bucks Off) vs V_{IN}

Unless otherwise noted, operating conditions are: V_{IN} = 3.8V, V_{OUT} = 1V, VIO and Enable = 1.8V, T_A = +25°C, f_{SW} = 4MHz, 2+1+1 configuration, L = 220nH per phase, SW1: C_{OUT} = 2x22µF + 2x4.3µF + 4x1µF, SW2-3: C_{OUT} = 1x22µF + 4x4.3µF. **(Continued)**

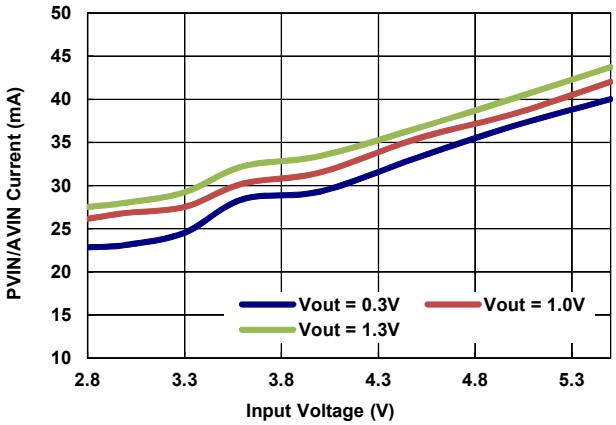


Figure 31. Single-Phase PVIN/AVIN Current (PWM Switching) vs V_{IN}

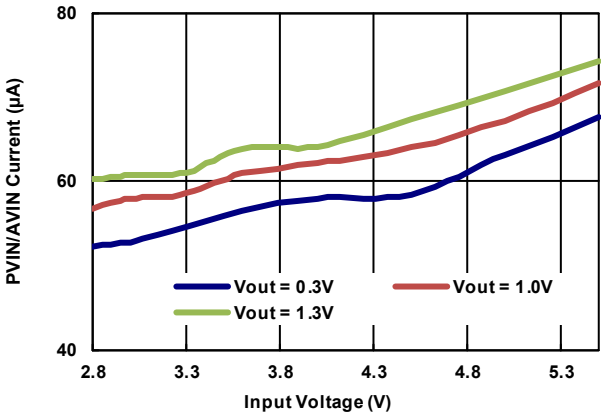


Figure 32. Single-Phase PVIN/AVIN Current (PFM Switching) vs V_{IN}

5. Applications Information

5.1 Inductor Selection

The ISL91301A and ISL91301B are high performance PMICs with integrated synchronous buck converters that can deliver up to 4A of continuous current per phase at 0.3V to 2V regulated voltage. The ISL91301B is designed to operate with up to four single phases (1+1+1+1 configuration), and the ISL91301A is designed to work with two single phases and one dual phase (2+1+1 configuration) at an optimized switching frequency of 2MHz ~ 4MHz. For support relating to a switching frequency of 6MHz, contact your local Renesas sales office. In the dual phase configuration, each channel requires an inductor of equal value and should be capable of delivering the maximum load divided by two.

Table 5. Recommended Output Inductors

Manufacturer	Part Number	L x W x H (mm)	Value (nH)	DCR mΩ (Typ)	ISAT (Typ)
Cyntec	HMLB25201T	2.5x2.0x1.0	220	9.4	7.0
Taiyo Yuden	MAKK2520HR22M	2.5x2.0x1.0	220	16	8.5
Cyntec	HTTN2016T	2.0x1.6x1.0	220	13	7.2
Murata	DFE2016E	2.0x1.6x1.0	240	16	7.0
Coilcraft	XEL4020-561ME	4.0x4.0x2.0	560	8.0	11.3

5.2 Output Capacitor Selection

Output capacitors are needed to filter square voltage at the phase node into a regulated output voltage. The amount of output capacitance required is based on the maximum load step, the slew rate of the load step, and the maximum allowable voltage regulation tolerance during the transient. The amount of ripple voltage at the output capacitor is also a design constraint; the total peak-to-peak ripple voltages produced from the output capacitor is equal to its ESR, multiplied by the worst case inductor ripple current.

Use ceramic capacitors due to their low ESR and ESL properties. Make sure to select X7R or X5R type capacitors and account for DC bias effects. A wide range of output capacitor values can be used.

Table 6. Recommended Output Capacitors

Manufacturer	Part Number	Case Size	Value (µF)	Voltage (V)
TDK	C1608X5R1A226M080AC	0603	22	10
TDK	C0510X6S0G105M030AC	0204	1	4
Murata	LLD154R60G435ME01	0402	4.3	4
Murata	LLL1U4R60G435ME22	0204	4.3	4

5.3 Input Capacitor Selection

Ceramic input capacitors source the AC component of the input current flowing into the high-side MOSFETs. Place them as close to the IC as possible. A 10µF local decoupling capacitor is recommended for each phase PVIN. If long wires are used to bring power to the IC, use additional “bulk” capacitors between C_{IN} and the battery/power supply to dampen ringing and overshoot at start-up.

Internal analog reference circuits also require additional filtering at the AVIN_FILT pin.

Table 7. Recommended Input Capacitors

Manufacturer	Part Number	Case Size	Value (µF)	Volt (V)	Input
TDK Corp	CGB2A1X5R1A105M033BC	0402	1	10	AVIN_FILT
Kemet	C0402C104K8RACTU	0402	0.1	10	AVIN_FILT
Samsung	CL05A10MP5NUNC	0402	10	10	PVIN

5.4 Dynamic Voltage Scaling (DVS)

The ISL91301A and ISL91301B has several options to achieve Dynamic Voltage Scaling (DVS). Each buck controller has four independently programmable voltage settings that can set the output voltage. The settings are DVS0, DVS1, DVS2, and DVS3. By changing the DVS number selected, the corresponding output voltage is selected. The two methods to select the DVS are:

Method 1) Use internal registers to select DVS by writing to the BUCKx_DVSSELECT[1:0] bits in the BUCKx_DVSSEL register for each respective buck using SPI or I^2C.

To use this method, the BUCKx_DVSCTRL[0] bit has to be set to “0x0” for the corresponding buck. The BUCKx_DVSSELECT[1:0] setting allows you to switch between the four different DVS settings, each of which corresponds to a set of DVS registers holding the DVS information.

For example, DVS0 corresponds to BUCKx_DVS0VOUT92[7:0] and BUCKx_DVS0VOUT10[1:0]. The two register values combined represent the complete 10-bit DAC code for DVS0.

Table 8. DVS Method Selection

BUCKx_DVSCTRL[0]	
0x0	Use BUCKx_DVSSELECT[1:0] to select active DVS configuration
0x1	Use DVS pin(s) to control DVS selection

Table 9. DVS Pointers

BUCKx_DVSSELECT[1:0]	Active DVS for BUCKx
0x0	DVS0
0x1	DVS1
0x2	DVS2
0x3	DVS3

Each output voltage is set writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the most significant eight bits and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register has been written. Table 10 shows the relationship between the DVS word and VOUT.

Table 10. 10-Bit DVS Code to Voltage Translation

FBDIV	1.0	0.8	0.6
DAC [9:0]	V_{OUT} (V)	V_{OUT} (V)	V_{OUT} (V)
0x000	0.0000	0.0000	0.0000
0x001	0.0012	0.0015	0.0020
…			
0x200	0.6173	0.7716	1.0288
0x201	0.6185	0.7731	1.0308
…			
0x3E5	1.199	1.4988	1.9983

Method 2) Use the GPIO/MPIO pins to configure DVS. There are five variations depending on the IO_PINMODE register setting. See Table 2 for information about the variations.

Note: To use DVS with the GPIO/MPIO pins, IO_PINMODE must be OTP programmed before a startup boot sequence is initiated. On-the-fly programming is not recommended for the following configurations.

(i) IO_PINMODE = 0x3: SPI with multiple buck DVS pins.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
SCK	SS_B	MOSI	MISO	DVS_A	DVS_B

BUCKx_DVSPIN_CFG[1:0] bits in BUCKx_SHUTDN_DLY registers maps the particular buck DVS to DVS_x GPIO pin. Same pin can be used to control DVS for all buck controllers. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. The active DVS follows the DVS_x pin logic for the respective buck. See Table 11 for more information.

Table 11.

BUCKx_DVSPIN_CFG[1:0]	Function	
0x0	DVS_A pin	Active DVS for BUCKx
	0	DVS0
	1	DVS1
0x1	DVS_B pin	Active DVS for BUCKx
	0	DVS0
	1	DVS1
0x2	Reserved	
0x3	BUCKx DVS0 pointer follows I^2C/SPI programmed register setting.	

(ii) IO_PINMODE = 0x4: I^2C with Global DVS and PGOOD pins

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
DVS_PIN1	DVS_PIN0	PGOOD1	PGOOD2	I2C_CLK	I2C_SDA

The BUCKx_DVSPIN_CTRL[1:0] bits in the BUCKx_DVSCFG register in combination with the DVS_PIN1 and DVS_PIN2 set the active DVS for the respective BUCK. See Table 12 for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence.

Table 12. Global DVS Pin Logic

BUCKx_DVSPIN_CTRL[1:0]	DVS_PIN1	DVS_PIN0	Active DVS
0x0	X	X	DVS0
0x1	X	0	DVS0
	X	1	DVS1
0x2	0	X	DVS0
	1	X	DVS2
0x3	0	0	DVS0
	0	1	DVS1
	1	0	DVS2
	1	1	DVS3

Note: The 'X' indicates that either a 0 or 1 is acceptable.

(iii) IO_PINMODE = 0x5: I²C with two DVS pins for Buck1 and two DVS pins for Buck2

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK2_DVS1	I2C_CLK	I2C_SDA

The active DVS is selected based on the combined BUCKx_DVS0 and BUCKx_DVS1 input pin logic. See Table 13 for more information. BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence.

Table 13. Active DVS for 2 DVS Pins Configuration

BUCKx_DVS1	BUCKx_DVS0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1
1	0	DVS2
1	1	DVS3

(iv) IO_PINMODE = 0x6: I²C with full 2-pin DVS control for Buck1 and 1-pin DVS control for Buck2 and Buck3.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK1_DVS1	BUCK2_DVS0	BUCK3_DVS0	I2C_CLK	I2C_SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. BUCK1_DVS0 and BUCK1_DVS0 follow the same active DVS table as in IO_PINMODE = 0x5. See Table 13 for more information.

Table 14. Active DVS for 1 DVS Pin Configuration

BUCKx_DVS1	BUCKx_DVS0	Active DVS for BUCKx
0	0	DVS0
0	1	DVS1

(v) IO_PINMODE = 0x7: I²C with 1 pin DVS control for each buck.

MPIO0	MPIO1	MPIO2	MPIO3	GPIO0	GPIO1
BUCK1_DVS0	BUCK2_DVS0	BUCK3_DVS0	BUCK4_DVS0	I2C_CLK	I2C_SDA

BUCKx_DVSCTRL[0] should be OTP programmed high before the startup sequence. BUCKx_DVS0 follows the same active DVS table for 1 DVS pin configuration as in IO_PINMODE = 0x6. See Table 14 for more information.

5.5 Configuring DVS Speed

5.5.1 Power-Up and Shutdown Slew Rate Setting

The BUCKx_RSPPUP[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates (DVS speed) in BUCKx only during V_{OUTx} power-up. Similarly, the BUCKx_RSPPDN[2:0] bits in the BUCKx_RSPCFG0 register set the slew rates in BUCKx during normal V_{OUTx} shutdown. The achievable slew rates vary with different FBDIV settings (factory OTP programmed). For more details, see Register "BUCK1_RSPCFG0".

6. DVS Transition Slew Rate Setting

The BUCKx_RSPUP[2:0] and BUCKx_RSPDN[2:0] bits in the BUCKx_RSPCFG1 register set the slew rates (DVS speed) in BUCKx during normal DVS transition. The achievable slew rates will vary with different FBDIV settings (factory OTP programmed). For more details, see Register "BUCK1_RSPCFG1".

6.1 Output Voltage Setting

Each output voltage is set by writing a 10-bit word to DVS Configuration 1 (BUCKx_DVS0CFG1 register) and DVS Configuration 0 (BUCKx_DVS0CFG0 register) in each buck. Configuration 1 holds the MSB and Configuration 0 holds the last two bits of the 10-bit word. The output voltage does not change until the LSB register is written. "BUCK1_DVS0CFG1" shows the relationship between the DVS word and V_{OUT}.

6.2 Power Sequencing

When the master chip Enable (EN) pin is brought above an NMOS threshold, the ISL91301A and ISL91301B powers up its key biasing circuits, loads the OTP configuration registers, and performs one of the following actions based on the preprogrammed OTP setting:

- **Manual buck start-up:**
  Program the internal IO_BUCKx_EN bits to "1" from I^2C/SPI to enable the respective buck. When IO_PINMODE = 0x1, the EN_A and EN_B pins can also be used to enable the respective bucks. If using this pin mode, the internal IO_BUCKx_EN bits should be set high in OTP. The slew rate of each buck during its soft-start is specified by the BUCKx_RSPPUP[2:0] bits.

Note: The programmable delay (1ms to 63ms) using BUCKx_EN_DLY[5:0] is not used for Manual Buck startup.

- **Auto Buck start-up from master chip enable pin:**
  Run a predetermined startup sequence for the buck outputs as soon as BOOT is complete. The slew rate of each buck during its soft-start is specified in BUCKx_RSPPUP[2:0].

Figure 33 provides an example of power-up configuration. The master chip enable pin (EN) transitions from 0 to 1 and OTP is loaded for 1.4ms. After initial 1.4ms boot interval, the buck output start-up sequence begins. BUCK1_EN_DLY is set for 0ms, BUCK2_EN_DLY is set for 1ms, BUCK3_EN_DLY is set for 2ms, and BUCK3_EN_DLY is set for 3ms.

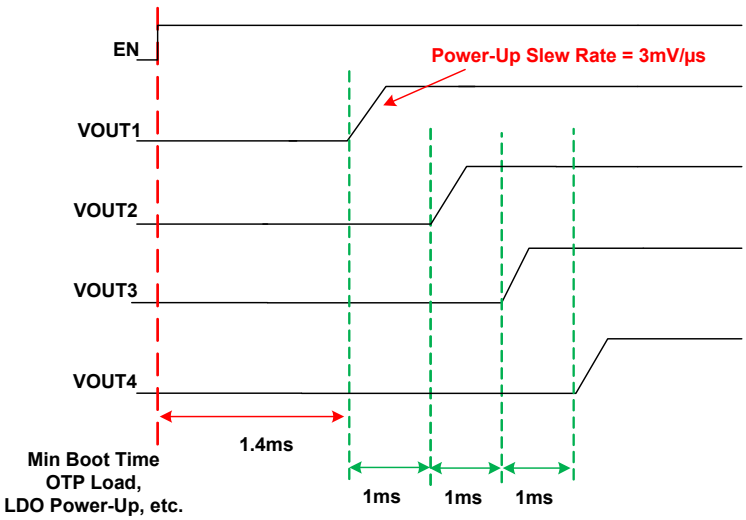


Figure 33. Master Chip Enable Power-Up Example

The buck outputs can also be programmed to execute a controlled shutdown in two ways:

• Manual Buck power-down:
Program the internal IO_BUCKx_EN bit to “0” through I^2C/SPI or lower the Buck Enable pin (EN_A and EN_B when IO_PINMODE = 0x1). The manual method can be used to power down a specific buck (with a controlled slew rate) while keeping the rest of the chip alive.
Note: The programmable (0ms to 63ms) delay from BUCKx_SHUTDN_DLY[5:0] is **not** used for manual buck power-down.

• Auto Buck power-down from master chip enable pin:
When the master chip Enable pin (EN) is brought below the falling threshold of the comparator, the Bucks are ramped down at a controlled rate using preprogrammed delays. The bias circuits then power down, forcing the chip into shutdown. The slew rate of each buck during its power-down (down to ~250mV) is specified in BUCKx_RSPPDN[2:0].

Figure 34 provides an example of power-down configurability. The master chip enable pin (EN) transitions from logic 1 to 0. In the Figure 34 example, BUCK1_SHUTDN_DLY is set for 1ms, BUCK2_SHUTDN_DLY is set for 1ms, BUCK3_SHUTDN_DLY is set for 1ms, and BUCK4_SHUTDN_DLY is set for 1ms.

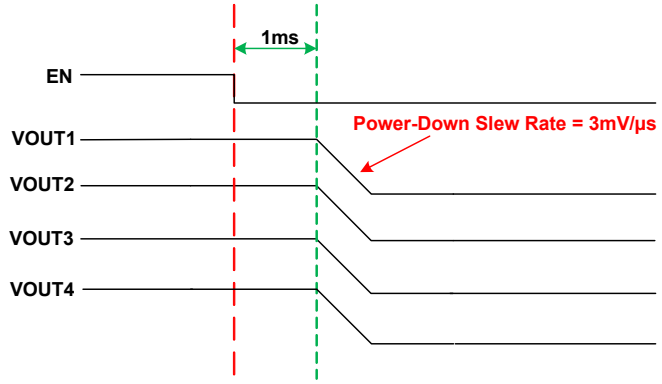


Figure 34. Auto Chip Power-Down Example

The actual slew rate that each buck ramps down to is specified by the register “BUCKx_RSPPDN”. The default slew rate for each buck discharging during power-down sequence is 3mV/µs. This slew rate is controlled until the output voltage is ~250mV. Below 250mV, there are two output voltage decay options:

Option 1: If the disable event for a buck output is the master chip enable pin (EN) falling below its logic high threshold, then when the output falls below 250mV, the output voltage decay is dictated by the system load passively discharging the buck output capacitance. PULL_DOWN_DISCHARGE bit per the BUCK2_CFG2 register is **not** used in this method.

Option 2: If the disable event for a buck output is the master chip enable pin (EN) remaining high and the enable register bit (IO_BUCKx_EN) transitioning form a logic 1 to a logic 0, then PULL_DOWN_DISCHARGE bit per the BUCK2_CFG2 register is used enabling an internal weak pull down.

Note: The weak pull-down can be disabled (using factory OTP).

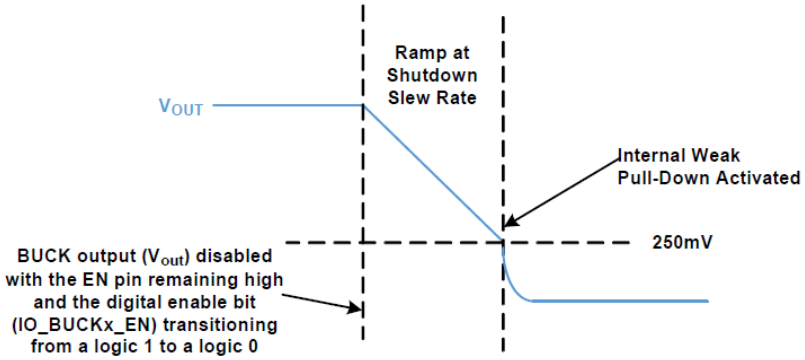


Figure 35. Buck Disable Waveform

6.3 Watchdog Time (WDOG_RST Pin)

The ISL91301A and ISL91301B implement a watchdog function that allows the output voltages to return to a safe OTP default when communication to the processor host is lost. This is determined by monitoring the state of the WDOG_RST pin. If the pin goes low for more than $t_{DEBOUNCE}$, the default voltages from OTP are restored.

All four bucks respond to the WDOG_RST pin. The polarity of the WDOG_RST pin is programmable to active low.

Table 15. WDOG_RST Function

Action	
At Boot Up	DVS registers are loaded with values stored in OTP
After Debounce Time	Restore selected output voltages to their original values stored in OTP (DVS0) and slew the buck outputs to that voltage

Total recovery time for the buck is the sum of the t_{SLEW} and $t_{DEBOUNCE}$. The WDOG_RST pin resets the ISL91301A and ISL91301B buck outputs to the target voltage set by DVS0, which resides in the BUCKx_DVS0CFG1 and BUCKx_DVS0CFG0 registers. t_{SLEW} is determined by the default output voltage divided by 3mV/µs, while $t_{DEBOUNCE}$ is set at 10ms.

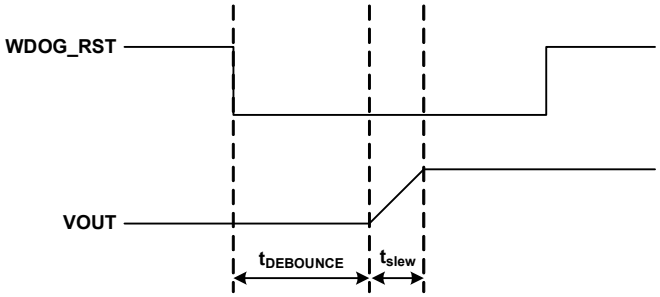


Figure 36. Watchdog Timer Example Case

6.4 Interrupt Pin

The ISL91301A and ISL91301B can alert the host when a warning or a fault has occurred through an IRQ interrupt request signal with configurable masking options that is connected to a configurable interrupt (INT) pin. The interrupt pin can be programmed to be active high, active low, an open drain, or a CMOS output.

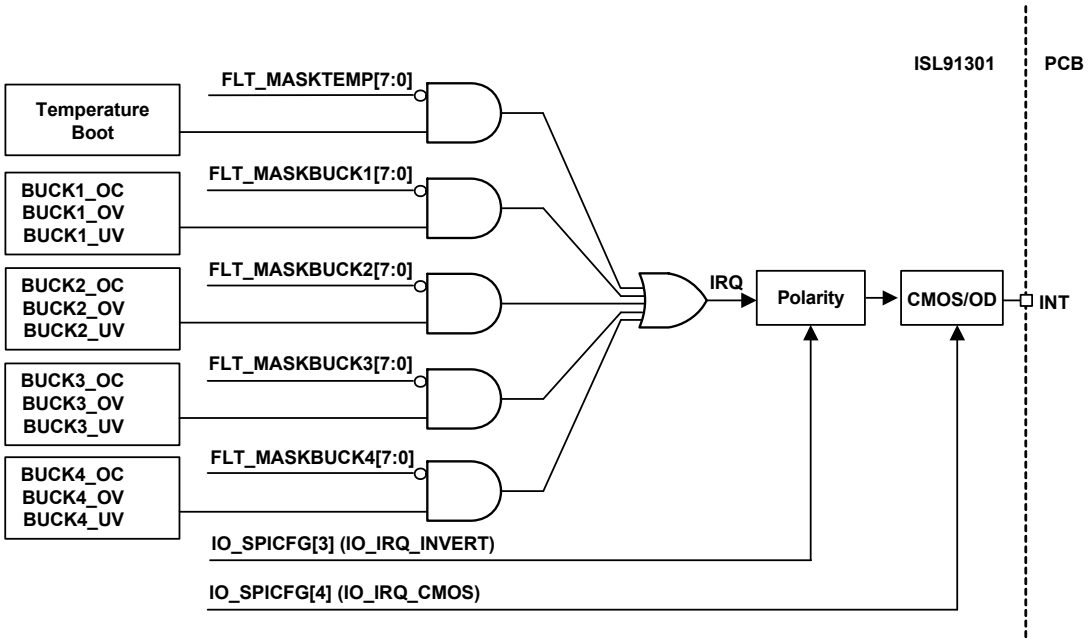


Figure 37. Interrupt Tree

7. Protection Features (FAULTS)

The ISL91301A and ISL91301B have Overcurrent (OC), Overvoltage (OV), Undervoltage (UV), and Over-Temperature (OT) protection features.

7.1 Over-Temperature (OT) Protection

The OT protection circuit continuously monitors the chip's die temperature and raises a fault when the temperature exceeds +150°C. By default, when the OT fault occurs, all the buck converters shut down and are re-enabled when the OT fault deasserts. Hysteresis enables the circuit to clear the fault once the temperature is below a predefined safe temperature. Hysteresis is hard coded as the difference between +95°C and +150°C.

7.2 Overcurrent (OC) Protection Mode

The OC protection block has a current comparator that compares the load current through the high-side power FET with the reference current level through a replica device. After R-C delay filtering and/or cycle detection filtering, the output of the OC protection block goes to the fault detection block, which makes the decision to disable the buck and latch the power-stage into high impedance mode. The digital core periodically re-enables the buck to detect if the fault has cleared.

7.3 Overvoltage (OV) and Undervoltage (UV) Protection

The ISL91301A and ISL91301B protect against output overvoltage and undervoltage fault conditions. The OV/UV protection circuitry has low power comparators configured with differential input and single-ended outputs capable of working over a large common-mode input range. This comparator monitors the output voltage in both DCM and CCM for faults. By default, when an OV event is triggered, the buck converter crowbars the output by turning on the low-side NMOS for a duration of 32µs to 64µs. After that, the buck shuts down and exits crowbar. The buck tries to start up and if the fault condition still exists, the buck reacts to OV again until the fault is removed. When a UV event is triggered, the buck converter shuts down and re-starts until the fault is cleared. The UV/OV threshold is a configurable window around the VOUT DAC target. The default setting is ±250mV.

8. Serial Communication Interface

The ISL91301A and ISL91301B have two serial interface protocols to read/write the registers.

- SPI
- I^2C

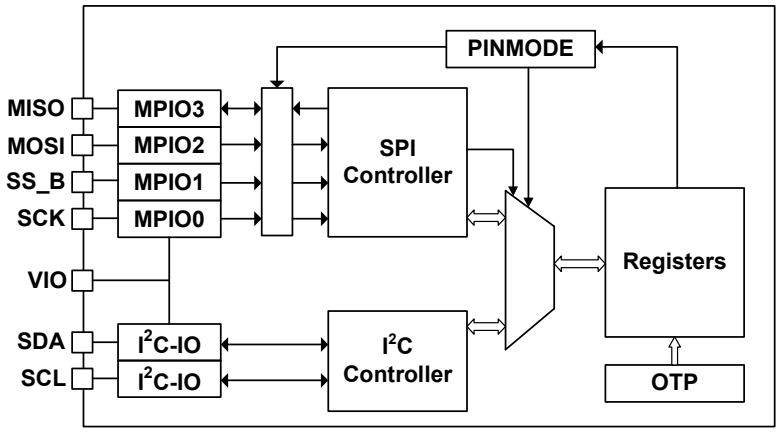


Figure 38. SPI/I^2C Interface

The arbitration of the register access bus, between SPI and I^2C, is determined by the register IO_PINMODE and the pad MPIO1 as shown in Table 16:

Table 16. SPI/I^2C Register Access

Register IO_PINMODE	Pad MPIO_1 (SPI_B)	Register Access
0	0	SPI (Read/Write Access (Note 10)
	1	I^2C (Note 11)

Notes:
10. When the device is configured for SPI access, I^2C should not be addressed with the device ID.
11. When the device is configured for I^2C access, in PINMODE 0, SPI_B line must be held high.

After switching from SPI to I^2C or vice versa, a minimum of 50ns wait time is required before starting a transaction.

8.1 SPI Interface

The SPI interface is a general specification 4-wire slave interface capable of operating at a clock speed of up to 26MHz. It is based on byte transfers.

8.1.1 SPI Data Protocol

Both Read and Write SPI transactions begin when SS_B goes low and end when SS_B goes high.

8.1.1.1 Write Operation

To write to the ISL91301A and ISL91301B, the master (controller) needs to drive SS_B low, then send the Control Byte followed by the register address, packet length (if IO_SPIMODE = 1), and Data bytes to be written. Finally, the master drives SS_B high to terminate the transaction as shown in Figure 39. The MSB of the Control byte is the R/W bit, which needs to be set to the 'write' operation (see "IO_SPIRWPOL"). Bit 6, AI indicates whether the operation is a single byte write or a multibyte write. Bits 1 and 0 of the Control byte indicate the page number of the register location to be written (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address needs to be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the master needs to send the data bytes. When all eight bits of data are received, they get written to the specified register address and the ISL91301A and ISL91301B increment the register address. In a single byte transaction, (AI = 0 or Packet length = 1), the ISL91301A and ISL91301B go into the wait state and wait for SS_B to go high. In a multibyte transaction with IO_SPIMODE = 1, the ISL91301A and ISL91301B write the subsequently received data bytes to sequentially incrementing addresses until the number of bytes, as specified by 'packet length', are received, then go into the wait state and wait for SS_B to go high. For multibyte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91301A and ISL91301B keep writing the subsequently received data bytes to sequentially incrementing addresses until SS_B goes high. If SS_B goes high in the middle of a transaction, the transaction is terminated. All the data bytes are written if all eight bits are received.

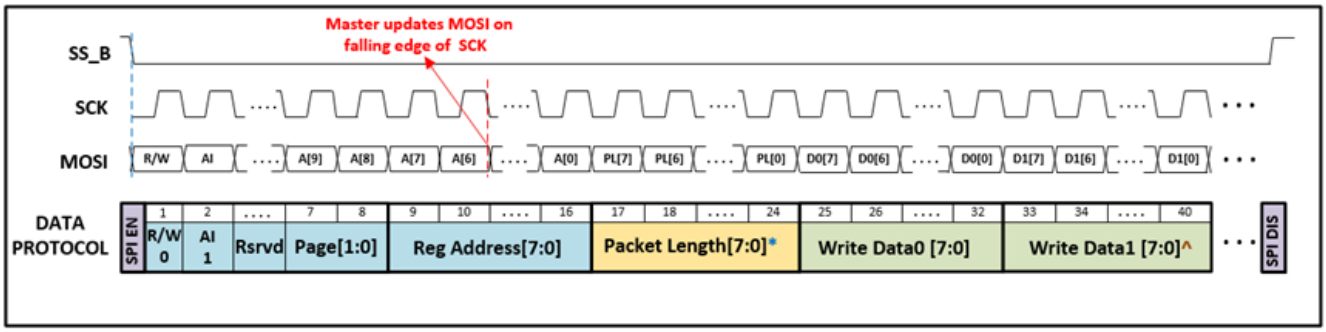


Figure 39. SPI Write Transaction With IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

8.1.1.2 Read Operation

To read from the ISL91301A and ISL91301B, the master (controller) needs to drive SS_B low then send the Control Byte followed by the register address and packet length (if IO_SPIMODE = 1). The ISL91301A and ISL91301B then send the data bytes from the requested registers. Finally, the master drives SS_B high to terminate the transaction as shown in Figure 40. The MSB of the Control byte is the R/W bit, which needs to be set to the 'read' operation (see IO_SPIRWPOL). Bit 6, AI indicates whether the operation is a single byte read or a multibyte read. Bits 1 and 0 of the Control byte indicate the page number of the register location to be read (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address needs to be followed by an 8-bit packet length which indicates the number of bytes to be written. Following the packet length field, the ISL91301A and

ISL91301B send the data from the requested register. When all eight bits of data from the requested register address are sent, the ISL91301A and ISL91301B increment the register address. In a single byte transaction, (AI = 0 or Packet length = 1), the ISL91301A and ISL91301B go into the wait state and wait for SS_B to go high. In a multibyte transaction with IO_SPIMODE = 1, the ISL91301A and ISL91301B send the data bytes from sequentially incrementing addresses until the number of bytes as specified by 'packet length' are sent, then go into the wait state and wait for SS_B to go high. For multibyte transactions with IO_SPIMODE = 0 and AI = 1, the ISL91301A and ISL91301B keep sending data bytes from sequentially incrementing addresses until SS_B goes high.

Note: The MISO pin is pulled low while SS_B is high.

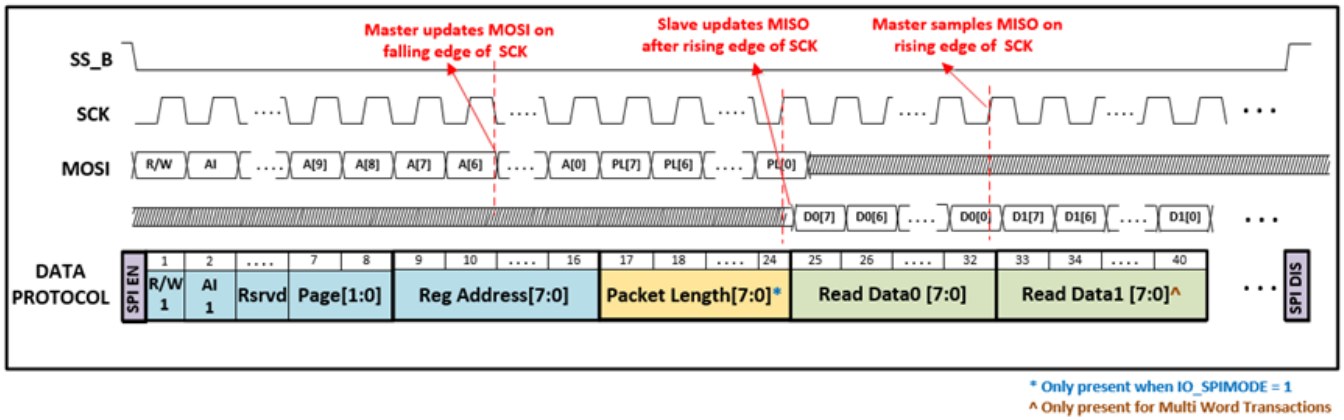


Figure 40. SPI Read Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

R/W	Read/Write Bit Indicating Read or Write Operation
AI	Auto Increment. 1 indicates multibyte transfer, 0 indicates single byte transfer
Page	2-bit page address of the register to be written/read
Address	8-bit register address of the register to be written/read
Packet Length	8-bit packet length indicating number of data bytes to be transferred. Overrides AI when IO_SPIMODE = 1
Read Data	Data in the register at Address [7:0] + n
Write Data	Data to be written to the register at Address [7:0] + n

8.1.2 SPI Configuration

The following register bits configure the SPI operation:

- **IO_SPICPOL:** SPI clock polarity, ISL91301A and ISL91301B are configured as active high, IO_SPICPOL = 0
- **IO_SPICPHA:** SPI clock phase, ISL91301A and ISL91301B sample data on rising edge of SPI clock, IO_SPICPHA = 0

The four possible clocking modes are shown in Figure 41.

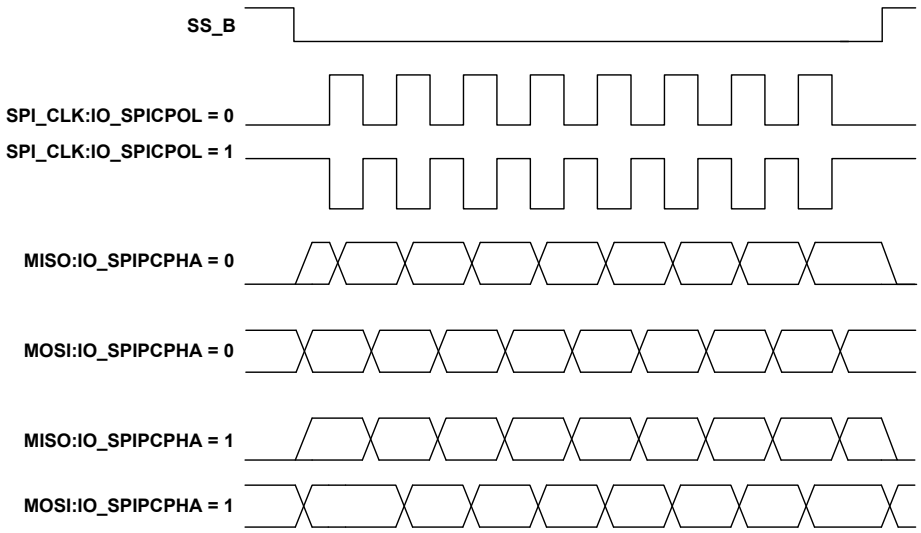


Figure 41. Four Possible Clocking Modes

- **IO_SPIRWPOL**: R/W bit polarity, ISL91301A and ISL91301B SPI_RWPOL is set to 0, 1: Read, 0: Write.

SPI_RWPOL	R/W	OPERATION
0	0	Write
0	1	Read

- **IO_SPIMODE**: Packet length enable. The ISL91301A and ISL91301B use packet length mode by default, meaning the third data byte from the master is the packet length and indicates the total number of data words to be sent/received in a burst transaction.

8.1.3 SPI Timing

Figure 42 shows SPI timing for IO_SPICPOL = 0; IO_SPICPHA = 0. The timing values in Table 17 are true for other values of IO_SPICPOL and IO_SPICHPA as well.

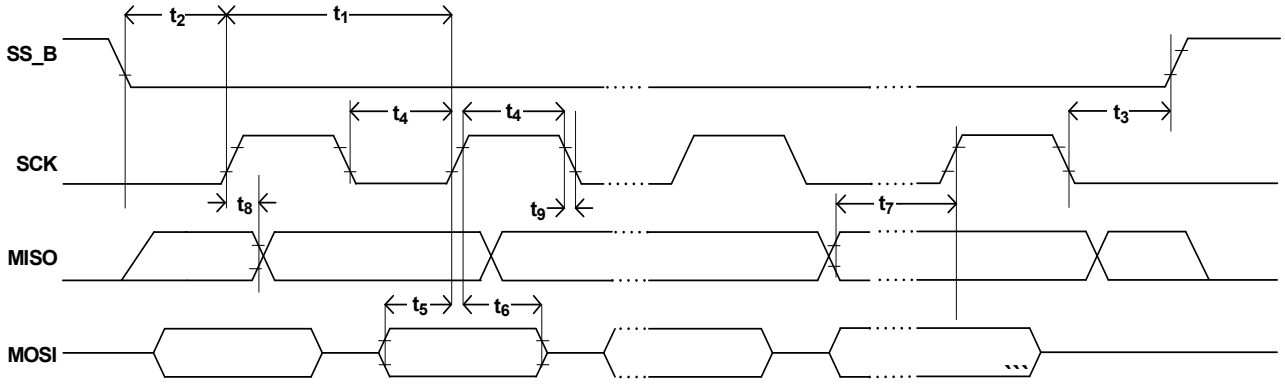


Figure 42. SPI Timing for IO_SPICPHA = 0, IO_SPICPOL = 0

Table 17. Timing Values

Parameter	Symbol	Min	Max	Units
Clock Period	t_1	38.4		ns
Enable Lead Time	t_2	12		ns
Enable Lag Time	t_3	12		ns
Clock High or Low Time	t_4	15		ns
Data Setup Time (Input)	t_5	12		ns
Data Hold Time (Input)	t_6	10		ns
Time MISO is Stable before the Next Rising Edge of CLK	t_7	5		ns
Data Held after Clock Edge (Output)	t_8	5		ns
Load Capacitance	CL		10	pF

8.2 I²C Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of a serial clock control (SCL/I2C_CLK) and serial data signal (SDA/I2C_SDA). The ISL91301A and ISL91301B host a slave I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the ISL91301A and ISL91301B and is supplied by the controller, whereas SDA is bidirectional. The ISL91301A and ISL91301B have an open-drain output to transmit data on SDA. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The ISL91301A and ISL91301B use a 7-bit hardware address scheme. The default address is set to 0x1F by a onetime programmable fuse.

8.2.1 I²C Bus Operation

The chip supports 7-bit addressing. The ISL91301A and ISL91301B I²C device address is reconfigurable through the OTP. All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 47).

All I²C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. The ISL91301A and ISL91301B continuously monitor the SDA and SCL lines for the START condition and do not respond to any command until this condition is met. All I²C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH.

An ACK (Acknowledge) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge reception of the eight bits of data (Figure 47). The ISL91301A and ISL91301B respond with an ACK after recognizing a START condition followed by a valid Identification (I²C Address) Byte. The ISL91301A and ISL91301B also respond with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

8.2.1.1 Write Operation

A Write operation requires a START condition, followed by an ISL91301A and ISL91301B I²C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. After each byte, the ISL91301A and ISL91301B respond with an ACK. After every data byte, the ISL91301A and ISL91301B auto increment the register address so subsequent data bytes get written to sequentially incremental register locations. A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

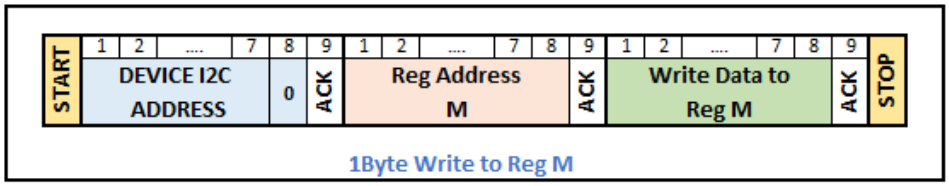


Figure 43. 1-Byte Write to Register M

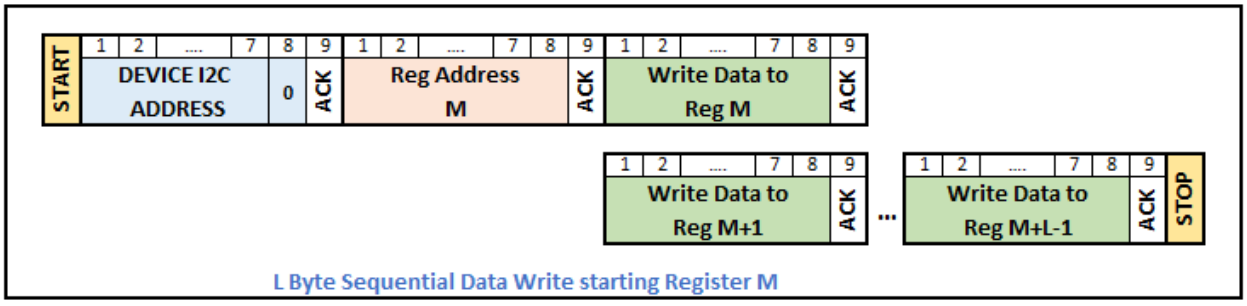


Figure 44. L-Byte Sequential Data Write Starting Register M

8.2.1.2 Read Operation

A Read operation consists of a three-byte “dummy write” instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation, issuing the following sequence: a START condition, followed by an ISL91301A and ISL91301B I^2C Address byte with the R/W bit set to “0”, a Register Address Byte, a second START, and a second ISL91301A and ISL91301B I^2C Address byte with the R/W bit set to “1”. After each of the three bytes, the ISL91301A and ISL91301B respond with an ACK. The ISL91301A and ISL91301B then transmit Data Bytes. The master terminates the Read operation from the ISL91301A and ISL91301B by issuing a STOP condition following the last bit of the last data byte. After every data byte, the ISL91301A and ISL91301B auto increment the register address so subsequent data bytes are sent from sequentially incremental register locations.

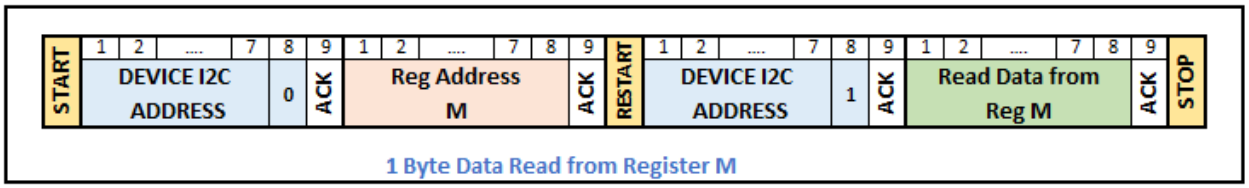


Figure 45. 1-Byte Data Read From Register M

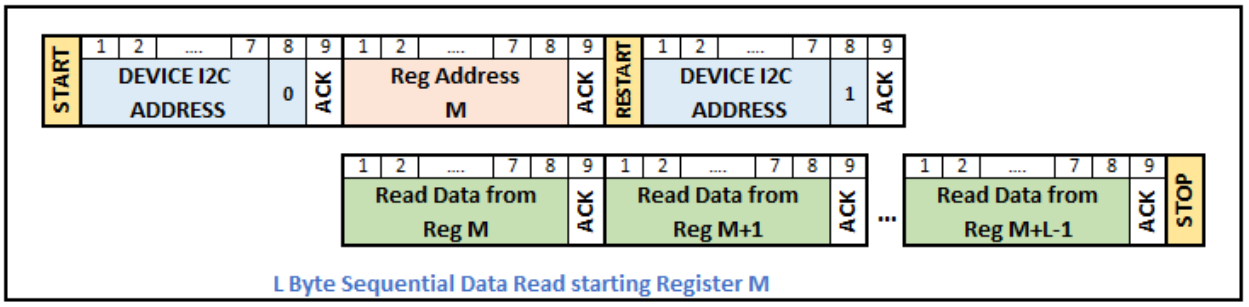


Figure 46. L-Byte Sequential Data Read Starting Register M

8.2.2 I²C Timing

The timing specifications of the I²C I/O from the I²C specification are shown in Figure 47 and Table 18. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in Standard, Fast, Fast+, and High Speed modes.

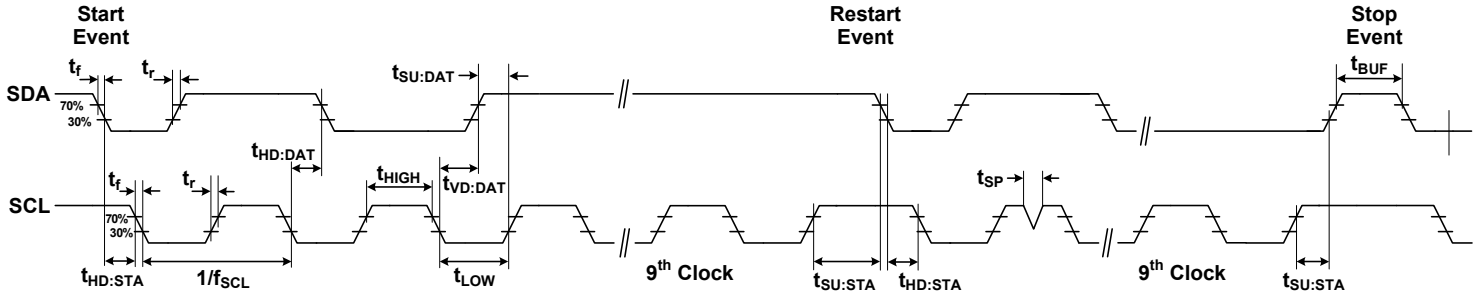


Figure 47. I²C Timing

Table 18. I²C Timing Specifications

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition (The first clock pulse is generated after this period)	$t_{HD;STA}$	4000		600		260		160		ns
LOW Period of the SCL Clock	t_{LOW}	4700		1300		500		160		ns
HIGH Period of the SCL Clock	t_{HIGH}	4000		600		260		60		ns
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	4700		600		260		160		ns
Data Hold Time	$t_{HD;DAT}$	15		15		15		15	70	ns
Data Set-Up Time	$t_{SU;DAT}$	250		100		50		10		ns
Rise Time of SCL	t_{rCL}		1000		300		120		40	ns
Fall Time of SCL	t_{fCL}		300		300		120		40	ns
Rise Time of SDA	t_{rDA}		1000		300		120		80	ns
Fall Time of SDA	t_{fDA}		300		300		120		80	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	4000		600		260		160		ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700		1300		500				ns

Table 18. I^2C Timing Specifications (Continued)

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Capacitive Load for each Bus Line	C_b		400		400		400		100	pF
Output Fall Time from VIHmin to VILmax	t_{of}		250[5]	20 × (V_{DD} /5.5V)[6]	250[5]	20 × (V_{DD}/5.5V)[6]	120[7]	10 (Note 13)	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}			0	50	0	50	0	10	ns

Notes:

12. Only valid for V_{DD} < 4V.
13. Only valid for V_{DD} < 1.9V.
14. V_{DD} is the pull-up source to the I^2C lines (GPIO0, GPIO1).

9. Board Layout Recommendations

The ISL91301A and ISL91301B are 4-channel PMICs consisting of high frequency switching regulators with dual and single phase capability. Proper PCB layout is a very important design practice to ensure satisfactory performance. The power loop is composed of the output inductor L, the output capacitor C_{OUT}, the SW pin, and the PGND pin. It is important to make the power loop as small as possible. The connecting traces among the components should be direct, short, and wide. The same practice should be applied to connections at the PVIN. Place the input capacitor as close as possible to PVIN and PGND pins of the corresponding power stage.

The switching node of the converter, the SW pin, and the traces connected to this node are very noisy, so keep the remote sense lines and other noise sensitive traces away from these traces. Keep the trace connecting between the SW pin and the inductor short and wide, use multiple copper planes in parallel with sufficient vias in between to maximize thermal performance and efficiency. Renesas recommends descending only one layer for the phase traces to reduce the effective path to the inductor. Also, ensure the length and width of each inductor trace and number of vias used match resistances to help ensure proper current matching when using the dual phase configuration on the ISL91301A.

The ground of the input and output capacitors should be connected as close as possible. Use as much ground plane as possible underneath the ISL91301A and ISL91301B to support high current flow and to create a low impedance path for return current between the ISL91301A and ISL91301B and the load. Use a solid ground plane as much as possible, because it helps isolate SW node traces and high-speed clock signals from interfering with remote sense lines in adjacent layers, and is helpful for good EMI performance.

Place an AVIN filter capacitor as close as possible to the ISL91301A and ISL91301B but away from noise sources, and always reference the GND pad of the decoupling capacitor to a quiet GND plane. The AVIN and GND pins of the ISL91301A and ISL91301B should reference to a copper plane.

Do not use plated through-holes when passing the WLCSP pins to lower layers. If microvias are required to pass down multiple layers, Renesas recommends staggering them.

VOUT and RTN lines sense the output voltage and should be routed directly to the load. Connecting the RTN line to ground away from the load causes a ground error in the output voltage load regulation due to parasitic ground resistance. Also, keep these traces away from switching nodes, which could be phase nodes or high-speed digital signals. The use of small low inductance (ESL) capacitors at the load improves noise immunity and transient response to the ISL91301A and ISL91301B.

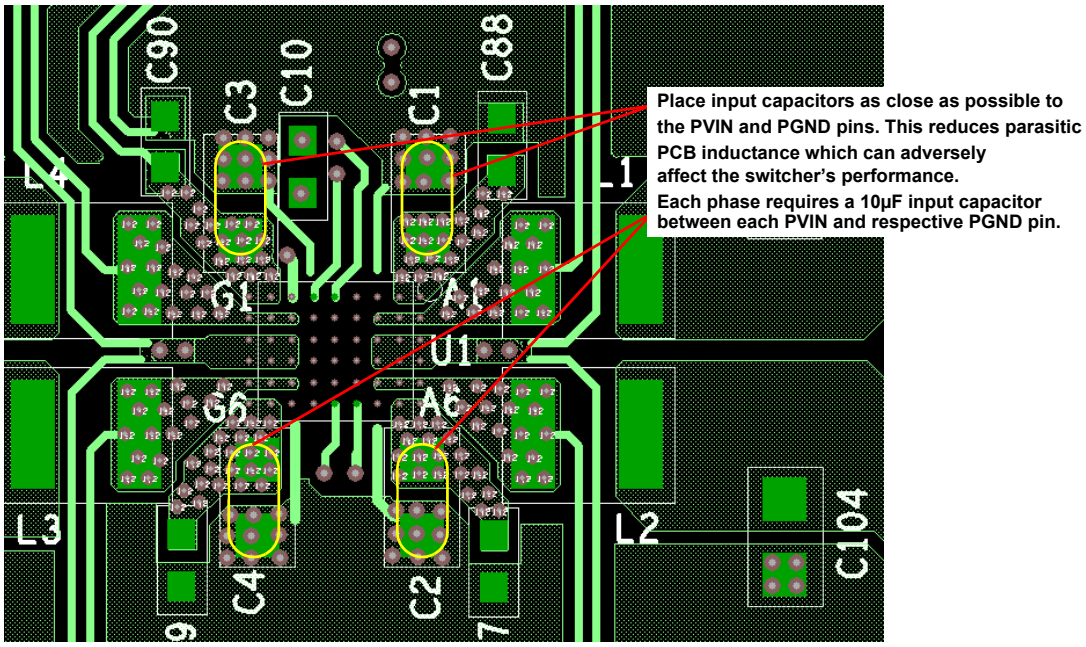
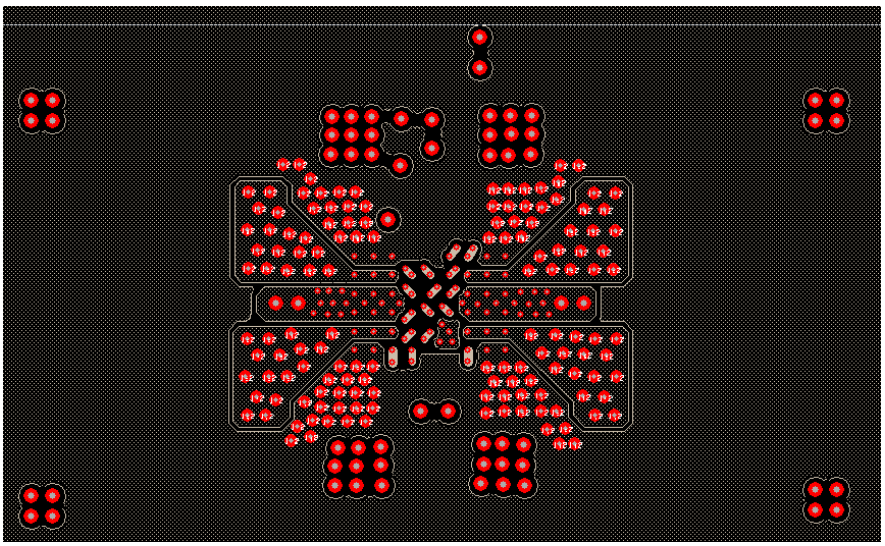


Figure 48. Recommended PCB Layout Top Layer



Provide a solid ground plane in the adjacent layer to provide a low impedance path to support high current flow. Copper planes need to be paralleled with the phase traces on the top layer to minimize resistance, and they must be surrounded by a GND plane to prevent noise coupling.

Figure 49. Recommended PCB Layout Second Layer

Feedback lines must be kept away from noise sources such as the switching node, inductor, and high-speed digital signals.
Run the traces to cut through the surrounding ground plane areas to minimize noise pick up. Add ground planes above and below the signals when applicable.

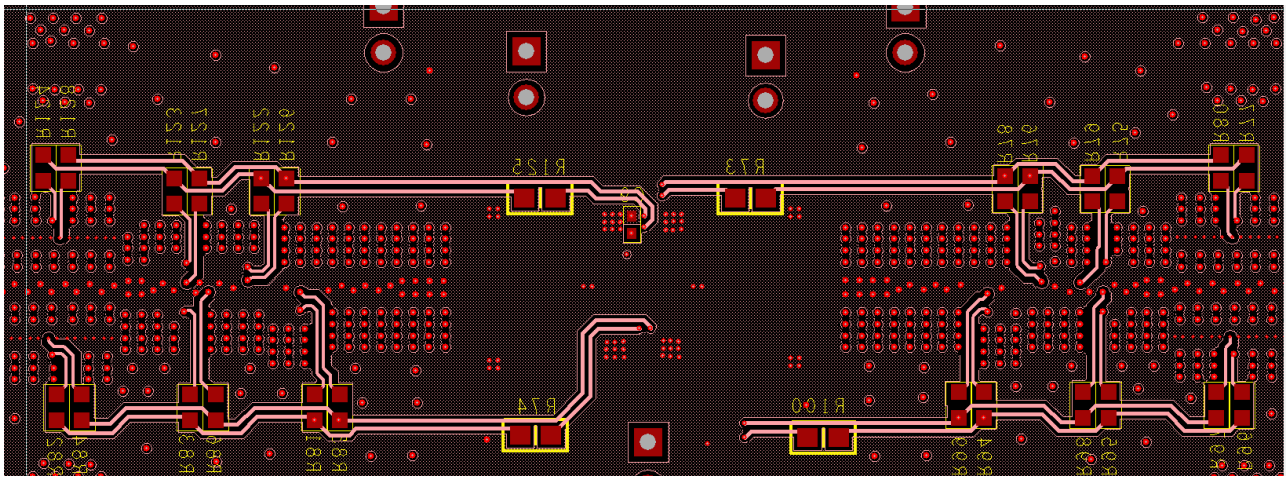


Figure 50. Recommended PCB Layout Bottom Layer

9.1 PCB Layout Summary

- Place input capacitors as close as possible to their respective PVIN and PGND pins
- Route phase nodes with short, wide traces, and avoid any sensitive nodes
- Route VOUT and RTN lines directly to the load using small, low inductance (ESL) capacitors at the load for bypassing
- Output capacitors should be close to the inductors and have low impedance path to the PGND pins
- Keep digital and phase nodes from intersecting AVIN_FILT, VOUT, and RTN lines
- Create a PGND plane on the 2nd layer of the PCB below the power components and bumps carrying high switching currents

9.2 PCB Design for WLCSP Recommendations

Table 19. PCB Design For WLCSP Recommendations

Design Feature	Design Specification
Cu Pad Diameter	0.4mm pitch: 0.215 ±0.012mm
Microvia Structure	All microvias should be copper filled.
Microvia Stacking	Avoid microvia stacking if possible. Use staggered vias instead. If microvia stacking is absolutely necessary for the layout, the maximum number of recommended via stacks is two.
Plated Through-Hole (PTH) Location	No PTH should be placed under the CSP bump pads. Microvias and trace routing should be used to fan the PTH away from the CSP bump array.

10. Register Address Map

Address	Register
0x01	IO_CHIPNAME
0x13	FLT_RECORDTEMP
0x14	FLT_RECORDBUCK1
0x15	FLT_RECORDBUCK2
0x16	FLT_RECORDBUCK3
0x17	FLT_RECORDBUCK4
0x23	IO_SPICFG
0x24	IO_MODECTRL
0x32	FLT_MASKTEMP
0x33	FLT_MASKBUCK1
0x34	FLT_MASKBUCK2
0x35	FLT_MASKBUCK3
0x36	FLT_MASKBUCK4
0x3B	BUCK1_EA2
0X3E	BUCK1_DCM
0x3F	BUCK1_CFG3
0x46	BUCK1_PHADD
0x48	BUCK1_DVS0CFG1
0x49	BUCK1_DVS0CFG0
0x4A	BUCK1_DVS1CFG1
0x4B	BUCK1_DVS1CFG0
0x4C	BUCK1_DVS2CFG1
0x4D	BUCK1_DVS2CFG0
0x4E	BUCK1_DVS3CFG1
0x4F	BUCK1_DVS3CFG0
0x53	BUCK1_DVSSEL
0x54	BUCK1_RSPCFG1

Address	Register
0x55	BUCK1_RSPCFG0
0x56	BUCK1_EN_DLY
0x57	BUCK1_SHTDN_DLY
0x58	BUCK2_EA2
0x5B	BUCK2_DCM
0x5C	BUCK2_CFG3
0x5D	BUCK2_CFG2
0x62	BUCK2_DVS0CFG1
0x63	BUCK2_DVS0CFG0
0x64	BUCK2_DVS1CFG1
0x65	BUCK2_DVS1CFG0
0x66	BUCK2_DVS2CFG1
0x67	BUCK2_DVS2CFG0
0x68	BUCK2_DVS3CFG1
0x69	BUCK2_DVS3CFG0
0x6D	BUCK2_DVSSEL
0x6E	BUCK2_RSPCFG1
0x6F	BUCK2_RSPCFG0
0x70	BUCK2_EN_DLY
0x71	BUCK2_SHTDN_DLY
0x72	BUCK3_EA2
0x75	BUCK3_DCM
0x76	BUCK3_CFG3
0x7C	BUCK3_DVS0CFG1
0x7D	BUCK3_DVS0CFG0
0x7E	BUCK3_DVS1CFG1
0x7F	BUCK3_DVS1CFG0

Address	Register
0x80	BUCK3_DVS2CFG1
0x81	BUCK3_DVS2CFG0
0x82	BUCK3_DVS3CFG1
0x83	BUCK3_DVS3CFG0
0x87	BUCK3_DVSSEL
0x88	BUCK3_RSPCFG1
0x89	BUCK3_RSPCFG0
0x8A	BUCK3_EN_DLY
0x8B	BUCK3_SHTDN_DLY
0x8C	BUCK4_EA2
0x8F	BUCK4_DCM
0x90	BUCK4_CFG3
0x96	BUCK4_DVS0CFG1
0x97	BUCK4_DVS0CFG0
0x98	BUCK4_DVS1CFG1
0x99	BUCK4_DVS1CFG0
0x9A	BUCK4_DVS2CFG1
0x9B	BUCK4_DVS2CFG0
0x9C	BUCK4_DVS3CFG1
0x9D	BUCK4_DVS3CFG0
0xA1	BUCK4_DVSSEL
0xA2	BUCK4_RSPCFG0
0xA3	BUCK4_RSPCFG1
0xA4	BUCK4_EN_DLY
0xA5	BUCK4_SHTDN_DLY

IMPORTANT: The registers not listed in the register map and the RESERVED bits are reserved for factory use only. Changing these registers/bits can result in unexpected operation.

11. Register Description by Address

Address	Bit	Name	R/W	Default	Description
IO_CHIPNAME					
0x01	7:0	IO_CHIPNAME	R	0x04	Chip Name 0x04: ISL91301A and ISL91301B
FLT_RECORDTEMP					
0x13	7	FLT_BOOT	R	0x0	BOOT Occurred Read only, cleared when read 0x0: No boot process has occurred. 0x1: Boot process has occurred, OTP read is finished.
	6:2	RSVD	R	0x0	Reserved
	1	FLT_TEMPSDR	R	0x0	Over-Temperature (OT) Shutdown (Rising Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	0	FLT_TEMPSDF	R	0x0	Over-Temperature (OT) Shutdown (Falling Threshold) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
FLT_RECORDBUCK1					
0x14	7	RSVD	R	0x0	Reserved
	6	FLT_BUCK1_OC	R	0x0	Overcurrent (OC) for BUCK1 Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	5	FLT_BUCK1_OV	R	0x0	Overvoltage (OV) Read only, cleared when read 0x0: No fault, less than threshold. 0x1: Fault, greater than threshold.
	4	FLT_BUCK1_UV	R	0x0	Undervoltage (UV) Read only, cleared when read 0x0: No fault, less then threshold. 0x1: Fault, greater than threshold.
	3:0	RSVD	R	0x0	Reserved

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">FLT_RECORDBUCK2</td></tr>
<tr><td rowspan="6">0x15</td><td>7</td><td>RSVD</td><td>R</td><td>0x0</td><td>See “FLT_RECORDBUCK1”</td></tr>
<tr><td>6</td><td>FLT_BUCK2_OC</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>5</td><td>FLT_BUCK2_OV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>4</td><td>FLT_BUCK2_UV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>3:0</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td colspan="6">FLT_RECORDBUCK3</td></tr>
<tr><td rowspan="6">0x16</td><td>7</td><td>RSVD</td><td>R</td><td>0x0</td><td>See “FLT_RECORDBUCK1”</td></tr>
<tr><td>6</td><td>FLT_BUCK3_OC</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>5</td><td>FLT_BUCK3_OV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>4</td><td>FLT_BUCK3_UV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>3:0</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td colspan="6">FLT_RECORDBUCK4</td></tr>
<tr><td rowspan="6">0x17</td><td>7</td><td>RSVD</td><td>R</td><td>0x0</td><td>See “FLT_RECORDBUCK1”</td></tr>
<tr><td>6</td><td>FLT_BUCK4_OC</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>5</td><td>FLT_BUCK4_OV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>4</td><td>FLT_BUCK4_UV</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>3:0</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td colspan="6">IO_SPICFG</td></tr>
<tr><td rowspan="5">0x23</td><td>7:5</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>4</td><td>IO_IRQ_CMOS</td><td>R/W</td><td>0x0</td><td>IRQ Type
0x0 OD Output
0x1 CMOS Output</td></tr>
<tr><td>3</td><td>IO_IRQ_INVERT</td><td>R/W</td><td>0x1</td><td>IRQ Polarity
0x0 Active High
0x1 Active Low</td></tr>
<tr><td>2:1</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>0</td><td>RSVD</td><td>R</td><td>0x1</td><td>Reserved</td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
IO_MODECTRL					
0x24	7	IO_BUCK1_EN	R/W	0x1	Enable for BUCK1 0x0 Buck1 disabled. 0x1 Buck1 enabled.
	6	IO_BUCK2_EN	R/W	0x1	Enable for BUCK2 0x0 Buck2 disabled. 0x1 Buck2 enabled.
	5	IO_BUCK3_EN	R/W	0x1	Enable for BUCK3 0x0 Buck3 disabled. 0x1 Buck3 enabled.
	4	IO_BUCK4_EN	R/W	0x1	Enable for BUCK4 0x0 Buck4 disabled. 0x1 Buck4 enabled.
	3	RSVD	R	0x0	Reserved
	2	IO_ENVPPPULLDOWN	R/W	0x01	Enable for weak Pull-down on EN/VPP Pin 0x0 Weak pull-down disabled. 0x1 Weak pull-down enabled.
	1	RSVD	R	0x0	Reserved
	0	RSVD	R	0x1	Reserved
FLT_MASKTEMP					
0x32	7	FLT_MASKBOOT	R/W	0x0	Mask IRQ for FLT_BOOT 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	6:2	RSVD	R	0x0	Reserved
	1	FLT_MASKEMPSDR	R/W	0x0	Mask IRQ for FLT_TEMPSDR 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	0	FLT_MASKTEMPSDF	R/W	0x0	Mask IRQ for FLT_TEMPSDF 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.

Address	Bit	Name	R/W	Default	Description
FLT_MASKBUCK1					
0x33	7	RSVD	R	0x0	Reserved
	6	FLT_BUCK1_MASKOC	R/W	0x0	Mask IRQ for FLT_BUCK1_OC 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	5	FLT_BUCK1_MASKOV	R/W	0x0	Mask IRQ for FLT_BUCK1_OV 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	4	FLT_BUCK1_MASKUV	R/W	0x0	Mask IRQ for FLT_BUCK1_UV 0x0 IRQ passed to output pin. 0x1 IRQ masked from output pin.
	3:0	RSVD	R	0x0	Reserved
FLT_MASKBUCK2					
0x34	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK2_MASKOC	R/W	0x0	
	5	FLT_BUCK2_MASKOV	R/W	0x0	
	4	FLT_BUCK2_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	
FLT_MASKBUCK3					
0x35	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK3_MASKOC	R/W	0x0	
	5	FLT_BUCK3_MASKOV	R/W	0x0	
	4	FLT_BUCK3_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	
FLT_MASKBUCK4					
0x36	7	RSVD	R	0x0	See "FLT_MASKBUCK1"
	6	FLT_BUCK4_MASKOC	R/W	0x0	
	5	FLT_BUCK4_MASKOV	R/W	0x0	
	4	FLT_BUCK4_MASKUV	R/W	0x0	
	3:0	RSVD	R	0x0	

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_EA2</td></tr>
<tr><td rowspan="2">0x3B</td><td>7:6</td><td>BUCK1_VOUTFBDIV</td><td>R/W</td><td>0x0</td><td>V_{OUT} feedback divider ratio for the control loop. Should only be changed when the Buck is Disabled (BUCK1_EN = 0).
<table><tr><th></th><th>Feedback Divider (FBDIV) (%)</th><th>V_{OUT} Max (V)</th></tr><tr><td>0x0</td><td>100</td><td>1.2</td></tr><tr><td>0x1</td><td>80</td><td>1.5</td></tr><tr><td>0x2</td><td>60</td><td>2.0</td></tr><tr><td>0x3</td><td>Reserved</td><td>Reserved</td></tr></table></td></tr>
<tr><td>5:0</td><td>RSVD</td><td>R/W</td><td>N/A</td><td>Reserved. Not Available.</td></tr>
<tr><td colspan="6">BUCK1_DCM</td></tr>
<tr><td rowspan="3">0x3E</td><td>7:3</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>2</td><td>BUCK1_FCCM</td><td>R/W</td><td>0x0</td><td><table><tr><td colspan="2">Forced Continuous Conduction Mode</td></tr><tr><td>0x0</td><td>DCM allowed during light load conditions</td></tr><tr><td>0x1</td><td>Always operate in CCM (Continuous Conduction Mode)</td></tr></table></td></tr>
<tr><td>1:0</td><td>Reserved</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_CFG3</td></tr>
<tr><td rowspan="3">0x3F</td><td>7:6</td><td>BUCK1_FSEL</td><td>ORW</td><td>0x2</td><td>Buck’s steady-state switching frequency.
<table><tr><td>0x0</td><td>2MHz</td></tr><tr><td>0x1</td><td>3MHz</td></tr><tr><td>0x2</td><td>4MHz</td></tr><tr><td>0x3</td><td>Reserved</td></tr></table></td></tr>
<tr><td>5:1</td><td>RSVD</td><td>N/A</td><td>N/A</td><td>Reserved</td></tr>
<tr><td>0</td><td>RSVD</td><td>N/A</td><td>N/A</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_PHADD</td></tr>
<tr><td rowspan="2">0x46</td><td>7:3</td><td>RSVD</td><td>N/A</td><td>0x0</td><td>Reserved. Not Available</td></tr>
<tr><td>2</td><td>BUCK1_MANUALMODE</td><td>ORW</td><td>0x0</td><td><table><tr><td colspan="2">Automatic Phase Add/Drop Control</td></tr><tr><td>0x0</td><td>Automatic Phase Add/Drop</td></tr><tr><td>0x1</td><td>Manual Phase Add/Drop</td></tr></table>Note: This functionality is only available in ISL91301A.</td></tr>
<tr><td>1:0</td><td>BUCK1_MANUALPH</td><td>ORW</td><td>0x2</td><td><table><tr><td colspan="2">Sets the number of active phases when using Manual Phase Add/Drop Mode</td></tr><tr><td>0x1</td><td>1-phase mode</td></tr><tr><td>0x0, 0x2, 0x3</td><td>2-phase mode</td></tr></table>Note: In Manual Phase Add/Drop mode (BUCK1_MANUALMODE = 0x1) and 2-phase mode (BUCK1_MANUALPH = 0x0 or 0x2 or 0x3), the part operates in Forced CCM 2-phase configuration.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_DVS0CFG1</td></tr>
<tr><td>0x48</td><td>7:0</td><td>BUCK1_DVS0VOUT92</td><td>R/W</td><td>TRIM for 0.9V</td><td>Upper eight bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS Configuration 0.
Note: V_{OUT} must be programmed above 0.3V.
FBDIV is set by factory OTP to 1x, 0.8x, 0.6x.
<table>
<tr><td>FBDIV</td><td>1.0</td><td>0.8</td><td>0.6</td></tr>
<tr><td>DAC</td><td>V_{OUT} (V)</td><td>V_{OUT} (V)</td><td>V_{OUT} (V)</td></tr>
<tr><td>0x000</td><td>0.0000</td><td>0.0000</td><td>0.0000</td></tr>
<tr><td>0x001</td><td>0.0012</td><td>0.0015</td><td>0.0020</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x200</td><td>0.6173</td><td>0.7716</td><td>1.0288</td></tr>
<tr><td>0x201</td><td>0.6185</td><td>0.7731</td><td>1.0308</td></tr>
<tr><td>…</td><td></td><td></td><td></td></tr>
<tr><td>0x3E5</td><td>1.199</td><td>1.4988</td><td>1.9983</td></tr>
</table></td></tr>
<tr><td colspan="6">BUCK1_DVS0CFG0</td></tr>
<tr><td rowspan="4">0x49</td><td>7:6</td><td>BUCK1_DVS0VOUT10</td><td>R/W</td><td>TRIM for 0.9V</td><td>Lower two bits of a 10-bit DAC[9:0] value to generate V_{OUT} for DVS configuration.
Note: When DVS Configuration 0 is selected (using pins or registers) any write to BUCK1_DVS0CFG0 causes a DVS ramping to occur.
For details, see “Dynamic Voltage Scaling (DVS)” on page 22.</td></tr>
<tr><td>5</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>4:1</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>0</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK1_DVS1CFG1</td></tr>
<tr><td>0x4A</td><td>7:0</td><td>BUCK1_DVS1VOUT92</td><td>R/W</td><td>0xBF</td><td>See “BUCK1_DVS0CFG1”</td></tr>
<tr><td colspan="6">BUCK1_DVS1CFG0</td></tr>
<tr><td rowspan="4">0x4B</td><td>7:6</td><td>BUCK1_DVS1VOUT10</td><td>R/W</td><td>0x3</td><td>See “BUCK1_DVS0CFG0”</td></tr>
<tr><td>5</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td>4:1</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td>0</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td colspan="6">BUCK1_DVS2CFG1</td></tr>
<tr><td>0x4C</td><td>7:0</td><td>BUCK1_DVS2VOUT92</td><td>R/W</td><td>0x58</td><td>See “BUCK1_DVS0CFG1”</td></tr>
<tr><td colspan="6">BUCK1_DVS2CFG0</td></tr>
<tr><td rowspan="4">0x4D</td><td>7:6</td><td>BUCK1_DVS2VOUT10</td><td>R/W</td><td>0x0</td><td>See “BUCK1_DVS0CFG0”</td></tr>
<tr><td>5</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td>4:1</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td>0</td><td>RSVD</td><td>R</td><td>0x0</td></tr>
<tr><td colspan="6">BUCK1_DVS3CFG1</td></tr>
<tr><td>0x4E</td><td>7:0</td><td>BUCK1_DVS3VOUT92</td><td>R/W</td><td>0x00</td><td>See “BUCK1_DVS0CFG1”</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_DVS3CFG0</td></tr>
<tr><td rowspan="4">0x4F</td><td>7:6</td><td>BUCK1_DVS3VOUT10</td><td>R/W</td><td>0x0</td><td>See “BUCK1_DVS0CFG0”</td></tr>
<tr><td>5</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>4:1</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td>0</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td colspan="6">BUCK1_DVSSEL</td></tr>
<tr><td rowspan="2">0x53</td><td>7:3</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td>2</td><td>BUCK1_DVSCTRL</td><td>R/W</td><td>0x0</td><td>BUCK1 DVS Control
0x0 Use BUCK1_DVSSELECT to select active DVS configuration.</td></tr>
<tr><td></td><td>1:0</td><td>BUCK1_DVSSELECT</td><td>R/W</td><td>0x0</td><td>BUCK1 DVS Selection
0x0 Use DVS Configuration 0 in BUCK1_DVS0CFG and BUCK1_DVS0VOUT.
0x1 Use DVS Configuration 1 in BUCK1_DVS1CFG and BUCK1_DVS1VOUT.
0x2 Use DVS Configuration 2 in BUCK1_DVS2CFG and BUCK1_DVS2VOUT.
0x3 Use DVS Configuration 3 in BUCK1_DVS3CFG and BUCK1_DVS3VOUT.
Note: When BUCK1_DVSCTRL = 0x0 any write to the register BUCK1_DVSSEL causes a DVS ramping event to occur.</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_RSPCFG1</td></tr>
<tr><td>0x54</td><td>7</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>6:4</td><td>BUCK1_RSPUP</td><td>R/W</td><td>0x0</td><td>
V_{OUT} Ramp Slew Rate
RSP = BUCK1_RSPUP[1:0], Ramp Speed
FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6)
Slow = BUCK1_RSPUP[2] = 0
Fast = BUCK1_RSPUP[2] = 1
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>1.0</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>1.0</td><td>24</td><td>6</td></tr>
<tr><td>0x2</td><td>1.0</td><td>58</td><td>14</td></tr>
<tr><td>0x3</td><td>1.0</td><td>115</td><td>29</td></tr>
<tr><td colspan="4"></td></tr>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.8</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.8</td><td>24</td><td>6</td></tr>
<tr><td colspan="4"></td></tr>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.6</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.6</td><td>24</td><td>6</td></tr>
</table>
</td></tr>
<tr><td></td><td>3</td><td>RSVD</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>2:0</td><td>BUCK1_RSPDN</td><td>R/W</td><td>0x0</td><td>See “BUCK1_RSPUP” for rate definition</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_RSPCFG0</td></tr>
<tr><td>0x55</td><td>7</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>6:4</td><td>BUCK1_RSPPUP</td><td>R/W</td><td>0x1</td><td>VOUT Ramp Slew Rate
RSP = BUCK1_RSPUP[1:0], Ramp Speed
FBDIV = BUCK1_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6)
Slow = BUCK1_RSPUP[2] = 0
Fast = BUCK1_RSPUP[2] = 1
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>1.0</td><td>6</td><td>1.2</td></tr>
<tr><td>0x1</td><td>1.0</td><td>12</td><td>3</td></tr>
<tr><td>0x2</td><td>1.0</td><td>29</td><td>7.2</td></tr>
<tr><td>0x3</td><td>1.0</td><td>58</td><td>15</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.8</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.8</td><td>24</td><td>6</td></tr>
</table>
<table>
<tr><th rowspan="2">RSP</th><th rowspan="2">FBDIV</th><th colspan="2">V_{OUT} Ramp Speed mV/µs</th></tr>
<tr><th>Fast</th><th>Slow</th></tr>
<tr><td>0x0</td><td>0.6</td><td>12</td><td>3</td></tr>
<tr><td>0x1</td><td>0.6</td><td>24</td><td>6</td></tr>
</table></td></tr>
<tr><td></td><td>3</td><td>BUCK</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>2:0</td><td>BUCK1_RSPPDN</td><td>R/W</td><td>0x1</td><td>See “BUCK1_RSPPUP” for rate definition</td></tr>
<tr><td colspan="6">BUCK1_EN_DLY</td></tr>
<tr><td>0x56</td><td>7:6</td><td>BUCK1_ENPIN_CFG</td><td>R/W</td><td>0x0</td><td>EN_X pin control is valid only in PINMODE 1.
BUCK EN Control = IO_BUCK1_EN and BUCK1_EN_PIN
If not in PINMODE 1, BUCK1_EN_PIN is default high, only IO_BUCK1_EN can toggle BUCK1 EN
<table>
<tr><th colspan="2">BUCK1_EN_PIN</th></tr>
<tr><td>0x0</td><td>EN_A</td></tr>
<tr><td>0x1</td><td>EN_B</td></tr>
<tr><td>0x2</td><td>RSVD</td></tr>
<tr><td>0x3</td><td>1</td></tr>
</table></td></tr>
<tr><td></td><td>5:0</td><td>BUCK1_EN_DLY</td><td>R/W</td><td>0x0</td><td>Delay time from BUCK_EN pin and IO_REGVAID go high to buck1_en control asserted.
Delay = (integer value of register) ms
[1ms/LSB]</td></tr>
</table>

<table>
<tr><th>Address</th><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td colspan="6">BUCK1_SHUTDN_DLY</td></tr>
<tr><td>0x57</td><td>7:6</td><td>BUCK1_DVSPIN_CFG</td><td>R/W</td><td>0x0</td><td>DVS_PIN_X pin control is valid only in PINMODE 3.
DVS_1 = 0
DVS_0 = BUCK1_DVS_PIN0 and BUCK1_DVS_CTRL
If not in PINMODE 3, DVS_PIN_x function is disabled
<table><tr><td colspan="2">BUCK1_DVS_PIN0</td></tr><tr><td>0x0</td><td>EN_A</td></tr><tr><td>0x1</td><td>EN_B</td></tr><tr><td>0x2</td><td>RSVD</td></tr><tr><td>0x3</td><td>1</td></tr></table></td></tr>
<tr><td></td><td>5:0</td><td>BUCK1_SHUTDN_DLY</td><td>R/W</td><td>0x0</td><td>Delay time from BUCK_EN pin or IO_REGVAID go low to buck1_en control de-asserted.
Delay = (integer value of register) ms [1ms/LSB]</td></tr>
<tr><td colspan="6">BUCK2_EA2</td></tr>
<tr><td>0x58</td><td>7:6</td><td>BUCK2_VOUTFBDIV</td><td>R/W</td><td>0x0</td><td>See “BUCK1_EA2”</td></tr>
<tr><td></td><td>5:0</td><td>RSVD</td><td>R/W</td><td>N/A</td><td></td></tr>
<tr><td colspan="6">BUCK2_DCM</td></tr>
<tr><td>0x5B</td><td>7:3</td><td>Reserved</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>2</td><td>BUCK2_FCCM</td><td>R/W</td><td>0x0</td><td>See “BUCK1_DCM”</td></tr>
<tr><td></td><td>1:0</td><td>Reserved</td><td>R/W</td><td>0x0</td><td>Reserved</td></tr>
<tr><td colspan="6">BUCK2_CFG3</td></tr>
<tr><td>0x5C</td><td>7:6</td><td>BUCK2_FSEL[1:0]</td><td>R/W</td><td>0x0</td><td>See “BUCK1_CFG3”</td></tr>
<tr><td></td><td>5:0</td><td>RSVD</td><td>R/W</td><td>N/A</td><td></td></tr>
<tr><td colspan="6">BUCK2_CFG2</td></tr>
<tr><td>0x5D</td><td>7:4</td><td>RSVD</td><td>R/W</td><td>0x8</td><td>Reserved</td></tr>
<tr><td></td><td>3</td><td>RSVD</td><td>R</td><td>TRIM</td><td>Reserved</td></tr>
<tr><td></td><td>2</td><td>RSVD</td><td>R</td><td>0x0</td><td>Reserved</td></tr>
<tr><td></td><td>1:0</td><td>PULL_DOWN_
DISCHARGE</td><td>R/W</td><td>0x0</td><td><table><tr><td colspan="2">VOUT pulldown when BUCK is shut off</td></tr><tr><td>0x0</td><td>Disable VOUT pulldown</td></tr><tr><td>0x1</td><td>Enable VOUT pulldown.</td></tr></table>Applies the weak pull-down feature for all the buck outputs.
1: Weak pull-down resistor is enabled when the buck output is turned off by software and master EN remains asserted.
0: Weak pull-down resistor is disabled when the buck output is turned off by software and master EN remains asserted.</td></tr>
<tr><td colspan="6">BUCK2_DVS0CFG1</td></tr>
<tr><td>0x62</td><td>7:0</td><td>BUCK2_DVS0VOUT92</td><td>R/W</td><td>0xBF</td><td>See “BUCK1_DVS0VOUT92”</td></tr>
<tr><td colspan="6">BUCK2_DVS0CFG0</td></tr>
<tr><td>0x63</td><td>7:6</td><td>BUCK2_DVS0VOUT10</td><td>R/W</td><td>0x3</td><td>See “BUCK1_DVS0CFG0”</td></tr>
<tr><td></td><td>5</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td></td><td>4:1</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
<tr><td></td><td>0</td><td>RSVD</td><td>R</td><td>0x0</td><td></td></tr>
</table>

Address	Bit	Name	R/W	Default	Description
BUCK2_DVS1CFG1					
0x64	7:0	BUCK2_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK2_DVS1CFG0					
0x65	7:6	BUCK2_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS2CFG1					
0x66	7:0	BUCK1_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK2_DVS2CFG0					
0x67	7:6	BUCK2_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVS3CFG1					
0x68	7:0	BUCK2_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK2_DVS3CFG0					
0x69	7:6	BUCK2_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK2_DVSSEL					
0x6D	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK1_DVSCTRL	R/W	0x0	
	1:0	BUCK1_DVSSELECT	R/W	0x0	
BUCK2_RSPCFG1					
0x6E	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK2_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPDN	R/W	0x3	
BUCK2_RSPCFG0					
0x6F	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK2_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK2_RSPPDN	R/W	0x3	
BUCK2_EN_DLY					
0x70	7:6	BUCK2_ENPIN_CFG	R/W	0x1	See "BUCK1_ENPIN_CFG"
	5:0	BUCK2_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK2_SHUTDN_DLY					
0x71	7:6	BUCK2_DVSPIN_CFG	R/W	0x1	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK2_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"

Address	Bit	Name	R/W	Default	Description
BUCK3_EA2					
0x72	7:6	BUCK3_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK3_DCM					
0x75	7:3	Reserved	R	0x0	Reserved
	2	BUCK3_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK3_CFG3					
0x76	7:6	BUCK3_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK3_DVS0CFG1					
0x7C	7:0	BUCK3_DVS0VOUT92	R/W	0xFF	See "BUCK1_DVS0VOUT92"
BUCK3_DVS0CFG0					
0x7D	7:6	BUCK3_DVS0VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS1CFG1					
0x7E	7:0	BUCK3_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK3_DVS1CFG0					
0x7F	7:6	BUCK3_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS2CFG1					
0x80	7:0	BUCK3_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"
BUCK3_DVS2CFG0					
0x81	7:6	BUCK3_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVS3CFG1					
0x82	7:0	BUCK3_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK3_DVS3CFG0					
0x83	7:6	BUCK3_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK3_DVSSEL					
0x87	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK3_DVSCTRL	R/W	0x0	
	1:0	BUCK3_DVSSELECT	R/W	0x0	

Address	Bit	Name	R/W	Default	Description
BUCK3_RSPCFG1					
0x88	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK3_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPDN	R/W	0x3	
BUCK3_RSPCFG0					
0x89	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK3_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK3_RSPPDN	R/W	0x3	
BUCK3_EN_DLY					
0x8A	7:6	BUCK3_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK3_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK3_SHUTDN_DLY					
0x8B	7:6	BUCK3_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK3_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"
BUCK4_EA2					
0x8C	7:6	BUCK4_VOUTFBDIV	R/W	0x0	See "BUCK1_EA2"
	5:0	RSVD	R/W	N/A	
BUCK4_DCM					
0x8F	7:3	Reserved	R	0x0	Reserved
	2	BUCK4_FCCM	R/W	0x0	See "BUCK1_DCM"
	1:0	Reserved	R/W	0x0	Reserved
BUCK4_CFG3					
0x90	7:6	BUCK4_FSEL[1:0]	R/W	0x0	See "BUCK1_CFG3"
	5:0	RSVD	R/W	N/A	
BUCK4_DVS0CFG1					
0x96	7:0	BUCK4_DVS0VOUT92	R/W	0xFF	See "BUCK1_DVS0VOUT92"
BUCK4_DVS0CFG0					
0x97	7:6	BUCK4_DVS0VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS1CFG1					
0x98	7:0	BUCK4_DVS1VOUT92	R/W	0xBF	See "BUCK1_DVS0CFG1"
BUCK4_DVS1CFG0					
0x99	7:6	BUCK4_DVS1VOUT10	R/W	0x3	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS2CFG1					
0x9A	7:0	BUCK4_DVS2VOUT92	R/W	0x58	See "BUCK1_DVS0CFG1"

Address	Bit	Name	R/W	Default	Description
BUCK4_DVS2CFG0					
0x9B	7:6	BUCK4_DVS2VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVS3CFG1					
0x9C	7:0	BUCK4_DVS3VOUT92	R/W	0x00	See "BUCK1_DVS0CFG1"
BUCK4_DVS3CFG0					
0x9D	7:6	BUCK4_DVS3VOUT10	R/W	0x0	See "BUCK1_DVS0CFG0"
	5	RSVD	R	0x0	
	4:1	RSVD	R	0x0	
	0	RSVD	R	0x0	
BUCK4_DVSSEL					
0xA1	7:3	RSVD	R	0x0	See "BUCK1_DVSSEL"
	2	BUCK4_DVSCTRL	R/W	0x0	
	1:0	BUCK4_DVSSELECT	R/W	0x0	
BUCK4_RSPCFG0					
0xA2	7	RSVD	R	0x0	See "BUCK1_RSPCFG0"
	6:4	BUCK4_RSPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPDN	R/W	0x3	
BUCK4_RSPCFG1					
0xA3	7	RSVD	R	0x0	See "BUCK1_RSPCFG1"
	6:4	BUCK4_RSPPUP	R/W	0x7	
	3	RSVD	R	0x0	
	2:0	BUCK4_RSPPDN	R/W	0x3	
BUCK4_EN_DLY					
0xA4	7:6	BUCK4_ENPIN_CFG	R/W	0x2	See "BUCK1_ENPIN_CFG"
	5:0	BUCK4_EN_DLY	R/W	0x0	See "BUCK1_EN_DLY"
BUCK4_SHUTDN_DLY					
0xA5	7:6	BUCK4_DVSPIN_CFG	R/W	0x2	See "BUCK1_DVSPIN_CFG"
	5:0	BUCK4_SHUTDN_DLY	R/W	0x0	See "BUCK1_SHUTDN_DLY"

12. Revision History

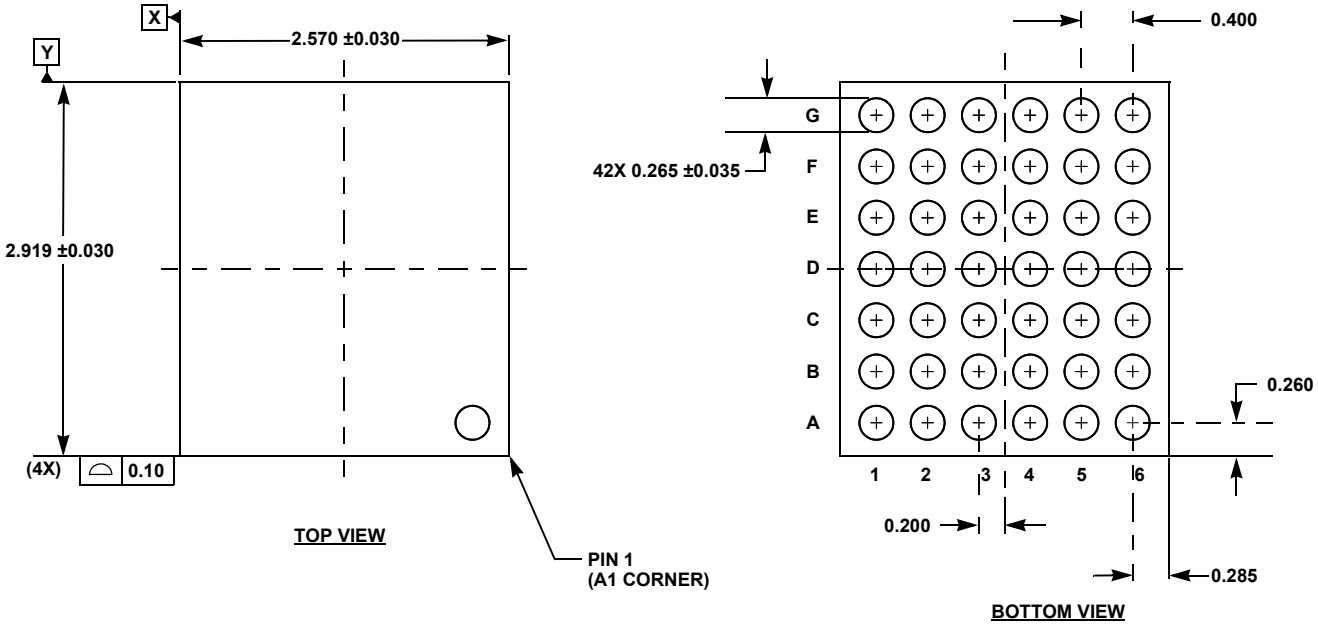
Rev.	Date	Description
4.01	Feb 20, 2020	Removed Addendum. Updated Note 3 to correct JEDEC Pb-free classification.
4.00	Dec 13, 2019	Added Note 1 to Ordering Information table. Added important note to register map table. Added Addendum to page 58.
3.00	Sep 5, 2019	Updated Features, Applications, and Figures 1 and 2 on page 1. Updated Key Differences table on page 7. Updated Pkg. Dwg. # in the Ordering Information table from W6x7.42 to W6x7.42B. Updated Abs Max table on page 11. Electrical Spec table - Updated Buck Output Voltage Range (Each Output) for BUCKx_VOUTFBDIV[1:0] = 0x01: changed Min value from 0.3V to 0.375V. - Updated BUCKx_VOUTFBDIV[1:0] = 0x02: changed Min value from: 0.3V to: 0.5V - I^2C Frequency Capability: removed Min value Updated: I/O Pin Configuration, Output Configuration diagrams Typical Performance Curves: updated Figures 8-15. Updated: Inductor Selection, Input Capacitor Selection, Dynamic Voltage Scaling (DVS). Added: Configuring DVS Speed section/subsections. Updated Figures 33 and 34. Watchdog Time section - updated 10ms to tdebounce. Updated Figure 36. Updated Interrupt Pin section and Figure 37. Updated Overvoltage (OV) and Undervoltage (UV) Protection section. In Serial Communication Interface section, updated Figure 38 and Table 12. Updated SPI Interface section. Updated Figures 41, 42, 47, 48, 49, 50. Table 14 I^2C Timing Specifications, removed Min specification for Rise and fall time of SCL and SDA. Updated Register Address Map table. Updated Register Description by Address table. Updated Disclaimer.
2.00	Apr 6, 2018	Updated dimensions in Features bullet. Update figure titles for Figures 1, 2, 8-13, 17-19, Updated Figures 4-7, 14, 15, 26, and 37. Updated package dimensions in ordering information table. Updated Pin Description for C4. Updated Absolute Maximum Ratings table split out the VOUTs. Updated Table 5 by adding Coilcraft inductor information. Updated 0x3FF to 0x3E5 in Table 10. Updated Table 15 Microvia Structure description. Updated description for IO_OUTPUTCFG[0] row 0x0 Power Stage Configuration column on page 44. Updated description for BUCK1_DVS0VOUT92[7:0] on page 51.

Rev.	Date	Description
1.00	Feb 20, 2018	Updated features bullet on page 1. Added Table 1 on page 7. Updated Recommended Operating Conditions (replaced entire table) on page 11. Added heading to Analog Specification table on page 12. Updated Buck Output Voltage Range and Output Voltage Step Size specifications on page 12. Added High-Side and Low-Side Switch ON-Resistance specifications on page 13. Added Note 8 on page 14. Updated images in Table 4 on pages 15 and 16. Updated Table 10 on page 23. Updated Figure 42 on page 32. Updated Data Hold Time minimum specifications for all modes in Table 14 on page 35 changed from 0ns to 15ns. Updated Figures 48-50 on pages 36 and 37. Added BUCK1_EA2, BUCK2_EA2, BUCK3_EA2, and BUCK4_EA2 information to the Register Map and Register Detail sections. Updated BUCK1_RSPUP[2:0] and BUCK1_RSPPUP[2:0] descriptions removed FBDIV = 0.5 section. Removed About Intersil section. Updated disclaimer.
0.00	Oct 9, 2017	Initial release

13. Package Outline Drawing

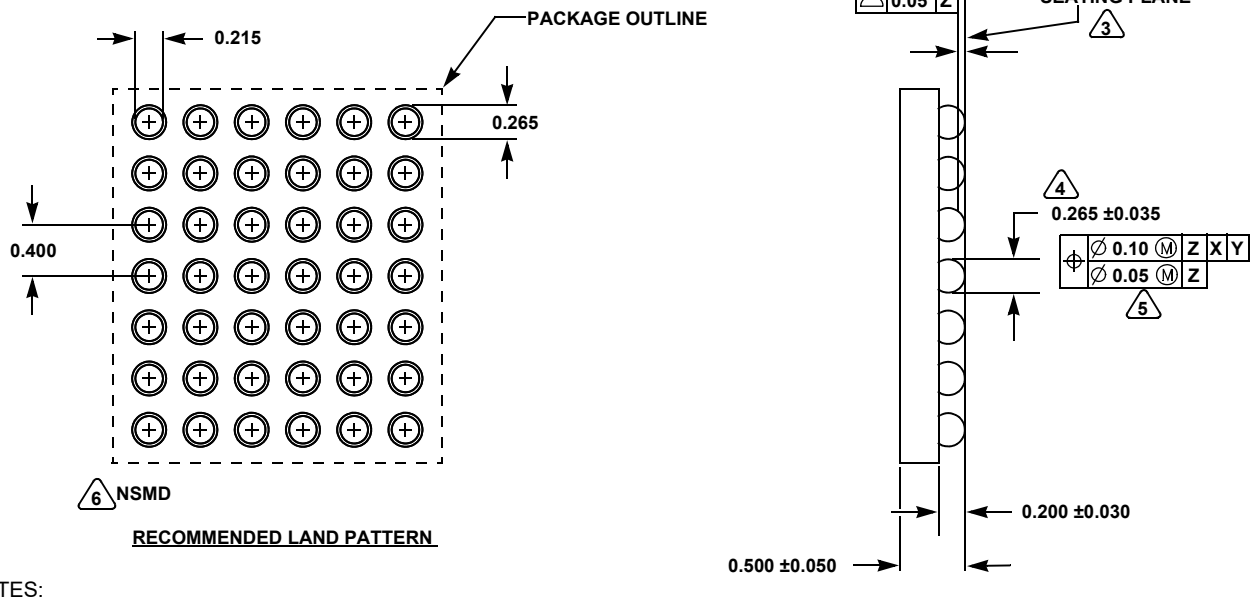
For the most recent package outline drawing, see W6x7.42B.

W6x7.42B
42 BALL WAFER LEVEL CHIP SCALE PACKAGE (WLCSP 0.4mm PITCH)
Rev 0, 1/17



TOP VIEW

BOTTOM VIEW



RECOMMENDED LAND PATTERN

SIDE VIEW

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerance per ASME Y14.5M-1994.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
5. Bump position designation per JESD 95-1, SPP-010.
6. NSMD refers to non-solder mask defined pad design per Techbrief TB451.

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