Buck Regulator, Synchronous, 3.33 MHz, 1 A

FAN53745

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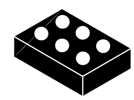
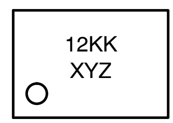


WLCSP6
CASE 567UH

MARKING DIAGRAM



12	= Alphanumeric Device Code (see Ordering Information for specific device marking)
KK	= Lot Run Number
X	= Alphanumeric Year Code
Y	= 2−Weeks Date Code
Z	= Assembly Plant Code

Description

The FAN53745 is a low quiescent current step−down DC/DC converter that delivers a regulated output voltage from an input supply of 2.3 V to 5.5 V. The combination of built−in power transistors, synchronous rectification, and a tiny solution size make the device ideal for portable applications.

The converter normally operates in PWM Mode at a typical fixed−frequency of 3.33 MHz. At moderate and light loads, the device will transition into PFM Mode to maintain high efficiency and excellent transient response. Additionally, a low power Shutdown Mode reduces power consumption when the device is disabled.

The FAN53745 is available in 6−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

Features

- Proprietary Current Mode Architecture
- Wide Input Voltage Range: 2.3 V to 5.5 V
- 1 A Load Capability
- PFM / PWM Modes for High Efficiency
- I^2C−compatible Interface
- Programmable Output Voltage: 1.5 V to 3.3 V
- Programmable Current Limit: 440 mA to 2090 mA
- Internal Soft−Start
- Protection Faults (OT, Input UVLO, Output Short and Reverse Current)
- Automatic Pass−Through Operation
- Hardware Reset when Holding SCL Low
- Pb−Free and RoHS Compliant

Applications

- Smart Phones
- Smart Watch
- Health Monitoring
- Sensor Drive
- Energy Harvesting
- Utility and Safety Modules
- RF Modules

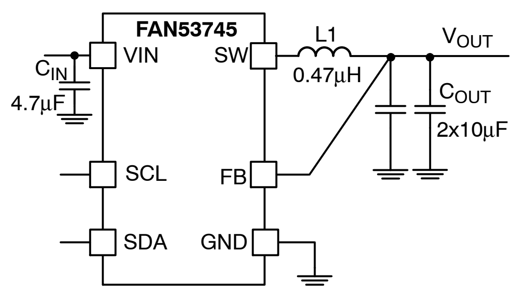


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Device Marking	Output Voltage	Inductor	Temperature Range	Package	Shipping†
FAN53745UC00X	MJ	2.60 V	0.47 μH	−25°C to +85°C	6−bump WLCSP, S/B 1.50 x 0.94	Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BLOCK DIAGRAM

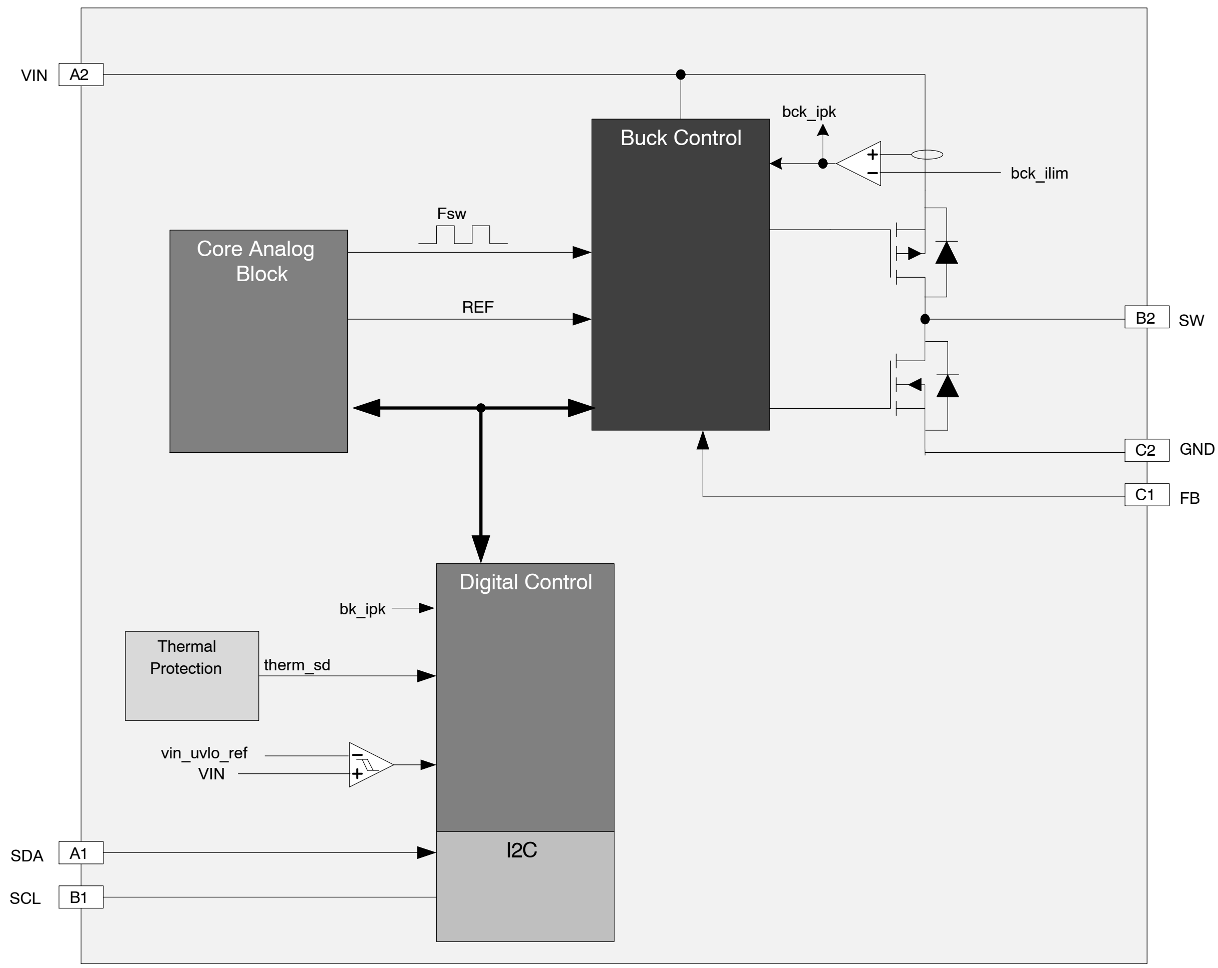


Figure 2. Block Diagram

PRODUCT PIN ASSIGNMENTS

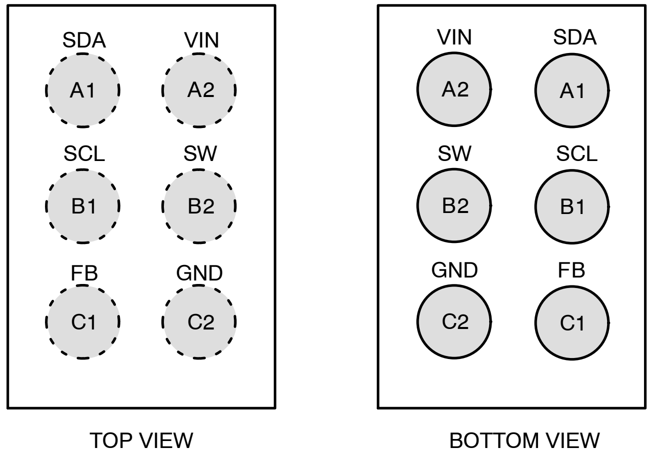


Figure 3. Pin Arrangement

PIN DESCRIPTION

Pin No.	Name	Description
A1	SDA	Serial Interface Data. I^2C input/output data line pin. Do not leave this pin floating.
A2	VIN	Input Voltage. Power input to converter. Place input decoupling capacitor as close to the this pin as possible.
B1	SCL	Serial Interface Clock. I^2C Clock input pin. Holding this pin low for 100 ms will generate a hardware reset. Do not leave this pin floating.
B2	SW	Switching Node. Connect to one side of the inductor.
C1	FB	Feedback. Connect to positive side of output capacitor.
C2	GND	Ground. Power and IC ground. All signals are referenced to this pin.

MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		−0.3	–	6.0	V
V_{SW}	Voltage on SW Pin		−0.3	–	6.0	V
V_{CTRL}	SDA and SCL Pins		−0.3	–	(Note 1)	V
	FB Pin		−0.3	–	(Note 1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model	–	2.0	–	kV
ESD	Electrostatic Discharge Protection Level	Charged Device Model	–	500	–	V
T_J	Junction Temperature		−40	–	+150	°C
T_{STG}	Storage Temp		−40	–	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6 V or VIN + 0.3 V.

THERMAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{JA}	Junction−to−Ambient Thermal Resistance		–	65	–	°C/W

2. Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with two−layer 2s2p with VIAs boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature TJ(max) at a given ambient temperature TA.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Supply Voltage Range		2.3	–	5.5	V
L	Inductor		–	0.47	–	μH
C_{IN}	Input Capacitor		–	4.7	–	μF
C_{OUT}	Output Capacitor		–	2x10	–	μF
I_{OUT}	Output Current		–	–	1000	mA
T_A	Operating Ambient Temperature		−25	–	+85	°C
T_J	Junction Temperature		−40	–	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{IN} = 3.8 V, V_{OUT} = 1.5 to 3.3 V, T_J = –25°C to +125°C unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.8 V, V_{OUT} = 2.6 V)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OPERATING CURRENT						
I_{RESET}	Shutdown Supply Current	ENABLE bit = 0, No Load, SCL pulled low	–	0.25	–	µA
I_{IDLE}	Standby Supply Current	ENABLE bit = 0, No Load	–	15.4	–	µA
IQ_{PFM}	PFM Quiescent Current	ENABLE bit = 1, PFM Mode, Non Switching, No Load	–	43	–	µA
IQ_{PWM}	PWM Quiescent Current (Note 4)	ENABLE bit = 1, FPWM Mode, No Load	–	8.5	–	mA
IQ_{PT_PFM}	PASS−THRU from PFM Current Consumption (Note 4)	ENABLE = 1, V_{OUT_TARGET} > V_{IN} > V_{UVLO}	–	80	–	µA
IQ_{PT_PWM}	PASS−THRU from PWM Current Consumption (Note 4)	ENABLE bit = 1, V_{OUT_TARGET} > V_{IN} > V_{UVLO}	–	80	–	µA
OUTPUT VOLTAGE						
VO_{MIN}	Minimum Programmable Voltage	2.3 V ≤ V_{IN} ≤ 4.9 V	–	1.500	–	V
VO_{MAX}	Maximum Programmable Voltage	3.8 V ≤ V_{IN} ≤ 4.9 V	–	3.30	–	V
VO_{DVS}	Programmable Voltage Slew Rate	1.5 V ≤ V_{OUT} ≤ 3.3 V	–	0.5, 1.0, 1.25, 2.0, 2.5, 3.75, 5, 10	–	mV/µs
VO_{DVS_ACC}	Programmable Voltage Slew Rate for 0.5 to 3.75 mV/µs Scaling Settings	V_{IN} = 2.3 to 4.9 V & V_{IN} > V_{OUT} + 500 mV	−10	–	+10	%
	Programmable Voltage Slew Rate for 5 mV/µs and 10 mV/µs	V_{IN} = 2.3 to 4.9 V & V_{IN} > V_{OUT} + 500 mV	−20	–	+20	%
T_{DVS}	Period from I²C command to ramp start	V_{IN} = 2.3 to 4.9 V & V_{IN} > V_{OUT} + 500 mV	–	–	40	µs
PWM VOLTAGE ACCURACY						
$VOUT_{ACC}$	Output Voltage Accuracy	V_{IN} = 2.3 to 4.9 V & V_{IN} > V_{OUT} + 500 mV, V_{OUT} = 1.5 V to 3.3 V, Forced PWM Mode, I_{OUT} = 0 A; −40°C to 85°C	−40	–	+40	mV
PFM VOLTAGE ACCURACY						
$VOUT_{ACC}$	Output Voltage Accuracy	V_{IN} = 2.3 to 4.9 V & V_{IN} > V_{OUT} + 500 mV, V_{OUT} = 1.5 V to 3.3 V, PFM Mode, I_{OUT} = 0 A; −40°C to 85°C	−2	–	+3	%
CURRENT LIMIT						
$ILIM_{PWM\_ACC}$	Peak Inductor Current Limit Accuracy	Peak current accuracy for ≤ 1.0 A pk setting, open loop	−25	–	+25	%
		Peak current accuracy for > 1.0 A pk setting, open loop	−12	–	+12	%
$ILIM_{PFM\_ACC}$		PFM peak current accuracy for < 1.0 A pk setting, open loop	−30	–	+30	%
		PFM peak current accuracy for > 1.0 A pk setting, open loop	−20	–	+20	%
$ILIM_{NEG}$	Negative Current		−700	−1000	−1300	mA
PFM <−> PWM THRESHOLDS						
I_{PFM}	I_{OUT} where part transitions into PFM	V_{IN} = 3.8 V, V_{OUT} = 1.5 V – 3.3 V	–	103	–	mA
I_{PWM}	I_{OUT} where part transitions into PWM	V_{IN} = 3.8 V, V_{OUT}= 1.5 V – 3.3 V	–	135	–	mA

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at V_{IN} = 3.8 V, V_{OUT} = 1.5 to 3.3 V, T_J = −25°C to +125°C unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = 3.8 V, V_{OUT} = 2.6 V) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
UVLO DETECTION						
V_{UVLO_RISE}	Under−Voltage Lockout Threshold	Rising V_{IN}	2.10	2.15	2.20	V
V_{UVLO_FALL}	Under−Voltage Lockout Threshold	Falling V_{IN}	2.00	2.05	2.10	V
V_{UVLO_HYS}	UVLO Hystersis		–	100	–	mV
POWER MOSFETs RDSON						
RDS_{ON_NMOS}	NMOS Resistance (Ball−to−Ball)	VIN = VGS = 3.8 V	–	92	–	mΩ
RD_{ON_PMOS}	PMOS Resistance (Ball−to−Ball)	VIN = VGS = 3.8 V	–	125	–	mΩ
GENERAL						
F_{SW}	Switching Frequency	PWM, I_{OUT} = 0 A	3.00	3.33	3.67	MHz
R_{BK_DIS}	Output Discharge Resistance		80	100	120	Ω
I²C TIMING AND PERFORMANCE						
V_{IL}	SDA and SCL Logic Low threshold		–	–	0.4	V
V_{IH}	SDA and SCL Logic High threshold		1.2	–	5.5	V
V_{OL}	SDA Logic Low Output	3 mA Sink	–	–	0.4	V
I_{OL}	SDA Sink Current		2.0	–	–	mA
f_{SCL}	SCL Clock Frequency	Fast Mode Plus		–	1000	kHz
t_{BUF}	Bus−Free Time Between STOP and START Conditions (Note 4)	Fast Mode Plus	0.5	–	–	μs
t_{HD}; STA	START or Repeated START Hold Time	Fast Mode Plus	260	–	–	ns
t_{LOW}	SCL LOW Period	Fast Mode Plus	0.5	–	–	μs
t_{HIGH}	SCL HIGH Period	Fast Mode−Plus	260	–	–	ns
t_{SU}; STA	Repeated START Setup Time	Fast Mode−Plus	260	–	–	ns
t_{SU}; DAT	Data Setup Time	Fast Mode Plus	50	–	–	ns
t_{VD}; DAT	Data Valid Time	Fast Mode Plus	–	–	450	ns
t_{VD}; ACK	Data Valid Acknowledge Time	Fast Mode Plus	–	–	450	ns
t_R	SDA and SCL Rise Time (Note 4)	Fast Mode Plus	–	–	120	ns
t_F	SDA and SCL Fall Time (Note 4)	Fast Mode Plus, V_{DD} = 1.8 V	6.55	–	120	ns
t_{SU}; STO	Stop Condition Setup Time	Fast Mode Plus	260	–	–	ns
C_i	SDA and SCL Input Capacitance (Note 5)		–	–	10	pF
C_b	Capacitive Load for SDA and SCL (Note 5)		–	–	550	pF
t_{SP}	Spike pulse width that input filter must be suppress	SCL, SDA only	0	–	50	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Refer to Typical Characteristics waveforms/graphs for closed loop data and variation with input supply and temperature. Electrical specifications reflects both steady state and dynamic close loop data associated with the recommended external components.
4. Guaranteed by Design. Characterized on the ATE or Bench
5. Guaranteed by Design Only. Not Characterized or Production Tested

SYSTEM SPECIFICATIONS (The following system specifications are guaranteed by designed and verified during bench evaluation, but are not performed in production testing. Recommended operating conditions, unless otherwise noted are, V_{IN} = 2.3 V to 4.9 V & V_{IN} > V_{OUT} + 500 mV, T_A = –25°C to 85°C, V_{OUT} = 2.6 V. Typical values are based on V_{IN} = 3.8 V, V_{OUT} = 2.6 V and T_A = 25°C. System Specifications area based on circuit per Figure 1. L = 0.47 μH, C_{IN} = 4.7 μF, C_{OUT} = 2 x 10 μF) (Note 6)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOUT REGULATION						
$LOAD_{REG}$	Load Regulation	1 mA ≤ I_{OUT} ≤ 1000 mA, V_{IN} = 2.3 to 4.9 V & V_{IN} ≥ V_{OUT} + 500 mV, V_{OUT} = 1.5, 2.6, 3.2 V FPWM	–5	–	+5	mV
V_{TRRP}	Load Transient	I_{OUT} = 0 mA <–> 1 A, T_R = T_F = 500 mA/ms, Auto Mode, V_{IN} = 3.8 V, V_{OUT} = 1.5, 2.6 and 3.2 V	–30	–	+45	mV
$LINE_{TRAN}$	Line Transient	V_{IN} = 3.0 V <–> 3.6 V, 100 mV/μs, I_{OUT} = 300 mA, PWM, V_{OUT} = 2.6 V	–35	–	+35	mV
RIPPLE						
V_{RIPPLE}	Output Ripple	V_{IN} = 2.3 to 4.9 V, I_{OUT} = 1 mA and 10 mA, PFM Mode, V_{OUT} = 1.5, 2.6 and 3.2 V	–	31	50	mV
V_{RIPPLE}	Output Ripple	V_{IN} = 2.3 to 4.9 V, I_{OUT} = 500 mA and 1.0 A, V_{OUT} = 1.5, 2.6 and 3.2 V, PWM Mode	–	5	15	mV

6. System Specification are tested closed loop while using the recommended external components table.

TYPICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 2.6 V, Auto Mode, T_A = 25°C, circuit and components according to the recommended external components and layout.

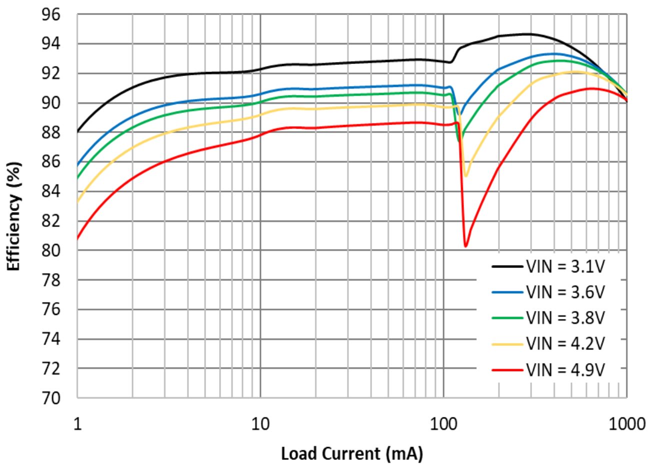


Figure 4. Efficiency vs. Load Current and Input Voltage

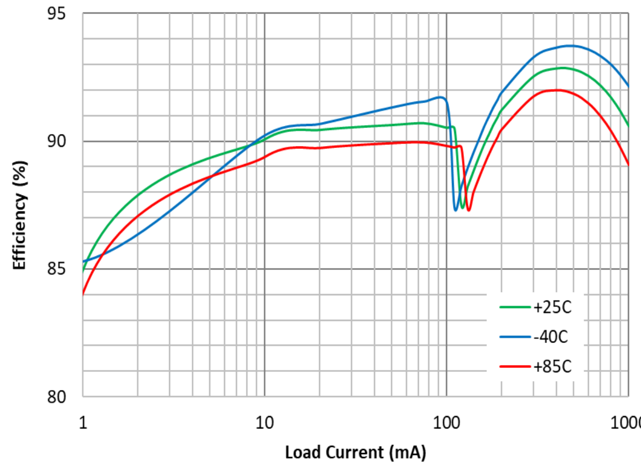


Figure 5. Efficiency vs. Load Current and Temperature

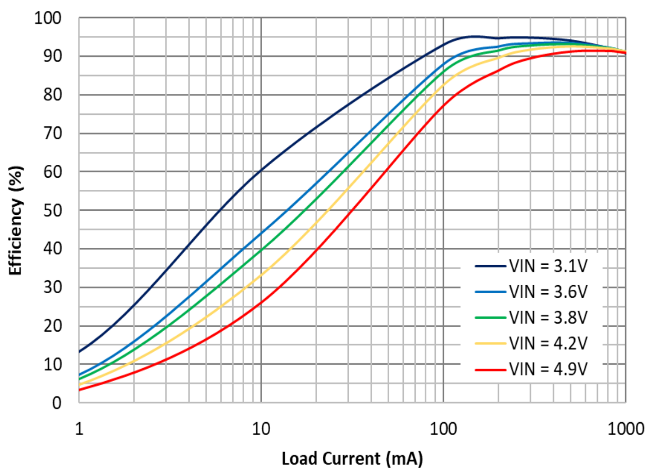


Figure 6. Efficiency vs. Load Current and Input Voltage, FPWM Mode

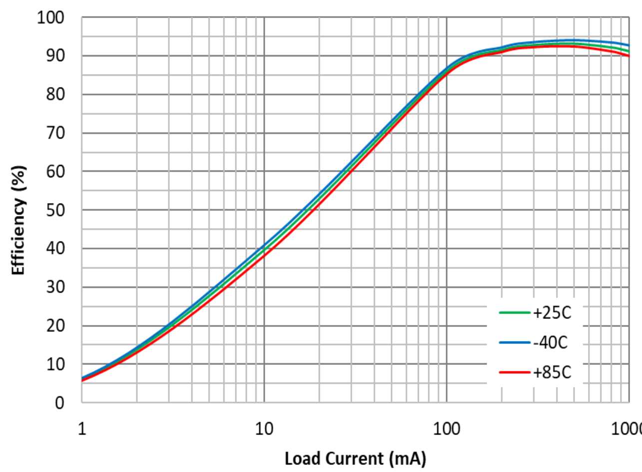


Figure 7. Efficiency vs. Load Current and Temperature, FPWM Mode

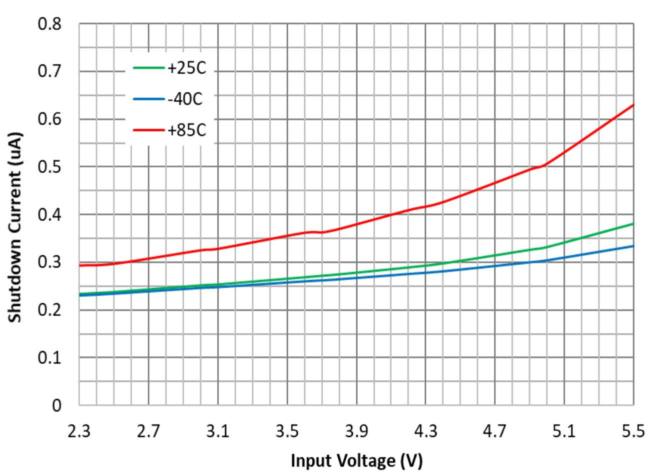


Figure 8. Shutdown Current vs. Input Voltage and Temperature

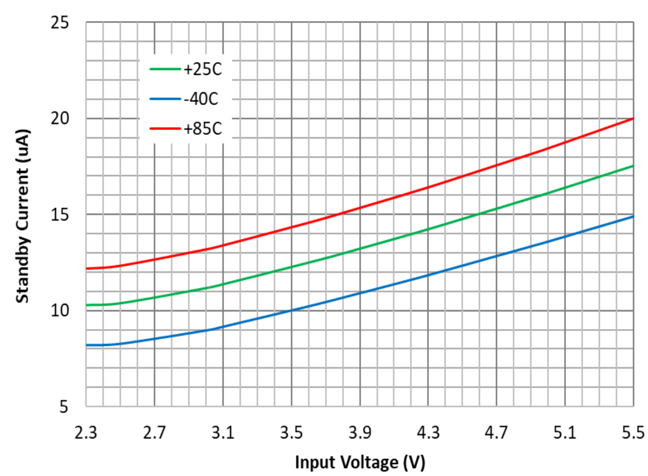


Figure 9. Standby Current vs. Input Voltage and Temperature

TYPICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 2.6 V, Auto Mode, T_A = 25°C, circuit and components according to the recommended external components and layout.

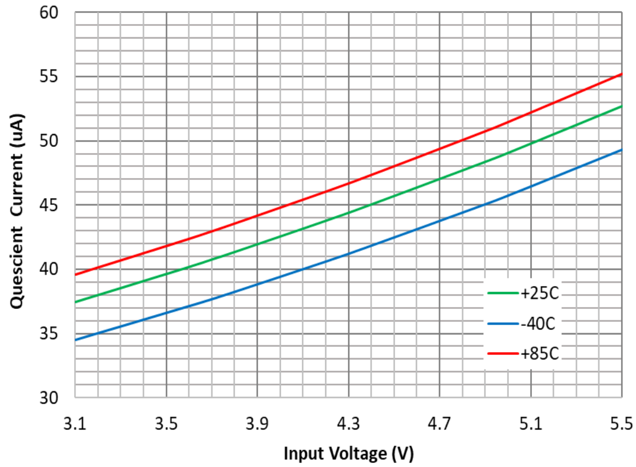


Figure 10. PFM Quiescent Current vs. Input Voltage and Temperature

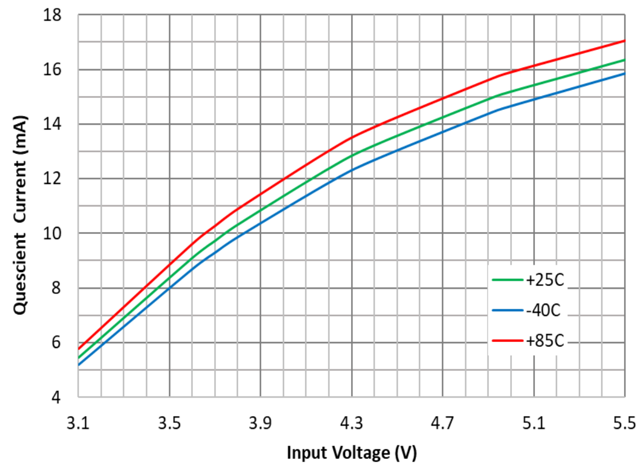


Figure 11. PWM Quiescent Current vs. Input Voltage and Temperature

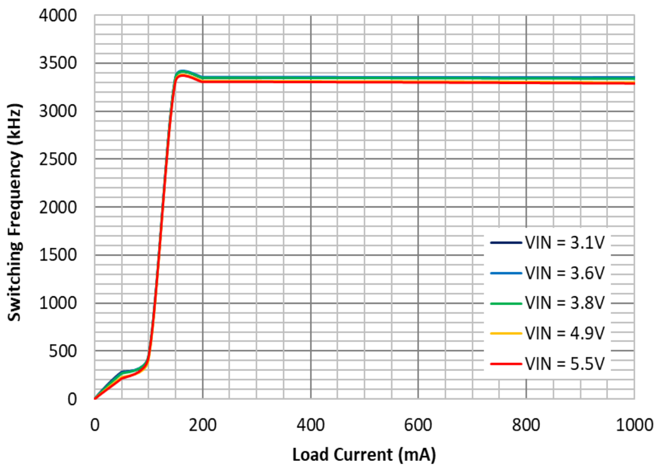


Figure 12. Frequency vs. Load Current and Input Voltage

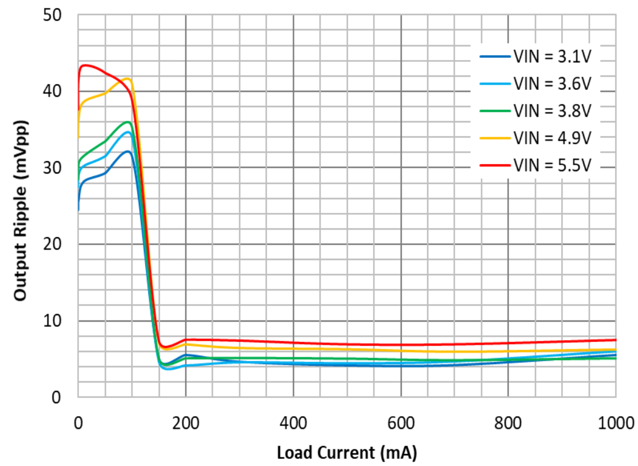


Figure 13. Output Ripple vs. Load Current and Input Voltage

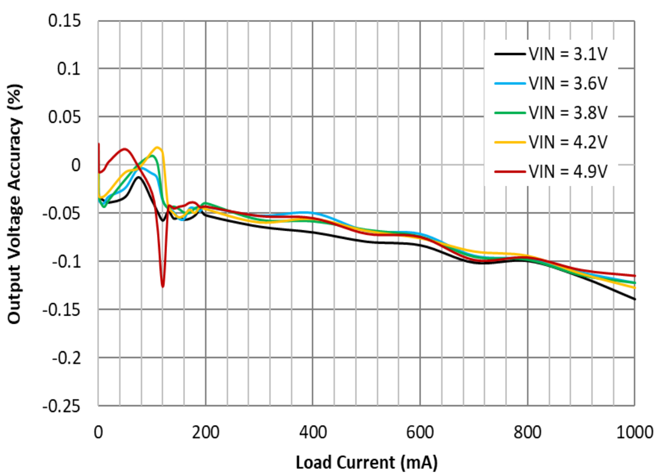


Figure 14. Output Voltage Accuracy (%) and Input Voltage

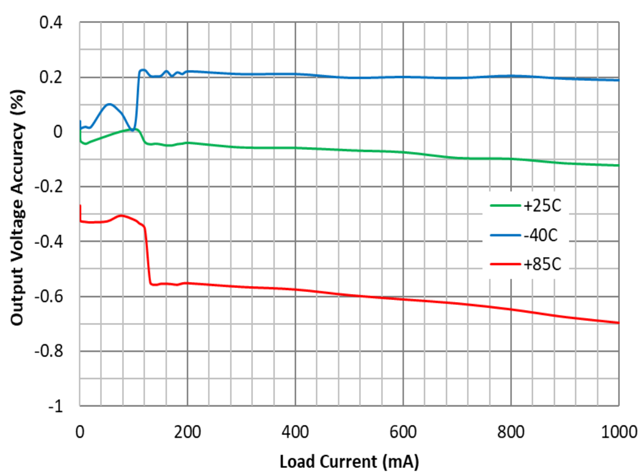


Figure 15. Output Voltage Accuracy (%) and Temperature

TYPICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 2.6 V, Auto Mode, T_A = 25°C, circuit and components according to the recommended external components and layout.

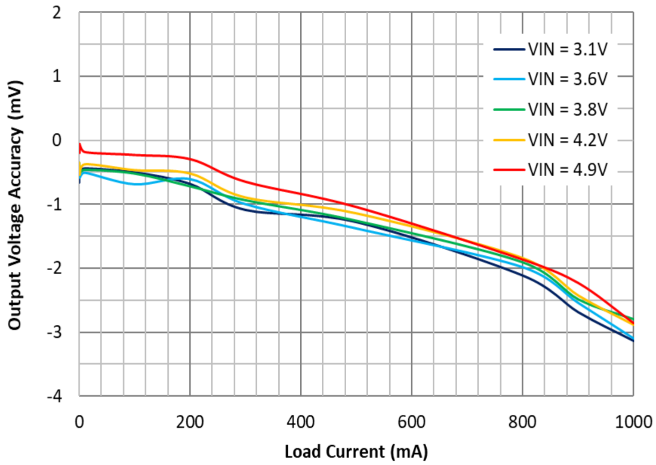


Figure 16. FPWM Output Voltage Accuracy (mV) and Input Voltage

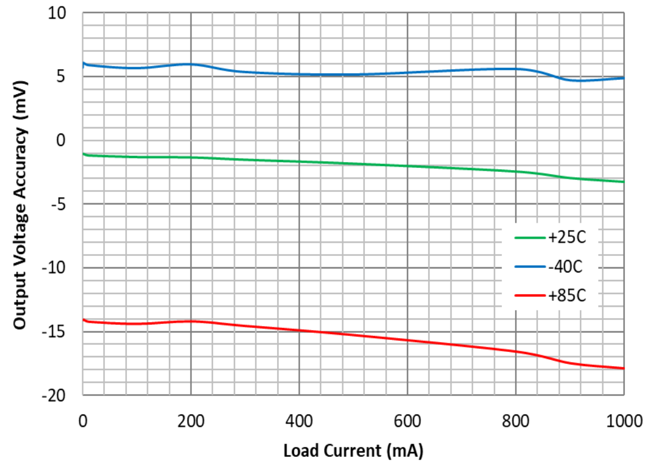


Figure 17. FPWM Output Voltage Accuracy (mV) and Temperature

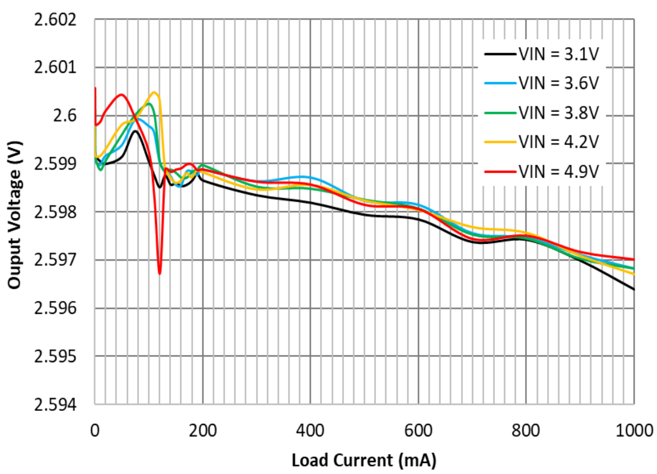


Figure 18. Load Regulation and Input Voltage

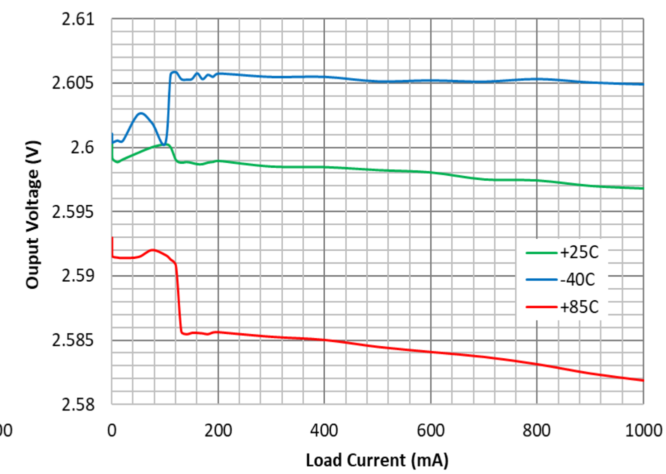


Figure 19. Load Regulation and Temperature

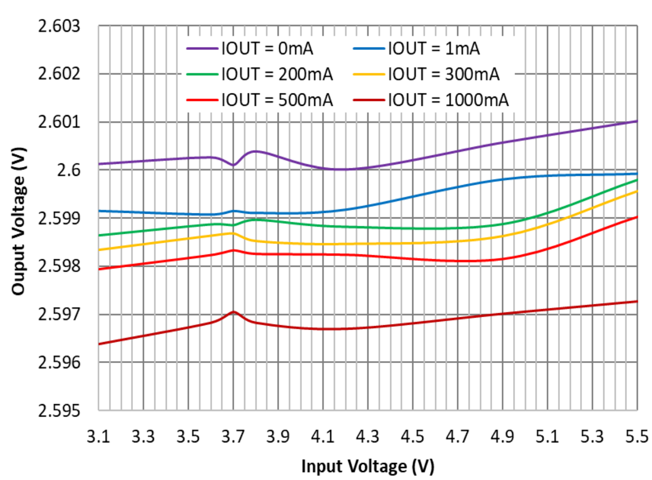


Figure 20. Line Regulation and Load Current

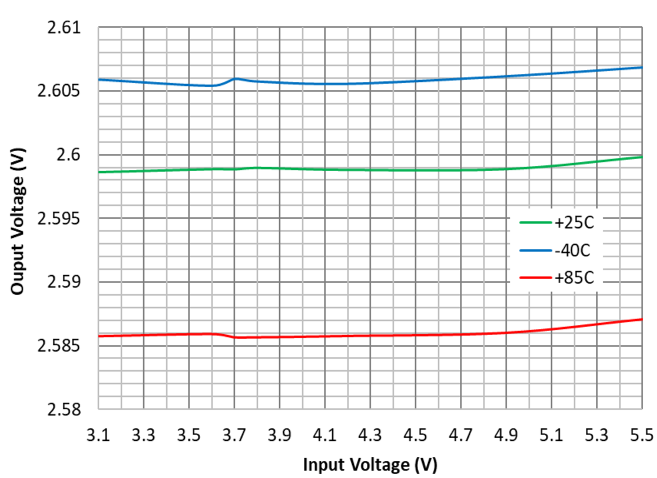


Figure 21. Line Regulation and Temperature, I_{OUT} = 200 mA

TYPICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 2.6 V, Auto Mode, T_A = 25°C, circuit and components according to the recommended external components and layout.

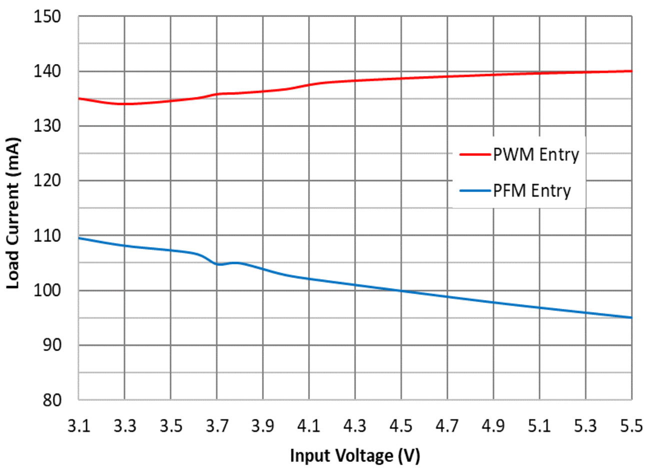


Figure 22. PFM−PWM Entry, V_{OUT} = 2.6 V

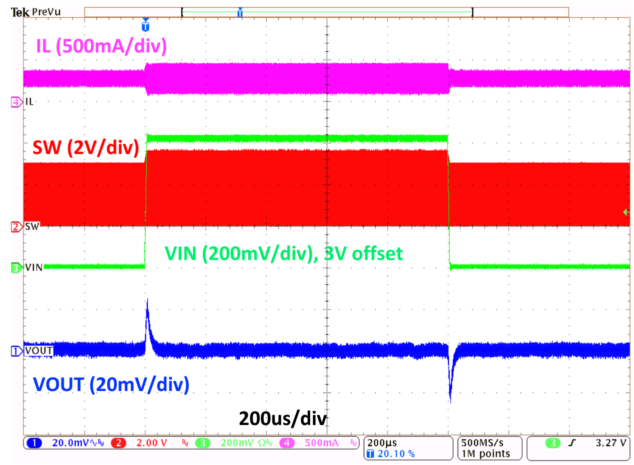


Figure 23. Line Transient, V_{OUT} = 2.6 V, 3 V ←→ 3.6 V, 6 μs Edge, 300 mA Load

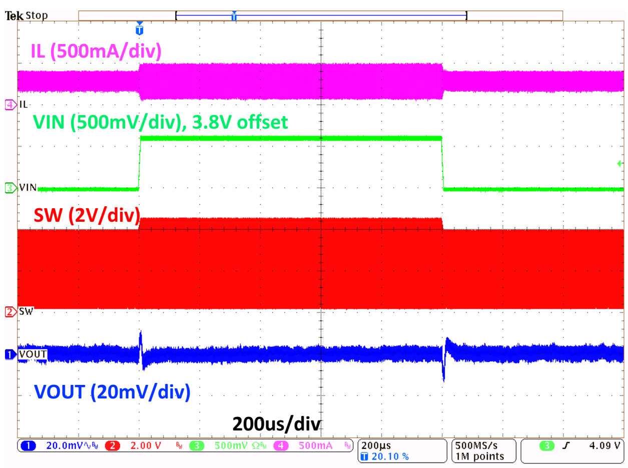


Figure 24. Line Transient, V_{OUT} = 3.3 V, 3.8 V ←→ 4.4 V, 6 μs Edge, 300 mA Load

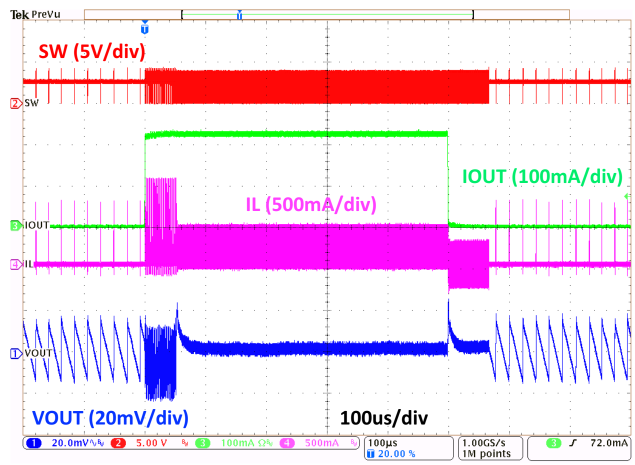


Figure 25. Load Transient 10 mA ←→ 200 mA, 1 μs Edge

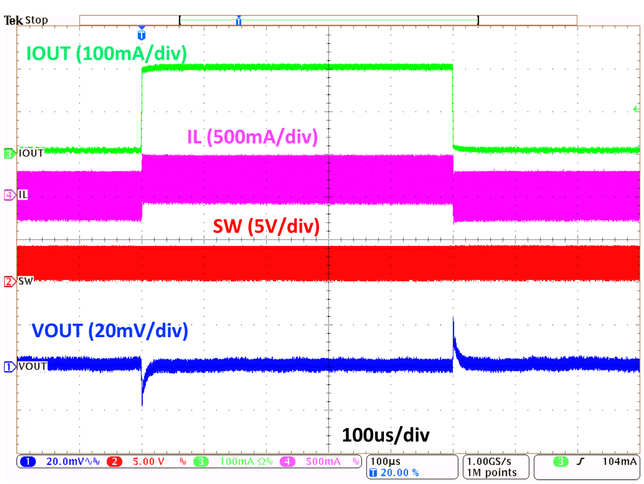


Figure 26. Load Transient 10 mA ←→ 200 mA, 1 μs Edge, FPWM Mode

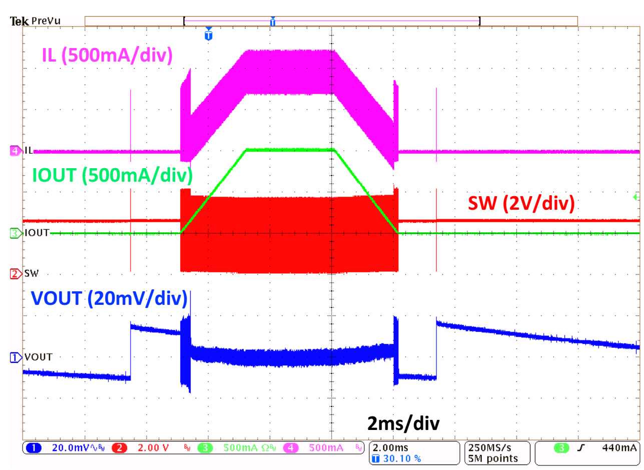


Figure 27. Load Transient 0 A ←→ 1 A, 2 ms Edge

TYPICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 2.6 V, Auto Mode, T_A = 25°C, circuit and components according to the recommended external components and layout.

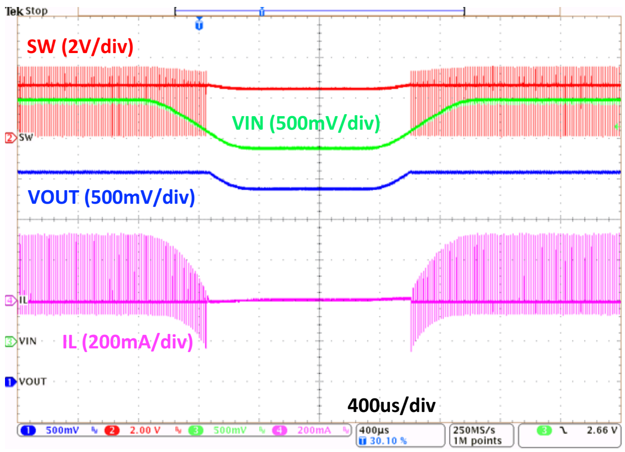


Figure 28. Pass Thru Operation, I_{OUT} = 10 mA, V_{IN} = 3 ←→ 2.4 V, V_{OUT} = 2.6 V

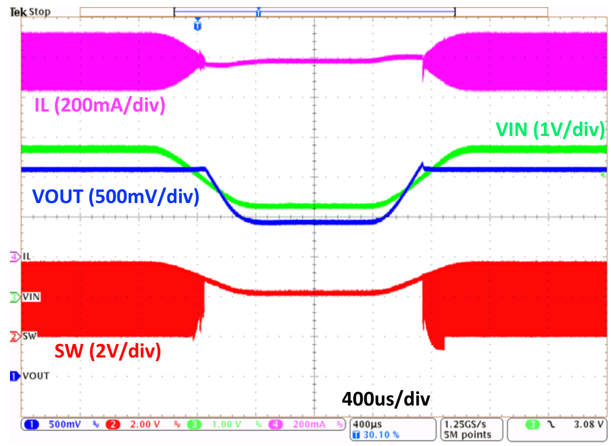


Figure 29. Pass Thru Operation, I_{OUT} = 1 A, V_{IN} = 3.8 ←→ 2.4 V, V_{OUT} = 2.6 V

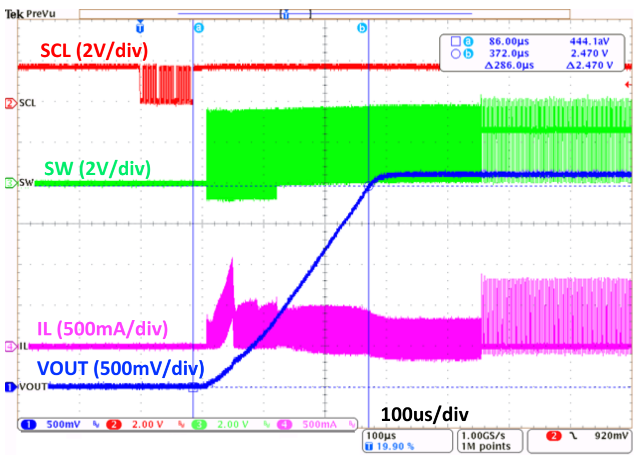


Figure 30. Startup into 100 mA Load

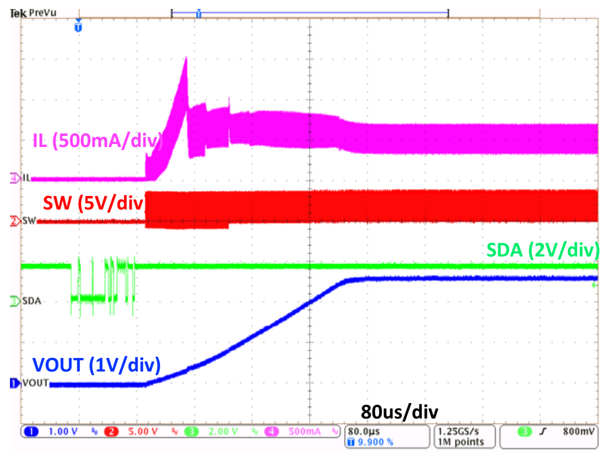


Figure 31. Startup into 500 mA Load

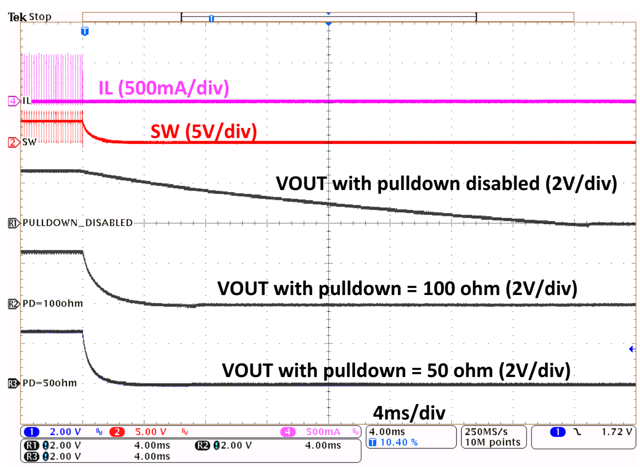


Figure 32. V_{OUT} Discharge with Different Pulldown Settings

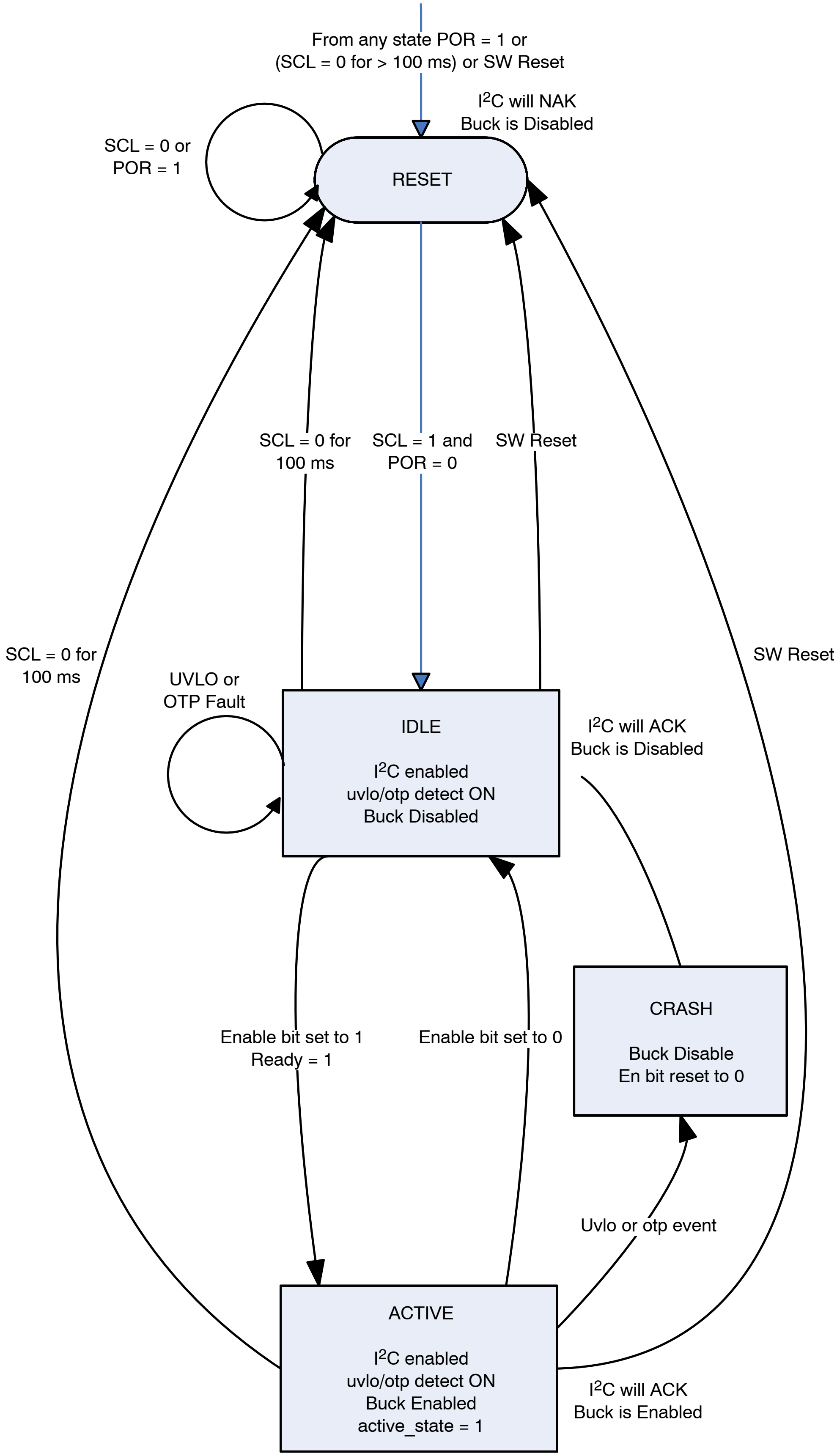
FUNCTIONAL SPECIFICATIONS

Device Operation

Operation Description

The FAN53745 uses a proprietary current mode architecture with synchronous rectification to convert input voltages down to a regulated output voltage while limiting the peak inductor current.

During medium to heavy loading of the output, the FAN53745 operates in PWM operation to ensure excellent regulation. During light loading, the device automatically switches to PFM operation for high efficiency. To avoid potential noise interference by PFM switching frequencies with the load or other circuitry, the device can be programmed into Forced PWM operation. More details on PFM and PWM operation can be found under the Modes of Operation heading.



Ready status = ((idle_state or active_state) and pwr_ok and ($\overline{\text{over\_temp\_fault}}$ or $\overline{\text{uvlo\_fault}}$)

Figure 33. State Diagram

Device States

Reset State

When power is applied to the FAN53745, the device will go through a Power On Reset (POR) and then the FAN53745 checks the state of the I^2C SCL pin. If the SCL pin is low, the device will stay in the Reset State. If the SCL is high or if it at anytime goes high, the device moves to the Idle State. During Reset State, all I^2C registers are cleared to their default values and cannot be written to or read. If at anytime the input voltage were to fall below the POR threshold, the device will completely power off.

Software Reset

If the correct Reset code is written to the RESET register or the SCL pin is pulled low for more than 100 ms, the device will exit the present state (Active or Idle) and enter the Reset State. For a SW reset, by setting the Reset register, the device will only enter the Reset State momentarily to clear the registers and then the device will enter Idle State.

SCL Low Reset

If the device entered Reset because the SCL was held low for more than 100 ms, house keeping circuitry will be powered down to reduce power consumption and all registers will be reset to their default values. The device will remain in the Reset State as long as the SCL is held low. Once the SCL is released high, a wait time of ~20 μs or more should be allowed for the I^2C to properly read any I^2C commands. After the housekeeping circuitry is stable, the READY bit will be set and the ENABLE bit can be set for the device to move from the Idle State to Active State.

Note: Care should be used when sharing the I^2C with another slave which may stretch the clock for more than 100 ms. If the application requires for the FAN53745 to ignore the SCL being held low, please consult your local On Semiconductor representative.

Idle State

In Idle State the I^2C registers are read/write accessable and the UVLO comparator is activated. The READY bit in the Status Register 0x02h will be ”1” while in the Idle State, providing there isn’t a UVLO or OT fault. If the input voltage is less than UVLO rising threshold upon entering the Idle State from the Reset State, a UVLO fault will be generated and the device will stay in this state as long as POR < VIN < UVLO rising.

When the device enters Idle State due to either a UVLO or OT condition, the device waits 20 ms for the fault to clear. If the fault still exists after the 20 ms, the device will remain in the Idle State and READY = 0 until the fault clears. If the ENABLE bit is set to a ”1” while either a UVLO or OT fault condition exists, the bit will be immediately cleared and the device will not advance to the Active State. Only after the fault has cleared and ENABLE is then set to ”1” will the device move to the Active State.

Active State

In Active State, the buck converter is enabled and provides a regulated output voltage to the load. If during Active State the input voltage falls between POR and UVLO_Falling, the device will exit Active State, the Enable bit will be cleared and the device will return to an Idle State.

If the device temperature exceeds the OTP threshold while in the Active State, the Enable bit will be cleared and the device will return to the Idle State. The device will remain in the idle state until it cools below the hysteresis level and the ENABLE bit is set again to ”1”.

When a UVLO or OTP fault occurs, the associated STATUS and FAULT register bits are set. The Status bit will be cleared when the input voltage recovers or the die temperature returns below the hysteresis level. The Fault bits will remain set to ”1” until they are read.

Startup Behavior

Startup Description

To enable the FAN53745, the ENABLE Register bit must be set to “1”. The FAN53745 has internal soft−start which limits the input current from the battery by incrementing the voltage up to the target output voltage. This limits the current drawn and prevents brown out conditions. The device starts up within 520 μs typical using the recommended external components table.

Shutdown Behavior

Disable

To disable the FAN53745, the ENABLE reg bit should be configured to code 0. When the part is disabled, the output will tristate. If the DISCHARGE SEL bits are set to something other than ”00”, the output will be discharged through the selected resistance. Otherwise, if DISCHARGE SEL = ”00”, the output will only be discharged by the load.

Active Pull Down

The FAN53745 has an active pull down to discharge the output capacitance. Once the ENABLE reg bit is set to 0, within ~2 μs, the active pull down is enabled and discharges the VOUT via an internal resistor. The strength of the pull down can be selected between 50 Ω, 100 Ω (Default), 200 Ω and open by setting the DISCHARGE SEL I^2C bit. If the DISCHARGE I^2C bit is set to 1, the resistor selected by DISCHARGE SEL will be used to discharge the output during voltage programming transitions from a higher to lower voltage.

Modes of Operation

PFM

Pulsed Frequency Modulation (PFM) operation adjusts the switching frequency relative to the load. By reducing the switching frequency at lighter load conditions, higher efficiency is realized at these light loads. In Automode operation, the device enters PFM mode when the load falls below IPFM threshold.

PWM

During Pulse Width Modulation (PWM) mode, the device switches at a nominal fixed frequency of 3.3 MHz, which reduces the values of the external components. During Auto Mode, the part enters PWM when load currents exceed IPWM typ. In PWM mode the device has excellent load regulation, ideal for powering loads which are sensitive to deviations in supply voltage. The FAN53745 can be forced into PWM (FPWM) regardless of the load current by setting FORCE_PWM to a “1”.

Pass Thru

To ensure there is not sub−harmonic behavior when Vin is close to the Vout_Target, the device enters Pass−Thru automatically. Using a proprietary method, the device maintains excellent regulation when transitioning into and out of Pass−Thru mode.

Protection Features

SHORT FAULT

If the output voltage falls below one−half the programmed voltage during normal operation, the device will declare a Short fault immediately without a debounce period and the SHORT FAULT bit will be set.

PFM Current Limit

During PFM operation, the peak current is limited to control the ripple and prevent the inductor from saturating. The open loop PFM current limit can be programmed between 500 mA and 1325 mA in 55 mA steps. Due to inherent delays, the closed loop PFM current limit is expected to be 10 to 15% higher than the open loop PFM ILIMIT threshold of the device. Once the current limit is set, it can be locked by setting the locking bit V_I_LIMIT_LOCK.

PWM Current Limit

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from damaging the device. After 500 μs of current limit, the regulator triggers an over−current fault, causing the regulator to shut down for about 20 ms before attempting a restart. If the fault is caused by a short circuit, the soft−start circuit attempts to restart after about 20 ms and produces a SHORT FAULT if the fault persisted.

The open Loop Peak Inductor Current Limit can be programmed via I^2C and range from 440 mA to 2090 mA max in 110 mA steps. Due to inherent delays, the closed loop current limit is expected to be 10 to 15% higher than the open loop ILIMIT threshold of the device.

UVLO

- Rising

While in Idle or Active State, the UVLO detection is enabled. The FAN53745 is designed to check the input voltage before enabling the converter. For Idle State, the input voltage must be above the UVLO rising threshold when the ENABLE bit is set to enable the buck converter. Otherwise, once loaded by the buck converter, the input voltage may fall below the UVLO falling threshold, resulting in start−up hiccup behavior. If the voltage is below the UVLO rising threshold when the ENABLE bit is set, the UVLO fault and status bits will be set and the ENABLE bit cleared.

- Falling

If the input voltage falls below the UVLO_falling threshold during Active State, the buck ENABLE bit will be cleared, the device will go to the Idle State and the PASS−THRU and PFM−PWM bits in the Status Reg are set to their default values of ”0” and ”1” respectively.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the ENABLE bit is cleared and the device returns to Idle State and the OVER TEMP Status and Fault bits are set. The PASS−THRU and PFM−PWM bits in the Status Reg are set to their default values of ”0” and ”1” respectively.

By monitoring the OVER TEMP bit in the FAULT STATUS register, when the die temperature falls below the hysteresis temperature and OVER_TEMP falls to ”0”, the buck can be re−enabled.

Negative Current Limit

The FAN53745 has a negative current limit protection which limits the current through the NFET in PWM Mode. If a voltage is applied to the buck output and is higher than VOUT target while in PWM, a negative current will be detected. Once the inductor current hits −1 A for one cycle, the output begins to tristate until the applied voltage is released and the output voltage falls below the regulated voltage.

In PFM mode, the Zero Crossing Detection does not allow any negative current to flow within inductor, any voltage higher than vout target applied to output will cause the regulator to enter tri−state and block current back through inductor.

NOTE: If a voltage applied to VOUT is greater than VIN, the body diode of high side FET will conduct.

Output Voltage

Programmable Output Voltage

The FAN53745 output voltage can be programmed in 10 mV steps from 1.5 to 3.3 V using the VESL register. The voltage transition is implemented by stepping through the voltage programming DAC up−to/down−to the new target voltage. The FAN53745 provides DVS functionality where by the period of time between each step can be controlled by setting the DVS register bits.

Limiting the Programmable Range

If a new voltage value is written into the VSEL register which is either higher than VMAX or lower than VMIN, the DAC will scale to the limit(VMAX or VMIN), preventing the voltage from going beyond the limit.

If a new value for VMAX or VMIN is written to the registers and is either lower than or higher than respectively of the present voltage in the VSEL register, the output voltage will remain at it’s present voltage until commanded to change when a new VSEL value is written.

Dynamic Voltage Scaling

The FAN53745 DVS operation for programming the voltage to a new level can be controlled by setting the DVS register bits for rates of 0.5 to 10 mV/μs. If the DVS EN bit in the MODE Register, 0x03 is set to a ”1” when the output voltage is commanded to a lower voltage, the DAC decrements through the programmable output voltage steps until the reference value for target voltage is reached. The output voltage will fall at a rate dependent on the amount of distributed capacitance and load. The speed of the reduction in voltage can be accelerated by setting the DISCHARGE register bit in the SHUTDOWN register. The discharge resistance will be disabled when the DAC reference value is reached. The drawings below provide an example of the behavior during rising and falling DVS control.

Note:

- If there is little or no load on the output during the ramp, some non−linear ramping of the output voltage may be observed during DVS ramping.
- Simply setting the DVS bit to a ”1” does not initiate voltage change. Voltage change is only initiated when the VSEL register value is changed.

I²C Interface

Introduction

The FAN53745 serial interface is compatible with the Standard−mode, Fast−mode and Fast−mode Plus I²C bus specifications. The SCL pin is an input and the SDA pin is bi−directional with an open−drain output configuration. The IC supports single register read and write transactions as well as multiple register read transactions.

Slave Address

The default I²C address is shown below in the Device Address Values table. Other slave addresses can be accommodated upon request. Contact your On Semiconductor representative.

Table 1. DEVICE ADDRESS VALUES

Device	Hex	Binary
FAN53745	7h20	0100000X

Table 2. 7−BIT BINARY ADDRESS

7	6	5	4	3	2	1	X
0	1	0	0	0	0	0	R/W

READE = 1
WRITE = 0

I²C Timing Diagrams

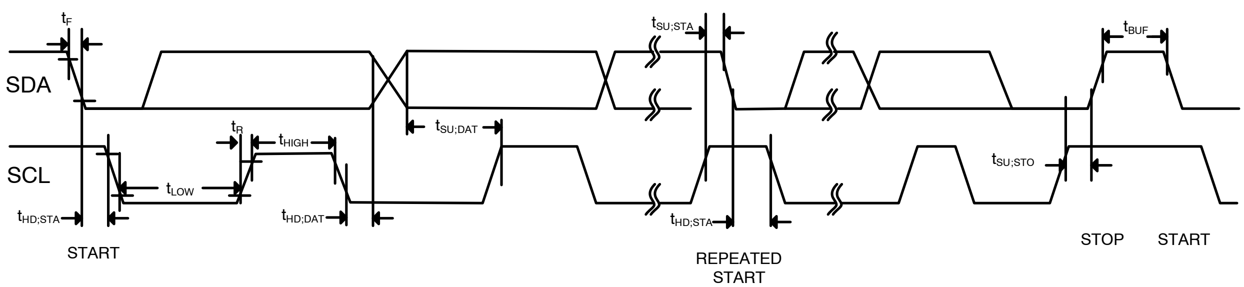


Figure 34. I²C Interface Timing for Fast−Mode Plus, Fast−Mode and Standard−Mode

Normally, data transfer occurs when the SCL is LOW. Data is clocked in on the rising edge of SCL. Typically data transitions at or after the subsequent falling edge of SCL to provide ample setup time for the next data bit to be ready before the subsequent rising edge of the SCL.

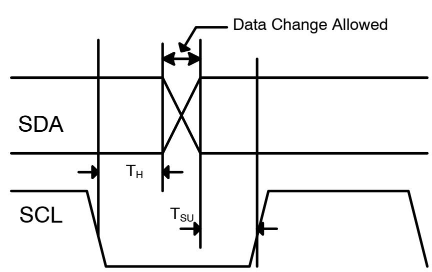


Figure 35. Data Transfer Timing

The idle state of I²C bus is with both SCL and SDA HIGH. Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from High to LOW with SCL HIGH.

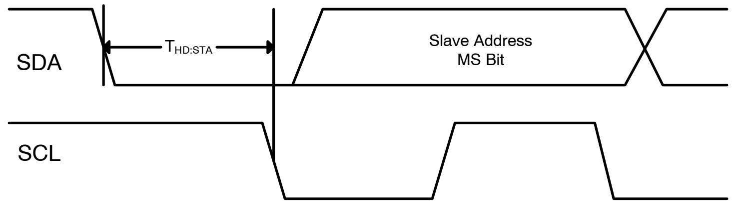


Figure 36. Start Bit Timing

A valid transaction ends with a STOP condition which occurs when SDA transaction from LOW to HIGH while SCL remains HIGH.

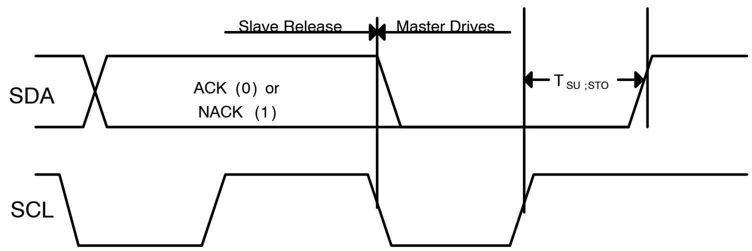


Figure 37. Stop Bit Timing

A REPEATED START condition is functionally equivalent to a STOP condition followed by a START condition. During a read from the IC, the master issues a REPEATED START after sending the register address and before re−sending the slave address. The REPEATED START is a HIGH to LOW transition on SDA while SCL is HIGH.

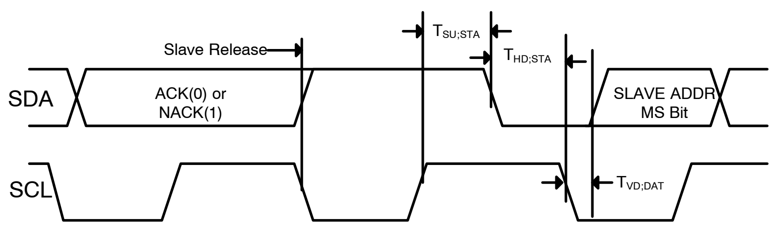


Figure 38. Repeated Start Timing

Read and Write Transactions

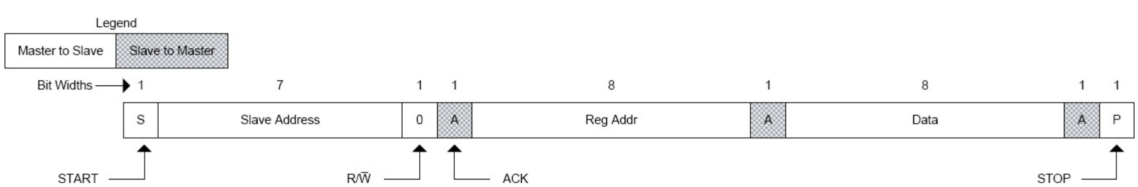


Figure 39. Single Register Write Transaction

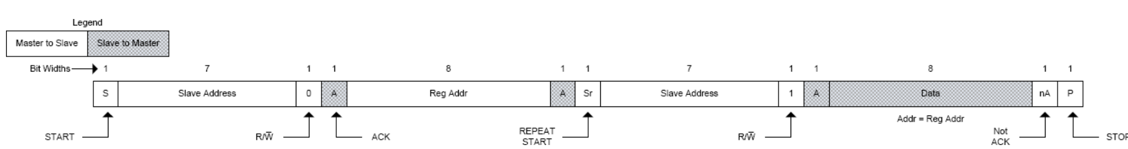


Figure 40. Single Register Read Transaction

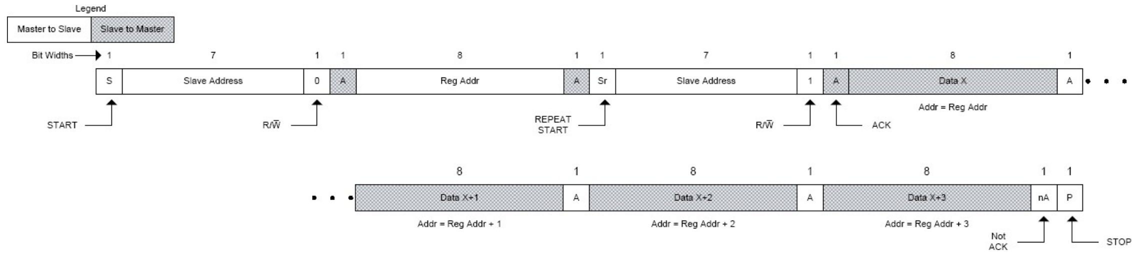


Figure 41. Multiple Register Write Transaction

I²C Hardware Reset

The FAN53745 can be reset and the I²C registers cleared to their default values by pulling SCL low for more than 100 ms.

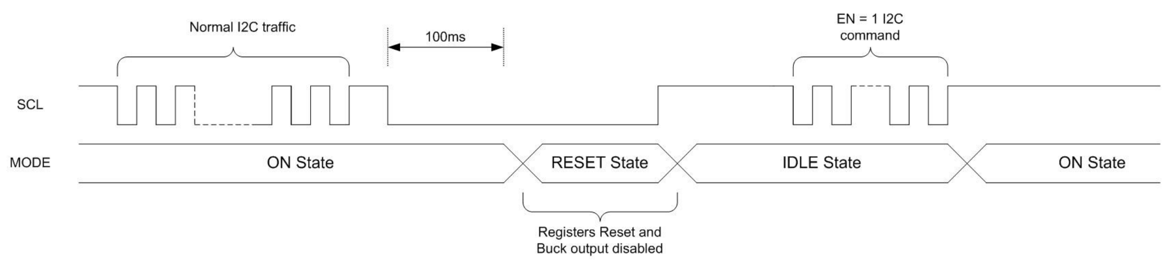


Figure 42. I²C Timing

FUNCTIONAL BEHAVIOR

Defined Behavior

PFM <–> PWM Thresholds

Device will transition into PWM when IOUT reaches IPWM and transition back to PFM when load current falls below IPFM.

REGISTER MAPPING TABLE

Table 3. REGISTER MAPPING

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x00	Product ID_REV	Product ID				Silicon Revision			
0x01	FAULT FLAGS	0			STARTUP TIMEOUT FAULT	UVLO FAULT	OVER TEMP FAULT	SHORT FAULT	ILIM FAULT
0x02	STATUS	0	READY	PASS-THRU OPERATION	PFM_PWM	UVLO	OVER TEMP	VOUT SHORT	CURRENT LIMIT
0x03	MODE	ENABLE	FORCE_PWM	V_I_LIMIT_LOCK	SS TIMEOUT	DVS EN	DVS		
0x04	VSEL	BUCK_VOUT							
0x05	VMIN	VOUT_MIN							
0x06	VMAX	VOUT_MAX							
0x07	SHUT DOWN	0					DISCHARGE SEL		DISCHARGE
0x08	ILIMIT	PFM ILIM				PWM ILIM			
0x09	RESET	SOFT_RESET							

REGISTER DETAILS

Table 4. REGISTER DETAILS – 0X00 PRODUCT ID_REV

0x00 Product ID_REV				Default = 00000001	
Bit	**Name**	**Default**	**Type**	**Description**	
7:4	Product ID	0000	Read	Code represents part number	
				Code	**<<Effect>>**
				0000	–
				0001	FAN53745
				0010	Reserved
				0011	Reserved
				0100	Reserved
				0101	Reserved
				0110	Reserved
				0111	Reserved
				1000	Reserved
				1001	Reserved
				1010	Reserved
				1011	Reserved
				1100	Reserved
				1101	Reserved
				1110	Reserved
				1111	Reserved
3:0	Silicon Revision	0001	Read	Represents silicon revision	
				Code	**Revision**
				0000	Initial Silicon
				0001	Increment register with each iteration
				….	
				….	
				1111	

Table 5. REGISTER DETAILS – 0X01 FAULT FLAGS

0x01 FAULT FLAGS				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:5	UNUSED				
4	STARTUP TIMEOUT FAULT	0	R/CLR	Displays startup timeout fault status. This indicator is latched when startup timeout occurs and causes a fault. The flag is cleared upon read.	
				Code	**Start Up Time−Out Fault**
				0	No startup timeout fault occurred
				1	A startup timeout fault occurred
3	UVLO FAULT	0	R/CLR	Displays UVLO fault status. This indicator is latched when UVLO occurs and causes a fault. The flag is cleared upon read.	
				Code	**Under Voltage Fault Occurance**
				0	No UVLO fault occurred
				1	A UVLO fault occurred
2	OVER TEMP FAULT	0	R/CLR	Displays over temp fault status. This indicator is latched when over temp occurs and causes a fault. The flag is cleared upon read.	
				Code	**Start Up Time−Out Fault**
				0	No over temp fault
				1	An over temp fault occurred
1	SHORT FAULT	0	R/CLR	Displays Vout short fault status. This indicator is latched when Vout short occurs and causes a fault. The flag is cleared upon read.	
				Code	**Vout Short Fault**
				0	The output has not shorted
				1	The output was shorted
0	ILIM FAULT	0	R/CLR	During PWM operation, if the peak current limit is hit continuously for 500 μs, a fault is generated. The flag is cleared upon read.	
				Code	**Vout Short Fault**
				0	The output has not shorted
				1	The output was shorted

Table 6. REGISTER DETAILS – 0X02 STATUS

<table>
<tr><th colspan="4">0x02 STATUS</th><th>Default = 00010000</th></tr>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>7</td><td>UNUSED</td><td></td><td></td><td></td></tr>
<tr><td>6</td><td>READY</td><td>0</td><td>Read</td><td>Reset condition: 0<table><tr><th>Code</th><th>DEVICE READY</th></tr><tr><td>0</td><td>Indicates that either the device is not in Idle mode or that there is a UVLO or over temperature fault.</td></tr><tr><td>1</td><td>Indicates that the device is in IDLE mode; that the input voltage is good and the die temperature is within safe operating range.</td></tr></table></td></tr>
<tr><td>5</td><td>PASS−THRU OPERATION</td><td>0</td><td>Read</td><td>Reset condition: 0
The Pass−Thru Operation bit gives the status of the converter.<table><tr><th>Code</th><th>State of Operation</th></tr><tr><td>0</td><td>Converter functioning in PFM or PWM operation.</td></tr><tr><td>1</td><td>Converter is in pass−thru mode</td></tr></table></td></tr>
<tr><td>4</td><td>PFM_PWM</td><td>1</td><td>Read</td><td>Reset condition: 0
This bit indicates the device is operating in PFM mode or PWM mode.<table><tr><th>Code</th><th>PFM or PWM Switching</th></tr><tr><td>0</td><td>PFM operation</td></tr><tr><td>1</td><td>Device is operating in fixed frequency PWM</td></tr></table></td></tr>
<tr><td>3</td><td>UVLO</td><td>0</td><td>Read</td><td>Displays UVLO comparator status.<table><tr><th>Code</th><th>UVLO Status</th></tr><tr><td>0</td><td>Input voltage is good</td></tr><tr><td>1</td><td>The input voltage is presently below the UVLO threshold</td></tr></table></td></tr>
<tr><td>2</td><td>OVER TEMP</td><td>0</td><td>Read</td><td>Displays over temp comparator status.<table><tr><th>Code</th><th>Die Temperature Status</th></tr><tr><td>0</td><td>The die temperature is safe for operation</td></tr><tr><td>1</td><td>The die is too hot to operate</td></tr></table></td></tr>
<tr><td>1</td><td>VOUT SHORT</td><td>0</td><td>Read</td><td>Displays Vout short comparator status.<table><tr><th>Code</th><th>Output Shorted</th></tr><tr><td>0</td><td>No Vout short fault</td></tr><tr><td>1</td><td>The output is presently shorted or is in a state of recovery after a short</td></tr></table>This bit will be cleared when the buck is disabled.</td></tr>
<tr><td>0</td><td>CURRENT LIMIT</td><td>0</td><td>Read</td><td>Displays over current comparator status.<table><tr><th>Code</th><th>Current Limit Detect</th></tr><tr><td>0</td><td>No over current fault</td></tr><tr><td>1</td><td>The buck converter is presently hitting peak current limit</td></tr></table></td></tr>
</table>

Table 7. REGISTER DETAILS – 0X03 MODE

0x03 MODE				Default = 00001111	
Bit	**Name**	**Default**	**Type**	**Description**	
7	ENABLE2	0	R/W	This register enables/disables the buck regulator. Setting a code 0 shutdowns the device, where as code 1 enables the device.	
				Code	**Effect**
				0	Buck Converter disabled
				1	Buck Converter enabled
6	FORCE_PWM	0	R/W	Forces the part to operate in PWM mode regardless of the load current.	
				Code	**Mode**
				0	Auto (PFM/PWM depending on load current)
				1	Force PWM
5	V_I_LIMIT_LOCK	0	R/W	Reset condition: 0	
				Code	**LOCK**
				0	VMIN, VMAX, PFM and PWM Ilimit levels are not locked.
				1	Locks the minimum (VMIN), Maximum(VMAX) voltages and PFM and PWM current limits that the device can be programmed to.
4	SS TIMEOUT	0	R/W	This register activates/deactivates the soft start time−out timer.	
				Code	**Status of Soft Start Timer**
				0	The converter will continuous attempt to reach output regulation.
				1	A timer is activated when the converter is enabled. If the converter output fails to reach regulation in 2ms, a fault will be declared.
3	DVS EN	1	R/W	Reset condition: 0 This register bit enables/disables the DVS functionality	
				Code	**DVS Enable**
				0	DVS operation is disabled
				1	DVS will be performed per Mode Control register bits 2:0
2:0	DVS	111	R/W	Reset condition: 0 DVS rate control register bits	
				Code	**Voltage Scaling Rate**
				000	0.5 mV/μs
				001	1.0 mV/μs
				010	1.5 mV/μs
				011	2.0 mV/μs
				100	2.5 mV/μs
				101	3.5 mV/μs
				110	5.0 mV/μs
				111	10 mV/μs

Table 8. REGISTER DETAILS – 0X04 VSEL

0x04 SEL				Default = 10111001							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	BUCK_VOUT	10111001	R/W	Sets the buck regulation target voltage.							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	Reserved	40	Reserved	80	2.030	C0	2.670
				01	Reserved	41	Reserved	81	2.040	C1	2.680
				02	Reserved	42	Reserved	82	2.050	C2	2.690
				03	Reserved	43	Reserved	83	2.060	C3	2.700
				04	Reserved	44	Reserved	84	2.070	C4	2.710
				05	Reserved	45	Reserved	85	2.080	C5	2.720
				06	Reserved	46	Reserved	86	2.090	C6	2.730
				07	Reserved	47	Reserved	87	2.100	C7	2.740
				08	Reserved	48	Reserved	88	2.110	C8	2.750
				09	Reserved	49	Reserved	89	2.120	C9	2.760
				0A	Reserved	4A	Reserved	8A	2.130	CA	2.770
				0B	Reserved	4B	1.500 V	8B	2.140	CB	2.780
				0C	Reserved	4C	1.510 V	8C	2.150	CC	2.790
				0D	Reserved	4D	1.520 V	8D	2.160	CD	2.800
				0E	Reserved	4E	1.530 V	8E	2.170	CE	2.810
				0F	Reserved	4F	1.540 V	8F	2.180	CF	2.820
				10	Reserved	50	1.550 V	90	2.190	D0	2.830
				11	Reserved	51	1.560 V	91	2.200	D1	2.840
				12	Reserved	52	1.570 V	92	2.210	D2	2.850
				13	Reserved	53	1.580 V	93	2.220	D3	2.860
				14	Reserved	54	1.590 V	94	2.230	D4	2.870
				15	Reserved	55	1.600 V	95	2.240	D5	2.880
				16	Reserved	56	1.610 V	96	2.250	D6	2.890
				17	Reserved	57	1.620 V	97	2.260	D7	2.900
				18	Reserved	58	1.630 V	98	2.270	D8	2.910
				19	Reserved	59	1.640 V	99	2.280	D9	2.920
				1A	Reserved	5A	1.650 V	9A	2.290	DA	2.930
				1B	Reserved	5B	1.660 V	9B	2.300	DB	2.940
				1C	Reserved	5C	1.670 V	9C	2.310	DC	2.950
				1D	Reserved	5D	1.680 V	9D	2.320	DD	2.960
				1E	Reserved	5E	1.690 V	9E	2.330	DE	2.970
				1F	Reserved	5F	1.700 V	9F	2.340	DF	2.980
				20	Reserved	60	1.710 V	A0	2.350	E0	2.990
				21	Reserved	61	1.720 V	A1	2.360	E1	3.000
				22	Reserved	62	1.730 V	A2	2.370	E2	3.010
				23	Reserved	63	1.740 V	A3	2.380	E3	3.020
				24	Reserved	64	1.750 V	A4	2.390	E4	3.030

Table 8. REGISTER DETAILS – 0X04 VSEL (continued)

0x04 SEL				Default = 10111001							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	BUCK_VOUT	10111001	R/W	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				25	Reserved	65	1.760 V	A5	2.400	E5	3.040
				26	Reserved	66	1.770 V	A6	2.410	E6	3.050
				27	Reserved	67	1.780 V	A7	2.420	E7	3.060
				28	Reserved	68	1.790 V	A8	2.430	E8	3.070
				29	Reserved	69	1.800 V	A9	2.440	E9	3.080
				2A	Reserved	6A	1.810 V	AA	2.450	EA	3.090
				2B	Reserved	6B	1.820 V	AB	2.460	EB	3.100
				2	Reserved	6C	1.830 V	AC	2.470	EC	3.110
				2	Reserved	6D	1.840 V	AD	2.480	ED	3.120
				2	Reserved	6E	1.850 V	AE	2.490	EE	3.130
				2	Reserved	6F	1.860 V	AF	2.500	EF	3.140
				30	Reserved	70	1.870 V	B0	2.510	F0	3.150
				31	Reserved	71	1.880 V	B1	2.520	F1	3.160
				32	Reserved	72	1.890 V	B2	2.530	F2	3.170
				33	Reserved	73	1.900 V	B3	2.540	F3	3.180
				34	Reserved	74	1.910 V	B4	2.550	F4	3.190
				35	Reserved	75	1.920 V	B5	2.560	F5	3.200
				36	Reserved	76	1.930 V	B6	2.570	F6	3.210
				37	Reserved	77	1.940 V	B7	2.580	F7	3.220
				38	Reserved	78	1.950 V	B8	2.590	F8	3.230
				39	Reserved	79	1.960 V	B9	2.600	F9	3.240
				3A	Reserved	7A	1.970 V	BA	2.610	FA	3.250
				3B	Reserved	7B	1.980 V	BB	2.620	FB	3.260
				3C	Reserved	7C	1.990 V	BC	2.630	FC	3.270
				3D	Reserved	7D	2.000 V	BD	2.640	FD	3.280
				3E	Reserved	7E	2.010 V	BE	2.650	FE	3.290
				3F	Reserved	7F	2.020 V	BF	2.660	FF	3.300

Table 9. REGISTER DETAILS – 0X05 VMIN

0x05 VMIN				Default = 01001011							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VOUT_MIN	01001011	R/W	Sets the minimum voltage the buck can be programmed to.							
				Hex	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				00	Reserved	40	Reserved	80	2.030	C0	2.670
				01	Reserved	41	Reserved	81	2.040	C1	2.680
				02	Reserved	42	Reserved	82	2.050	C2	2.690
				03	Reserved	43	Reserved	83	2.060	C3	2.700
				04	Reserved	44	Reserved	84	2.070	C4	2.710
				05	Reserved	45	Reserved	85	2.080	C5	2.720
				06	Reserved	46	Reserved	86	2.090	C6	2.730
				07	Reserved	47	Reserved	87	2.100	C7	2.740
				08	Reserved	48	Reserved	88	2.110	C8	2.750
				09	Reserved	49	Reserved	89	2.120	C9	2.760
				0A	Reserved	4A	Reserved	8A	2.130	CA	2.770
				0B	Reserved	4B	1.500 V	8B	2.140	CB	2.780
				0C	Reserved	4C	1.510 V	8C	2.150	CC	2.790
				0D	Reserved	4D	1.520 V	8D	2.160	CD	2.800
				0E	Reserved	4E	1.530 V	8E	2.170	CE	2.810
				0F	Reserved	4F	1.540 V	8F	2.180	CF	2.820
				10	Reserved	50	1.550 V	90	2.190	D0	2.830
				11	Reserved	51	1.560 V	91	2.200	D1	2.840
				12	Reserved	52	1.570 V	92	2.210	D2	2.850
				13	Reserved	53	1.580 V	93	2.220	D3	2.860
				14	Reserved	54	1.590 V	94	2.230	D4	2.870
				15	Reserved	55	1.600 V	95	2.240	D5	2.880
				16	Reserved	56	1.610 V	96	2.250	D6	2.890
				17	Reserved	57	1.620 V	97	2.260	D7	2.900
				18	Reserved	58	1.630 V	98	2.270	D8	2.910
				19	Reserved	59	1.640 V	99	2.280	D9	2.920
				1A	Reserved	5A	1.650 V	9A	2.290	DA	2.930
				1B	Reserved	5B	1.660 V	9B	2.300	DB	2.940
				1C	Reserved	5C	1.670 V	9C	2.310	DC	2.950
				1D	Reserved	5D	1.680 V	9D	2.320	DD	2.960
				1E	Reserved	5E	1.690 V	9E	2.330	DE	2.970
				1F	Reserved	5F	1.700 V	9F	2.340	DF	2.980
				20	Reserved	60	1.710 V	A0	2.350	E0	2.990
				21	Reserved	61	1.720 V	A1	2.360	E1	3.000
				22	Reserved	62	1.730 V	A2	2.370	E2	3.010
				23	Reserved	63	1.740 V	A3	2.380	E3	3.020
				24	Reserved	64	1.750 V	A4	2.390	E4	3.030

Table 9. REGISTER DETAILS – 0X05 VMIN (continued)

0x05 VMIN				Default = 01001011							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VOUT_MIN	01001011	R/W	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				25	Reserved	65	1.760 V	A5	2.400	E5	3.040
				26	Reserved	66	1.770 V	A6	2.410	E6	3.050
				27	Reserved	67	1.780 V	A7	2.420	E7	3.060
				28	Reserved	68	1.790 V	A8	2.430	E8	3.070
				29	Reserved	69	1.800 V	A9	2.440	E9	3.080
				2A	Reserved	6A	1.810 V	AA	2.450	EA	3.090
				2B	Reserved	6B	1.820 V	AB	2.460	EB	3.100
				2	Reserved	6C	1.830 V	AC	2.470	EC	3.110
				2	Reserved	6D	1.840 V	AD	2.480	ED	3.120
				2	Reserved	6E	1.850 V	AE	2.490	EE	3.130
				2	Reserved	6F	1.860 V	AF	2.500	EF	3.140
				30	Reserved	70	1.870 V	B0	2.510	F0	3.150
				31	Reserved	71	1.880 V	B1	2.520	F1	3.160
				32	Reserved	72	1.890 V	B2	2.530	F2	3.170
				33	Reserved	73	1.900 V	B3	2.540	F3	3.180
				34	Reserved	74	1.910 V	B4	2.550	F4	3.190
				35	Reserved	75	1.920 V	B5	2.560	F5	3.200
				36	Reserved	76	1.930 V	B6	2.570	F6	3.210
				37	Reserved	77	1.940 V	B7	2.580	F7	3.220
				38	Reserved	78	1.950 V	B8	2.590	F8	3.230
				39	Reserved	79	1.960 V	B9	2.600	F9	3.240
				3A	Reserved	7A	1.970 V	BA	2.610	FA	3.250
				3B	Reserved	7B	1.980 V	BB	2.620	FB	3.260
				3C	Reserved	7C	1.990 V	BC	2.630	FC	3.270
				3D	Reserved	7D	2.000 V	BD	2.640	FD	3.280
				3E	Reserved	7E	2.010 V	BE	2.650	FE	3.290
				3F	Reserved	7F	2.020 V	BF	2.660	FF	3.300

Table 10. REGISTER DETAILS – 0X06 MAX

0x06 MAX				Default = 11111111
Bit	**Name**	**Default**	**Type**	**Description**
7:0	VOUT_MAX	11111111	R/W	Sets the maximum voltage the buck can be programmed to.

Hex	VOUT	Hex	VOUT	Hex	VOUT	Hex	VOUT
00	Reserved	40	Reserved	80	2.030	C0	2.670
01	Reserved	41	Reserved	81	2.040	C1	2.680
02	Reserved	42	Reserved	82	2.050	C2	2.690
03	Reserved	43	Reserved	83	2.060	C3	2.700
04	Reserved	44	Reserved	84	2.070	C4	2.710
05	Reserved	45	Reserved	85	2.080	C5	2.720
06	Reserved	46	Reserved	86	2.090	C6	2.730
07	Reserved	47	Reserved	87	2.100	C7	2.740
08	Reserved	48	Reserved	88	2.110	C8	2.750
09	Reserved	49	Reserved	89	2.120	C9	2.760
0A	Reserved	4A	Reserved	8A	2.130	CA	2.770
0B	Reserved	4B	1.500 V	8B	2.140	CB	2.780
0C	Reserved	4C	1.510 V	8C	2.150	CC	2.790
0D	Reserved	4D	1.520 V	8D	2.160	CD	2.800
0E	Reserved	4E	1.530 V	8E	2.170	CE	2.810
0F	Reserved	4F	1.540 V	8F	2.180	CF	2.820
10	Reserved	50	1.550 V	90	2.190	D0	2.830
11	Reserved	51	1.560 V	91	2.200	D1	2.840
12	Reserved	52	1.570 V	92	2.210	D2	2.850
13	Reserved	53	1.580 V	93	2.220	D3	2.860
14	Reserved	54	1.590 V	94	2.230	D4	2.870
15	Reserved	55	1.600 V	95	2.240	D5	2.880
16	Reserved	56	1.610 V	96	2.250	D6	2.890
17	Reserved	57	1.620 V	97	2.260	D7	2.900
18	Reserved	58	1.630 V	98	2.270	D8	2.910
19	Reserved	59	1.640 V	99	2.280	D9	2.920
1A	Reserved	5A	1.650 V	9A	2.290	DA	2.930
1B	Reserved	5B	1.660 V	9B	2.300	DB	2.940
1C	Reserved	5C	1.670 V	9C	2.310	DC	2.950
1D	Reserved	5D	1.680 V	9D	2.320	DD	2.960
1E	Reserved	5E	1.690 V	9E	2.330	DE	2.970
1F	Reserved	5F	1.700 V	9F	2.340	DF	2.980
20	Reserved	60	1.710 V	A0	2.350	E0	2.990
21	Reserved	61	1.720 V	A1	2.360	E1	3.000
22	Reserved	62	1.730 V	A2	2.370	E2	3.010
23	Reserved	63	1.740 V	A3	2.380	E3	3.020
24	Reserved	64	1.750 V	A4	2.390	E4	3.030

Table 10. REGISTER DETAILS – 0X06 MAX (continued)

0x06 MAX				Default = 11111111							
Bit	**Name**	**Default**	**Type**	**Description**							
7:0	VOUT_MAX	11111111	R/W	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**	**Hex**	**VOUT**
				25	Reserved	65	1.760 V	A5	2.400	E5	3.040
				26	Reserved	66	1.770 V	A6	2.410	E6	3.050
				27	Reserved	67	1.780 V	A7	2.420	E7	3.060
				28	Reserved	68	1.790 V	A8	2.430	E8	3.070
				29	Reserved	69	1.800 V	A9	2.440	E9	3.080
				2A	Reserved	6A	1.810 V	AA	2.450	EA	3.090
				2B	Reserved	6B	1.820 V	AB	2.460	EB	3.100
				2	Reserved	6C	1.830 V	AC	2.470	EC	3.110
				2	Reserved	6D	1.840 V	AD	2.480	ED	3.120
				2	Reserved	6E	1.850 V	AE	2.490	EE	3.130
				2	Reserved	6F	1.860 V	AF	2.500	EF	3.140
				30	Reserved	70	1.870 V	B0	2.510	F0	3.150
				31	Reserved	71	1.880 V	B1	2.520	F1	3.160
				32	Reserved	72	1.890 V	B2	2.530	F2	3.170
				33	Reserved	73	1.900 V	B3	2.540	F3	3.180
				34	Reserved	74	1.910 V	B4	2.550	F4	3.190
				35	Reserved	75	1.920 V	B5	2.560	F5	3.200
				36	Reserved	76	1.930 V	B6	2.570	F6	3.210
				37	Reserved	77	1.940 V	B7	2.580	F7	3.220
				38	Reserved	78	1.950 V	B8	2.590	F8	3.230
				39	Reserved	79	1.960 V	B9	2.600	F9	3.240
				3A	Reserved	7A	1.970 V	BA	2.610	FA	3.250
				3B	Reserved	7B	1.980 V	BB	2.620	FB	3.260
				3C	Reserved	7C	1.990 V	BC	2.630	FC	3.270
				3D	Reserved	7D	2.000 V	BD	2.640	FD	3.280
				3E	Reserved	7E	2.010 V	BE	2.650	FE	3.290
				3F	Reserved	7F	2.020 V	BF	2.660	FF	3.300

Table 11. REGISTER DETAILS – 0X07 SHUTOWN

0x07 SHUTDOWN				Default = 0000100	
Bit	**Name**	**Default**	**Type**	**Description**	
7:3	UNUSED				
2:1	DISCHARGE SEL	10	R/W	This register sets the strength of the pulldown resistor.	
				Code	**Strength of Pulldown**
				00	OPEN
				01	200 Ω
				10	100 Ω
				11	50 Ω
0	DISCHARGE	0	R/W	This register activates/deactivates the internal pulldown resistor. Setting to Code 1, the pulldown is active when ENABLE goes from 1 to 0 and on any negative V_{OUT} transitions.	
				Code	**Status of Pulldown**
				0	Pulldown not used (OFF)
				1	Pulldown active during transition

Table 12. REGISTER DETAILS – 0X08 ILIMIT

0x08 ILIMIT				Default = 10101101	
Bit	**Name**	**Default**	**Type**	**Description**	
7:4	PFM ILIM	1010	R/W	Reset condition: 0	
				Sets the open loop peak PFM current limit	
				Code	**PFM Peak Current Limit**
				0000	500 mA
				0001	555 mA
				0010	610 mA
				0011	665 mA
				0100	720 mA
				0101	775 mA
				0110	830 mA
				0111	885 mA
				1000	940 mA
				1001	995 mA
				1010	1050 mA
				1011	1105 mA
				1100	1160 mA
				1101	1215 mA
				1110	1270 mA
				1111	1325 mA
3:0	PWM ILIM	1101	R/W	Sets the open loop peak inductor current limit thresholds. The Range is from 440 mA to 2090 mA in 110 mA steps.	
				Code	**PWM Peak Current Limit**
				0000	440 mA
				0001	550 mA
				0010	660 mA
				0011	770 mA
				0100	880 mA
				0101	990 mA
				0110	1100 mA
				0111	1210 mA
				1000	1320 mA
				1001	1430 mA
				1010	1540 mA
				1011	1650 mA
				1100	1760 mA
				1101	1870 mA
				1110	1980 mA
				1111	2090 mA

Table 13. REGISTER DETAILS – 0X09 RESET

0x09 RESET				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	SOFT_RESET	00000000	Write	The software reset register allows all I^2C settings to be reverted to POR defaults when 0x45h code is written to it.

Table 14. PRIMARY COMPONENTS

Component	Manufacturer	Part Number	Description	Case Size	Voltage Rating
C_{IN}	Murata	GRM035R60J475ME15D	4.7 μF	0201/0603 (0.6 mm x 0.3 mm)	6.3 V
L	Samsung	CIGT201208EHR47MNE	0.47 μH I_{SAT} = 4.3 A I_{RAT} = 3.9 A R_{DC} = 31 Ω	0805/2012 (2 mm x 1.2 mm)	–
C_{OUT}	Murata	GRM155R60J106ME47D	2x 10 μF	0402/1005 (1.0 mm x 0.5 mm)	6.3 V

APPLICATION GUIDELINES

Input Capacitor Considerations

The 2.2 μF ceramic 0402 (1005 metric) input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Inductor Considerations

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects average current limit, the PWM−to−PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx (V_{OUT}/V_{IN}) \cdot ((V_{IN} - V_{OUT}) / (L \cdot fsw)) \quad \text{(eq. 1)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \Delta I/2 \quad \text{(eq. 2)}$$

The FAN53745 is optimized for operation with L = 0.47 μH. The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. It is recommended to select an inductor where its saturation current is above the $I_{LIM(PK)}$ value.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but because ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = SQRT\,(I_{OUT(DC)}{}^2 + \Delta I^2/12) \quad \text{(eq. 3)}$$

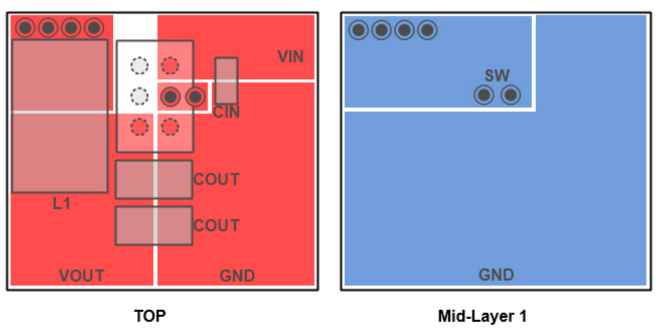
The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Output Capacitor Considerations

FAN53745 uses two 10 μF 0402 (1005 metric) for an output capacitor. The effective capacitor of ceramic capacitors decrease as the bias voltage increases. To overcome this increasing the output capacitor has no effect on loop stability and therefore the COUT can be increased to reduce the output voltage ripple or to improve transient response. Output voltage ripple is defined as:

$$\Delta V_{OUT} = \Delta I_L \cdot [(f_{SW} \cdot C_{OUT} \cdot ESR^2/(2 \cdot D \cdot (1 - D))) + (1/(8 \cdot f_{SW} \cdot C_{OUT}))] \quad \text{(eq. 4)}$$

Recommended Layout



NOTES
CIN = 0201 = 0.6mm x 0.3mm
L = 2012 = 2mm x 1.25mm
COUT = 0402 = 1mm x 0.5mm
Fan53745 = 1.5mm x 0.94mm

Layout Guideline
The Recommended Component placement and routing is illustrated below. Components are placed on the top PCB layer with top copper routing shown in RED. The SW pin is routed directly to L1 using Mid-Layer_1 with copper routing shown in BLUE.

For thermal reasons, it is recommended to maximize the pour area for all planes other than SW. The ground pour should be set to fill all available PCB surface area, and tied to internal layers with a cluster of thermal via.

Figure 43. Recommended Placement

Layout Considerations

To minimize spikes at V_{OUT}, C_{OUT} must be placed as close as possible to PGND and VOUT, as shown in

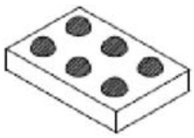
For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal via.

PACKAGE INFORMATION

Table 15. PACKAGE DIMENSIONS

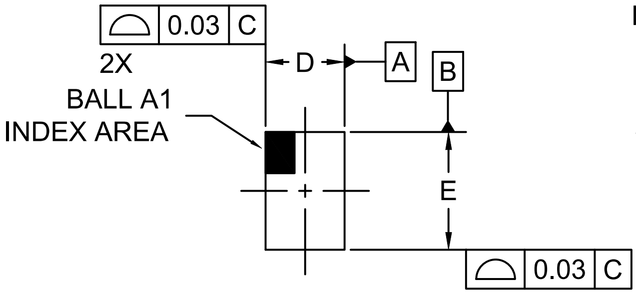
Product	D	E
FAN53745	1.50 mm +/− 30 μm	0.94 mm +/− 30 μm

1. Typical height to be 0.55 mm.
2. Dimensions shown in the table below are approximations.



WLCSP6, 0.94x1.50x0.581
CASE 567WU
ISSUE O

DATE 17 JUL 2018

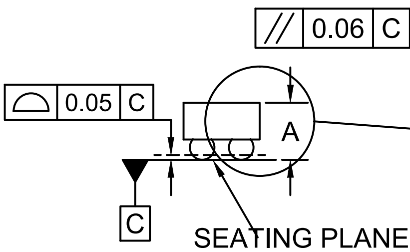


TOP VIEW

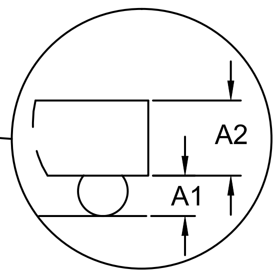
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

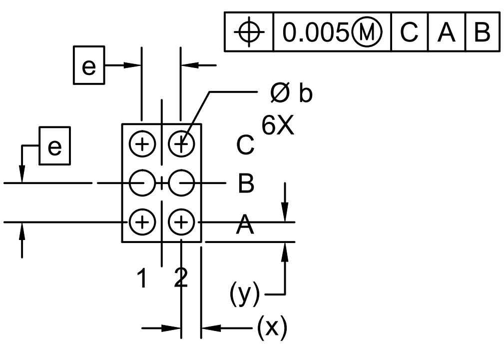
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.543	0.581	0.619
A1	0.185	0.203	0.221
A2	0.358	0.378	0.398
b	0.240	0.260	0.280
D	0.910	0.940	0.970
E	1.470	1.500	1.530
e	0.40 BSC		
x	0.255	0.270	0.285
y	0.335	0.350	0.365



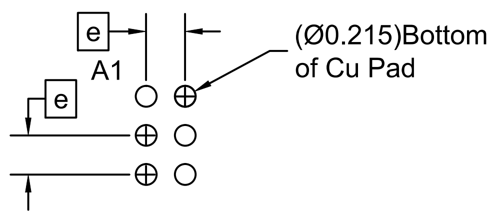
SIDE VIEW



DETAIL A



BOTTOM VIEW



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