NCP6360

Mini Buck Converter for RF Power Amplifiers

The NCP6360, a PWM synchronous step−down DC−to−DC converter, is optimized for supplying RF Power Amplifiers (PAs) used into 3G/4G wireless systems (Mobile/ Smart Phones, Phablets, Tablets, ...) powered by single−cell Lithium−Ion batteries. The device is able to deliver up to 800 mA. The output voltage is monitorable from 0.6 V to 3.4 V by an analog control pin VCON. The analog control allows dynamically optimizing the RF Power Amplifier's efficiency during a communication while for example in roaming situation with as a benefit an increased talk time. Also at light load for optimizing the DC−to−DC converter efficiency, the NCP6360 enters automatically in a PFM mode and operates in a slower switching frequency corresponding to a reduced quiescent current in regards to the PWM mode for which the device operates at a switching frequency of 6 MHz. Synchronous rectification offers improved system efficiency. The NCP6360 is available in a space saving, low profile 1.5 x 1.0 mm CSP−6 package.

Features

- Input Voltage from 2.7 V to 5.5 V for Battery Powered Applications
- Adjustable Output Voltage (0.6 V to 3.4 V)
- 6 MHz Switching Frequency
- Uses 470 nH Inductor and 4.7 μF Capacitor for Optimized Footprint and Solution Thickness
- PFM /PWM Automatic Mode Change for High Efficiency
- Low 30 μA Quiescent Current
- Thermal Protections to Avoid Damage of the IC
- Small 1.5 x 1.0 mm / 0.5 mm Pitch CSP Package
- This is a Pb−Free Device

Typical Applications

- 3G / 4G Wireless Systems, Smart Phones, Phablets and Webtablets

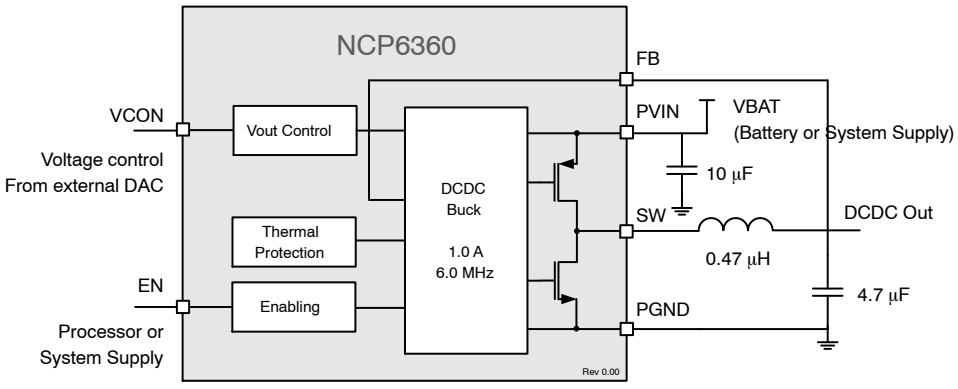

Figure 1. NCP6360 Block Diagram

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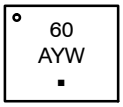
WLCSP6, 1.00x1.50
CASE 568AN

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 16 of this data sheet.

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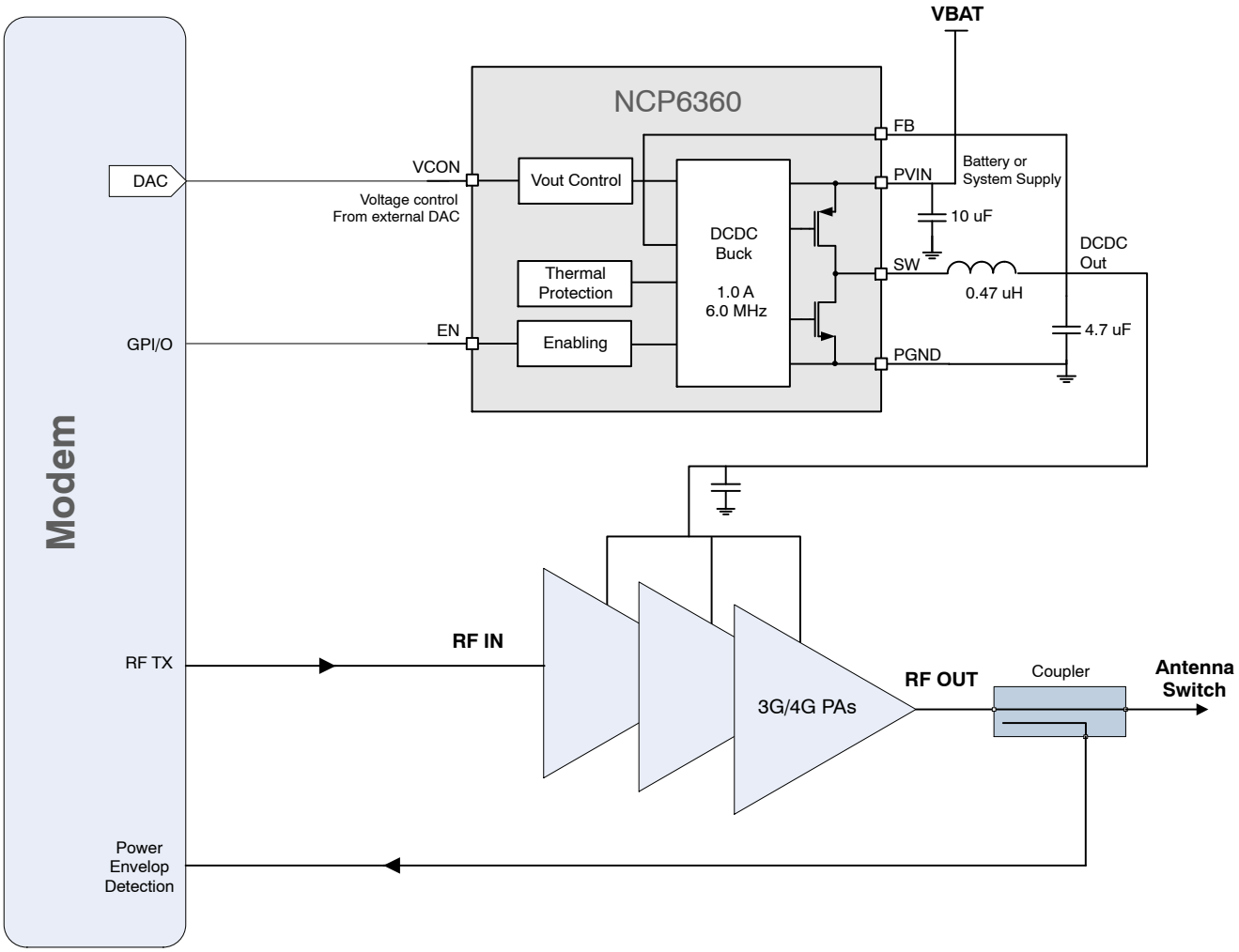


Figure 2. Typical Application

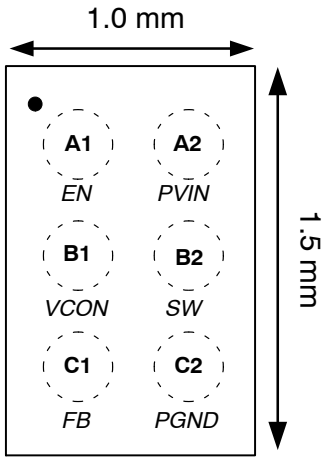


Figure 3. Pin Out (Top View)

PIN FUNCTION DESCRIPTION

Pin	Name	Type	Description
A1	EN	Input	Enable Control. Active high will enable the part. There is an internal pull down resistor on this pin.
A2	PV_{IN}	Power Input	DC−DC Power Supply. This pin must be decoupled to ground by a 10 μF and 1 μF ceramic capacitors. These capacitors should be placed as close as possible to this pin.
B1	VCON	Input	Voltage Control Analog Input. This pin controls the output voltage. It must be shielded to protect against noise. V_{OUT} = 2.5 x VCON
B2	SW	Power Output	DC−DC Switch Power. This pin connects the power transistors to one end of the inductor. Typical application (6 MHz) uses 0.470 μH inductor; refer to application section for more information.
C1	FB	Power Input	DC−DC Feedback Voltage. Must be connected to the output capacitor positive terminal. This is the input of the error amplifier.
C2	PGND	Ground	DC−DC Power Ground. This pin is the power ground and carries high switching current. High quality ground must be provided to prevent noise spikes. To avoid high−density current flow in a limited PCB track, a local ground plane that connects all power grounds together is recommended.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Analog and power pins: PV_{IN}, SW, FB		V_A	−0.3 to + 7.0	V
VCON pin		V_{VCON}	−0.3 to + V_A + 0.3 ≤ +7.0	V
Digital pin: EN: (Note 3)	Input Voltage Input Current	V_{DG} I_{DG}	−0.3 to V_A +0.3 ≤ 7.0 10	V mA
Operating Ambient Temperature Range		T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 1)		T_J	−40 to +125	°C
Storage Temperature Range		T_{STG}	−65 to + 150	°C
Maximum Junction Temperature		T_{JMAX}	−40 to +150	°C
Thermal Resistance Junction−to−Ambient (Note 2)		$R_{\theta JA}$	85	°C/W
Electrostatic Discharge (ESD) Protection, (Note 3)	Human Body Model Charged Device Model	HBM CDM	2.0 1.5	kV
Moisture Sensitivity (Note 4)		MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The thermal shutdown set to 165°C (typical) avoids potential irreversible damage on the device due to power dissipation.
2. The Junction−to−Ambient thermal resistance is a function of Printed Circuit Board (PCB) layout and application. This data is measured using 4−layer PCBs (2s2p). For a given ambient temperature T_A it has to be pay attention to not exceed the max junction temperature T_{JMAX}.
3. Human Body Model per JESD22−A114, Charge Device Model per JESD22−C101.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PV_{IN}	Power Supply (Note 5)		2.7		5.5	V
L	Inductor for DCDC converter (Note 6)	F = 6 MHz		0.47		μH
Co	Output Capacitor for DCDC Converter (Note 6)	F = 6 MHz, L = 0.47 μH	4.7	–	33	μF
Co	Output Capacitor for DCDC Converter (Note 6)	F = 6 MHz, L = 0.33 μH	33	–	220	μF
Cin	Input Capacitor for DCDC Converter (Note 6)		4.7	10		μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Operation above 5.5 V input voltage for extended period may affect device reliability.
6. Including de−ratings (refer to application information section of this document for further details)

ELECTRICAL CHARACTERISTICS

Min and Max Limits apply for T_J up to +125°C unless otherwise specified. PV_{IN} = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and default configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY CURRENT: PIN PV_{IN}						
I_Q	Operating quiescent current	DCDC on – no load – no switching, EN = High T_A = up to +85°C PVIN = 2.7 V to 5.5 V		30	50	μA
I_{SLEEP}	Product sleep mode current	PV_{IN} = 5.5 V V_{CON} < 0.1 V, EN = High T_A = up to +85°C		25	60	μA
I_{OFF}	Product off current	EN = Low PV_{IN} = 4.6 V T_A = up to +85°C		0.7	2.0	μA
DCDC CONVERTER						
PV_{IN}	Input Voltage Range (Note 7)		2.7		5.5	V
V_{OUT_MIN}	Minimum Output Voltage (Note 8)	V_{CON} = 0.24 V	0.55	0.6	0.65	V
V_{OUT_MAX}	Maximum Output Voltage (Note 8)	V_{CON} = 1.36 V	3.30	3.4	3.50	V
Gain	V_{CON} to V_{OUT} Gain (Note 10)			2.5		V/V
V_{OUT_ACC}	V_{OUT} Accuracy (Note 10)	Ideal = 2.5 x V_{CON}	–50 –3		+50 +3	mV %
F_{SW}	Switching Frequency (Note 9)		5.4	6.0	6.6	MHz
R_{ONHS}	P−Channel MOSFET On Resistance	From PV_{IN} to SW		168		mΩ
R_{ONLS}	N−Channel MOSFET On Resistance	From SW1 to PGND		78		mΩ
I_{PKHS}	Peak Inductor Current PMOS			1.5		A
DC_{MAX}	Maximum Duty Cycle (Note 10)			100		%
η	Efficiency (Note 10)	PV_{IN} = 3.6 V, V_{OUT} = 0.8 V I_{OUT} = 10 mA, PFM mode		82		%
		PV_{IN} = 3.6 V, V_{OUT} = 1.8 V I_{OUT} = 300 mA, PWM mode		90		%
		PV_{IN} = 3.9 V, V_{OUT} = 3.3 V I_{OUT} = 300 mA, PWM mode		94		%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Operation above 5.5 V input voltage for extended periods may affect device reliability.
8. Device tested under closed-loop conditions at PVIN = 4.0 V with VOUT_MIN and VOUT_MAX in line with VOUT accuracy specification.
9. Tested at 6 MHz / 48.
10. Guaranteed by design and characterized.

ELECTRICAL CHARACTERISTICS

Min and Max Limits apply for T_J up to +125°C unless otherwise specified. PV_{IN} = 3.6 V (Unless otherwise noted). Typical values are referenced to T_A = + 25°C and default configuration

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DCDC CONVERTER						
$LINE_{TR}$	Line Transient Response (Note 10)	PV_{IN} = 3.6 V to 4.2 V I_{OUT} = 100 mA, V_{OUT} = 0.8 V $T_R = T_F$ = 10 μs		50		mV_{pk}
$LOAD_{TR}$	Load Transient Response (Note 10)	PV_{IN} = 3.1 V / 3.6 V / 4.5 V I_{OUT} = 50 to 150 mA $T_R = T_F$ = 0.1 μs		50		mV_{pk}
EN						
V_{IH}	Positive Going Input High Voltage Threshold		1.1			V
V_{IL}	Negative Going Input Low Voltage Threshold				0.4	V
TOTAL DEVICE						
I_{OUTMAX}	PWM mode (Note 10)		800			mA
T_{VCON}	V_{OUT} step rise time from 0.6 V to 3.4 V to reach 3.26 V (Note 10)	PV_{IN} = 3.6 V, V_{OUT} = 0.6 V to 3.4 V, C_{OUT} = 4.7 μF, R_L = 10 Ω, T_{R_VCON} < 1 μs			25	μs
	V_{OUT} step fall time from 3.4 V to 0.6 V to reach 0.74 V (Note 10)	PV_{IN} = 3.6 V, V_{OUT} = 3.4 V to 0.6 V, C_{OUT} = 4.7 μF, R_L = 10 Ω, T_{F_VCON} < 1 μs			25	μs
T_{START}	Soft−Start Time (Time from EN transitions from Low to High to 90% of Output Voltage)	PV_{IN} = 4.2 V, C_{OUT} = 4.7 μF, V_{OUT} = 3.4 V, no load		100	140	μs
T_{SP_en}	Sleep mode Enter Time (Note 10)	Vcon < 75 mV		4.0		μs
T_{SP_ex}	Sleep mode Exit Time (Note 10)	Vcon > 75 mV		5.0		μs
V_{UVLO}	Under Voltage Lockout	PV_{IN} falling		2.35	2.5	V
V_{UVLOH}	Under Voltage Lockout Hysteresis	PV_{IN} rising − PV_{IN} falling		100		mV
T_{SD}	Thermal Shut Down Protection (Note 10)			155		°C
T_{SDH}	Thermal Shut Down Hysteresis (Note 10)			35		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Operation above 5.5 V input voltage for extended periods may affect device reliability.
8. Device tested under closed-loop conditions at PVIN = 4.0 V with VOUT_MIN and VOUT_MAX in line with VOUT accuracy specification.
9. Tested at 6 MHz / 48.
10. Guaranteed by design and characterized.

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

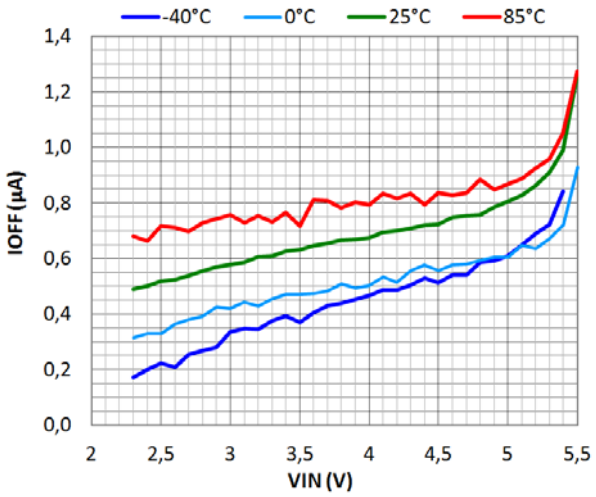


Figure 4. Shutdown Current vs Input Voltage (EN = Low, VCON = 0 V)

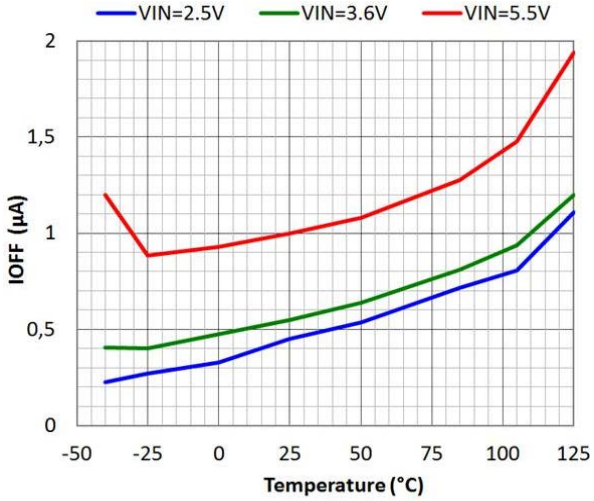


Figure 5. Shutdown Current vs Temperature (EN = Low, VCON = 0 V)

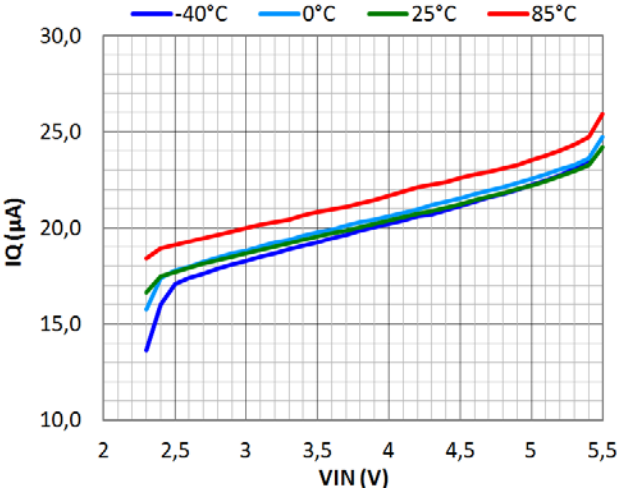


Figure 6. Sleep Mode Current vs Input Voltage (EN = High, VCON = 0 V, V_{OUT} = 0 V)

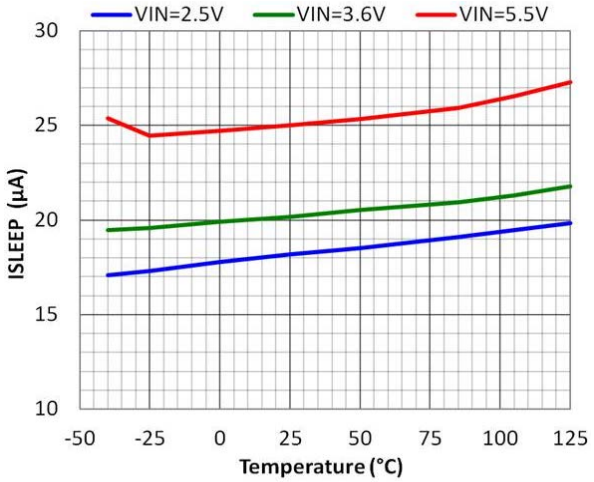


Figure 7. Sleep Mode Current vs. Temperature (EN = High, VCON = 0 V, V_{OUT} = 0 V)

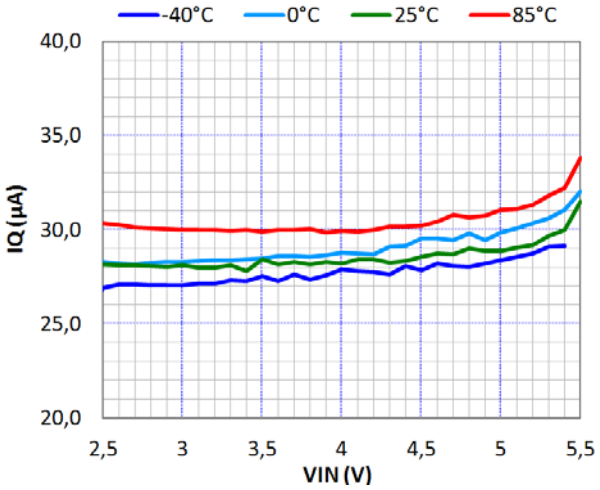


Figure 8. Quiescent Current vs Input Voltage (EN = High, VCON = 0.8 V, V_{OUT} = 2 V, no load)

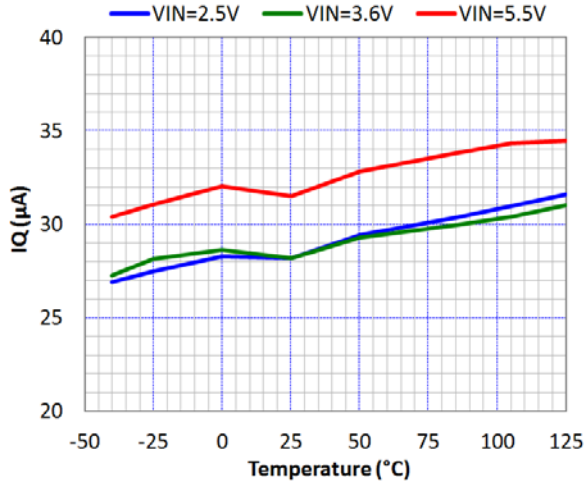


Figure 9. Quiescent Current vs Temperature (T_A) (EN = High, VCON = 0.8 V, V_{OUT} = 2 V, no load)

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

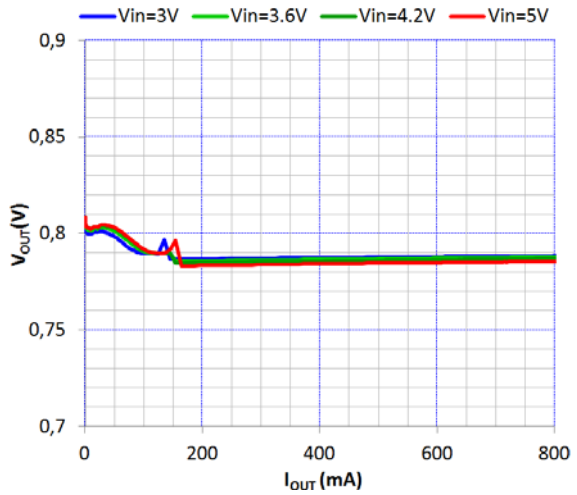


Figure 10. V_{OUT} Accuracy vs. Output Current vs. PV_{IN} @ 25°C, V_{OUT} = 0.8 V

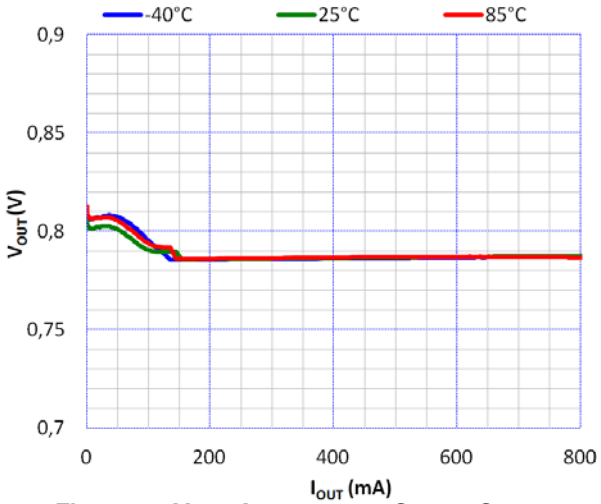


Figure 11. V_{OUT} Accuracy vs. Output Current vs. Temperature PV_{IN} = 3.6 V, V_{OUT} = 0.8 V

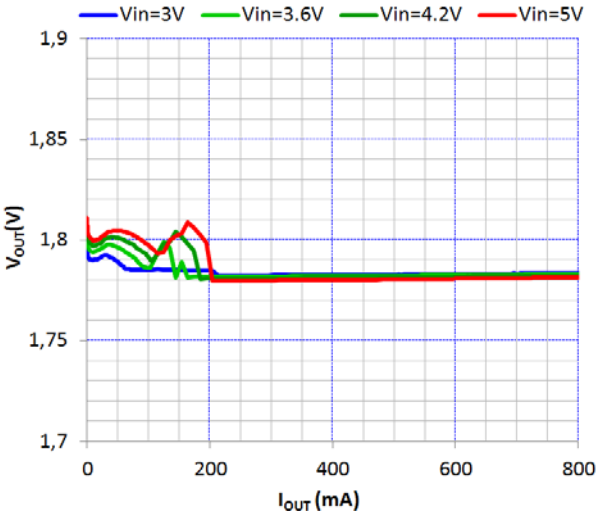


Figure 12. V_{OUT} Accuracy vs. Output Current vs. PV_{IN} @ 25°C, V_{OUT} = 1.8 V

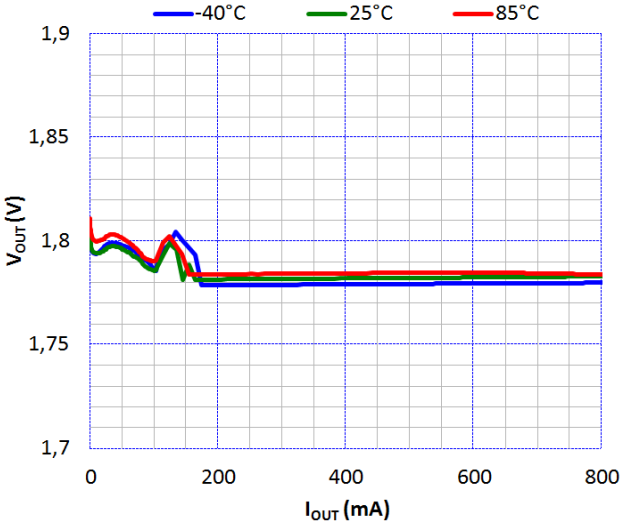


Figure 13. V_{OUT} Accuracy vs. Output Current vs. Temperature PV_{IN} = 3.6 V, V_{OUT} = 1.8 V

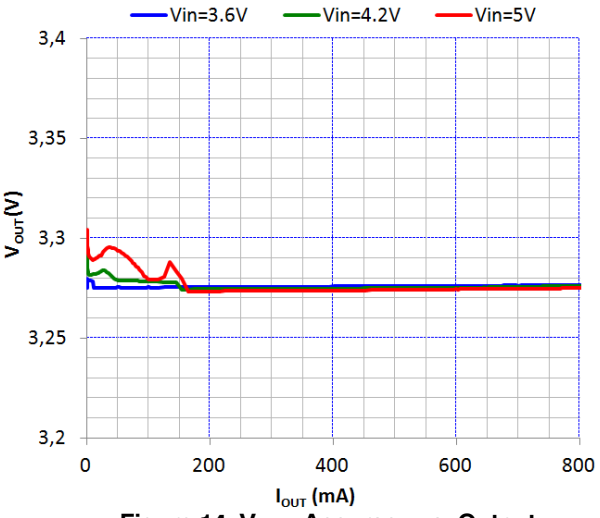


Figure 14. V_{OUT} Accuracy vs. Output Current vs. PV_{IN} @ 25°C, V_{OUT} = 3.3 V

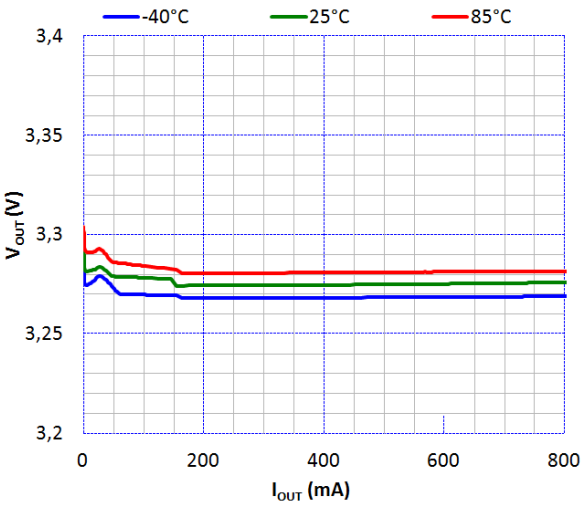


Figure 15. V_{OUT} Accuracy vs. Output Current vs. Temperature PV_{IN} = 4.2 V, V_{OUT} = 3.3 V

TYPICAL OPERATING CHARACTERISTIC

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

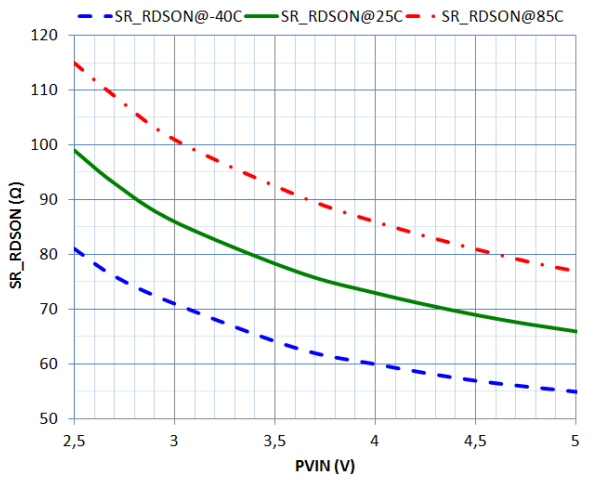


Figure 16. NMOS $R_{DS(on)}$ vs. PV_{IN}

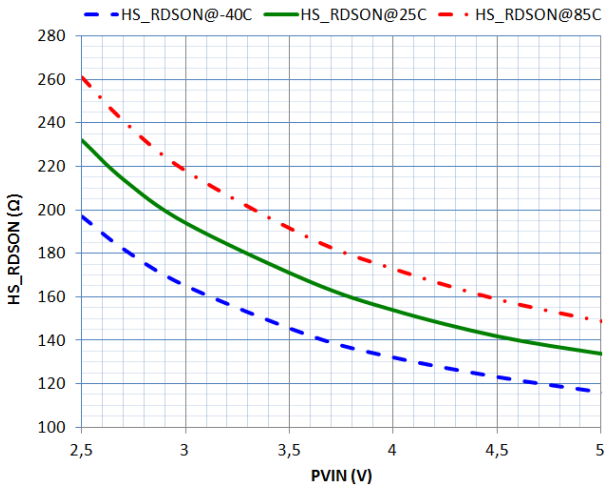


Figure 17. PMOS $R_{DS(on)}$ vs. PV_{IN}

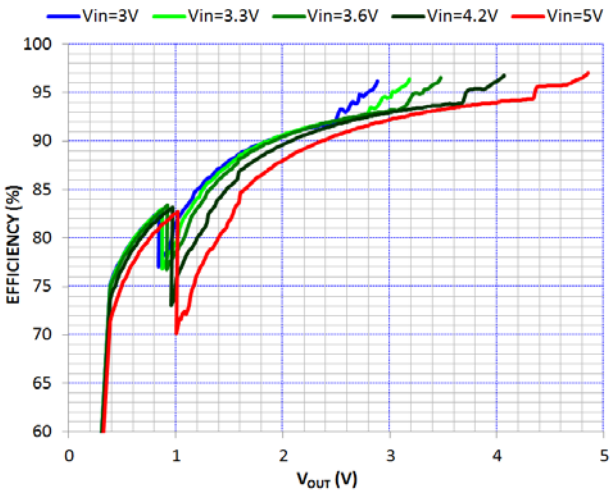


Figure 18. Efficiency vs. V_{OUT}
R_L = 6 Ω, Temp = 25°C

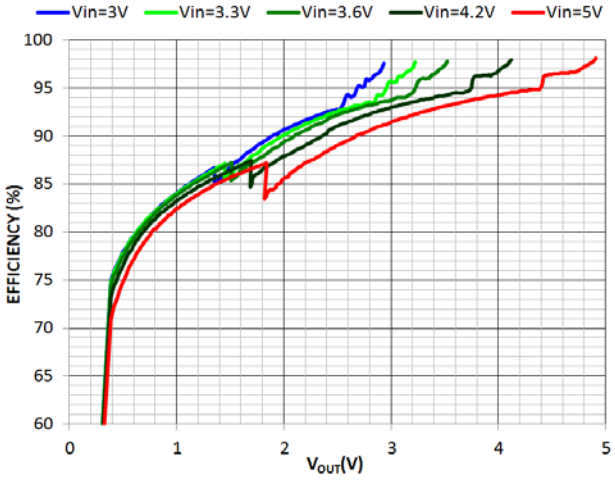


Figure 19. Efficiency vs. V_{OUT}
R_L = 10 Ω, Temp = 25°C

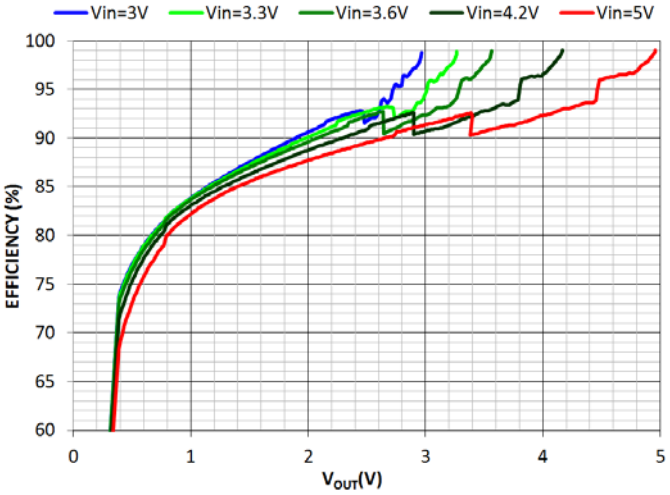


Figure 20. Efficiency vs. V_{OUT}
R_L = 22 Ω, Temp = 25°C

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

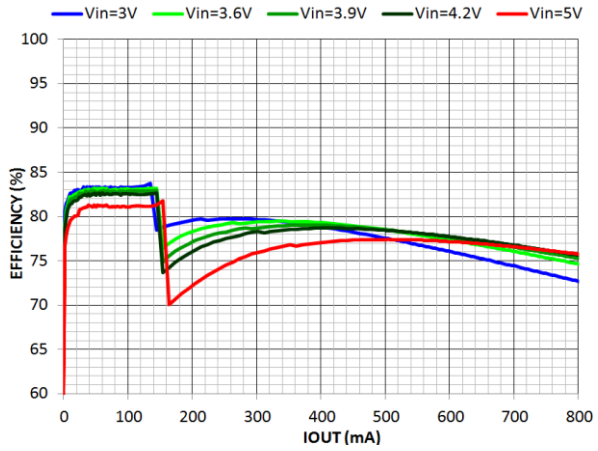


Figure 21. Efficiency vs. Output Current
V_{OUT} = 0.8 V, Temp = 25°C

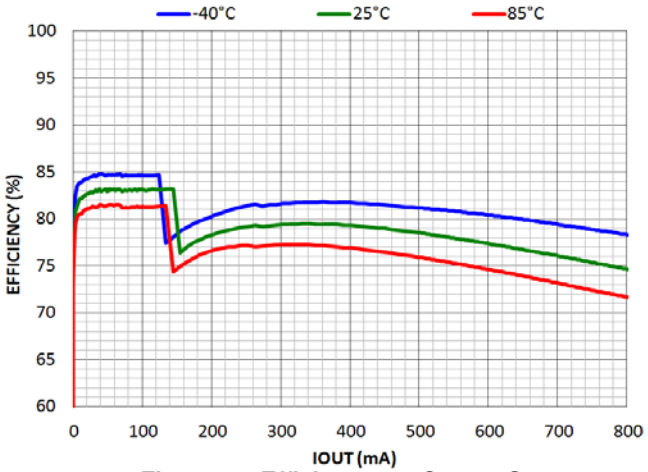


Figure 22. Efficiency vs. Output Current
V_{OUT} = 0.8 V, V_{IN} = 3.6 V

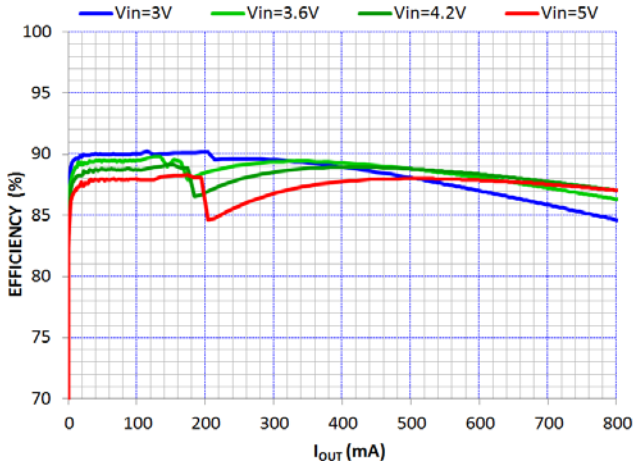


Figure 23. Efficiency vs. Output Current
V_{OUT} = 1.8 V, Temp = 25°C

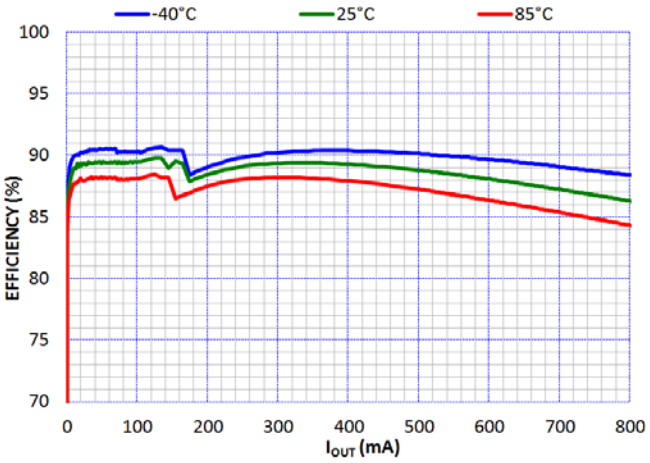


Figure 24. Efficiency vs. Output Current
V_{OUT} = 1.8 V, V_{IN} = 3.6 V

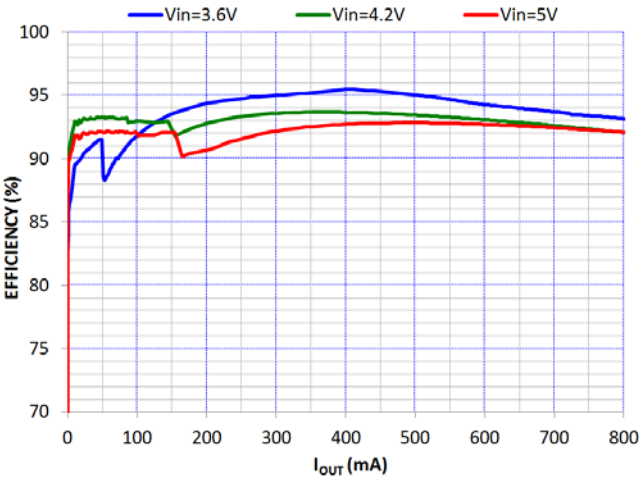


Figure 25. Efficiency vs. Output Current
V_{OUT} = 3.3 V, Temp = 25°C

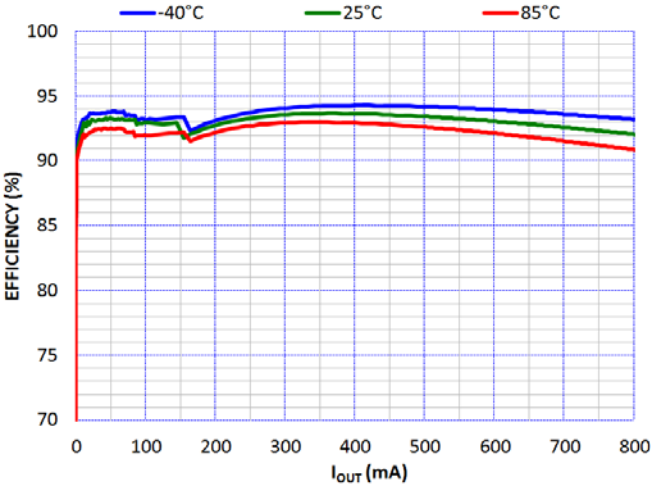


Figure 26. Efficiency vs. Output Current
V_{OUT} = 3.3 V, V_{IN} = 4.2 V

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

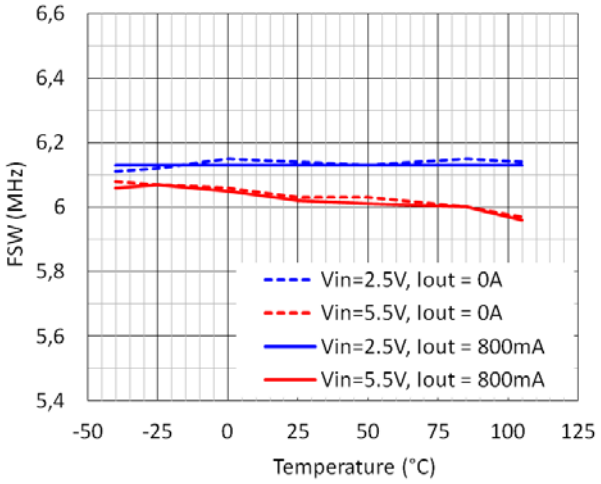


Figure 27. 6 MHz, Switching Frequency vs. Temperature (T_A)

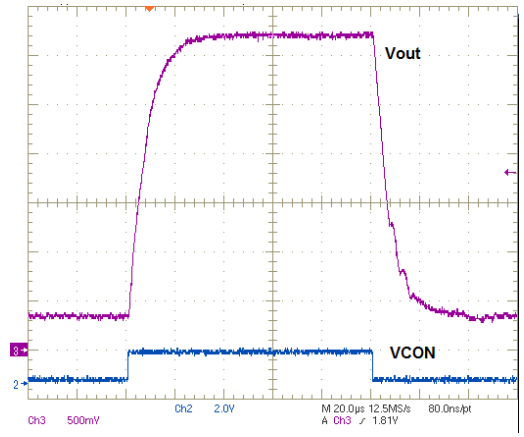


Figure 28. Transient, V_{OUT} vs. VCON, R_L = 10 Ω, V_{OUT} = 0.4 V to 3.6 V, PV_{IN} = 3.9 V w/ T_R = 7 μs, T_F = 10 μs

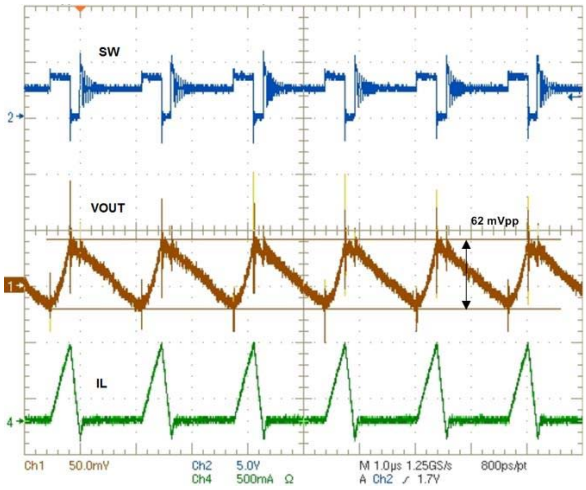


Figure 29. Output Voltage Waveforms in PFM Mode I_{OUT} = 100 mA, PV_{IN} = 3.6 V, V_{OUT} = 2.5 V, C_{OUT} = 4.7 μF

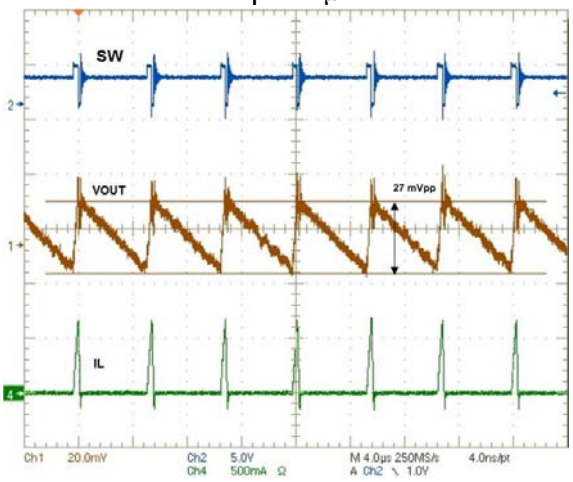


Figure 30. Output Voltage Waveforms in PFM Mode I_{OUT} = 100 mA, PV_{IN} = 3.6 V, V_{OUT} = 2.5 V, C_{OUT} = 2 x 4.7 μF

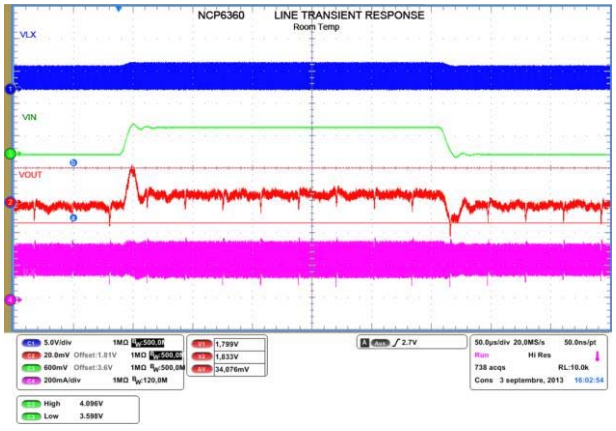


Figure 31. Line Transient Response < 20 mV Peak, PV_{IN} = 3.6 V to 4.1 V, R_L = 8 Ω, V_{OUT} = 1.8 V

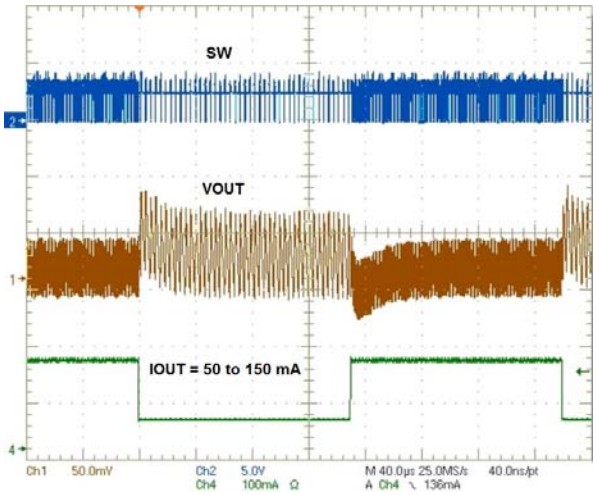


Figure 32. Load Transient Response w/ ΔV_{meas} < 50 mV Peak, I_{OUT} = 50 to 150 mA, V_{OUT} = 2.5 V

TYPICAL OPERATING CHARACTERISTICS

PV_{IN} = EN = 3.6 V, L = 0.47 μH, C_{OUT} = 4.7 μF, C_{IN} = 10 μF, F_{sw} = 6 MHz, T_A = 25°C (unless otherwise noted)

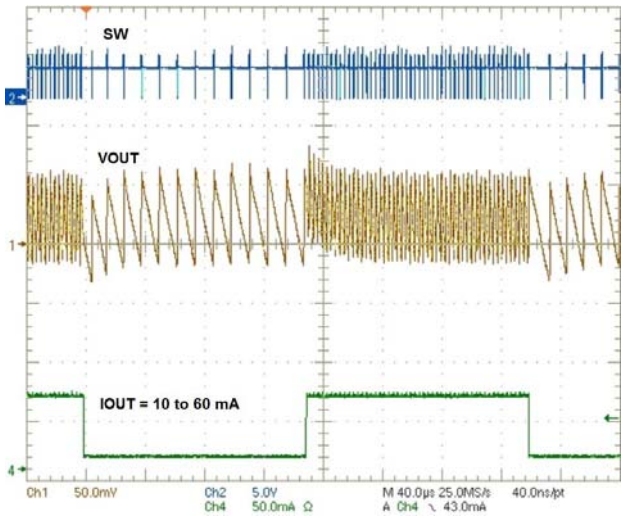


Figure 33. Load Transient Response w/ ΔV_{meas} < 50 mV Peak, I_{OUT} = 10 to 60 mA, V_{OUT} = 2.5 V

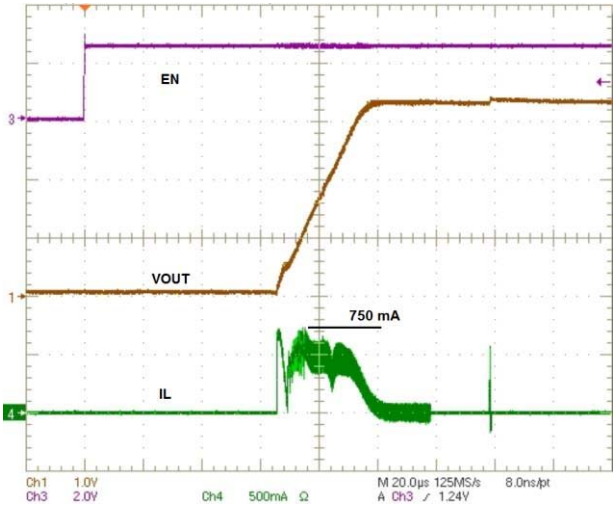


Figure 34. Power−up Transient Response PV_{IN} = 4.2 V, V_{OUT} = 3.4 V, R_L = 2.5 kΩ

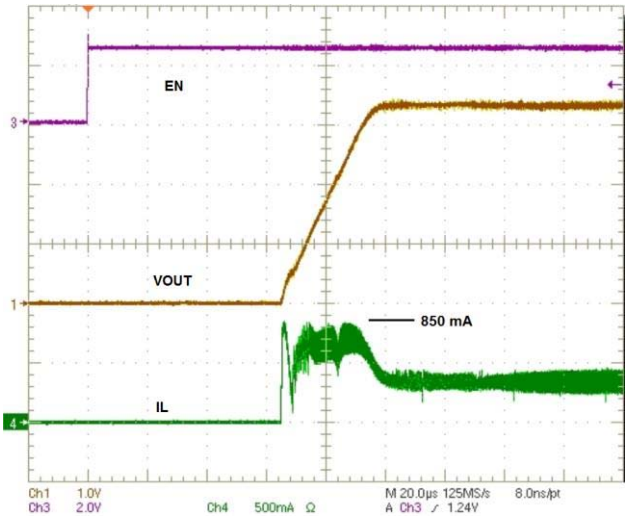


Figure 35. Power−up Transient Response PV_{IN} = 4.2 V, V_{OUT} = 3.4 V, R_L = 10 Ω

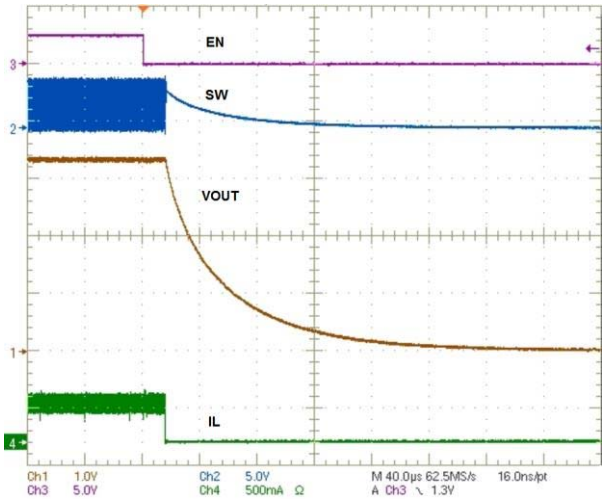


Figure 36. Power−down Transient Response PV_{IN} = 4.2 V, V_{OUT} = 3.4 V, R_L = 10 Ω

OPERATING DESCRIPTION

General Description

The NCP6360 is a voltage−mode standalone synchronous step−down DC−to−DC converter designed to supply RF Power Amplifiers (PAs) used into 3G/4G wireless systems (Mobile/ Smart Phones, Phablets, Tablets, ...) powered by single−cell Lithium−Ion batteries. The IC can deliver up to 800 mA when operating in PWM mode.

The buck converter output voltage ranging from 0.6 V to 3.4 V can be monitored by the system's PA output RF power through the control pin VCON. The control voltage range is from 0.24 V to 1.36 V and Vout is equal to 2.5 times this control voltage. VCON allows the PA to have its efficiency dynamically optimized during communication calls in the case for example of roaming situation involving a constant adjustment of the PA output power. The value−added benefit is an increase of the absolute talk time.

Synchronous rectification and automatic PFM/PWM operating mode transitions improve overall solution efficiency. The device operates at 6 MHz switching frequency.

Buck DC−to−DC Converter Operating

The converter is a synchronous rectifier type with both high side and low side integrated switches. Neither external transistor nor diodes are required for NCP6360 operation. Feedback and compensation network are also fully integrated. The device can operate in four different modes: shutdown mode (EN = Low, device off), Sleep Mode when VCON below about 0.1 V, PFM mode for efficiency optimization purpose when operating at light load and PWM mode when operating in medium and high loads. The transitions between PWM and PFM modes occur automatically.

Shutdown Mode

The NCP6360 enters shutdown mode when setting the EN pin Low (below 0.4 V) or when PVIN drops below its UVLO threshold value (2.35 V typical). In shutdown mode, the internal reference, oscillator and most of the control circuitries are turned off. The typical current consumption is 0.7 μA. Applying a voltage above 1.1 V to EN pin will enable the device for normal operation. A soft−start sequence is run when activating EN high. EN pin should be activated after the input voltage is applied.

PWM (Pulse Width Modulation) Operating Mode

In medium and high load conditions, the NCP6360 operates in PWM mode from a fixed clock (6 MHz) and adapts its duty cycle to regulate the desired output voltage. In this mode, the inductor current is in CCM (Continuous Current Mode) and the voltage is regulated by PWM. The internal N−MOSFET switch operates as synchronous rectifier and is driven complementary to the P−MOSFET switch. In CCM, the lower switch (N−MOSFET) in a synchronous converter provides a lower voltage drop than the diode in an asynchronous converter, which provides less loss and higher efficiency.

PFM (Pulse Frequency Modulation) Operating Mode

In order to save power and improve efficiency at low loads the NCP6360 operates in PFM mode as the inductor drops into DCM (Discontinuous Current Mode). The upper FET on time is kept constant and the switching frequency is variable. Output voltage is regulated by varying the switching frequency which becomes proportional to loading current. As it does in PWM mode, the internal N−MOSFET operates as synchronous rectifier after each P−MOSFET on−pulse. When load increases and current in inductor becomes continuous again, the controller automatically turns back to PWM mode.

Sleep Mode

The NCP6360 device enters the sleep mode in about 4μs when the control voltage VCON goes below typically 70 mV. Vout is extremely low, close to 0 V and in a state out of regulation. In this Vout condition the Sleep mode enables a low current state (40 μA typical range). The buck converter exits the sleep mode and returns in a regulation state when VCON goes above 110 mV after typically 5 μs.

Inductor Peak Current limitations

During normal operation, peak current limitation will monitor and limit the current through the inductor. This current limitation is particularly useful when size and/or height constrain inductor power. The High Side Switch (HSS) peak current limitation is typically 1.5 A, while the Low Side Switch (LSS) has a peak current up to 0.8 A. The HSS peak current contributes to limit the current during soft start sequence in high load conditions.

Under−voltage Lockout (UVLO)

NCP6360 core does not operate for voltages below the Under Voltage lock Out (UVLO) level. Below UVLO threshold (typical 2.35 V), all internal circuitry (both analog and digital) is held in reset. NCP6360 operation is not guaranteed down to VUVLO when battery voltage is dropping off. To avoid erratic on / off behavior,a typical 100 mV hysteresis is implemented. Restart is guaranteed at 2.6 V when VBAT voltage is recovering or rising.

Power−Up / Power−Down Sequencing

The EN pin controls NCP6360 start up. EN pin Low to High transition starts the power up sequencer which is combined with a soft start consisting to limit the inrush current at 800 mA while the output voltage is establishing. If EN is made low, the DC to DC converter is turned off and device enters shutdown mode.

A built−in pull−down resistor disables the device when this pin is left unconnected or not driven.

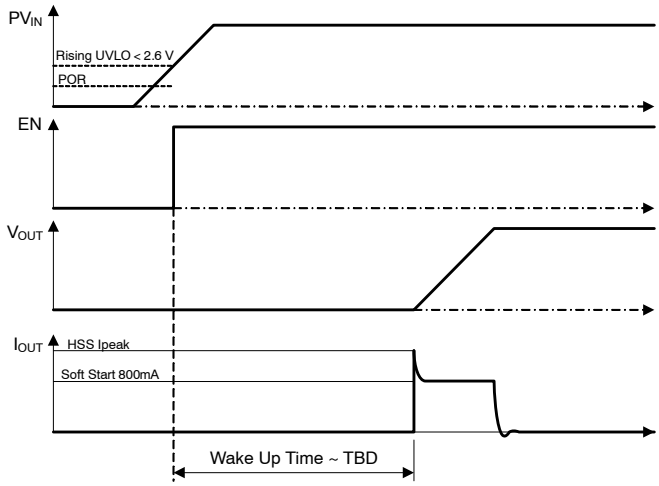


Figure 37. Power−Up Sequence

In order to power up the circuit, the input voltage PVIN has to rise above the UVLO threshold (Rising UVLO). This triggers the internal core circuitry power up which is the “Wake Up Time” (including “Bias Time”).

This delay is internal and cannot be bypassed.

The power down sequence is triggered by setting Low the EN pin. The output voltage goes down to 0 V.

Thermal Shutdown Feature (TSD)

The thermal capability of IC can be exceeded due to step down converter output stage power level. A thermal protection circuitry is therefore implemented to prevent the IC from damage. This protection circuitry is only activated when the core is in active mode (output voltage is turned on). During thermal shut down, output voltage is turned off and the device enters sleep mode.

Thermal shut down threshold is set at 155°C (typical) when the die temperature increases and, in order to avoid erratic on / off behavior, a 35°C hysteresis is implemented. So, after a typical 155°C thermal shut down, the NCP6360 will return to normal operation when the die temperature cools to 120°C. This normal operation depends on the input conditions and configuration at the time the device recovers.

APPLICATION INFORMATION

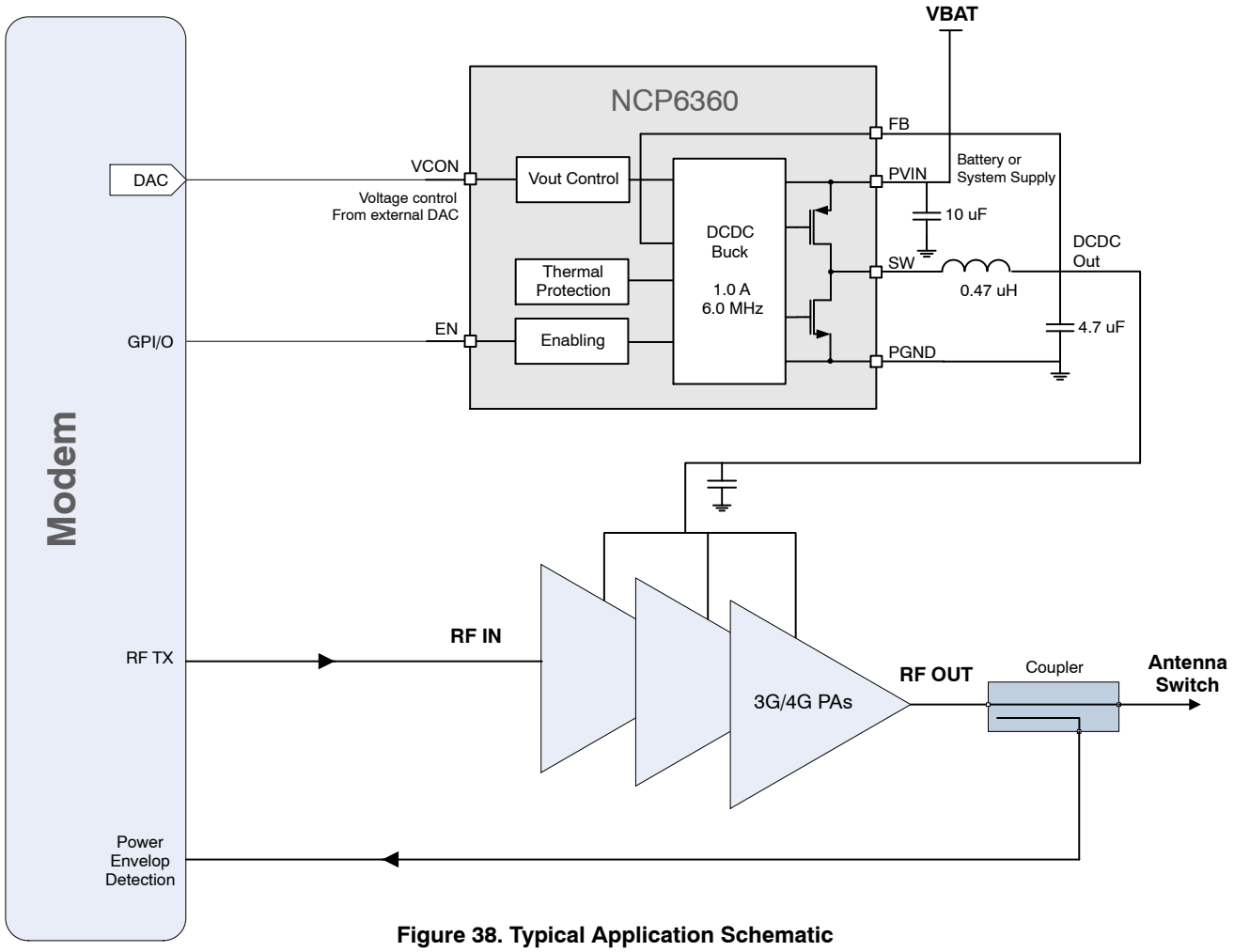


Figure 38. Typical Application Schematic

Output Filter Design Considerations

The output filter introduces a double pole in the system at a frequency of:

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \qquad \text{(eq. 1)}$$

The NCP6360 internal compensation network is optimized for a typical output filter comprising a 470 nH inductor and one 4.7 μF capacitor as described in the basic application schematic Figure 38.

Inductor Selection

The inductance of the inductor is determined by given peak−to−peak ripple current I_{LPP} of approximately 20% to 50% of the maximum output current I_{OUTMAX} for a trade−off between transient response and output ripple. The selected inductor must have high enough saturation current rating to be higher than the maximum peak current that is:

$$I_{LMAX} = I_{OUTMAX} + \frac{I_{LPP}}{2} \qquad \text{(eq. 2)}$$

The inductor also needs to have high enough current rating based on temperature rise concern. Low DCR is good for efficiency improvement and temperature rise reduction. Tables 1 shows recommended inductor references.

Table 1. RECOMMENDED INDUCTORS WHEN OPERATING AT 6 MHz

Supplier	Part#	Value (μH)	Size (L x I x T) (mm)	DC Rated Current (A)	DCR Max @ 25°C (mΩ)
TDK	TFM201610A−R47M−T00	0.47	2.0 x 1.6 x 1.0	3.5	46
TDK	TFM201210A−R47M−T00	0.47	2.0 x 1.2 x 1.0	2.5	65
Toko	DFE201610R−R47M−T00	0.47	2.0 x 1.6 x 1.0	3.8	48
Toko	DFE201610A−R47M−T00	0.47	2.0 x 1.6 x 1.0	3.7	58

Output Capacitor Selection

The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be used. For a given peak−to−peak ripple current I_{LPP} in the inductor of the output filter, the output voltage ripple across the output capacitor is the sum of three components as below.

$$V_{OUTPP} = V_{OUTPP(C)} + V_{OUTPP(ESR)} + V_{OUTPP(ESL)} \quad \text{(eq. 3)}$$

Where $V_{OUTPP(C)}$ is the ripple component coming from an equivalent total capacitance of the output capacitors, $V_{OUTPP(ESR)}$ is a ripple component from an equivalent ESR of the output capacitors, and $V_{OUTPP(ESL)}$) is a ripple component from an equivalent ESL of the output capacitors. In PWM operation mode, the three ripple components can be obtained by

$$V_{OUTPP(C)} = \frac{I_{L\_PP}}{8 \cdot C \cdot f_{SW}} \quad \text{(eq. 4)}$$

$$V_{OUTPP(ESR)} = I_{LPP} \cdot ESR \quad \text{(eq. 5)}$$

$$V_{OUT\_PP(ESL)} = \frac{ESL}{ESL + L} \cdot V_{IN} \quad \text{(eq. 6)}$$

And the peak−to−peak ripple current is:

$$I_{LPP} = \frac{\left(PV_{IN} - V_{OUT}\right) \cdot V_{OUT}}{PV_{IN} \cdot F_{SW} \cdot L} \quad \text{(eq. 7)}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUTPP}(C)$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUTPP} in PWM operation mode.

$$C_{MIN} = \frac{I_{LPP}}{8 \cdot V_{OUTPP} \cdot f_{SW}} \quad \text{(eq. 8)}$$

Input Capacitor Selection

One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail, ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding the input ripple voltage V_{INPP} is

$$C_{INMIN} = \frac{I_{OUTMAX} \cdot \left(D - D^2\right)}{V_{INPP} \cdot f_{SW}} \quad \text{(eq. 9)}$$

Where

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 10)}$$

In addition the input capacitor needs to be able to absorb the input current, which has a RMS value of:

$$I_{INRMS} = I_{OUTMAX} \cdot \sqrt{D - D^2} \quad \text{(eq. 11)}$$

The input capacitor needs also to be sufficient to protect the device from over voltage spike and a minimum of 4.7 μF capacitor is required. The input capacitor should be located as close as possible to the IC. PGND is connected to the ground terminal of the input cap which then connects to the ground plane. The PV_{IN} is connected to the V_{BAT} terminal of the input capacitor which then connects to the V_{BAT} plane.

Layout and PCB Design Recommendations

Good PCB layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC to connect the inner ground layers to reduce thermal impedance.
- Use large area copper especially in top layer to help thermal conduction and radiation.
- Use two layers for the high current paths (PVIN, PGND, SW) in order to split current in two different paths and limit PCB copper self heating.

(See demo board example Figure 40)

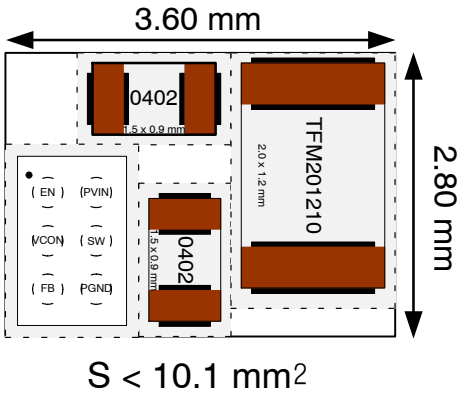


Figure 39. Layout Minimum Recommended Occupied Space Using 0402 Capacitors and 0805 (2.0 x 1.2 x 1.0 mm) Inductor

Input capacitor placed as close as possible to the IC.

- PV_{IN} directly connected to Cin input capacitor, and then connected to the Vin plane. Local mini planes used on the top layer (green) and layer just below top layer with laser vias.
- PGND directly connected to Cin input capacitor, and then connected to the GND plane: Local mini planes used on the top layer (green) and layer just below top layer with laser vias.
- SW connected to the Lout inductor with local mini planes used on the top layer (green) and layer just below top layer with laser vias.

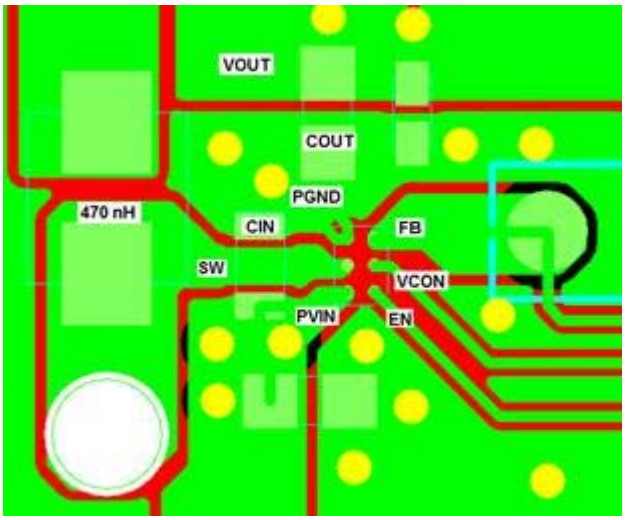


Figure 40. Example of PCB Implementation (PCB case with 0805 (2.0 x 1.2 mm) Capacitors and 2016 (2.0 x 1.6 x 1.0 mm) Inductors

ORDERING INFORMATION

Device	Package	Shipping†
NCP6360FCCT2G	WLCSP6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

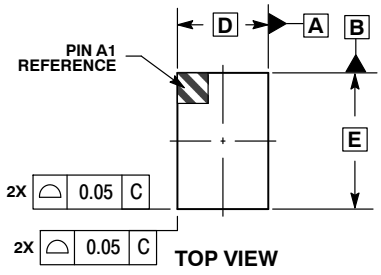
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

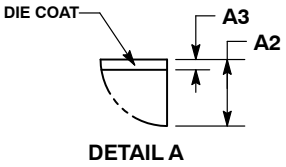
WLCSP6, 1.00x1.50
CASE 568AN
ISSUE A

SCALE 4:1

DATE 30 JAN 2014



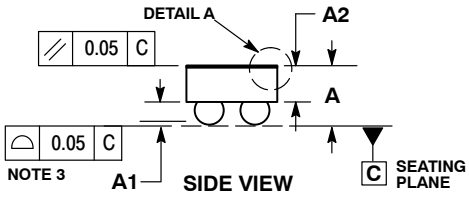
TOP VIEW



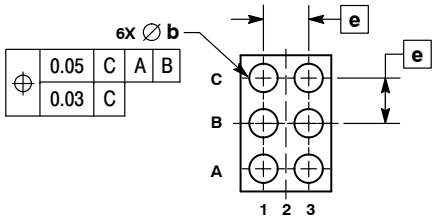
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.54	0.63
A1	0.21	0.26
A2	0.36 REF	
A3	0.02 REF	
b	0.315	0.335
D	1.00 BSC	
E	1.50 BSC	
e	0.50 BSC	

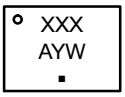


SIDE VIEW



BOTTOM VIEW

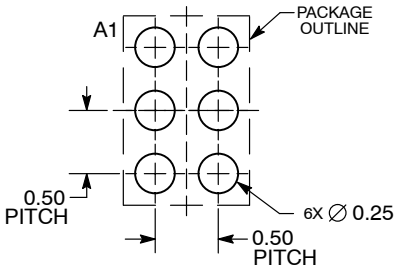
GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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