Synchronous Buck Regulator 6 MHz, 1.2 A

FAN53602

DESCRIPTION

The FAN53602 is a 6 MHz, step−down switching voltage regulator that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53602 is capable of delivering a constant load of 1.2 A.

The regulator operates at a nominal fixed frequency of 6 MHz, which reduces the value of the external components to as low as 470 nH for the output inductor and 4.7 μF for the output capacitor. In addition, the Pulse Width Modulation (PWM) modulator can be synchronized to an external frequency source.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate the device in Power−Save Mode with a typical quiescent current of 24 μA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed−frequency control, operating at 6 MHz. In Shutdown Mode, the supply current drops below 1 μA, reducing power consumption. For applications that require minimum ripple or fixed frequency, PFM Mode can be disabled using the MODE pin.

The FAN53602 is available in 6−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

Features

- 1.2 A Output Current Capability
- 24 μA Typical Quiescent Current
- 6 MHz Fixed−Frequency Operation
- Best−in−Class Load Transient Response
- Best−in−Class Efficiency
- 2.3 V to 5.5 V Input Voltage Range
- Low Ripple Light−Load PFM Mode
- Forced PWM and External Clock Synchronization
- Internal Soft−Start
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 6−Bump WLCSP, 0.4 mm Pitch

Application

- 3G, 4G, WiFi®, WiMAX™, and WiBro™ Data Cards
- Tablets
- DSC, DVC
- Netbooks

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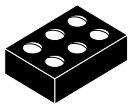
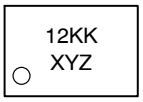


WLCSP6 1.16x0.86x0.586
CASE 567QE

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Run Code
X	= Alphabetical Year Code
Y	= 2 Weeks Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

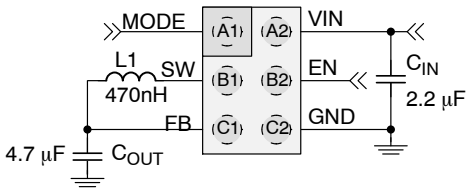


Figure 1. Typical Application

Table 1. ORDERING INFORMATION

Part Number	Output Voltage	Package	Temperature Range	Packing Method†	Device Marking
FAN53602UC123X	1.233 V	WLCSP – 6, 0.4 mm Pitch	–40 to 85°C	3000 / Tape & Reel	TZ

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN CONFIGURATION

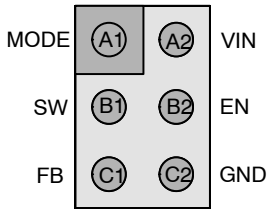


Figure 2. Bumps Facing Down

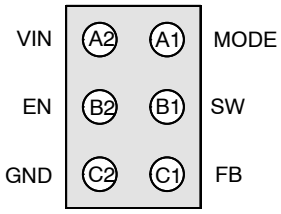


Figure 3. Bumps Facing Up

Table 2. PIN DEFINITIONS

Pin #	Name	Description
A1	MODE	MODE. Logic 1 on this pin forces the IC to stay in PWM Mode. A logic 0 allows the IC to automatically switch to PFM during light loads. The regulator also synchronizes its switching frequency to four times the frequency provided on this pin. Do not leave this pin floating.
B1	SW	Switching Node. Connect to output inductor.
C1	FB	Feedback / VOUT. Connect to output voltage.
C2	GND	Ground. Power and IC ground. All signals are referenced to this pin.
B2	EN	Enable. The device is in Shutdown Mode when voltage to this pin is < 0.4 V and enabled when > 1.2 V. Do not leave this pin floating.
A2	VIN	Input Voltage. Connect to input power source.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Input Voltage		–0.3	7.0	V
V_{SW}	Voltage on SW Pin		–0.3	V_{IN} + 0.3 (Note 1)	V
V_{CTRL}	EN and Mode Pin Voltage		–0.3	V_{IN} + 0.3 (Note 1)	V
	Other Pins		–0.3	V_{IN} + 0.3 (Note 1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22–A114	2.0		kV
		Charged Device Model per JESD22–C101	1.5		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Lesser of 7 V or V_{IN} + 0.3 V.

Table 4. THERMAL PROPERTIES

Symbol	Parameter	Typ.	Unit
θ_{JAn}	Junction–to–Ambient Thermal Resistance	125	°C/W

NOTE: Junction–to–ambient thermal resistance is a function of application and board layout. This data is measured with four–layer 2s2p boards without vias in accordance to JEDEC standard JESD51. Special attention must be paid to not exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	2.3		5.5	V
I_{OUT}	Output Current	1200			mA
L	Inductor		470		nH
C_{IN}	Input Capacitor		2.2		μF
C_{OUT}	Output Capacitor	1.6	4.7	12.0	μH
T_A	Operating Ambient Temperature	−40		+85	°C
T_J	Operating Junction Temperature	−40		+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ELECTRICAL CHARACTERISTICS (Note 2) Minimum and Maximum Values are at V_{IN} = V_{EN} = 2.3 V to 5.5 V, V_{MODE} = 0 V (AUTO Mode), T_A = −40°C to +85°C, circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = V_{EN} = 3.6 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	No Load, Not Switching		24	50	μA
		PWM Mode		8		mA
$I_{(SD)}$	Shutdown Supply Current	EN = GND, V_{IN} = 3.6 V,		0.25	1.00	μA
V_{UVLO}	Under−Voltage Lockout Threshold	Rising VIN		2.15	2.27	V
V_{UVHYST}	Under−Voltage Lockout Hysteresis			200		mV
Logic Inputs: EN and MODE Pins						
V_{IH}	Enable HIGH−Level Input Voltage		1.2			V
V_{IL}	Enable Low−Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			100		mV
I_{IN}	Enable Input Leakage Current	Pin to VIN or GND		0.01	1.00	μA
Switching and Synchronization						
f_{SW}	Switching Frequency (Note 3)	VIN = 3.6 V, T_A = 25°C, PWM Mode, IOUT = 10 mA	5.4	6.0	6.6	MHz
f_{SYNC}	MODE Synchronization Range (Note 3)	Square Wave at MODE Input	1.3	1.5	1.7	MHz
Regulation						
Vo	Output Voltage Accuracy	VIN = 3.6 V, IOUT = 0 mA, PWM	1.202	1.233	1.264	V
		AUTO Mode, IOUT = 0 to 1.2 A	1.171	1.233	1.281	V
t_{SS}	Soft−Start	VIN = 4.5 V, From EN Rising Edge to 95% VOUT		180	300	μs
Output Driver						
$R_{DS(on)}$	PMOS On Resistance	VIN = V_{GS} = 3.6 V		175		mΩ
	NMOS On Resistance	VIN = V_{GS} = 3.6 V		165		mΩ
$I_{LIM(OL)}$	PMOS Peak Current Limit	VIN = 3.6 V, T_A = 25°C	1.70	1.95	2.20	A
T_{TSD}	Thermal Shutdown			150		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. The Electrical Characteristics table reflects open−loop data. Refer to the Operation Description and Typical Characteristics Sections for closed−loop data.
3. Limited by the effect of t_{OFF} minimum (see Operation Description section).

TYPICAL PERFORMANCE CHARACTERISTIC

Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 V (AUTO Mode), V_{OUT} = 1.233 V, , T_A = 25°C

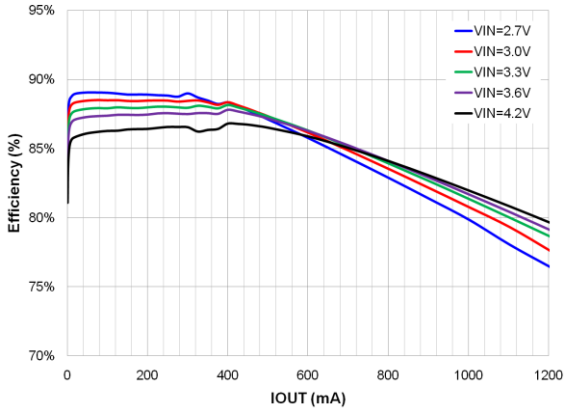


Figure 4. Efficiency vs. Load Current and Input Voltage

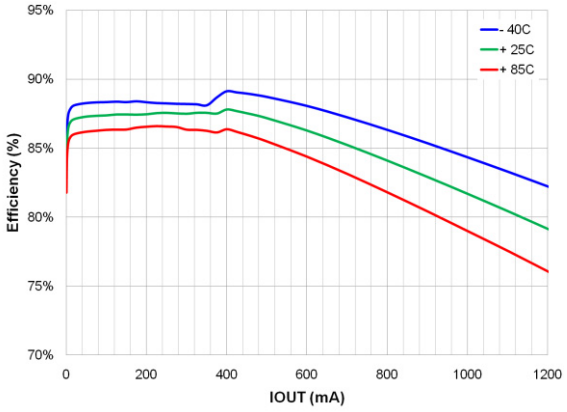


Figure 5. Efficiency vs. Load Current and Temperature

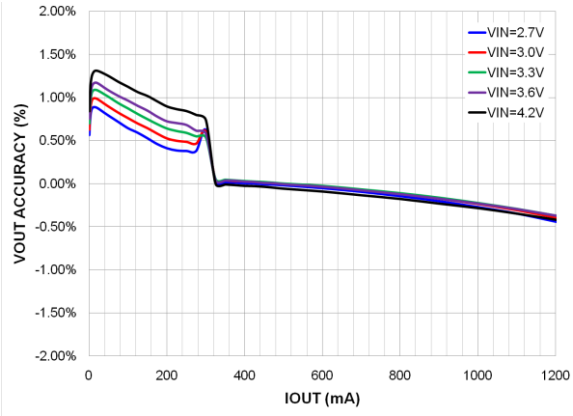


Figure 6. VOUT Accuracy vs. Load Current and Input Voltage

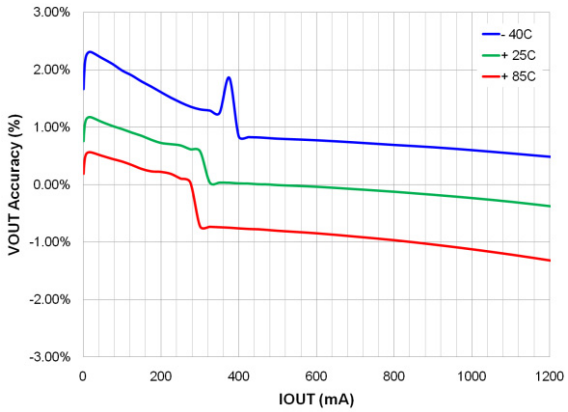


Figure 7. VOUT Accuracy vs. Load Current and Temperature

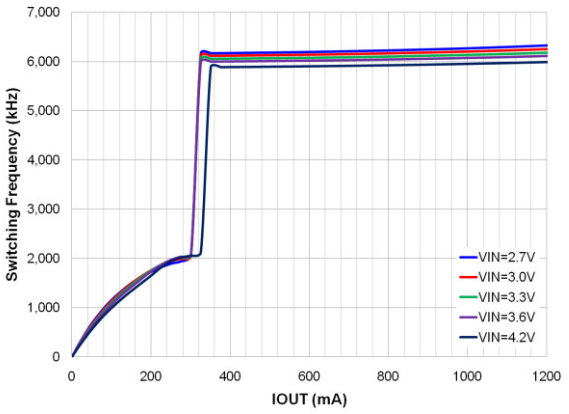


Figure 8. Switching Frequency vs. Load Current and Input Volatage

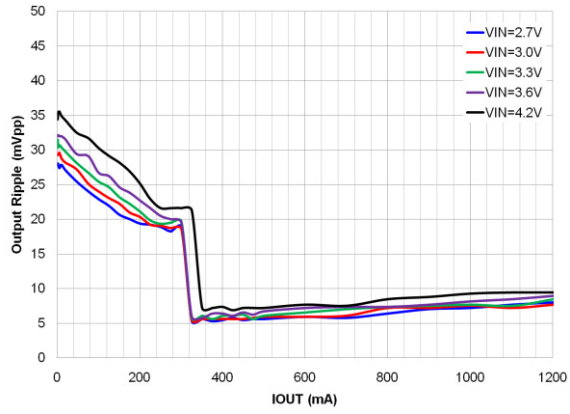


Figure 9. Output Ripple vs. Load Current and Input Voltage

TYPICAL PERFORMANCE CHARACTERISTIC (continued)

Unless otherwise noted, V_{IN} = V_{EN} = 3.6 V, V_{MODE} = 0 V (AUTO Mode), V_{OUT} = 1.233 V, , T_A = 25°C

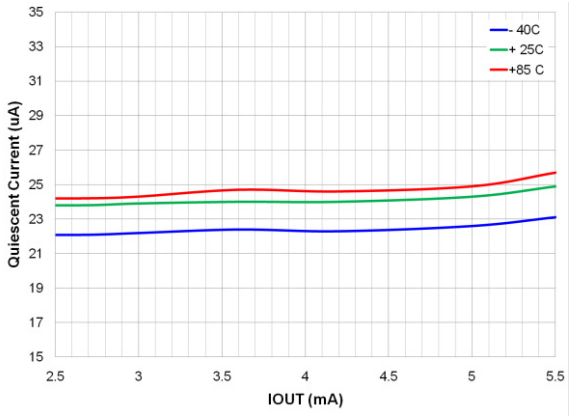


Figure 10. Quiescent Current vs. Input Voltage and Temperature

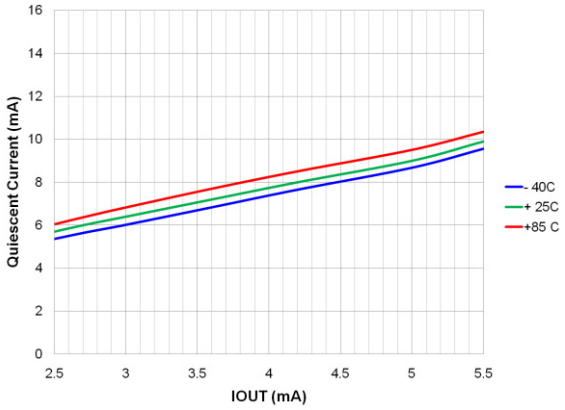


Figure 11. Quiescent Current vs. Input Volatage and Temperature, FPWM Mode

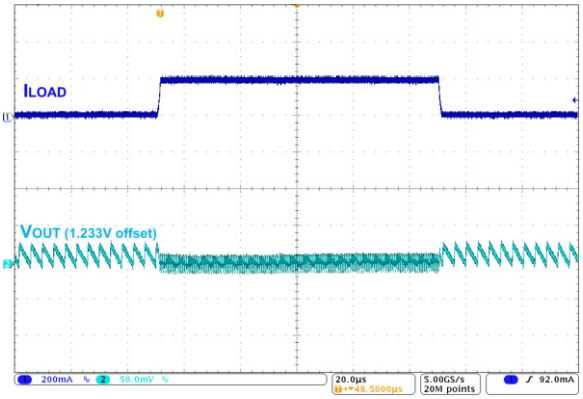


Figure 12. Load Transient, 10 mA ↔ 200 mA in 1 μs

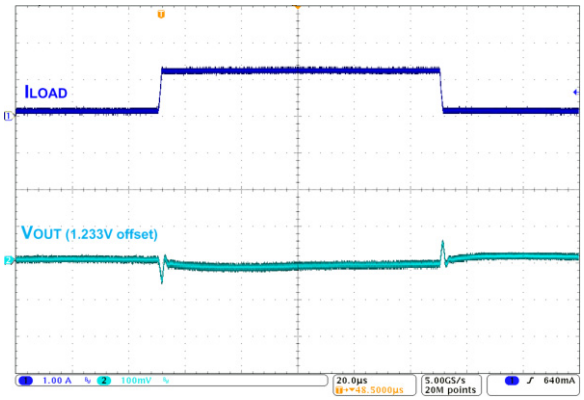


Figure 13. Load Transient, 150 mA ↔ 1200 mA in 1 μs

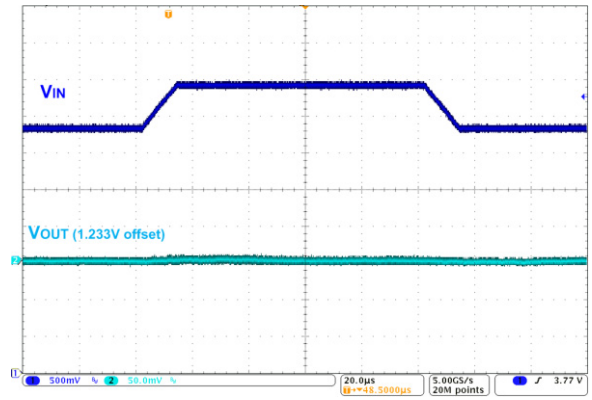


Figure 14. Line Transient, 3.3 V ↔ 3.9 V in 10 μs, 1200 mA Load

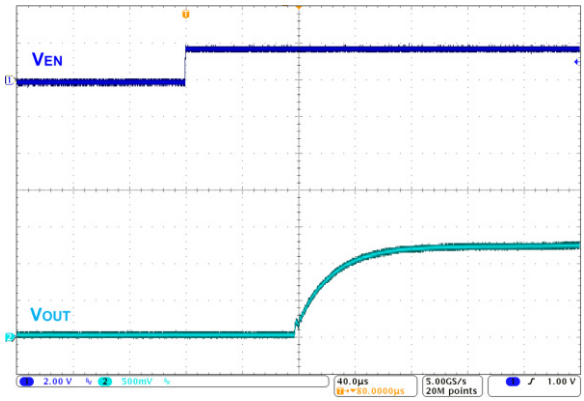


Figure 15. Startup, 800 mA Load

OPERATION DESCRIPTION

The FAN53602 is a 6 MHz, step−down switching voltage regulator that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53602 is capable of delivering a constant 1.2 A load current.

The regulator operates at a nominal fixed frequency of 6 MHz, which reduces the value of the external components to as low as 470 nH for the output inductor and 4.7 μF for the output capacitor. In addition, the PWM modulator can be synchronized to an external frequency source.

Control Scheme

The FAN53602 uses a proprietary, non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53602 operates in Discontinuous Current Mode (DCM) single−pulse PFM Mode, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, allowing for a smooth transition between DCM and CCM.

Combined with exceptional transient response characteristics, the very low quiescent current of the controller maintains high efficiency; even at very light loads, while preserving fast transient response for applications requiring tight output regulation.

Enable and Soft−Start

When EN is LOW, all circuits are off and the IC draws ~250 nA of current. When EN is HIGH and VIN is above its UVLO threshold, the regulator begins a soft−start cycle. The output ramp during soft−start is a fixed slew rate of 50 mV/μs from VOUT = 0 to 1 V, then 12.5 mV/μs until the output reaches its setpoint. Regardless of the state of the MODE pin, PFM Mode is enabled to prevent current from being discharged from COUT if soft−start begins when COUT is charged.

The current−limit fault response protects the IC in the event of an over−current condition present during soft−start. As a result, the IC may fail to start if heavy load is applied during startup and/or if excessive COUT is used.

The current required to charge COUT during soft−start commonly referred to as “displacement current” is given as:

$$I_{DISP} = C_{OUT} \cdot \frac{dV}{dt} \qquad \text{(eq. 1)}$$

Where $\frac{dV}{dt}$ refers to the soft−start slew rate.

To prevent shut down during soft−start, the following condition must be met:

$$I_{DISP} + I_{LOAD} < I_{MAX(DC)} \qquad \text{(eq. 2)}$$

Where $I_{MAX(DC)}$ is the maximum load current the IC is guaranteed to support.

Startup into Large C_{OUT}

Multiple soft−start cycles are required for no−load startup if COUT is greater than 15 μF. Large COUT requires light initial load to ensure the FAN53602 starts appropriately. The IC shuts down for 1.3 ms when IDISP exceeds ILIMIT for more than 200 μs of current limit. The IC then begins a new soft−start cycle. Since COUT retains its charge when the IC is off, the IC reaches regulation after multiple soft−start attempts.

MODE Pin

Logic 1 on this pin forces the IC to stay in PWM Mode. A logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled with a frequency between 1.3 MHz and 1.7 MHz, the converter synchronizes its switching frequency to four times the frequency on the MODE pin.

The MODE pin is internally buffered with a Schmitt trigger, which allows the MODE pin to be driven with slow rise and fall times. An asymmetric duty cycle for frequency synchronization is also permitted as long as the minimum time below $V_{IL(MAX)}$ or above $V_{IH(MAX)}$ is 100 ns.

Current Limit, Fault Shutdown and Restart

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. The regulator continues to limit the current cycle−by−cycle. After 16 cycles of current limit, the regulator triggers an over−current fault, causing the regulator to shut down for about 1.3 ms before attempting a restart.

If the fault is caused by short circuit, the soft−start circuit attempts to restart and produces an over−current fault after about 200 μs, which results in a duty cycle of less than 15%, limiting power dissipation.

The closed−loop peak−current limit is not the same as the open−loop tested current limit, ILIM(OL), in the Electrical Characteristics table. This is primarily due to the effect of propagation delays of the IC current limit comparator.

Under−Voltage Lockout (UVLO)

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Thermal Shutdown (TSD)

When the die temperature increases, due to a high load condition and/or a high ambient temperature; the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Minimum Off−Time Effect on Switching Frequency

$t_{OFF(MIN)}$ is 40 ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN53602 can provide or the maximum output voltage it can provide at low VIN while maintaining a fixed switching frequency in PWM Mode. When VIN is LOW, fixed switching is maintained as long as:

$$\frac{V_{OUT}}{V_{IN}} \le 1 - t_{OFF(MIN)} \cdot f_{SW} \approx 0.7$$

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 6 MHz to maintain regulation.

The calculation for switching frequency is given by:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, 6\ \text{MHz}\right) \quad \text{(eq. 3)}$$

Where:

$$t_{SW(MAX)} = 40\ \text{ns} \cdot \left(1 + \frac{V_{OUT} + I_{OUT} \cdot R_{OFF}}{V_{IN} - I_{OUT} \cdot R_{ON} - V_{OUT}}\right) \quad \text{(eq. 4)}$$

Where:

$$R_{OFF} = R_{DSON\_N} + DCR_L$$

$$R_{ON} = R_{DSON\_P} + DCR_L$$

APPLICATIONS INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects average current limit, the PWM−to−PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}}\right) \quad \text{(eq. 5)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad \text{(eq. 6)}$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero, I_{DCM}, is:

$$I_{DCM} = \frac{\Delta I}{2} \quad \text{(eq. 7)}$$

The FAN53602 is optimized for operation with L = 470 nH, but is stable with inductances up to 1 μH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but because ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{2} + \frac{\Delta I^2}{12}} \quad \text{(eq. 8)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 7 shows the effects of inductance higher or lower than the recommended 1 μH on regulator performance.

Output Capacitor

Table 8 suggests 0402 capacitors. 0603 capacitors may further improve performance in that the effective capacitance is higher. This improves transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right] \quad \text{(eq. 9)}$$

Input Capacitor

The 2.2 μF ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as VIN increases due to DC bias effects.

Table 7. EFFECTS OF CHANGES IN INDUCTOR VALUE (FROM 470 nH RECOMMENDED VALUE) ON REGULATOR PERFORMANCE

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT}	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

Table 8. RECOMMENDED PASSIVE COMPONENTS AND THEIR VARIATION DUE TO DC BIAS

Component	Description	Vendor	Min.	Typ.	Max.
L1	0.47 μH/5.3 A/26 mΩ 2.0 x 1.6 1.0 mm	Murata DFE201610E−R47M		470 nH	
C_{IN}	2.2 μF, 6.3 V, X5R, 0402	Murata or Equivalent GRM155R60J225ME15 GRM188R60J225KE19D	1.0 μF	2.2 μF	
C_{OUT}	4.7 μF, X5R, 0402	Murata or Equivalent GRM155R60G475M GRM155R60E475ME760	1.6 μF	4.7 μF	

PCB LAYOUT GUIDELINES

There are only three external components: the inductor and the input and output capacitors. For any buck switcher IC, including the FAN53602, it is important to place a low−ESR input capacitor very close to the IC, as shown in Figure 16. The input capacitor ensures good input decoupling, which helps reduce noise appearing at the output terminals and ensures that the control sections of the IC do not behave erratically due to excessive noise. This reduces switching cycle jitter and ensures good overall performance. It is important to place the common GND of CIN and COUT as close as possible to the C2 terminal. There is some flexibility in moving the inductor further away from the IC; in that case, VOUT should be considered at the COUT terminal.

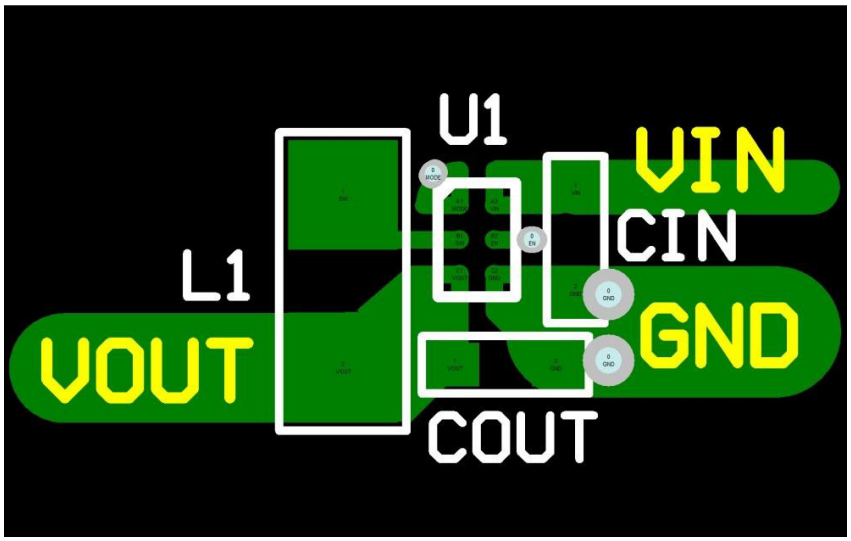


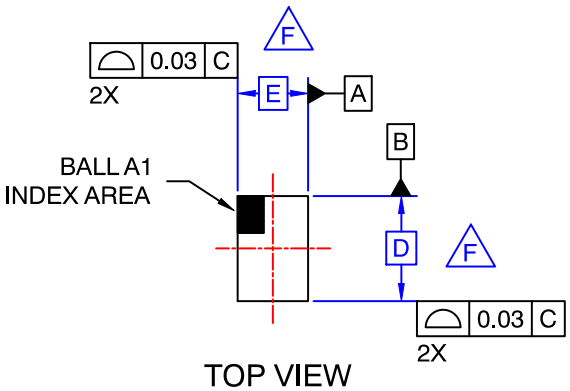
Figure 16. PCB Layout Guidance

PRODUCT−SPECIFIC DIMENSIONS

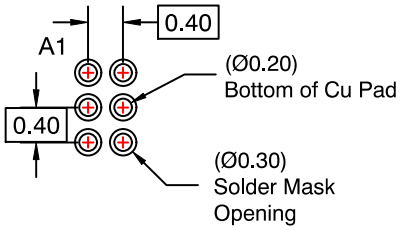
D	E	X	Y
1.160 ± 0.030	0.860 ± 0.030	0.230	0.180

WLCSP6 1.16x0.86x0.586
CASE 567QE
ISSUE O

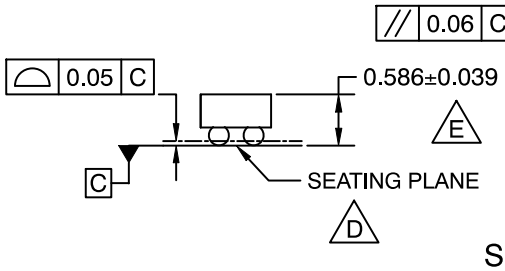
DATE 31 OCT 2016

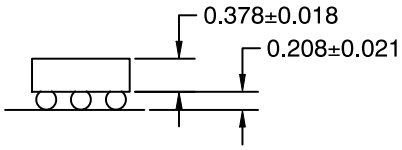


TOP VIEW

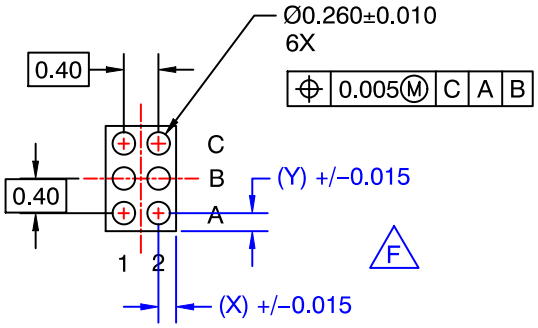


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 2009.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547–625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y, SEE PRODUCT DATASHEET.

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DESCRIPTION:	**WLCSP6 1.16x0.86x0.586**	**PAGE 1 OF 1**

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