ISL6745A

Improved Bridge Controller with Precision Dead Time Control

FN6703
Rev.2.00
Aug 14, 2017

The ISL6745A is a low-cost, double-ended, voltage-mode PWM controller designed for half-bridge and full-bridge power supplies and line-regulated bus converters. It provides precise control of switching frequency, adjustable soft-start, and overcurrent shutdown. In addition, the ISL6745A allows for accurate adjustment of MOSFET non-overlap time ("dead time") with dead times as low as 35ns, allowing power engineers to optimize the efficiency of open-loop bus converters. The ISL6745A also includes a control voltage input for closed-loop PWM and line voltage feed-forward functions. The ISL6745A is identical to the ISL6745, but is optimized for higher noise environments.

Low start-up and operating currents allow for easy biasing in both AC/DC and DC/DC applications. This advanced BiCMOS design also features adjustable switching frequency up to 1MHz, 1A FET drivers, and very low propagation delays for a fast response to overcurrent faults. The ISL6745A is available in a space-saving 10 Ld MSOP package and is assured to meet rated specifications across a wide -40°C to +105°C temperature range.

Related Literature

- For a full list of related documents, visit our website
  - ISL6745A product page

Features

- Precision duty cycle and dead time control
- 100µA start-up current
- Adjustable delayed overcurrent shutdown and restart
- Adjustable oscillator frequency up to 2MHz
- 1A MOSFET gate drivers
- Adjustable soft-start
- Internal over-temperature protection
- 35ns control to output propagation delay
- Small size and minimal external component count
- Input undervoltage protection
- Pb-free (RoHS compliant)

Applications

- Half-bridge converters
- Full-bridge converters
- Line-regulated bus converters
- AC/DC power supplies
- Telecom, datacom, and file server power

1. Overview

1.1 Internal Architecture

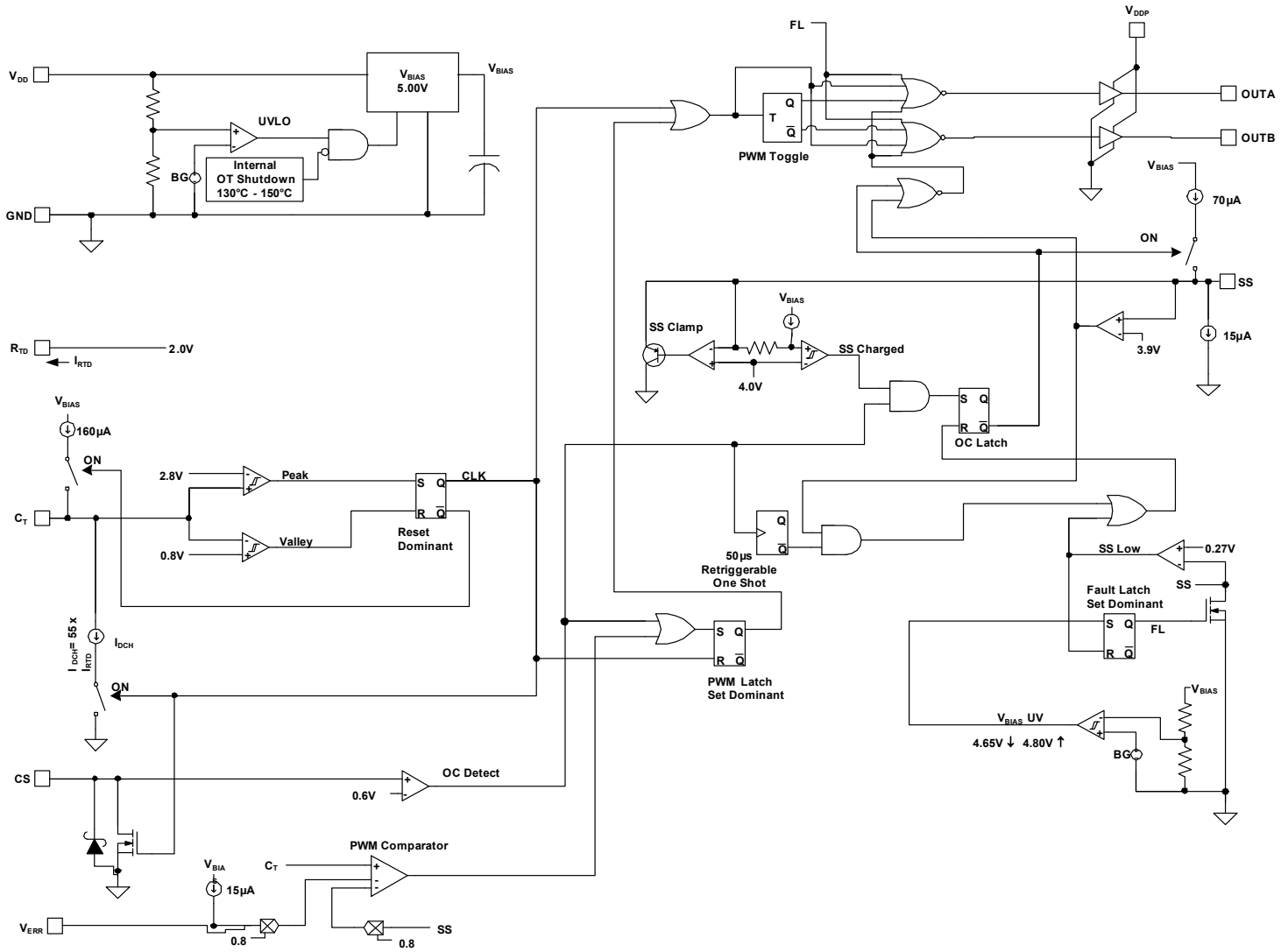


Figure 1. Internal Architecture

1.2 Typical Application - Telecom DC/DC Converter

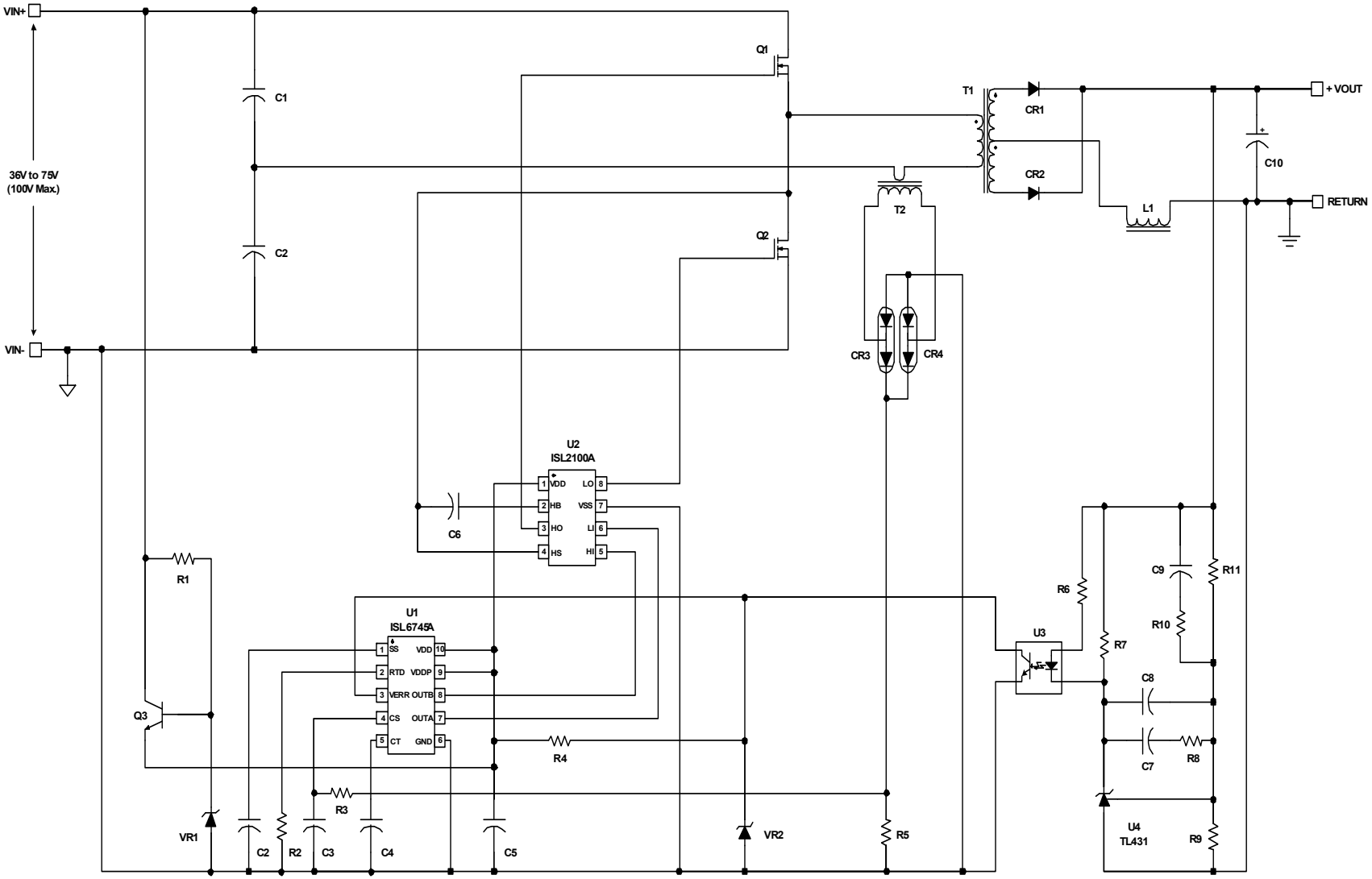


Figure 2. Typical Application

1.3 Ordering Information

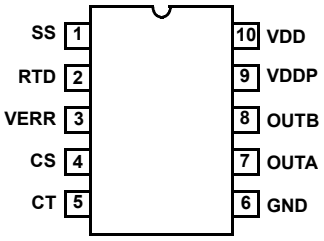
Part Number (Notes 1, 2, 3)	Part Marking	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL6745AAUZ	6745A	-40 to +105	10 Ld MSOP	M10.118
ISL6745ALEVAL3Z	Evaluation Board			

Notes:

1. Add “-T” suffix for 2.5k unit tape and reel option. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL6745A. For more information on MSL, refer to TB363.

1.4 Pin Configuration

ISL6745A
(10 Ld MSOP)
Top View



1.5 Pin Descriptions

Pin Name	Pin Number	Description
SS	1	Connect the soft-start timing capacitor between this pin and GND to control the duration of soft-start. The value of the capacitor determines the rate of increase of the duty cycle during start-up, controls the overcurrent shutdown delay, and the overcurrent and short-circuit hiccup restart period.
RTD	2	Oscillator timing capacitor discharge current control pin. A resistor is connected between this pin and GND. The current flowing through the resistor determines the magnitude of the discharge current. The discharge current is nominally 55x this current. The PWM dead time is determined by the timing capacitor discharge duration.
VERR	3	Inverting input of the PWM comparator. The error voltage is applied to this pin to control the duty cycle. Increasing the signal level increases the duty cycle. The node may be driven with an external error amplifier or an optocoupler.
CS	4	Input to the overcurrent protection comparator. The overcurrent comparator threshold is set at 0.600V nominal. The CS pin is shorted to GND at the end of each switching cycle. Depending on the current sensing source impedance, a series input resistor may be required due to the delay between the internal clock and the external power switch. Exceeding the overcurrent threshold will start a delayed shutdown sequence. When an overcurrent condition is detected, the soft-start charge current source is disabled. The soft-start capacitor begins discharging through a 15µA current source, and if it discharges to less than 3.9V (Sustained Overcurrent Threshold), a shutdown condition occurs and the OUTA and OUTB outputs are forced low. When the soft-start voltage reaches 0.27V (Reset Threshold) a soft-start cycle begins. If the overcurrent condition ceases, and then an additional 50µs period elapses before the shutdown threshold is reached, no shutdown occurs. The SS charging current is re-enabled and the soft-start voltage is allowed to recover.
CT	5	The oscillator timing capacitor is connected between this pin and GND.
GND	6	Reference and power ground for all functions on this device. Due to high peak currents and high frequency operation, a low impedance layout is necessary. Ground planes and short traces are highly recommended.
OUTA	7	Alternate half cycle output stages. Each output is capable of 1A peak currents for driving power MOSFETs or MOSFET drivers. Each output provides very low impedance to overshoot and undershoot.
OUTB	8	
VDDP	9	VDDP is the separate collector supply to the gate drive. Having a separate VDDP pin helps isolate the analog circuitry from the high power gate drive noise.
VDD	10	VDD is the power connection for the IC. To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible. The total supply current, I_{DD}, will be dependent on the load applied to outputs OUTA and OUTB. Total I_{DD} current is the sum of the quiescent current and the average output current. Knowing the operating frequency, f_{SW}, and the output loading capacitance charge, Q, per output, the average output current can be calculated from (EQ. 1): $I_{OUT} = 2 \bullet Q \bullet f_{SW}$ A (EQ. 1)

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	-0.3	+20.0	V
OUTA, OUTB	-0.3	V_{DD}	V
Signal Pins	-0.3	5	V
Peak GATE Current		1	A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
10 Ld MSOP Package (Note 4)	155

Notes:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-55	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	refer to TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-40	+105	°C
Supply Voltage Range (Typical)	9	16	V

2.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to Figure 1 on page 2 and Figure 2 on page 3. 9V < V_{DD} < 16V, R_{TD} = 51.1kΩ, C_T = 470pF, T_A = -40°C to +105°C, typical values are at T_A = +25°C.

Parameter	Test Conditions	Min (Note 5)	Typ	Max (Note 5)	Unit
Supply Voltage					
Start-Up Current, I_{DD}	V_{DD} < START Threshold	-	-	175	µA
Operating Current, I_{DD}	$C_{OUTA,B}$ = 1nF	-	5	8.5	mA
UVLO START Threshold		5.9	6.3	6.6	V
UVLO STOP Threshold		5.3	5.7	6.3	V
Hysteresis		-	0.6	-	V
Current Sense					
Current Limit Threshold		0.55	0.6	0.65	V
CS to OUT Delay		-	35	-	ns
CS Sink Current		8	10	-	mA

Recommended operating conditions unless otherwise noted. Refer to Figure 1 on page 2 and Figure 2 on page 3. 9V < V_{DD} < 16V, R_{TD} = 51.1kΩ, C_T = 470pF, T_A = -40°C to +105°C, typical values are at T_A = +25°C. **(Continued)**

Parameter	Test Conditions	Min (Note 5)	Typ	Max (Note 5)	Unit
Input Bias Current		-1	-	1	µA
Pulse Width Modulator					
Minimum Duty Cycle	V_{ERROR} < C_T Offset	-	-	0	%
Maximum Duty Cycle	C_T = 470pF, R_{TD} = 51.1kΩ	-	94	-	%
	C_T = 470pF, R_{TD} = 1.1kΩ	-	99	-	%
V_{ERR} to PWM Comparator Input Gain		-	0.8	-	V/V
C_T to PWM Comparator Input Gain		-	1	-	V/V
SS to PWM Comparator Input Gain		-	0.8	-	V/V
Oscillator					
Charge Current	T_A = +25°C	143	156	170	µA
R_{TD} Voltage		1.925	2	2.075	V
Discharge Current Gain		45	-	65	µA/µA
C_T Valley Voltage		0.75	0.8	0.85	V
C_T Peak Voltage		2.70	2.80	2.90	V
Soft-Start					
Net Charging Current		45	-	68	µA
SS Clamp Voltage		3.8	4.0	4.2	V
Overcurrent Shutdown Threshold Voltage		-	3.9	-	V
Overcurrent Discharge Current		12	15	23	µA
Reset Threshold Voltage		0.25	0.27	0.31	V
Output					
High-Level Output Voltage (V_{OH})	V_{DD} - V_{OUTA} or V_{OUTB}, I_{OUT} = -100mA	-	0.5	2.0	V
Low-Level Output Voltage (V_{OL})	I_{OUT} = 100mA	-	0.5	1.0	V
Rise Time	C_{GATE} = 1nF, V_{DD} = 12V	-	17	60	ns
Fall Time	C_{GATE} = 1nF, V_{DD} = 12V	-	20	60	ns
Thermal Protection					
Thermal Shutdown		-	145	-	°C
Thermal Shutdown Clear		-	130	-	°C
Hysteresis, Internal Protection		-	15	-	°C

Notes:

5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
6. All voltages are to be measured with respect to GND, unless otherwise specified.

3. Typical Performance Curves

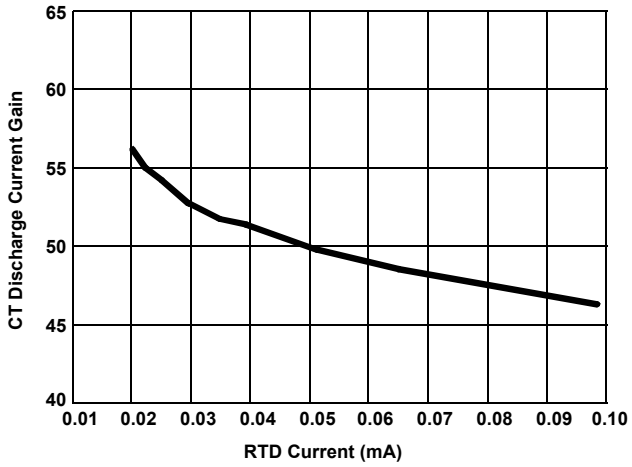


Figure 3. Oscillator C_T Discharge Current Gain

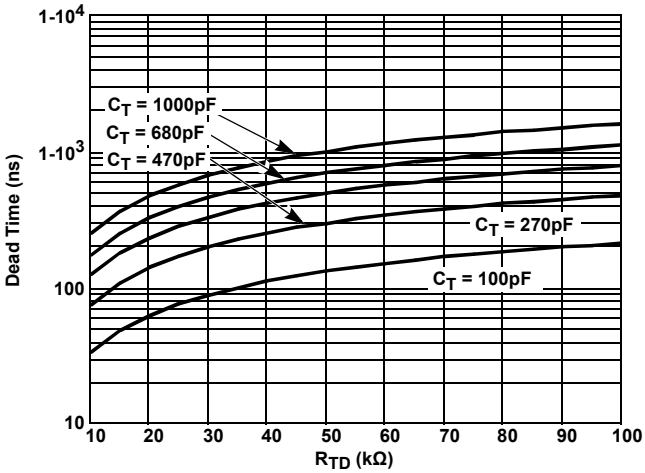


Figure 4. Dead Time vs Capacitance

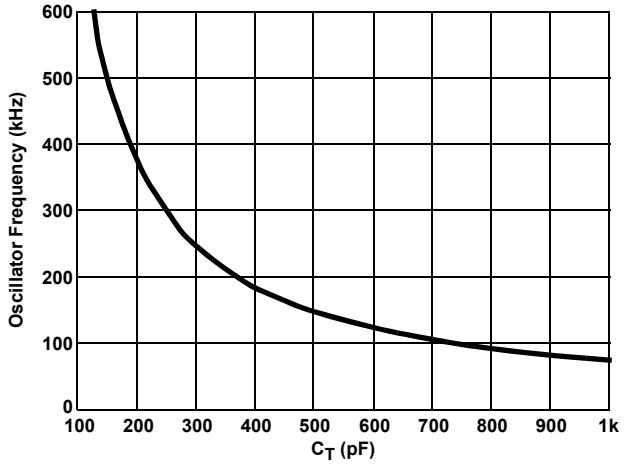


Figure 5. Capacitance vs Oscillator Frequency (R_{TD} = 49.9kΩ)

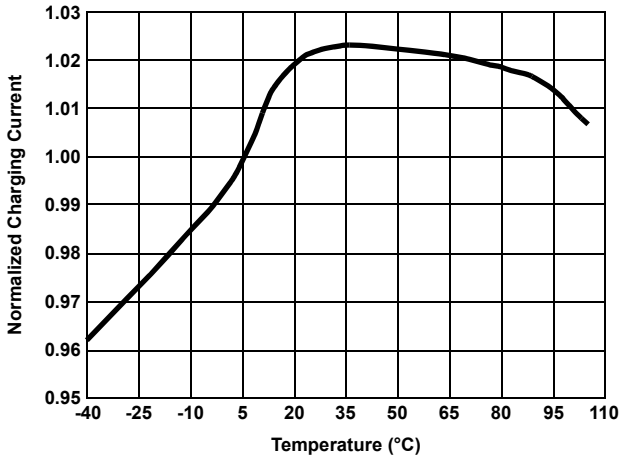


Figure 6. Charge Current vs Temperature

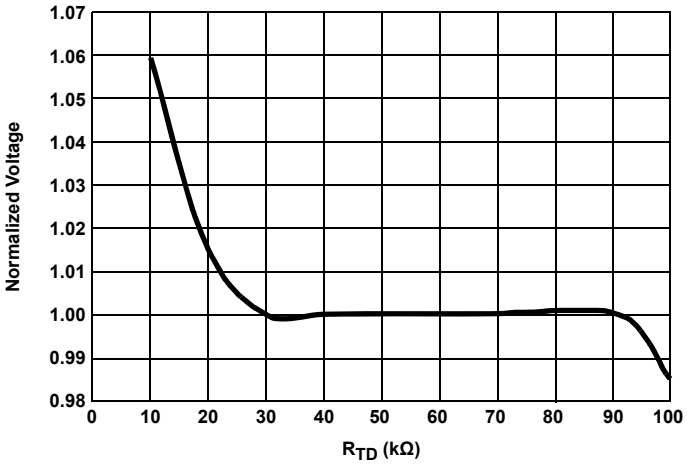


Figure 7. Timing Capacitor Voltage vs R_{TD}

4. Functional Description

4.1 Features

The ISL6745A PWM is an excellent choice for low cost bridge topologies for applications requiring accurate frequency and dead time control. Among its many features are 1A FET drivers, adjustable soft-start, overcurrent protection, and internal thermal protection, allowing a highly flexible design with minimal external components.

4.2 Oscillator

The ISL6745A has an oscillator with a frequency range to 2MHz, programmable using a resistor R_{TD} and capacitor C_T.

The switching period may be considered to be the sum of the timing capacitor charge and discharge durations. The charge duration is determined by C_T and the internal current source (assumed to be 160µA in the formula). The discharge duration is determined by R_{TD} and C_T.

$$T_C \approx 1.25 \times 10^4 \bullet C_T \quad s \qquad \text{(EQ. 2)}$$

$$T_D \approx \frac{1}{CTDischargeCurrentGain} \bullet R_{TD} \bullet C_T \quad s \qquad \text{(EQ. 3)}$$

$$T_{OSC} = T_C + T_D = \frac{1}{F_{OSC}} \quad s \qquad \text{(EQ. 4)}$$

where T_C and T_D are the approximate charge and discharge times, respectively, T_{OSC} is the oscillator free running period, and F_{OSC} is the oscillator frequency. One output switching cycle requires two oscillator cycles. The actual times will be slightly longer than calculated due to internal propagation delays of approximately 5ns/transition. This delay adds directly to the switching duration, and also causes overshoot of the timing capacitor peak and valley voltage thresholds, effectively increasing the peak-to-peak voltage on the timing capacitor. Additionally, if very low charge and discharge currents are used, there will be an increased error due to the input impedance at the C_T pin.

The above formulae help with the estimation of the frequency. Practically, effects like stray capacitances that affect the overall C_T capacitance, variation in R_{TD} voltage and charge current over-temperature, etc. exist, and are best evaluated in-circuit. (EQ. 2) follows from the basic capacitor current equation.

$$i = C \times \frac{dV}{dt}$$

In this case, with variation in dV with R_{TD} (Figure 7 on page 8), and in charge current (Figure 6 on page 8), results from (EQ. 2) would differ from the calculated frequency. The typical performance curves may be used as a tool along with the previous equations as a more accurate tool to estimate the operating frequency more accurately.

The maximum duty cycle, D, and dead time, DT, can be calculated from:

$$D = T_C / T_{OSC} \qquad \text{(EQ. 5)}$$

$$DT = (1 - D) \cdot T_{OSC} \quad s \qquad \text{(EQ. 6)}$$

4.3 Soft-Start Operation

The ISL6745A features a soft-start using an external capacitor in conjunction with an internal current source. Soft-start reduces stresses and surge currents during start-up.

The oscillator capacitor signal, C_T, is compared to the soft-start voltage, SS, in the SS comparator which drives the PWM latch. While the SS voltage is less than 3.5V, duty cycle is limited. The output pulse width increases as the soft-start capacitor voltage increases up to 3.5V. This has the effect of increasing the duty cycle from zero to the maximum pulse width during the soft-start period. When the soft-start voltage exceeds 3.5V, soft-start is completed. Soft-start occurs during start-up and after recovery from an overcurrent shutdown. The soft-start voltage is clamped to 4V.

Please note the capacitance of the soft-start capacitor, C_{SS}. If $C_{SS} \geq 0.1\mu F$, the user will need to add a resistor in series with the capacitor, 100Ω/µF (100Ω at least; 1k at most).

4.4 Gate Drive

The ISL6745A is capable of sourcing and sinking 1A peak current, and may also be used in conjunction with a MOSFET driver such as the ISL6700 for level shifting. To limit the peak current through the IC, an external resistor may be placed between the totem-pole output of the IC (OUTA or OUTB pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

4.5 Overcurrent Operation

Overcurrent delayed shutdown is enabled once the soft-start cycle is complete. If an overcurrent condition is detected, the soft-start charging current source is disabled and the soft-start capacitor is allowed to discharge through a 15µA source. At the same time a 50µs retriggerable one-shot timer is activated. It remains active for 50µs after the overcurrent condition ceases. If the soft-start capacitor discharges to 3.9V, the output is disabled. This state continues until the soft-start voltage reaches 270mV, at which time a new soft-start cycle is initiated. If the overcurrent condition stops at least 50µs prior to the soft-start voltage reaching 3.9V, the soft-start charging currents revert to normal operation and the soft-start voltage is allowed to recover.

4.6 Thermal Protection

An internal temperature sensor protects the device if the junction temperature exceeds +145°C. There is approximately +15°C of hysteresis.

4.7 Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. V_{DD} should be bypassed directly to GND with good high-frequency capacitance.

5. Revision History

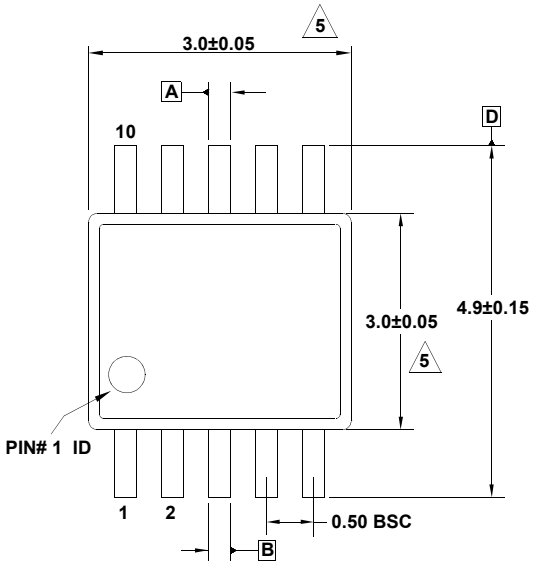
Rev.	Date	Description
2.00	Aug 14, 2017	Applied new formatting. Added Related Literature section. Updated Ordering information table. Update Absolute Maximum Ratings minimum values for Supply Voltage, OUTA, OUTB, and Signal Pins. Added Notes 3 and 6. Removed old Note 3 on EC table along with references as Note 6 covers this statement. Moved Pin Descriptions to table following Pin Configuration. Updated the Soft-Start Operation section on page 10. Added Revision History and About Intersil sections. Updated POD M10.118 to the latest revision. The updates are as follows: -Updated to new POD template. Added land pattern.

6. Package Outline Drawing

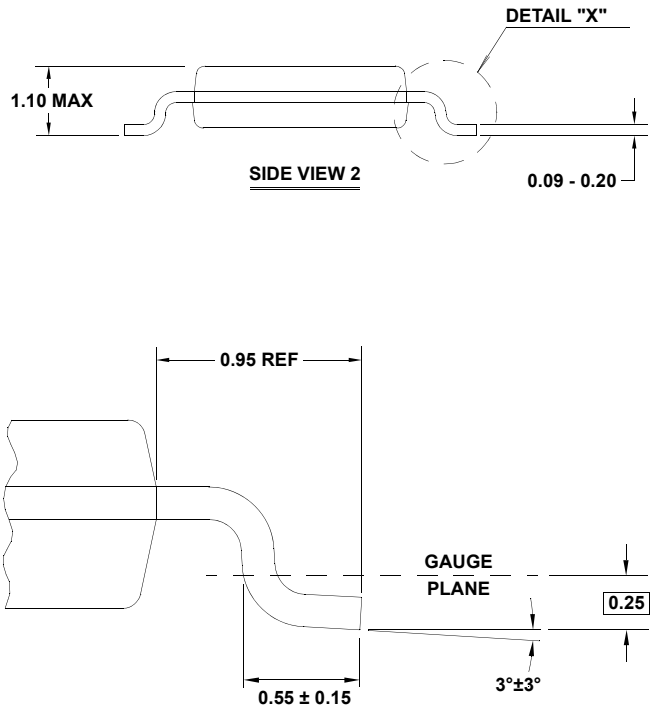
M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE
Rev 1, 4/12

For the most recent package outline drawing, see M10.118.



TOP VIEW



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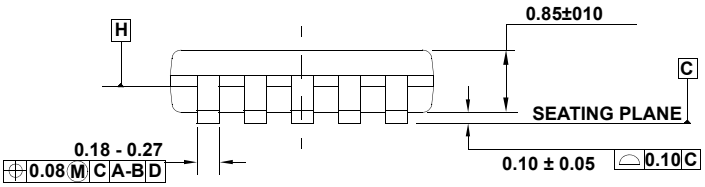
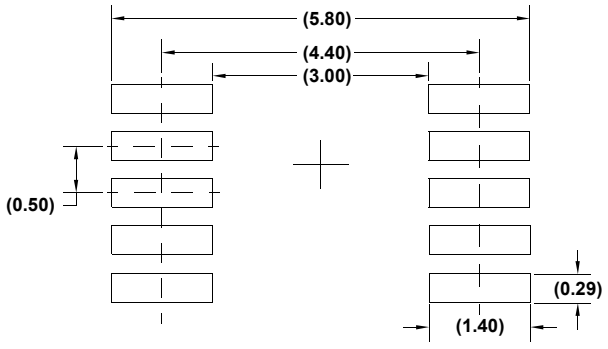


SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

7. About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit: www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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