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National Semiconductor

March 2006

LM5025B
Active Clamp Voltage Mode PWM Controller

General Description

The LM5025B is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025B are as follows:

- The maximum PWM duty cycle is limited to less than 75% to reduce voltage stress on the power MOSFETs.
- The CS2 hiccup mode threshold is increased to 0.5V
- The CS2 filter discharge device is disabled
- The V_{CC} regulator continues to operate when the line UVLO is below the threshold of normal operation
- The V_{REF} regulator is switched off when the line UVLO input falls below the operating threshold
- The internal 5kΩ COMP pin pull-up resistor is removed

The LM5025B PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp / Reset technique. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1MHz and total PWM and current sense propagation delays less than 100ns.

The LM5025B includes a high-voltage start-up regulator that operates over a wide input range of 13V to 100V. Additional features include: Line Under Voltage Lockout (UVLO), soft-start, oscillator UP/DOWN sync capability, precision reference and thermal shutdown.

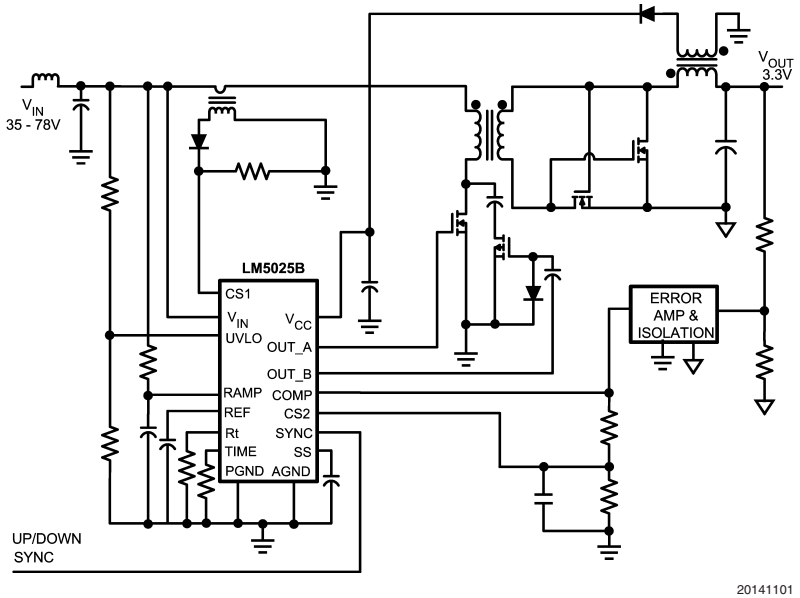
Features

- Internal start-up bias regulator
- 3A compound main gate driver
- Programmable line under-voltage lockout (UVLO) with adjustable hysteresis
- Voltage mode control with feed-forward
- Adjustable dual mode over-current protection
- Programmable overlap or deadtime between the main and active clamp outputs
- Volt x Second maximum duty cycle clamp
- Programmable soft-start
- Current sense leading edge blanking
- Single resistor programmable oscillator
- Oscillator up / down sync capability
- Precision 5V reference
- Thermal shutdown

Packages

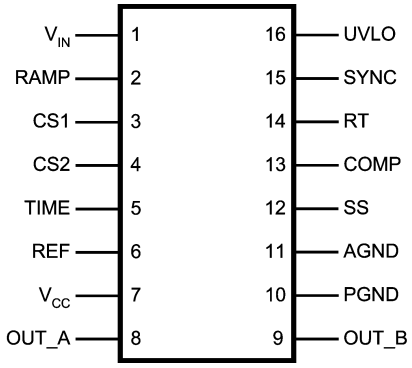
- TSSOP-16
- LLP-16 (5x5 mm) Thermally Enhanced

Typical Application Circuit



Simplified Active Clamp Forward Power Converter

Connection Diagram



16-Lead TSSOP, LLP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5025BMTC	TSSOP-16	MTC-16	92 Units per anti-static tube
LM5025BMTCX	TSSOP-16	MTC-16	2500 Units on Tape and Reel
LM5025BSD	LLP-16	SDA-16A	1000 Units on Tape and Reel
LM5025BSDX	LLP-16	SDA-16A	4500 Units on Tape and Reel

Pin Descriptions

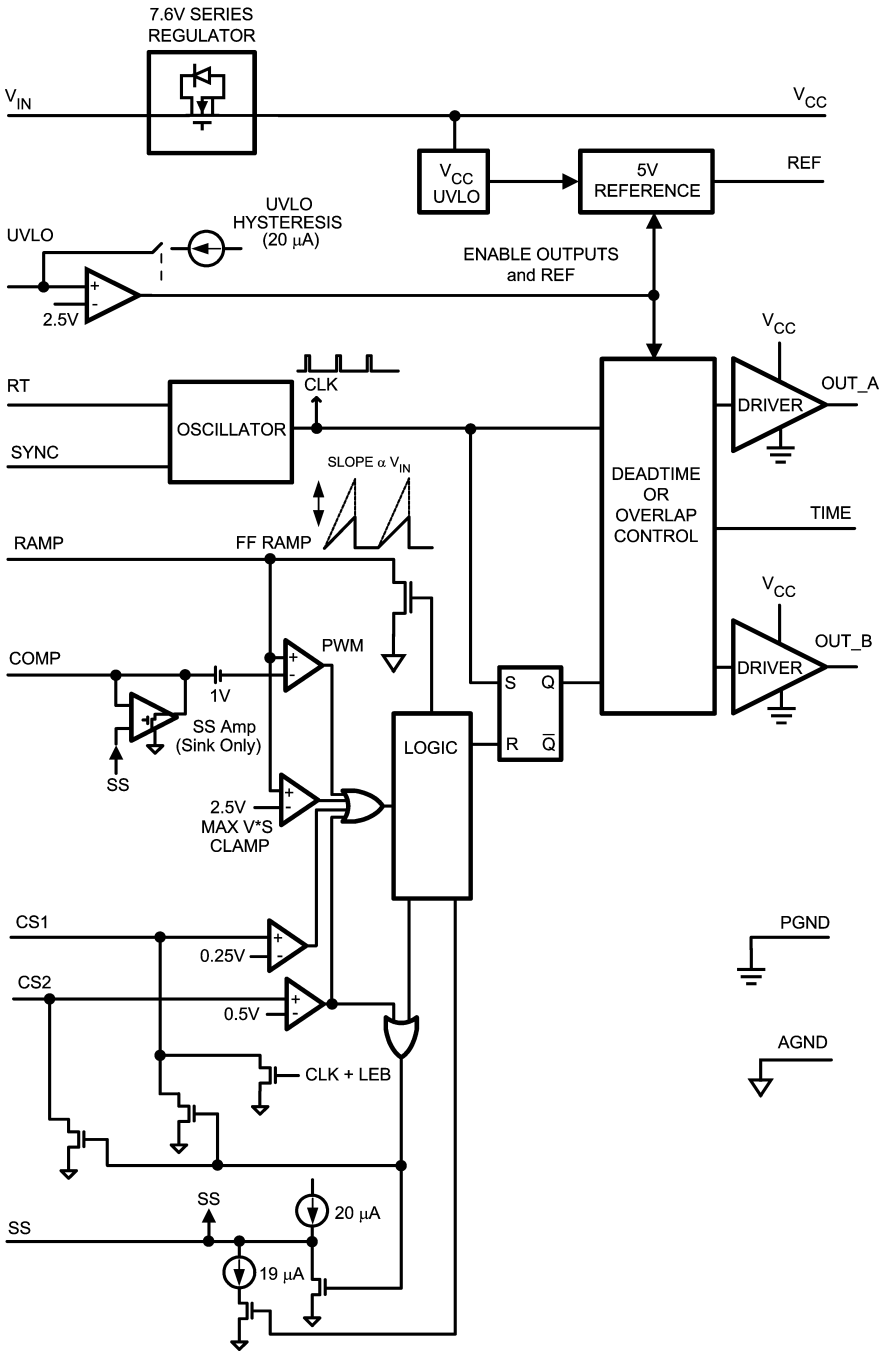
Pin	Name	Description	Application Information
1	V_{IN}	Source Input Voltage	Input to start-up regulator. Input range 13V to 100V, with transient capability to 105V.
2	RAMP	Modulator ramp signal	An external RC circuit from Vin sets the ramp slope. This pin is discharged at the conclusion of every cycle by an internal FET, initiated by either the internal clock or the V*Sec Clamp comparator.
3	CS1	Current sense input for cycle-by-cycle limiting	If CS1 exceeds 0.25V the outputs will go into Cycle-by-Cycle current limit. CS1 is held low for 50ns after OUT_A switches high providing leading edge blanking.
4	CS2	Current sense input for soft restart	If CS2 exceeds 0.5V the outputs will be disabled and a softstart commenced. The soft-start capacitor will be fully discharged and then released with a pull-up current of 1µA. After the first output pulse (when SS =1V), the SS charge current will revert back to 20µA.
5	TIME	Output overlap/Deadtime control	An external resistor (R_{SET}) sets either the overlap time or dead time for the active clamp output. An R_{SET} resistor connected between TIME and GND produces in-phase OUT_A and OUT_B pulses with overlap. An R_{SET} resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
6	REF	Precision 5 volt reference output	Maximum output current: 10mA Locally decouple with a 0.1µF capacitor. Reference stays low until the V_{CC} UV comparator and line UVLO comparator are satisfied.

Pin Descriptions (Continued)

Pin	Name	Description	Application Information
7	V_{CC}	Output from the internal high voltage start-up regulator. The V_{CC} voltage is regulated to 7.6V.	If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, reducing the IC power dissipation.
8	OUT_A	Main output driver	Output of the main switch PWM output gate driver. Output capability of 3A peak sink current.
9	OUT_B	Active Clamp output driver	Output of the Active Clamp switch gate driver. Capable of 1.25A peak sink current..
10	PGND	Power ground	Connect directly to analog ground.
11	AGND	Analog ground	Connect directly to power ground.
12	SS	Soft-start control	An external capacitor and an internal 20µA current source set the soft-start ramp. The SS current source is reduced to 1uA following a CS2 over-current event or an over temperature event.
13	COMP	Input to the Pulse Width Modulator	PWM duty cycle is controlled by the voltage applied to the COMP pin. The COMP pin voltage is reduced by a fixed 1V offset and compared with the RAMP pin signal.
14	RT	Oscillator timing resistor pin	An external resistor connected from RT to ground sets the internal oscillator frequency.
15	SYNC	Oscillator UP/DOWN synchronization input	The internal oscillator can be synchronized to an external clock with a frequency 20% lower than the internal oscillator's free running frequency. There is no constraint on the maximum sync frequency.
16	UVLO	Line Under-Voltage shutdown	An external voltage divider from the power source sets the shutdown comparator levels. The comparator threshold is 2.5V. Hysteresis is set by an internal current source (20µA) that is switched on or off as the UVLO pin potential crosses the 2.5V threshold.
-	EP	Exposed PAD, underside of the LLP package option	Internally bonded to the die substrate. Connect to GND potential with low thermal impedance.

Block Diagram

Simplified Block Diagram



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN} to GND	-0.3V to 105V
V_{CC} to GND	-0.3V to 16V
CS1, CS2 to GND	-0.3 to 1.00V
All other inputs to GND	-0.3 to 7V
ESD Rating (Note 2)	
Human Body Model	2kV
Storage Temperature Range	-55˚C to 150˚C
Junction Temperature	150˚C

Operating Ratings (Note 1)

V_{IN} Voltage	13 to 100V
External Voltage Applied to V_{CC}	8 to 15V
Operating Junction Temperature	-40˚C to +125˚C

Electrical Characteristics

Specifications with standard typeface are for T_J = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, V_{CC} = 10V, RT = 26.7kΩ, R_{SET} = 27.4kΩ) unless otherwise stated (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Startup Regulator						
V_{CC} Reg	V_{CC} Regulation	No Load	**7.3**	7.6	**7.9**	V
	V_{CC} Current Limit	(Note 4)	**20**	25		mA
I-V_{IN}	Startup Regulator Leakage (external Vcc Supply)	V_{IN} = 100V		165	**500**	µA
V_{CC} Supply						
	V_{CC} Under-voltage Lockout Voltage (positive going V_{cc})		**V_{CC} Reg - 220mV**	V_{CC} Reg - 120mV		V
	V_{CC} Under-voltage Hysteresis		**1.0**	1.5	**2.0**	V
	V_{CC} Supply Current (I_{CC})	C_{gate} = 0			**4.2**	mA
Reference Supply						
V_{REF}	Ref Voltage	I_{REF} = 0 mA	**4.85**	5	**5.15**	V
	Ref Voltage Regulation	I_{REF} = 0 to 10mA		25	**50**	mV
	Ref Current Limit		**10**	20		mA
Current Limit						
CS1 Prop	CS1 Delay to Output	CS1 Step from 0 to 0.4V Time to onset of OUT Transition (90%) C_{gate} = 0		40		ns
CS2 Prop	CS2 Delay to Output	CS2 Step from 0 to 0.6V Time to onset of OUT Transition (90%) C_{gate} = 0		50		ns
	Cycle by Cycle Threshold Voltage (CS1)		**0.22**	0.25	**0.28**	V
	Cycle Skip Threshold Voltage (CS2)	Resets SS capacitor; auto restart	**0.45**	0.5	**0.55**	V
	Leading Edge Blanking Time (CS1)			50		ns
	CS1 Sink Impedance (clocked)	CS1 = 0.2V		30	**50**	Ω
	CS1 Sink Impedance (Post Fault Discharge)	CS1 = 0.3V		55	**95**	Ω

Electrical Characteristics (Continued)

Specifications with standard typeface are for T_J = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, V_{CC} = 10V, RT = 26.7kΩ, R_{SET} = 27.4kΩ) unless otherwise stated (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	CS2 Sink Impedance (Post Fault Discharge)	CS2 = 0.6V		55	**95**	Ω
	CS1 and CS2 Leakage Current	CS = CS Threshold - 100mV			**1**	µA
Soft-Start						
	Soft-start Current Source Normal		**17**	22	**27**	µA
	Soft-start Current Source following a CS2 event		**0.5**	1	**1.5**	µA
Oscillator						
	Frequency1	T_A = 25˚C $T_J = T_{low}$ to T_{high}	180 **175**	200	220 **225**	kHz
	Frequency2	RT = 13.3 kΩ $T_J = T_{low}$ to T_{high} T_J = 0˚C to 125˚C	 **360** **364**	400	 **440** **436**	kHz
	Sync threshold			2		V
	Min Sync Pulse Width				**100**	ns
	Sync Frequency Range		**160**			kHz
PWM Comparator						
	Delay to Output	COMP step 5V to 0V Time to onset of OUT_A transition low		40		ns
	Maximum Duty Cycle 1	Measured at OUT_A		73		%
	Maximum Duty Cycle 2	Measured at OUT_A; RT = 13.3K	**66**	71	**75**	%
	COMP to PWM Offset		**0.75**	1	**1.15**	V
	COMP Input Current	COMP = 4V, SS open		50	**80**	µA
Volt x Second Clamp						
	Ramp Clamp Level	Delta RAMP measured from onset of OUT_A to Ramp peak. COMP = 5V	**2.4**	2.5	**2.6**	V
UVLO Shutdown						
	Undervoltage Shutdown Threshold		**2.44**	2.5	**2.56**	V
	Undervoltage Shutdown Hysteresis		**16**	20	**24**	µA
Output Section						
	OUT_A High Saturation	MOS Device @ Iout = -10mA,		5	**10**	Ω
	OUTPUT_A Peak Current Sink	Bipolar Device @ Vcc/2		3		A
	OUT_A Low Saturation	MOS Device @ Iout = 10mA,		6	**9**	Ω
	OUTPUT_A Rise Time	C_{gate} = 2.2nF		20		ns
	OUTPUT_A Fall Time	C_{gate} = 2.2nF		15		ns

Electrical Characteristics (Continued)

Specifications with standard typeface are for T_J = 25˚C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, V_{CC} = 10V, RT = 26.7kΩ, R_{SET} = 27.4kΩ) unless otherwise stated (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	OUT_B High Saturation	MOS Device @ Iout = -10mA,		10	**20**	Ω
	OUTPUT_B Peak Current Sink	Bipolar Device @ Vcc/2		1		A
	OUT_B Low Saturation	MOS Device @ Iout = 10mA,		12	**18**	Ω
	OUTPUT_B Rise Time	C_{gate} = 1nF		20		ns
	OUTPUT_B Fall Time	C_{gate} = 1nF		15		ns
Output Timing Control						
	Overlap Time	R_{SET} = 38 kΩ connected to GND, 50% to 50% transitions	**75**	105	**135**	ns
	Deadtime	R_{SET} = 29.5 kΩ connected to REF, 50% to 50% transitions	**75**	105	**135**	ns
Thermal Shutdown						
T_{SD}	Thermal Shutdown Threshold			165		˚C
	Thermal Shutdown Hysteresis			25		˚C
Thermal Resistance						
θ_{JA}	Junction to Ambient	MTC Package		125		˚C/W
		SDA Package		32		˚C/W
θ_{JC}	Junction to Case	MTC Package		30		˚C/W
		SDA Package		5		˚C/W

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

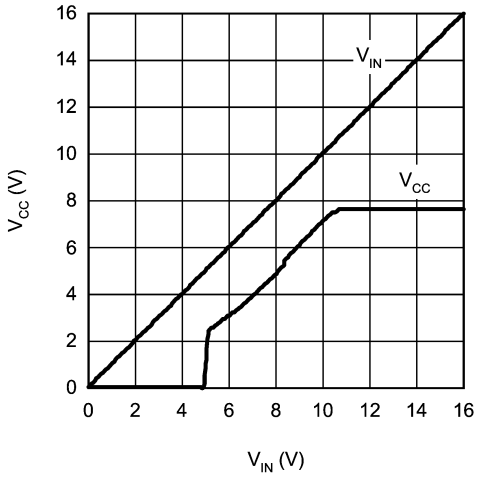
Note 2: For detailed information on soldering plastic TSSOP and LLP packages, refer to the Packaging Data Book available from National Semiconductor Corporation.

Note 3: All limits are guaranteed. All electrical characteristics having room temperature limits are tested during production with $T_A = T_J$ = 25˚C. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 4: Device thermal limitations may limit usable range.

Typical Performance Characteristics

V_{CC} Regulator Start-up Characteristics, V_{CC} vs Vin



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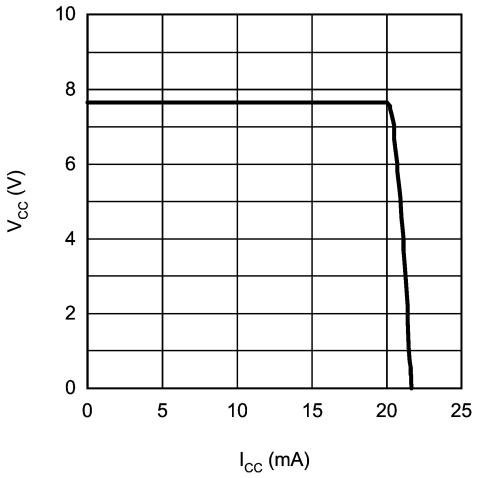
V_{CC} vs I_{CC}



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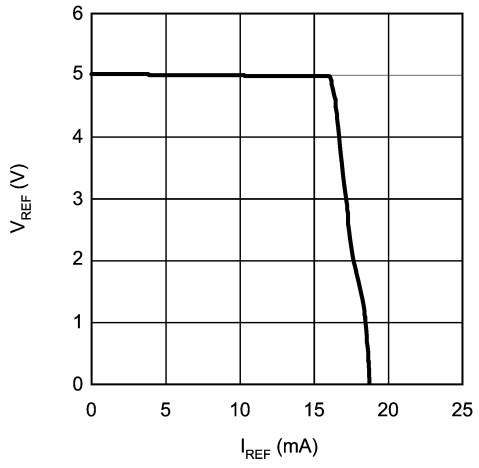
V_{REF} vs I_{REF}



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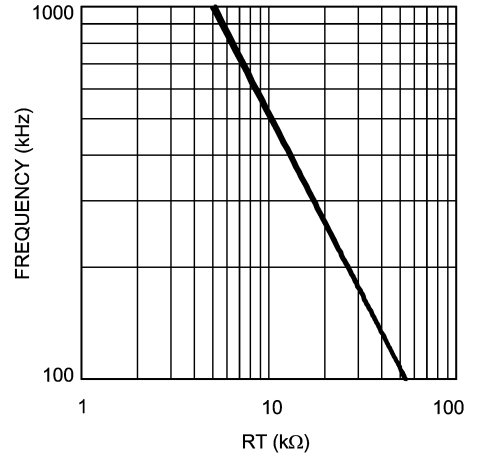
Oscillator Frequency vs RT



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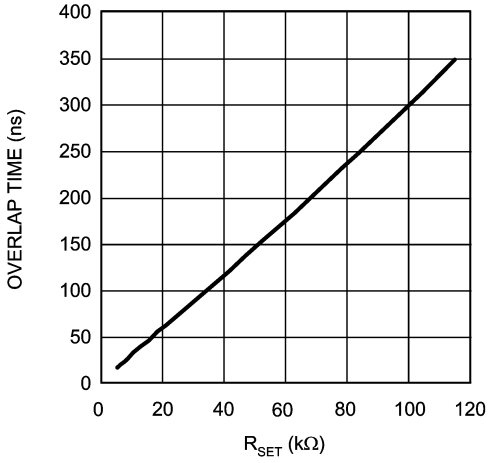
Overlap Time vs R_{SET}



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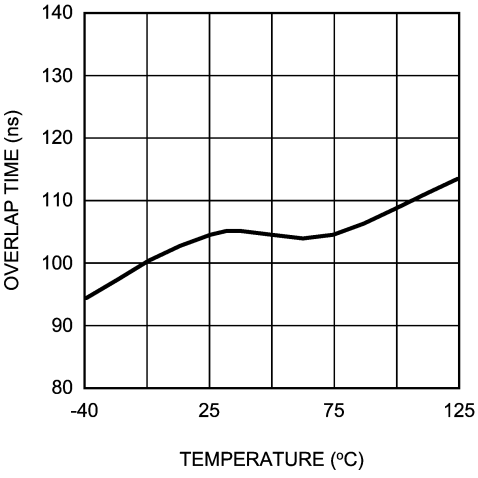
Overlap Time vs Temperature
R_{SET} = 38K



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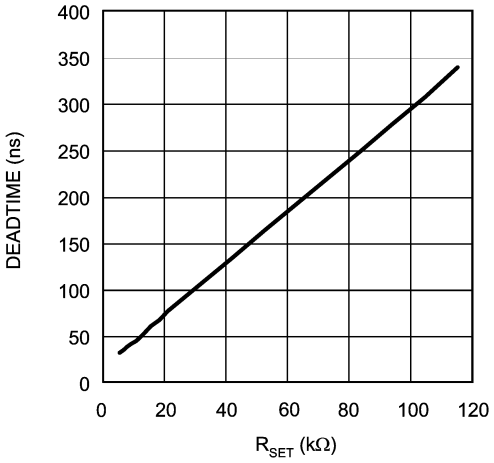
Typical Performance Characteristics (Continued)

Dead Time vs R_{SET}



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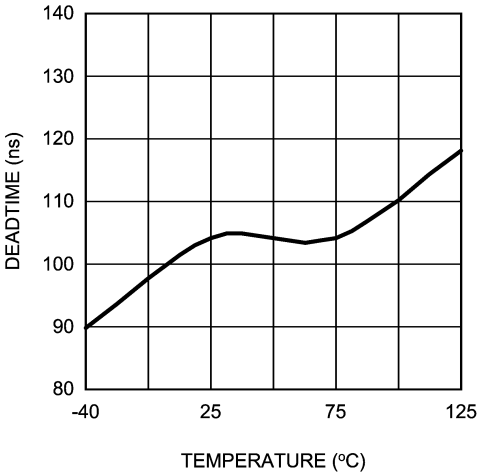
Dead Time vs Temperature
R_{SET} = 29.5K



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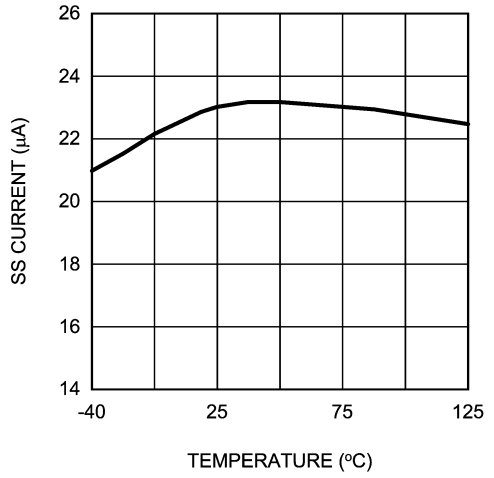
SS Pin Current vs Temperature



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Detailed Operating Description

The LM5025B is a functional variant of the LM5025 active clamp PWM controller. The functional differences of the LM5025B are as follows:

- The maximum PWM duty cycle is limited to less than 75% to reduce voltage stress on the power MOSFETs
- The CS2 hiccup mode threshold is increased to 0.5V
- The CS2 filter discharge device is disabled
- The V_{CC} regulator continues to operate when the line UVLO is below the threshold of normal operation
- The V_{REF} regulator is switched off when the line UVLO input falls below the operating threshold
- The internal 5kΩ COMP pin pull-up resistor is removed

The LM5025B PWM controller contains all of the features necessary to implement power converters utilizing the Active Clamp Reset technique. The device can be configured to control either a P-Channel clamp switch or an N-Channel clamp switch. With the active clamp technique higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp / reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The active clamp output can be configured for either a guaranteed overlap time (for P-Channel switch applications) or a guaranteed dead time (for N_Channel applications). The two internal compound gate drivers parallel both MOS and Bipolar devices, providing superior gate drive characteristics. This controller is designed for high-speed operation including an oscillator frequency range up to 1MHz and total PWM and current sense propagation delays less than 100ns. The LM5025B includes a high-voltage start-up regulator that operates over a wide input range of 13V to 100V. Additional features include: Line Under Voltage Lockout (UVLO), softstart, oscillator UP/DOWN sync capability, precision reference and thermal shutdown.

High Voltage Start-Up Regulator

The LM5025B contains an internal high voltage start-up regulator that allows the input pin (V_{IN}) to be connected directly to the line voltage. The regulator output is internally current limited to 20mA. When power is applied, the regulator is enabled and sources current into an external capacitor connected to the V_{CC} pin. The recommended capacitance range for the V_{CC} regulator is 0.1µF to 100µF. When the voltage on the V_{CC} pin reaches the regulation point of 7.6V and the internal voltage reference (REF) reaches its regulation point of 5V, the controller outputs are enabled. The outputs will remain enabled until V_{CC} falls below 6.2V or the line Under Voltage Lock Out detector indicates that V_{IN} is out of range. In typical applications, an auxiliary transformer winding is connected through a diode to the V_{CC} pin. This winding must raise the V_{CC} voltage above 8V to shut off the internal start-up regulator. Powering V_{CC} from an auxiliary winding improves efficiency while reducing the controller power dissipation.

When the converter auxiliary winding is inactive, external current draw on the V_{CC} line should be limited so the power dissipated in the start-up regulator does not exceed the maximum power dissipation of the controller.

An external start-up regulator or other bias rail can be used instead of the internal start-up regulator by connecting the V_{CC} and the V_{IN} pins together and feeding the external bias voltage into the two pins.

Line Under-Voltage Detector

The LM5025B contains a line Under Voltage Lock Out (UVLO) circuit. An external set-point voltage divider from Vin to GND, sets the operational range of the converter. The divider must be designed such that the voltage at the UVLO pin will be greater than 2.5V when Vin is in the desired operating range. If the undervoltage threshold is not met, both outputs and the VREF regulator are disabled. The VCC regulator is not disabled by UVLO. UVLO hysteresis is accomplished with an internal 20uA current source that is switched on or off into the impedance of the set-point divider. When the UVLO threshold is exceeded, the current source is activated to instantly raise the voltage at the UVLO pin. When the UVLO pin voltage falls below the 2.5V threshold, the current source is turned off causing the voltage at the UVLO pin to fall. The UVLO pin can also be used to implement a remote enable / disable function. Pulling the UVLO pin below the 2.5V threshold disables the PWM outputs.

PWM Outputs

The relative phase of the main (OUT_A) and active clamp outputs (OUT_B) can be configured for the specific application. For active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase with the active clamp output overlapping the main output. For active clamp configurations utilizing a high side N-Channel switch, the active clamp output should be out of phase with main output and there should be a dead time between the two gate drive pulses. A distinguishing feature of the LM5025B is the ability to accurately configure either dead time (both off) or overlap time (both on) of the gate driver outputs. The overlap / deadtime magnitude is controlled by the resistor value connected to the TIME pin of the controller. The opposite end of the resistor can be connected to either REF for deadtime control or GND for overlap control. The internal configuration detector senses the connection and configures the phase relationship of the main and active clamp outputs. The magnitude of the overlap/dead time can be calculated as follows:

Overlap Time (ns) = 2.8 x R_{SET} - 1.2

Dead Time (ns) = 2.9 x R_{SET} +20

R_{SET} in kΩ, Time in ns

PWM Outputs (Continued)

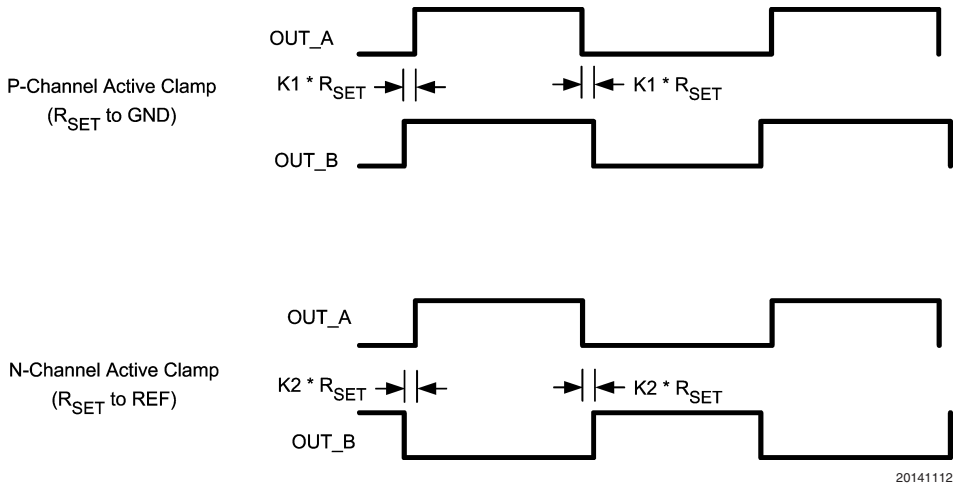
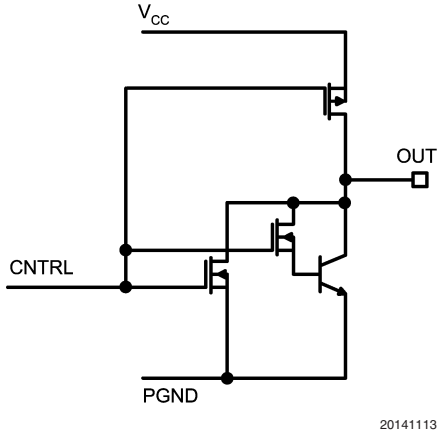


FIGURE 1.

Compound Gate Drivers

The LM5025B contains two unique compound gate drivers, which parallel both MOS and Bipolar devices to provide high drive current throughout the entire switching event. The Bipolar device provides most of the drive current capability and provides a relatively constant sink current which is ideal for driving large power MOSFETs. As the switching event nears conclusion and the Bipolar device saturates, the internal MOS device continues to provide a low impedance to compete the switching event.

During turn-off at the Miller plateau region, typically around 2V - 3V, is where gate driver current capability is needed most. The resistive characteristics of all MOS gate drivers are adequate for turn-on since the supply to output voltage differential is fairly large at the Miller region. During turn-off however, the voltage differential is small and the current source characteristic of the Bipolar gate driver is beneficial to provide fast drive capability.



PWM Comparator

The PWM comparator compares the ramp signal (RAMP) to the loop error signal (COMP). This comparator is optimized for speed in order to achieve minimum controllable duty cycles. The COMP pin is a high impedance comparator input. If the opto coupler is connected between the COMP pin and ground, then a pull-up resistor must be added between COMP and REF to bias the opto coupler transistor. The comparator polarity is such that 0V on the COMP pin will produce a zero duty cycle on both gate driver outputs.

Volt x Second Clamp

The Volt x Second Clamp comparator compares the ramp signal (RAMP) to a fixed 2.5V reference. By proper selection of RFF and CFF, the maximum ON time of the main switch can be set to the desired duration. The ON time set by Volt x Second Clamp varies inversely with the line voltage because the RAMP capacitor is charged by a resistor connected to Vin while the threshold of the clamp is a fixed voltage (2.5V). An example will illustrate the use of the Volt x Second Clamp comparator to achieve a 50% duty cycle limit, at 200KHz, at a 48V line input: A 50% duty cycle at a 200KHz requires a 2.5µs of ON time. At 48V input the Volt x Second product is 120V-µs (48V x 2.5µs). To achieve this clamp level choose RFF and CFF using the following equation:.

$$R_{FF} \times C_{FF} = V_{IN} \times T_{ON} / 2.5V =$$
$$48V \times 2.5\mu s / 2.5V = 48\mu s$$

Select C_{FF} = 470pF

R_{FF} = 102kΩ

The recommended capacitor value range for CFF is 100pF to 1000pF.

The C_{FF} ramp capacitor is discharged at the conclusion of every cycle by an internal discharge switch controlled by either the internal clock or by the Volt x Second Clamp comparator, whichever event occurs first.

Maximum Duty Cycle

At low line input voltages, the Volt x Second clamp will not limit the maximum PWM duty cycle because the RAMP signal does not charge to the 2.5V threshold voltage within the period of the PWM clock. In this case, the maximum duty cycle is determined by the internal PWM clock and the output overlap or deadtime programmed by the resistor RSET connected to the TIME pin. Referring to *Figure 1*, the initial transition of OUT_B corresponds to the leading edge

Maximum Duty Cycle (Continued)

of the PWM clock. The leading edge of OUT_A is delayed with respect to OUT_B by the overlap time which is determined by the TIME pin resistor (K1 x RSET) When operating at maximum duty cycle, the trailing edge of OUT_A corresponds to the trailing edge of the PWM clock. The duty cycle at OUT_A is therefore always less than the duty cycle of the clock. The internal clock of the LM5025B operates at a nominal duty cycle of 75%. If the clock frequency is 400KHz and the overlap time is set to 100ns, then the maximum PWM duty cycle will be:

Max Duty Cycle = 75% - 100ns x 400KHz = 71%

Current Limit

The LM5025B contains two modes of over-current protection. If the sense voltage at the CS1 input exceeds 0.25V the present power cycle is terminated (cycle-by-cycle current limit). If the sense voltage at the CS2 input exceeds 0.5V, the controller will terminate the present cycle, discharge the softstart capacitor and reduce the softstart current source to 1µA. The softstart (SS) capacitor is released after being fully discharged and slowly charges with a 1µA current source. When the voltage at the SS pin reaches approximately 1V, the PWM comparator will produce the first output pulse at OUT_A. After the first pulse occurs, the softstart current source will revert to the normal 20µA level. Fully discharging and then slowly charging the SS capacitor protects a continuously over-loaded converter with a low duty cycle hiccup mode.

These two modes of over-current protection allow the user great flexibility to configure the system behavior in over-load conditions. If it is desired for the system to act as a current source during an over-load, then the CS1 cycle-by-cycle current limiting should be used. In this case the current sense signal should be applied to the CS1 input and the CS2 input should be grounded. If during an overload condition it is desired for the system to briefly shutdown, followed by soft-start retry, then the CS2 hiccup current limiting mode should be used. In this case the current sense signal should be applied to the CS2 input and the CS1 input should be grounded. This shutdown / soft-start retry will repeat indefinitely while the over-load condition remains. The hiccup mode will greatly reduce the thermal stresses to the system during heavy overloads. The cycle-by-cycle mode will have higher system thermal dissipations during heavy overloads, but provides the advantage of continuous operation for short duration overload conditions.

It is possible to utilize both over-current modes concurrently, whereby momentary overload conditions activate the CS1 cycle-by-cycle mode while prolonged overloading activates the CS2 hiccup mode. Generally the CS1 input will always be configured to monitor the main switch FET current each cycle. The CS2 input can be configured in several different ways depending upon the system requirements.

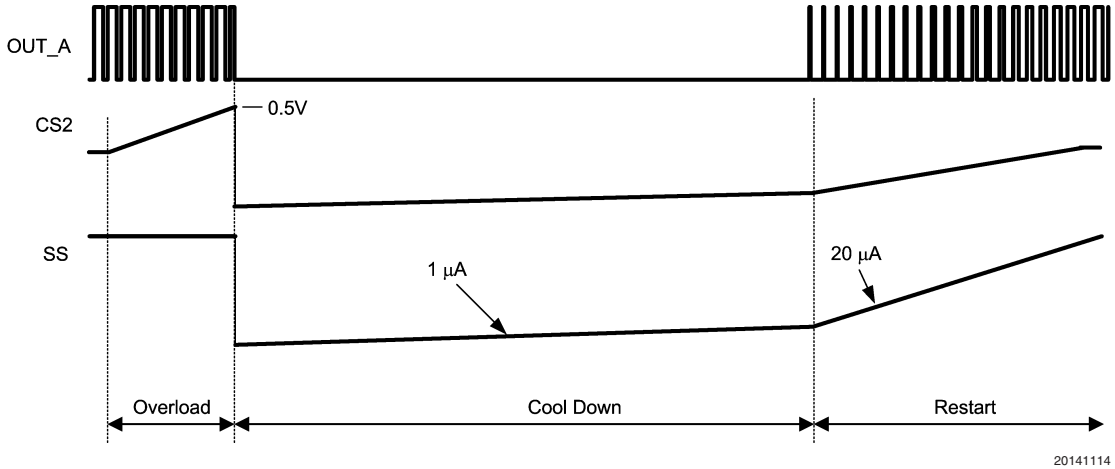
a) The CS2 input can also be set to monitor the main switch FET current except scaled to a higher threshold than CS1

b) An external over-current timer can be configured which trips after a pre-determined over-current time, driving the CS2 input high, initiating a hiccup event.

c) In a closed loop voltage regulaton system, the COMP input will rise to saturation when the cycle-by-cycle current limit is active. An external filter/delay timer and voltage divider can be configured between the COMP pin and the CS2 pin to scale and delay the COMP voltage. If the CS2 pin voltage reaches 0.5V a hiccup event will initiate.

A small RC filter, located near the controller, is recommended for each of the CS pins. The CS1 input has an internal FET which discharges the current sense filter capacitor at the conclusion of every cycle, to improve dynamic performance. This same FET remains on an additional 50ns at the start of each main switch cycle to attenuate the leading edge spike in the current sense signal. The CS2 discharge FET only operates following a CS2 event, UVLO and thermal shutdown.

The LM5025B CS comparators are very fast and may respond to short duration noise pulses. Layout considerations are critical for the current sense filter and sense resistor. The capacitor associated with the CS filter must be placed very close to the device and connected directly to the pins of the IC (CS and GND). If a current sense transformer is used, both leads of the transformer secondary should be routed to the filter network , which should be located close to the IC. If a sense resistor in the source of the main switch MOSFET is used for current sensing, a low inductance type of resistor is required. When designing with a current sense resistor, all of the noise sensitive low power ground connections should be connected together near the IC GND and a single connection should be made to the power ground (sense resistor ground point).



Oscillator and Sync Capability

The LM5025B oscillator is set by a single external resistor connected between the RT pin and GND. To set a desired oscillator frequency (F), the necessary RT resistor can be calculated from:

$$RT = (4960/F)^{1.02}$$

where F is in kHz and RT in kΩ.

The RT resistor should be located very close to the device and connected directly to the pins of the IC (RT and GND).

A unique feature of LM5025B is the ability to synchronize the oscillator to an external clock with a frequency that is either higher or lower than the frequency of the internal oscillator. The lower frequency sync frequency range is 80% of the free running internal oscillator frequency. There is no constraint on the maximum sync frequency. A minimum pulse width of 100ns is required for the synchronization clock . If the synchronization feature is not required, the SYNC pin should be connected to GND to prevent any abnormal interference . The internal oscillator can be completely disabled by connecting the RT pin to REF. Once disabled, the sync signal will act directly as the master clock for the controller. Both the frequency and the maximum duty cycle of the PWM controller can be controlled by the sync signal (within the limitations of the Volt x Second Clamp). The maximum duty cycle (D) will be (1-D) of the sync signal.

Feed-Forward Ramp

An external resistor (R_{FF}) and capacitor (C_{FF}) connected to V_{IN} and GND are required to create the PWM ramp signal. The slope of the signal at the RAMP pin will vary in proportion to the input line voltage. This varying slope provides line feedforward information necessary to improve line transient response with voltage mode control. The RAMP signal is compared to the error signal at the COMP pin by the pulse width modulator comparator to control the duty cycle of the main switch output. The Volt x Second Clamp comparator also monitors the RAMP pin and if the ramp amplitude exceeds 2.5V, the present cycle is terminated. The ramp signal is reset to GND at the end of each cycle by either the internal clock or the Volt x Second comparator, which ever occurs first.

Soft-start

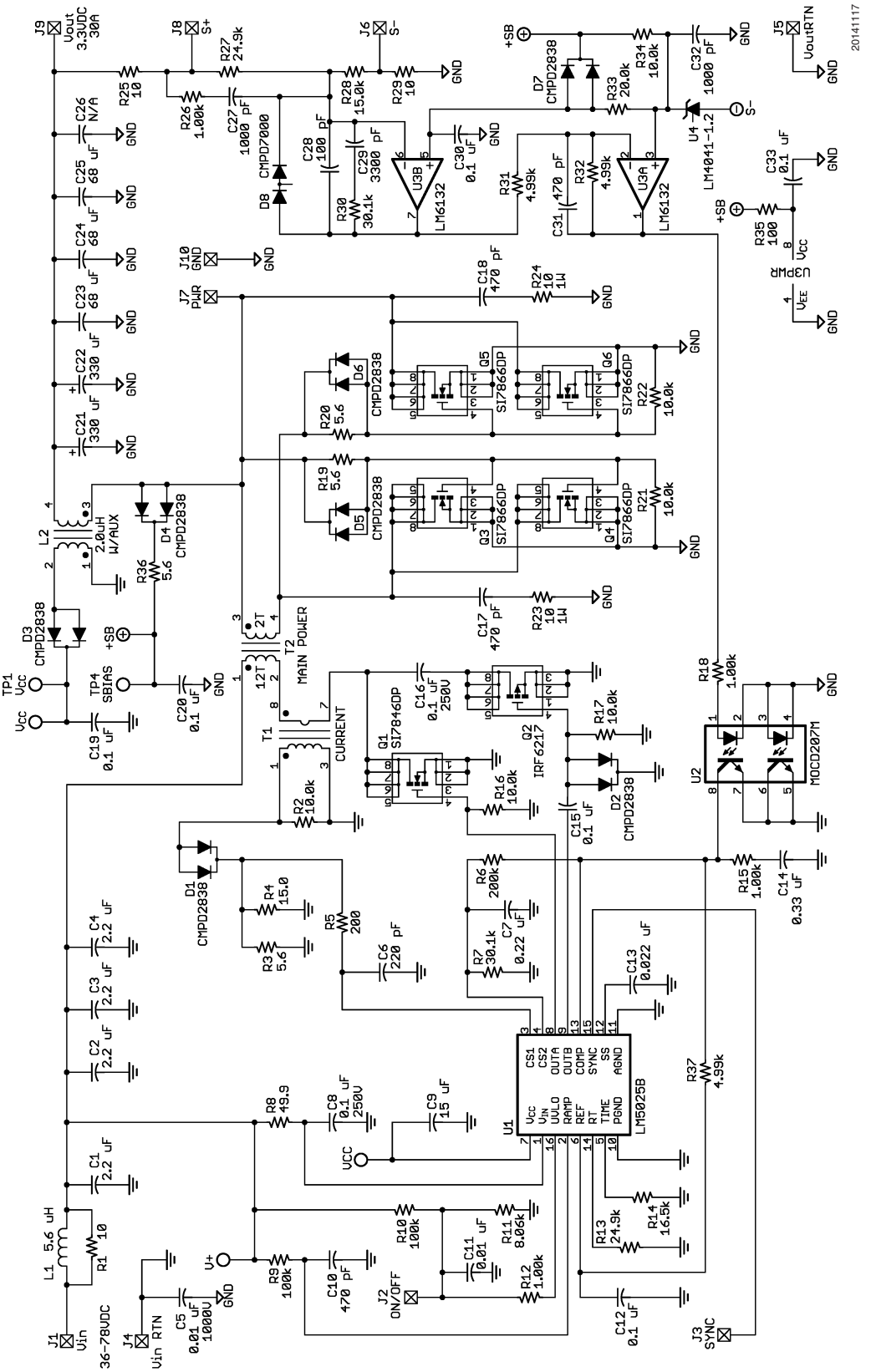
The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. At power on, a 20µA current is sourced out of the soft-start pin (SS) into an external capacitor. The capacitor voltage will ramp up slowly and will limit the COMP pin voltage and therefore the PWM duty cycle. In the event of a fault as determined by V_{CC} undervoltage, line undervoltage (UVLO) or second level current limit, the output gate drivers are disabled and the soft-start capacitor is fully discharged. When the fault condition is no longer present a soft-start sequence will be initiated. Following a second level current limit detection (CS2), the soft-start current source is reduced to 1µA until the first output pulse is generated by the PWM comparator. The current source returns to the nominal 20µA level after the first output pulse (~1V at the SS pin).

The soft-start circuit controls the COMP pin voltage through a unity gain amplifier with an open drain (sink only) output. If the SS pin voltage is less than the PWM control signal applied to the COMP pin, this amplifier will sink current from the external pull-up connected to the COMP pin to force the COMP voltage to follow the soft-start capacitor ramp. When the soft-start capacitor charges to a voltage that is greater than the control voltage applied to the COMP pin, the soft-start amplifier automatically disengages, allowing closed loop control of the PWM duty cycle. The soft-start amplifier output stage is capable of sinking up to 5mA. External pull-up circuits connected to the COMP pin must limit the current into the pin to a value less than 5mA.

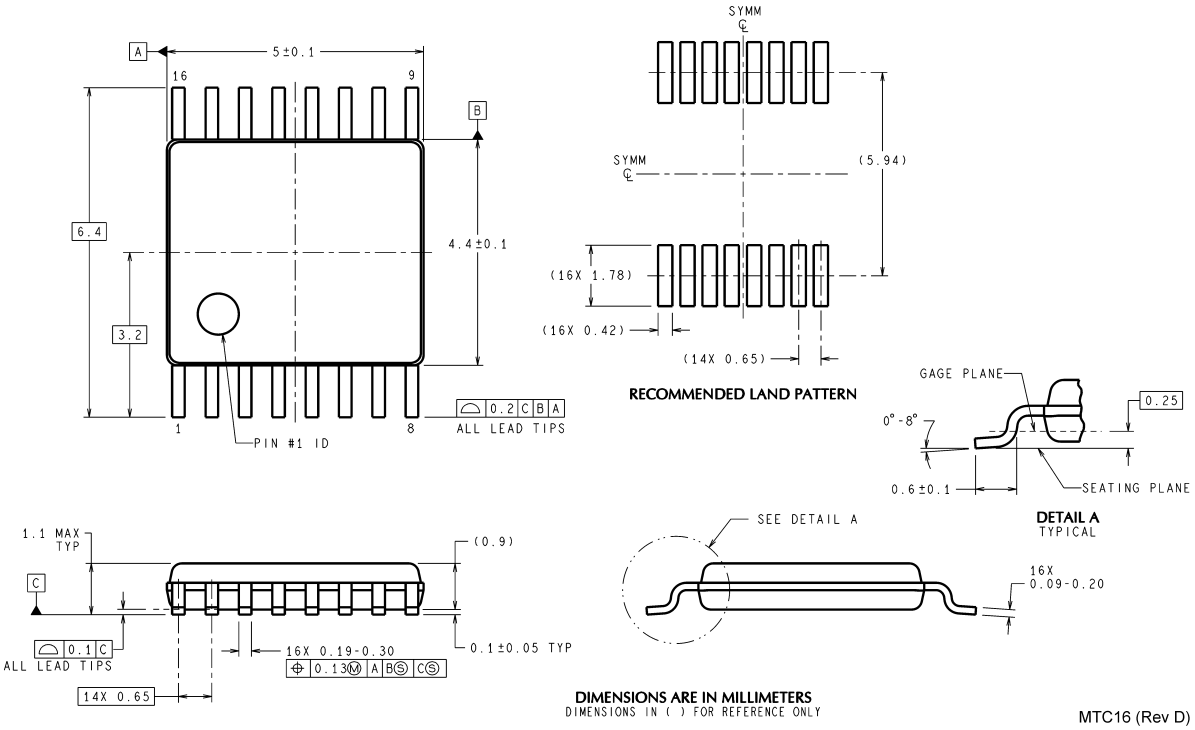
Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165˚C, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart after the thermal hysteresis (typically 25˚C). During a restart after thermal shutdown, the soft-start capacitor will be fully discharged and then charged in the low current mode (1µA) similar to a second level current limit event. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

Application Circuit: Input 36-78V, Output 3.3V, 30A

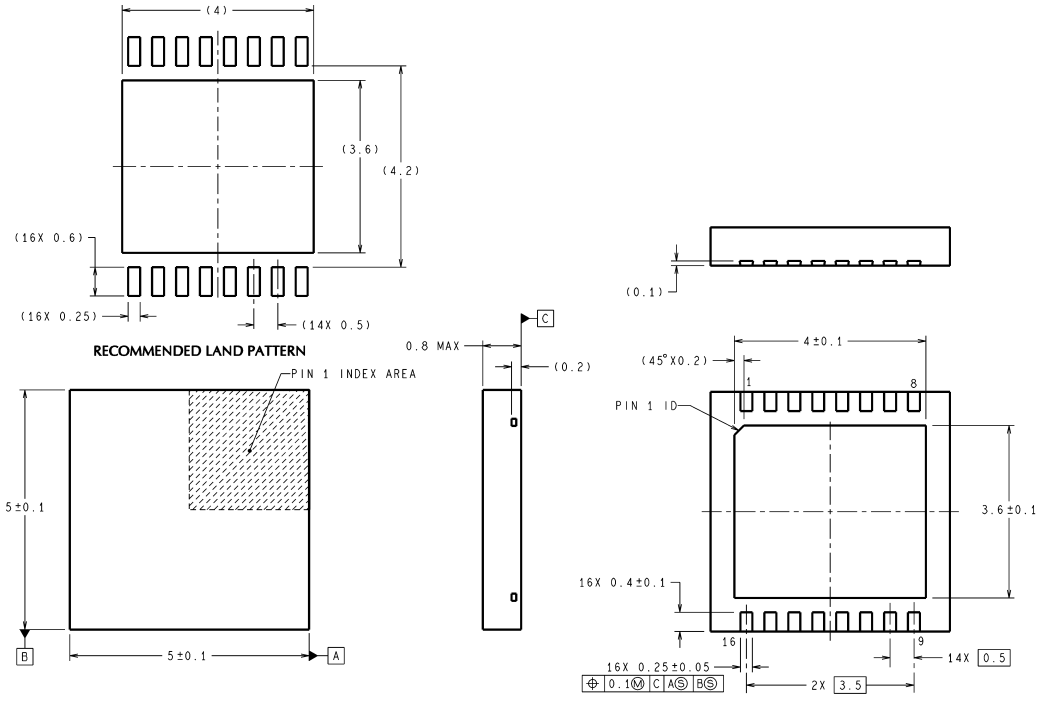


Physical Dimensions inches (millimeters)
unless otherwise noted



MTC16 (Rev D)

Molded TSSOP-16
NS Package Number MTC16



SDA16A (Rev A)

Note: It is recommended that the exposed pad be connected to Pin 11 (AGND)

16-Lead LLP Surface Mount Package
NS Package Number SDA16A

Notes

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