UNITRODE

Cellular Telephone Power Converter

UCC2930-3/-5
UCC3930-3/-5

PRELIMINARY

FEATURES

- BiCMOS Low Power RF/Cellular Power Management
- Negative Supply Voltage at 5mA for GaAs MESFET Amplifiers
- Separate Micro-Power Logic Supply Enable
- Low Quiescent, 3mA, Operating Current
- Three Low Dropout (200mV) Regulators
- Power Good Indicator for Managing Power Supply Sequencing
- Low Power Mode Input Quiescent Current, 2µA (Max)
- Low Battery Early Warning Detection Output

DESCRIPTION

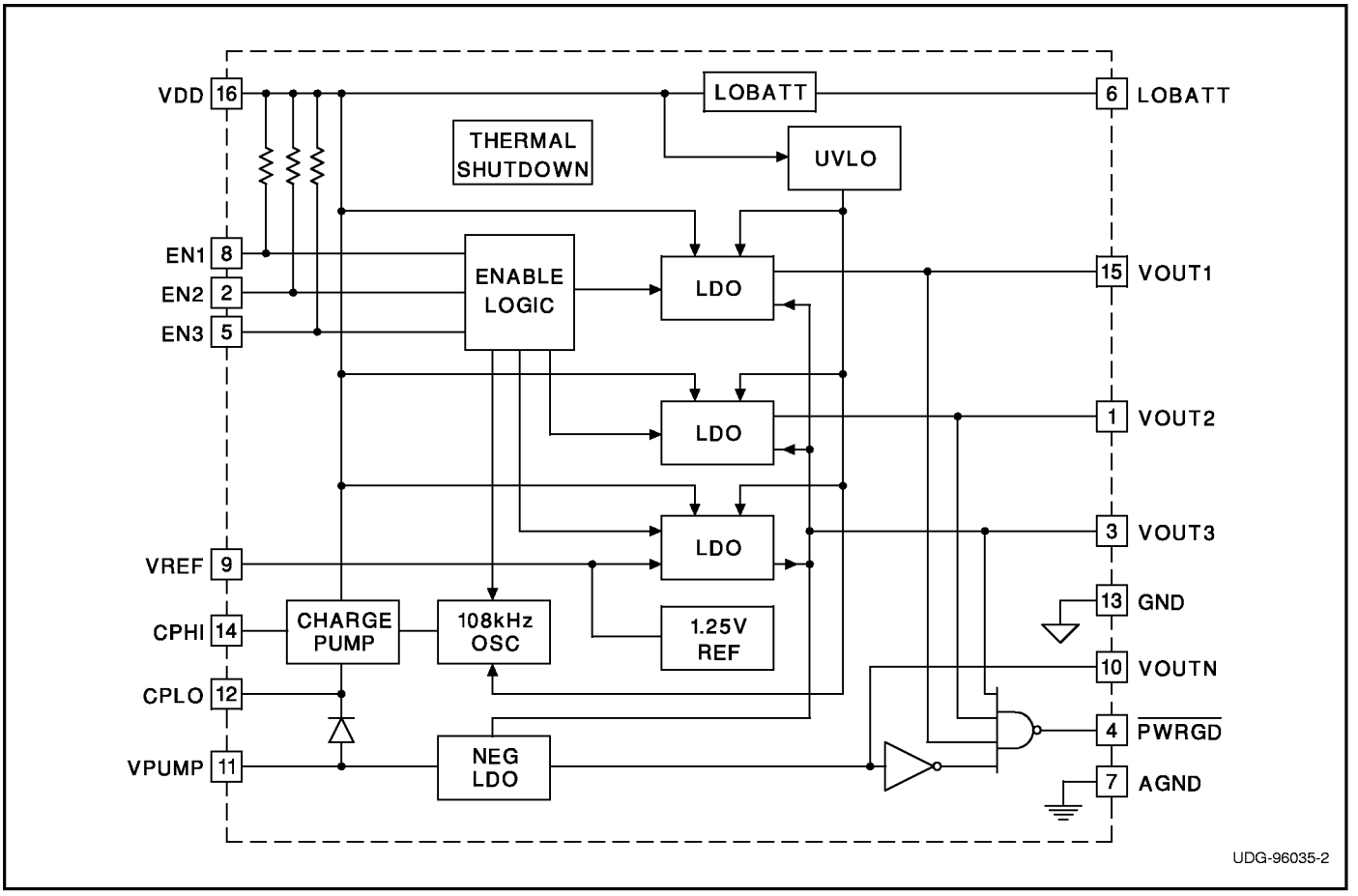
The UCC3930-3/-5 family of BiCMOS low power management controllers is designed for battery powered applications for RF/Cellular telephones, base stations, transmitters, receivers and pagers.

The circuit consists of three low dropout voltage regulators with <200mV maximum dropout, a low battery detection output, and a power good signal for managing power supply sequencing. Power management control is accomplished by the enable pins: EN1, EN2, and EN3 (See Table 1).

A negative supply for GaAs MESFET amplifiers is generated by a capacitive charge pump using a 0.1µF switching capacitor. The output noise of the negative supply is kept below 1mV by linearly regulating the coarse voltage present at the charge pump output.

Available packages include the 16-pin SSOP and 16-pin DIP. Consult Factory for exact SSOP-16 package dimensions.

BLOCK DIAGRAM



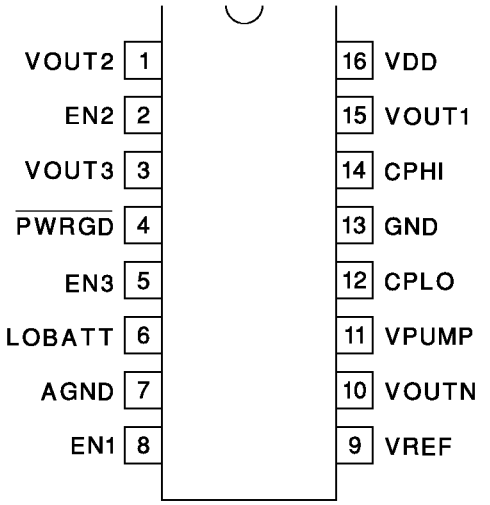
ABSOLUTE MAXIMUM RATINGS

Input Voltage (VDD) . . . . . +8V
EN Signal Voltage . . . . . –0.3V to VDD +0.3V
Regulator Output Current 900mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SSOP-16 (Top View)
N or J, M Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 0°C to 70°C for UCC3930-3/-5 and –40°C to +85°C for UCC2930-3/-5, C_{VPUMP} = 10µF, C_P = 0.1µF, C_{VOUT3} = C_{VOUTN} = 1.0µF, C_{VREF} = 0.1µF, C_{VDD} = 10µF, C_{VOUT1} = C_{VOUT2} = 2.2µF, 3.5V < V_{DD} < 8.0V for the UCC3930-3 and 5.2V < V_{DD} < 8.0V for the UCC3930-5, and EN1, EN2, and EN3 are 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Section (UCC3930-3)					
Shutdown Supply Current	EN1, EN2, EN3 = Open, 0°C≤ T_A ≤ 70°C		2	10	µA
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	µA
VDD Operating Current	I_{LOAD} = 0 for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		3.0	3.2	3.4	V
Regulator Section (UCC3930-3)					
Output Voltage, VPUMP	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA, VDD = 3.5V			–2.3	V
Output Voltage, VOUTN	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA	–2.7	–2.5	–2.3	V
Output Voltage, VOUT1, VOUT2	I_{LOAD} = 0mA to 50mA	3.22	3.3	3.383	V
Output Voltage, VOUT3	I_{LOAD} = 0mA to 5mA	3.22	3.3	3.383	V
	I_{LOAD} = 0mA to 5mA, EN1 = Low, EN2 = EN3 = Open	3.135		3.465	V
LDO VOUT1 Current Limit (Peak)	VDD = 3.5V (Note 1)	–900	–500		mA
LDO VOUT2 Current Limit (Peak)	VDD = 3.5V (Note 1)	–900	–500		mA
LDO VOUT3 Current Limit	VDD = 3.5V	–180	–100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		Ω
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	100	350	500	mV
Power Supply Section (UCC3930-5)					
Shutdown Supply Current	EN1, EN2, and EN3 = Open, 0°C≤ T_A ≤ 70°C		2	10	µA
Low Power Operating Current	EN1 = 0V, EN2 and EN3 = Open		28	40	µA
VDD Operating Current	I_{LOAD} = 0 for All Outputs, EN1, EN2, EN3 = Low		3	4.5	mA
Undervoltage Lockout		4.15	4.65	5.15	V

ELECTRICAL CHARACTERISTICS Unless otherwise specified, T_A = 0°C to 70°C for UCC3930-3/-5 and –40°C to +85°C for UCC2930-3/-5, C_{VPUMP} = 10µF, C_P = 0.1µF, C_{VOUT3} = C_{VOUTN} = 1.0µF, C_{VREF} = 0.1µF, C_{VDD} = 10µF, C_{VOUT1} = C_{VOUT2} = 2.2µF, 3.5V < V_{DD} < 8.0V for the UCC3930-3 and 5.2V < V_{DD} < 8.0V for the UCC3930-5, and EN1, EN2, and EN3 are 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Regulator Section (UCC3930-5)					
Output Voltage, VPUMP	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA, VDD = 5.2V			–4.1	V
Output Voltage, VOUTN	$VPUMP_{LOAD}$ = 0mA, $VOUTN_{LOAD}$ = –5mA	–4.6		–4.1	V
Output Voltage, VOUT1, VOUT2	I_{LOAD} = 0mA to 50mA	4.875	5	5.125	V
Output Voltage, VOUT3	I_{LOAD} = 0mA to 5mA	4.875	5	5.125	V
	I_{LOAD} = 0mA to 5mA, EN1 = Low, EN2 = EN3 = Open	4.75		5.25	V
LDO VOUT1 Current Limit (Peak)	VDD = 5.2V (Note 1)	–900	–500		mA
LDO VOUT2 Current Limit (Peak)	VDD = 5.2V (Note 1)	–900	–500		mA
LDO VOUT3 Current Limit	VDD = 5.2V	–180	–100		mA
VOUTN Current Limit			80	150	mA
VPUMP Output Resistance			150		Ω
Oscillator Frequency			108		kHz
Low Battery Detector Threshold	Referenced to VOUT3	100	450	650	mV
Thermal Shutdown					
Thermal Shutdown			165		°C
Thermal Shutdown Hysteresis			20		°C
Power Management Section					
Input Logic Low	Relative to GND			0.3	V
Input Logic High	Relative to VDD	VDD-0.5			V
Input Logic Pull-up Current	VDD = 8V	0.6	1.4	3	µA
Output Low Voltage	I_{LOAD} = 0.1mA, Relative to GND			0.5	V
Output High Voltage	I_{LOAD} = –0.1mA, Relative to VDD	VDD-0.5			V

Note 1: Once Thermal Cycling engages, the Average Current is much less in magnitude than this initial Peak Value.

PIN DESCRIPTIONS

AGND: This is the analog ground for power outputs.

CPHI, CPLO: These pins are used to connect a flying capacitor, typically 0.1µF, across the two internal single-pole, double-throw switches. The internal switches provide a charge pumped voltage on the VPUMP pin.

EN1, EN2, EN3: These input pins control the operating mode of the device. Operation follows the truth table presented below.

GND: This is the ground return for all on-chip switching functions. Typically this pin is connected to the ground plane. The bypass capacitors connected to GND should have the shortest possible lead lengths.

LOBATT: A digital output signal that indicates a low battery condition when the VDD voltage approaches its' minimum value required to maintain regulation. LOBATT is guaranteed to occur 100mV prior to the regulators dropping out of regulation. When only VOUT3 is enabled, LOBATT's output state is high.

$\overline{\text{PWRGD}}$: This pin, when low, is a digital indication that all of the regulators which are enabled have exceeded 80% of their steady state output voltage. When only VOUT3 is enabled, $\overline{\text{PWRGD}}$'s output state is high.

VDD: Positive supply input for the regulator. Bypass this pin to GND with a 10µF low ESR, ESL capacitor.

VOUT1, VOUT2, VOUT3: These outputs are low dropout regulators with varying drive capabilities. They are internally short circuit current protected. The VOUT3 output is the primary reference for all supplies. This output is typically connected to non-switching loads such as battery back-up static RAM or low power analog circuitry. The 50mA regulators are output compensated with 2.2µF low ESR capacitors. The VOUT3 regulator is compensated with a single 1µF capacitor.

VOUTN: This pin is the power source for GaAs MESFET amplifiers. A single 1.0µF output capacitor connected to AGND will provide adequate loop compensation and filtering of the regulator.

VPUMP: This output is a coarsely regulated negative supply for preregulating the VOUTN GaAs MESFET supply. A single 2.2µF capacitor connected to GND will provide adequate filtering of the charge pump output.

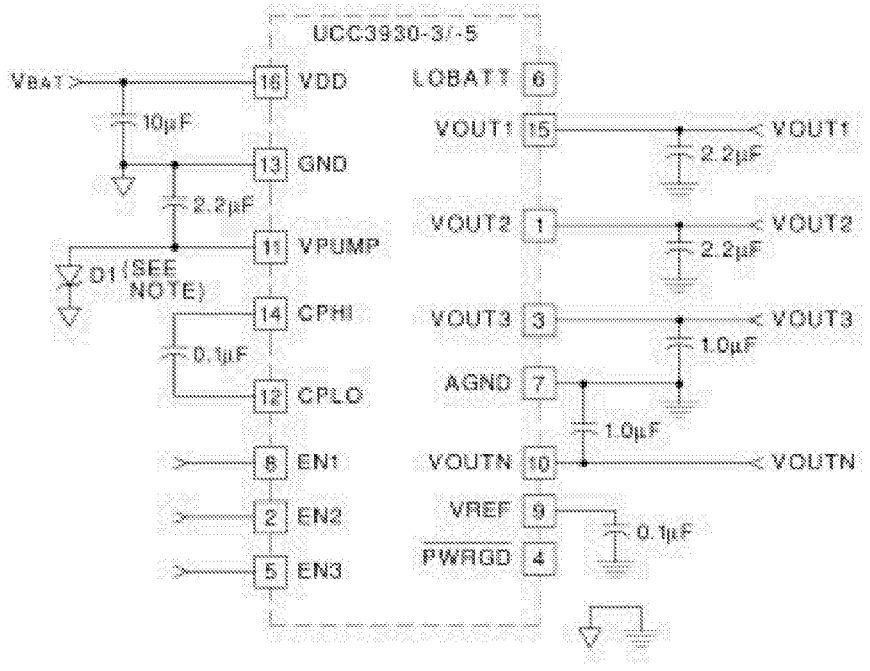
VREF: This output is the internal 1.25V bandgap reference. The regulator is output compensated with a minimum 0.01µF capacitor. By utilizing external compensation, the reference voltage noise is kept to a minimum.

EN1	EN2	EN3	VOUT1	VOUT2	VOUT3	VOUTN	VPUMP
0	0	0	ON	ON	ON	ON	ON
0	0	1	ON	OFF	ON	ON	ON
0	1	0	OFF	ON	ON	ON	ON
0	1	1	OFF	OFF	ON	OFF	OFF
1	0	0	NOT VALID				
1	0	1	NOT VALID				
1	1	0	NOT VALID				
1	1	1	OFF	OFF	OFF	OFF	OFF

Table 1. Enable Pins

APPLICATION INFORMATION

An application circuit for the UCC3930-3/-5 is shown in Figure 1. Careful attention must be paid to proper layout and decoupling techniques to insure low noise operation. The VDD and VPUMP pins should be bypassed directly to GND, while the output regulators and VREF should be separately bypassed to AGND. A single point connection should connect these two points as close to the IC as possible.



Note: Schottky diode D1, #SK12DICT-ND is recommended on VPUMP when using the UCC3930-3 to ensure proper clamping during Short Circuit Fault conditions.

Figure 1. Typical Application Circuit

TYPICAL CHARACTERISTICS

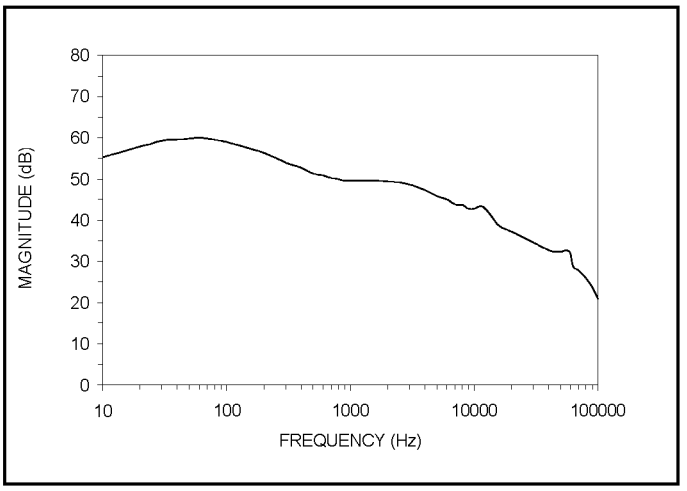


Figure 2. Ripple Rejection: VDD to VOUT1 (VOUT2)

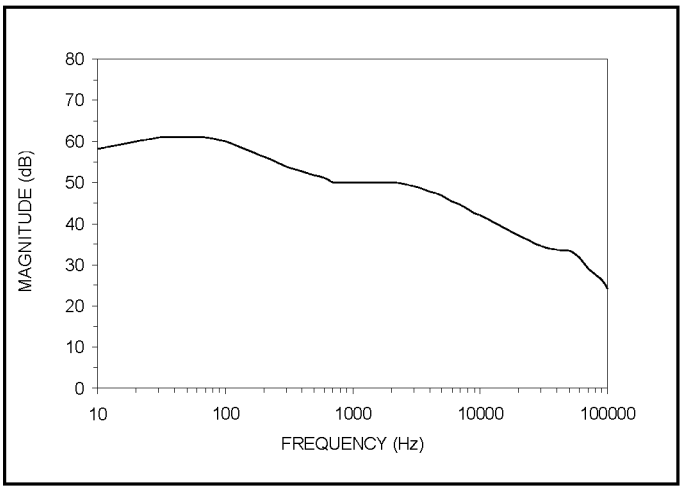


Figure 3. Ripple Rejection: VDD to VOUT3

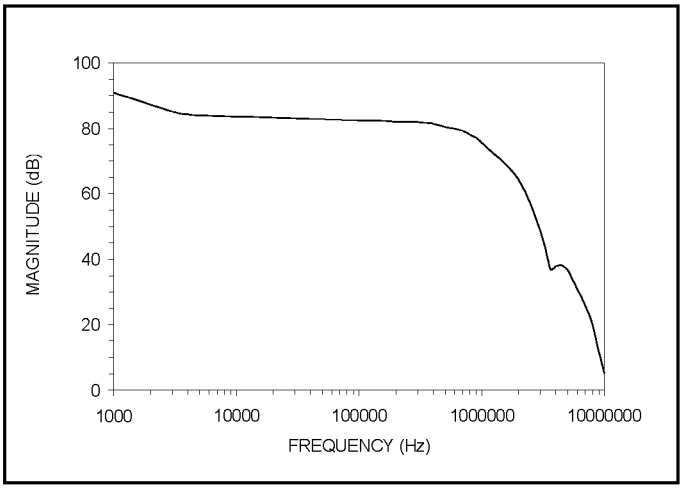


Figure 4. Channel to Channel Noise Rejection: VOUT1 to VOUT2 (VOUT3)

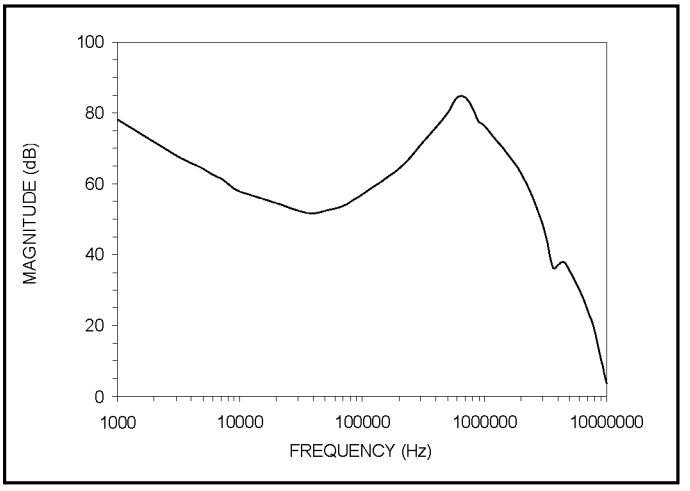


Figure 5. Channel to Channel Noise Rejection: VOUT2 to VOUT1 (VOUT3)

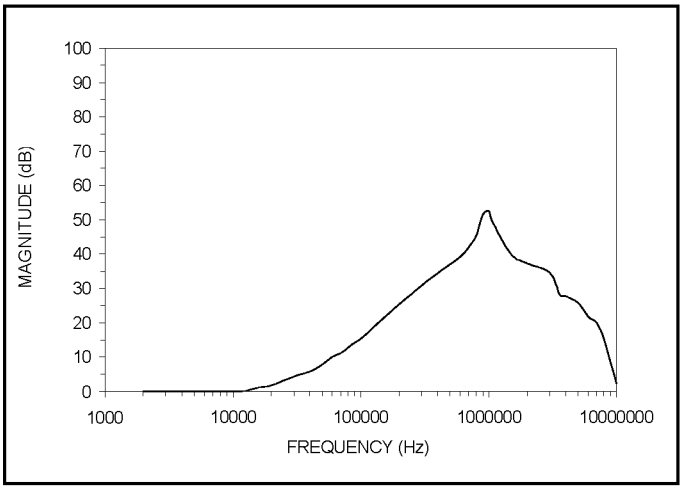


Figure 6. Channel to Channel Noise Rejection: VOUT3 to VOUT1 (VOUT2)

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Mechanical Drawings

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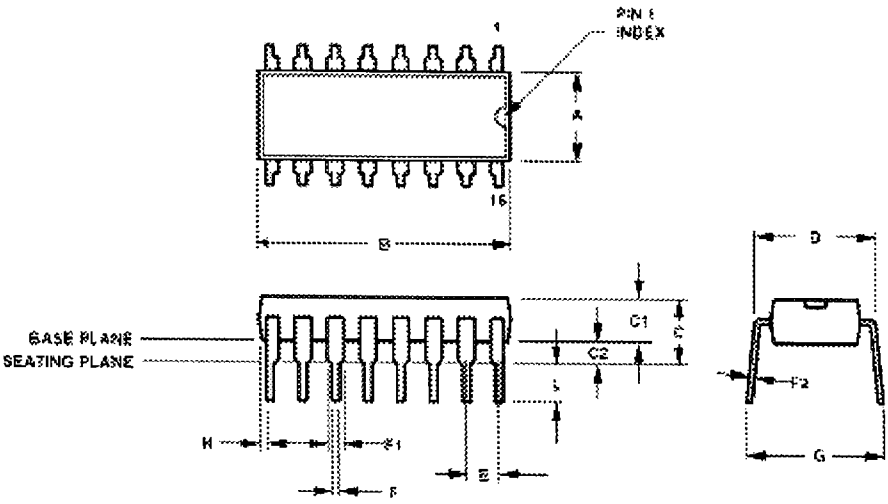
16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

P-3

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Mechanical Drawings

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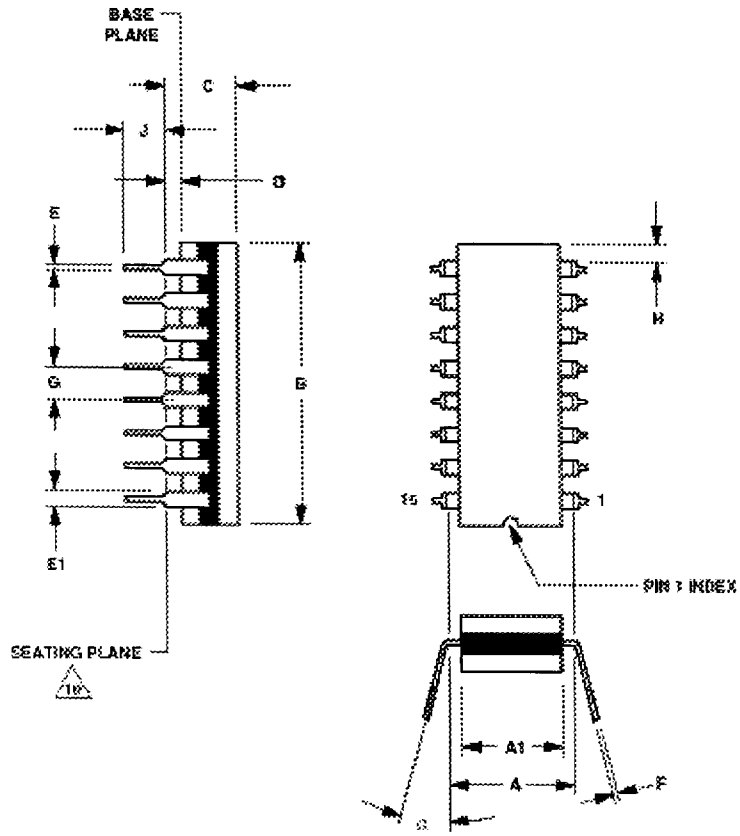
16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.840	-	21.34	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

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Mechanical Drawings

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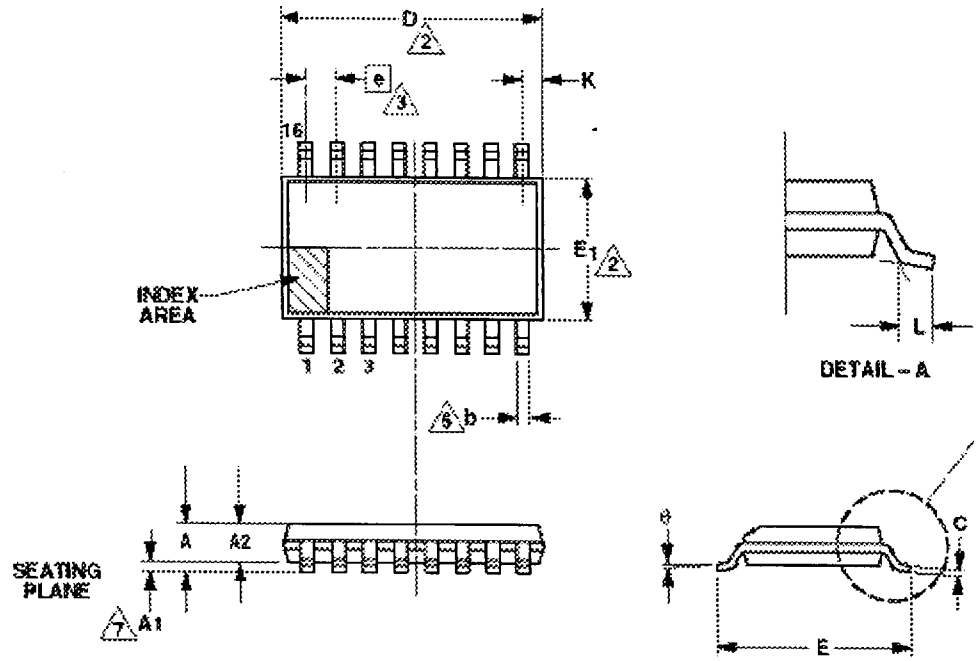
16-PIN SSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.42
A1	.004	.010	.10	.25
A2	-	.059	-	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.189	.197	4.80	5.00
E	.228	.244	5.79	6.20
E1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.009 REF		.23 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIO SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHA LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SH NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR C BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF TH PACKAGE BODY (BASE PLANE).