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National Semiconductor

September 8, 2011

LM8805

Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output, Manual Reset and Watchdog Timer

General Description

The LM8805 microprocessor supervisory circuit provides the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM8805 is available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when taken high.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

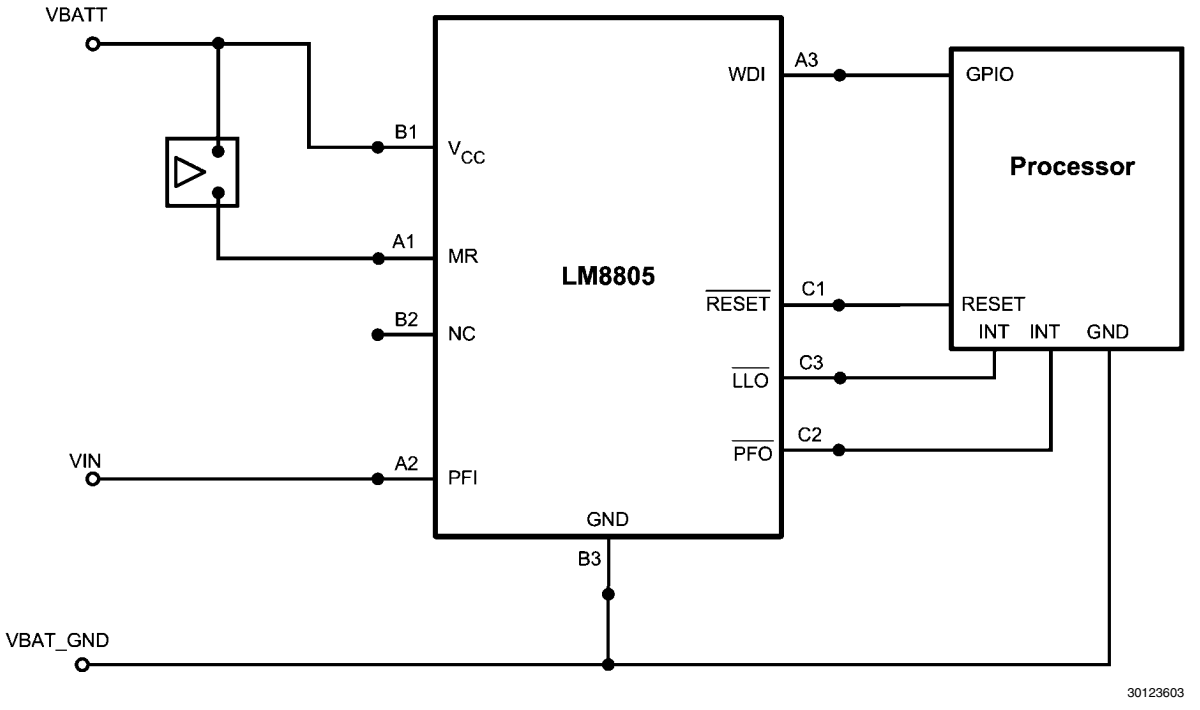
Features

- Standard Reset Threshold voltages:
  - Rising 2.6V
  - Falling 2.3V
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ output
- Precision supply voltage monitor
- Separate Power Fail comparator
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current
- Available in large bump micro SMD package

Applications

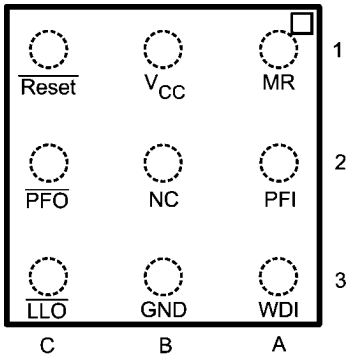
- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

Typical Application



Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
TLA09



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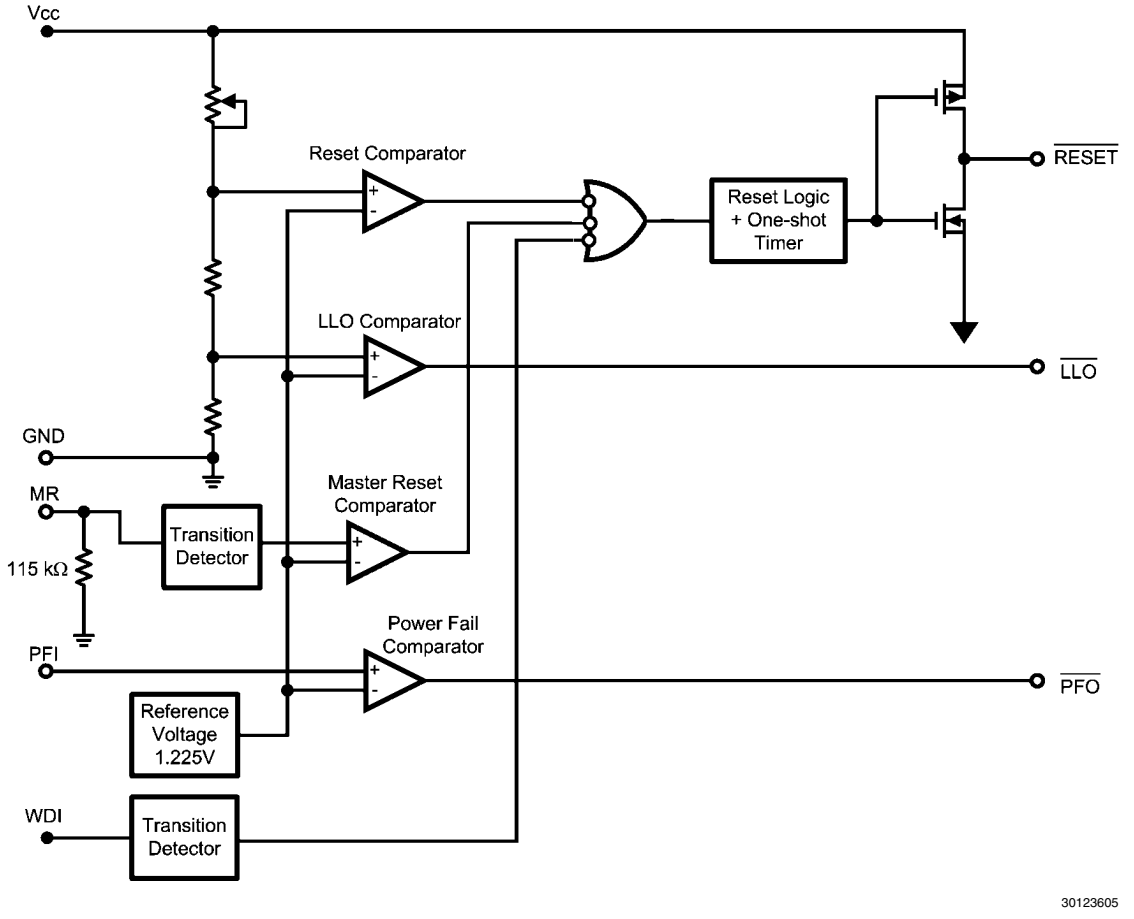
Pin Descriptions

Pin No. micro SMD	Name	Function
A1	MR	Manual-Reset input. When MR is triggered $\overline{\text{RESET}}$ is latched low after time t_{MR} until there is an event on V_{CC}.
B1	V_{CC}	Power Supply input.
C1	$\overline{\text{RESET}}$	Reset Logic Output. Reset remains low whenever V_{CC} is below the reset threshold. It remains low for t_{RP} after V_{CC} rises above the reset threshold.
C2	$\overline{\text{PFO}}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high.
C3	$\overline{\text{LLO}}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	GND	Ground reference for all signals.
A3	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), $\overline{\text{RESET}}$ is latched until there is an event on V_{CC}.
A2	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{\text{PFO}}$ goes low; otherwise, $\overline{\text{PFO}}$ remains high.
B2	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



Ordering Information LM8805

Order Number	Option	Production Identification	Supplied as
LM8805TLE/NOPB	2.6V	V3	250 Tape & Reel
LM8805TLX/NOPB	2.6V	V3	3000 Tape & Reel
LM8805TLE-3.0/NOPB	3.0V	V4	250 Tape & Reel
LM8805TLX-3.0/NOPB	3.0V	V4	3000 Tape & Reel

Absolute Maximum Ratings (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to 6.0V
All Other Inputs	−0.3V to V_{CC} + 0.3V
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
ESD Ratings (*Note 2*)	
Human Body Model	2.0kV
Machine Model	150V
Power Dissipation	(*Note 3*)

Operating Ratings (*Note 1*)

Temperature Range	−40°C ≤ T_J ≤ 85°C

Thermal Properties (*Note 1*)

Junction-To-Ambient Thermal Resistance	
$\theta_{J\text{-}A}$ JEDEC Board	110°C/W
$\theta_{J\text{-}A}$ 4Layer Board	68°C/W

LM8805 Electrical Characteristics

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range: V_{CC}		**1.0**		**5.5**	V
I_{CC}	V_{CC} Supply Current	All inputs = V_{CC}; all outputs floating		28	**50**	µA
RESET THRESHOLD						
V_{RST}	Reset Threshold	V_{CC} falling	−0.5 **−2**	V_{RST}	+0.5 **+2**	%
		V_{CC} falling: T_A = 0°C to 70°C	**−1.5**		**+1.5**	
V_{RSTH}	Reset Threshold Hysteresis		200	300	400	mV
t_{RP}	Reset Timeout Period	Reset Timeout Period = E, J, N, S	**1**	1.4	**2**	ms
t_{RD}	$V_{CC}$to Reset Delay	V_{CC} falling at 1mV/µs		20		µs
$\overline{\text{RESET}}$						
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0V, I_{SINK} = 50µA			**0.3**	V
		V_{CC} > 1.2V, I_{SINK} = 100µA			**0.3**	
		V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			

Symbol	Parameter	Conditions	Min	Typ	Max	Units
WDI						
WDI	Watchdog Input Current	$V_{WDI} = V_{CC}$	**–1**		**+1**	µA
WDI_T	Watchdog Input Threshold		**0.4**		**1.5**	V
t_{WD}	Watchdog Timeout Period	Watchdog Timeout Period (*Note 4*)	**90,000**	128,000	**160,000**	ms
PFI						
V_{PFT}	PFI Input Threshold		**1.200**	1.225	**1.250**	V
V_{PFTH}	PFI/MR Threshold Hysteresis	PFI/MR falling: $V_{CC} = V_{RST\ MAX}$ to 5.5V		0.0032•V_{RST}		mV
I_{PFI}	Input Current		–75		75	nA
MR						
V_{MRT}	MR Input Threshold		**0.4**		**1.5**	V
R_{MR}	MR Pull-down Resistance		90	115	140	kΩ
t_{MD}	MR to Reset Delay			12		µs
t_{MR}	MR Pulse Width		**25**			µs
$\overline{PFO}$, $\overline{LLO}$						
V_{OL}	$\overline{PFO}$, $\overline{LLO}$ Output Voltage	$V_{CC} > 2.25V$, $I_{SINK} = 900µA$			**0.3**	V
		$V_{CC} > 2.7V$, $I_{SINK} = 1.2mA$			**0.3**	
		$V_{CC} > 4.5V$, $I_{SINK} = 3.2mA$			**0.4**	
V_{OH}		$V_{CC} > 2.25V$, $I_{SOURCE} = 300µA$	**0.8 V_{CC}**			
		$V_{CC} > 2.7V$, $I_{SOURCE} = 500µA$	**0.8 V_{CC}**			
		$V_{CC} > 4.5V$, $I_{SOURCE} = 800µA$	**V_{CC} – 1.5V**			
$\overline{LLO}$ OUTPUT						
V_{LLOT}	$\overline{LLO}$ Output Threshold ($V_{\overline{LLO}} – V_{RST}$, V_{CC} falling)		**1.01•V_{RST}**	1.02•V_{RST}	**1.03•V_{RST}**	V
V_{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V_{RST}		mV
t_{CD}	Low-Line Comparator Delay	V_{CC} falling at 1mV/µs		20		µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

Note 2: The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperture is calculated using:

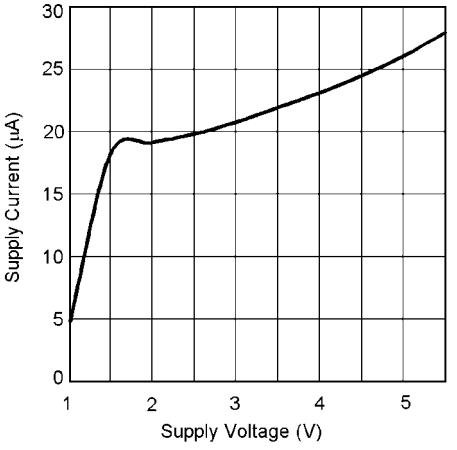
$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the 9-bump micro SMD package is 110°C/W in a typical PC board.

Note 4: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Typical Performance Characteristics

Supply Current vs Supply Voltage



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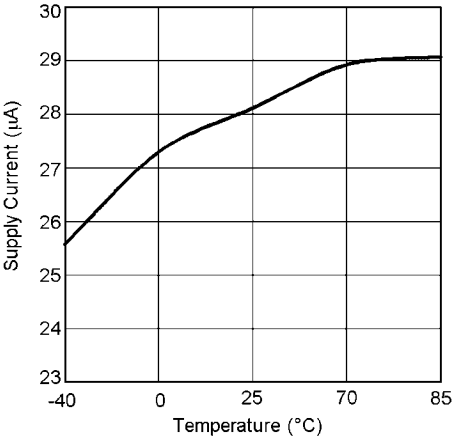
3.3V Supply Current vs Temperature



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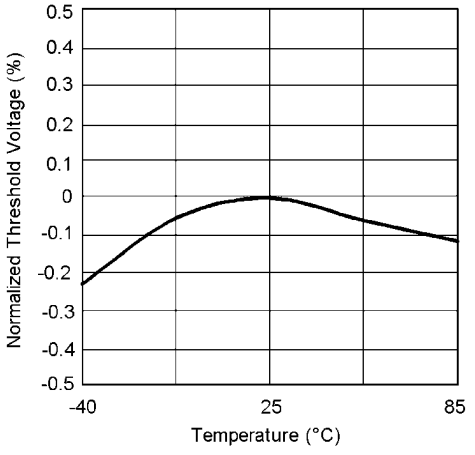
Normalized Reset Threshold Voltage vs Temperature



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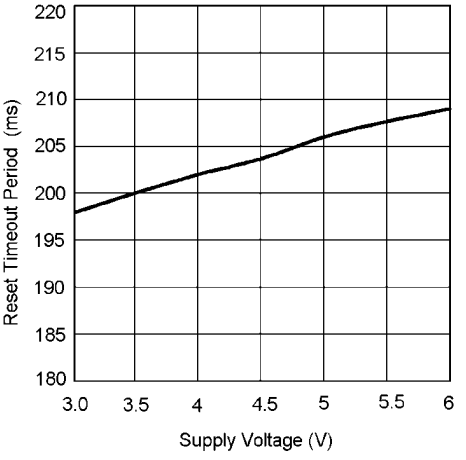
Reset Timeout Period vs V_{CC}



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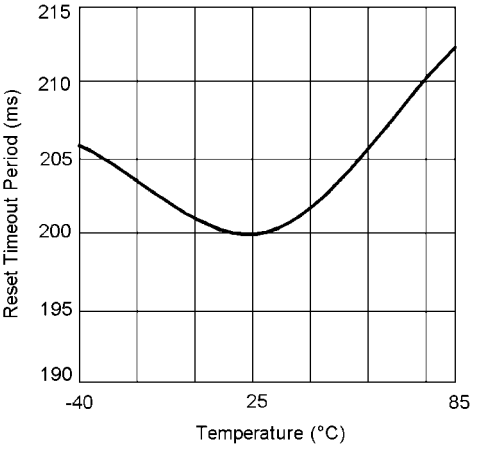
Reset Timeout Period vs Temperature



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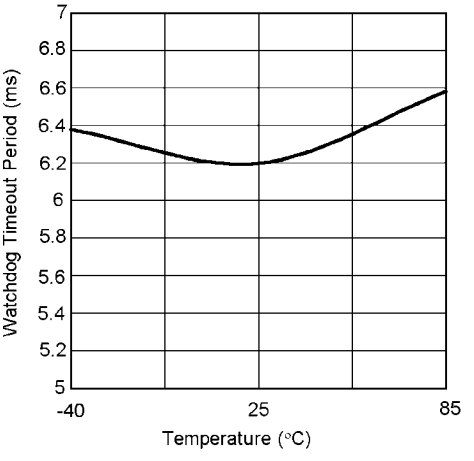
Watchdog Timeout Period vs Temperature



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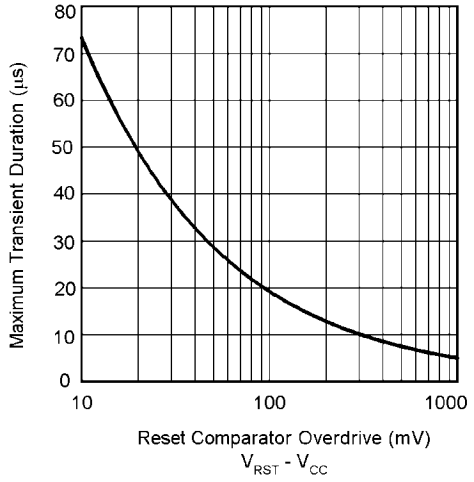
Max. Transient Duration vs Reset Comparator Overdrive (V_{CC} = 3.3V)



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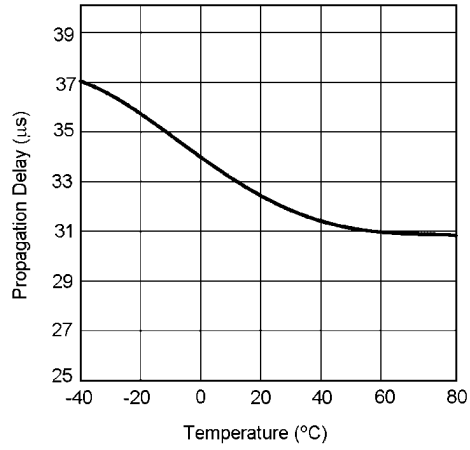
Low-Line Comparator Propagation Delay vs Temperature



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Circuit Information

RESET OUTPUT

The Reset input of a µP initializes the device into a known state. The LM8805 microprocessor supervisory circuit asserts a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is guaranteed valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM8805 offers an active-low $\overline{\text{RESET}}$.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input (MR) will initiate a forced reset also. See the *Manual Reset Input* section.

RESET THRESHOLD

The LM8805 is available with a reset threshold of 2.3V with a hysteresis of 300mV equating to a rising turn-on threshold of 2.60V.

MANUAL RESET INPUT (MR)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The MR input is fully debounced and provides an internal 115 kΩ pull-down. When the MR input pulses high, reset is asserted after a typical delay of 12 µs. Reset remains active until power is recycled and a V_{CC} rising edge is detected.

POWER-FAIL COMPARATOR (PFI/$\overline{\text{PFO}}$)

The PFI is compared to a 1.225V internal reference, V_{PFT}. If PFI is less than V_{PFT}, the Power Fail Output $\overline{\text{PFO}}$ drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage.

LOW-LINE OUTPUT ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

WATCHDOG TIMER INPUT (WDI)

The watchdog timer input monitors one of the microprocessor's output lines for activity. Each time a transition occurs on this monitored line, the watchdog counter is reset. However, if no transition occurs and the timeout period is reached, the LM8805 assumes that the microprocessor has locked up and the reset output is activated.

When tripped by the watchdog timer, the RESET pin will stay asserted and ignore any further activity from the WDI input. RESET can only be deasserted by a V_{CC} voltage event. Refer to *Figure 1* for more details

WDI is a high impedance input.

SPECIAL PRECAUTIONS FOR THE MICRO SMD PACKAGE

As with most integrated circuits, the LM8805 is sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the micro SMD package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

MICRO SMD MOUNTING

The micro SMD package requires specific mounting techniques which are detailed in National Semiconductor Application Note AN-1112. Referring to the section ***Surface Mount Technology (SMT) Assembly Considerations***, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the micro SMD device.

Timing Diagrams

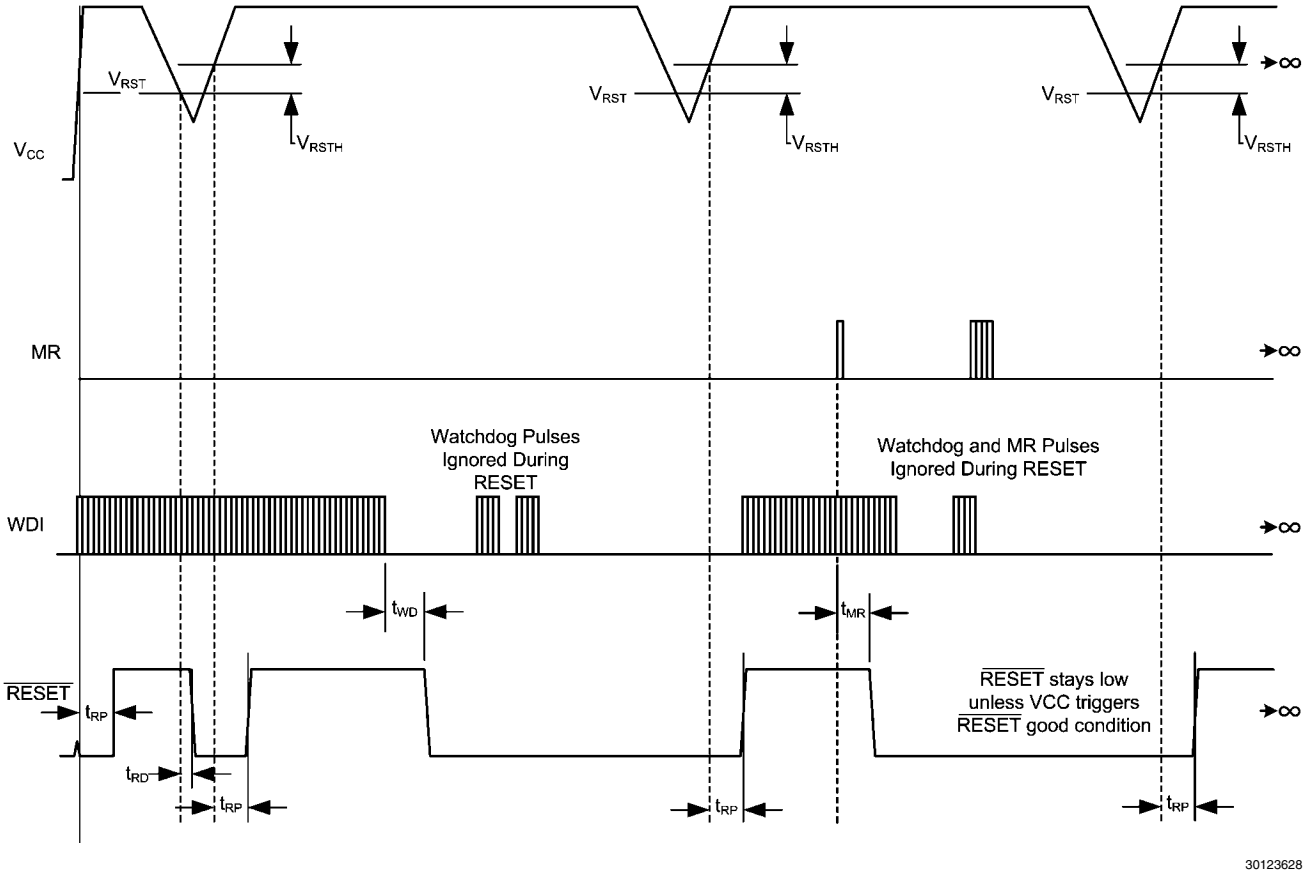


FIGURE 1. LM8805 Reset Time with MR and WDI

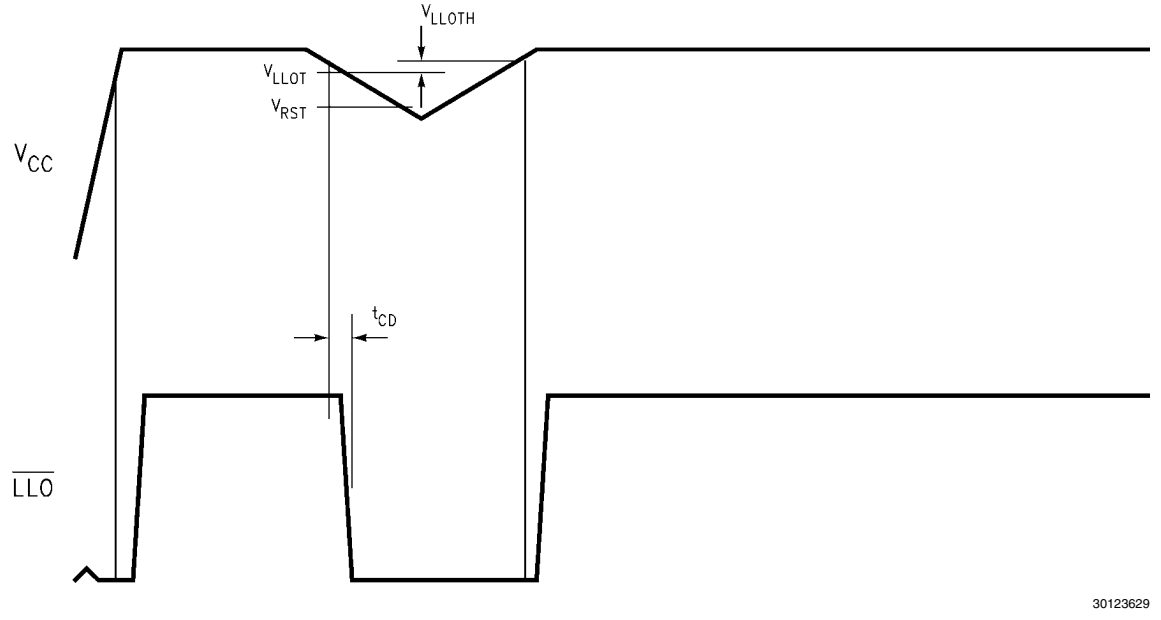


FIGURE 2. $\overline{\text{LLO}}$ Output

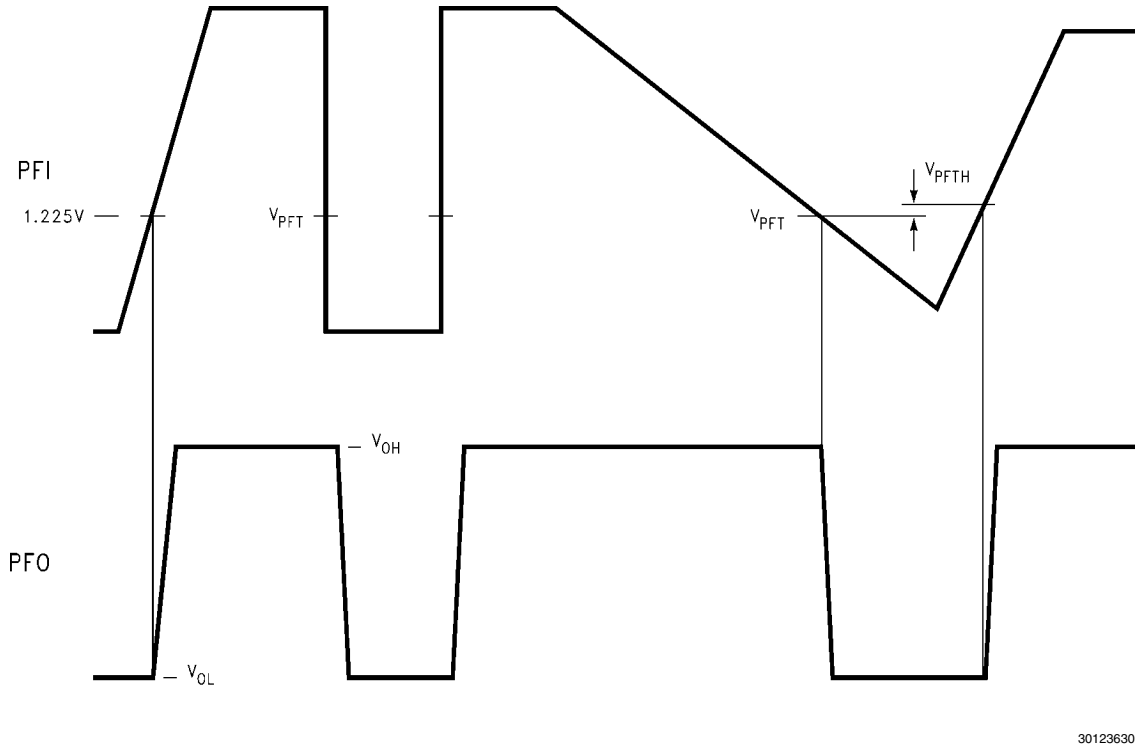
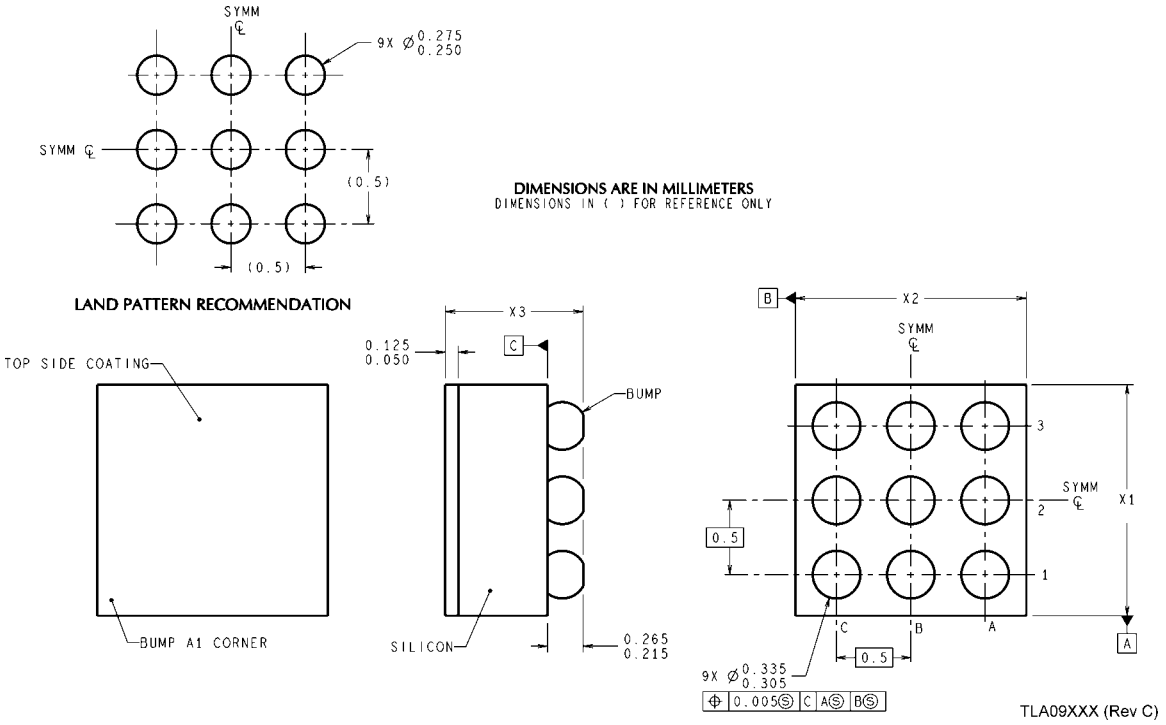


FIGURE 3. PFI Comparator Timing Diagram

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTER CLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

9 bump micro SMD Package
NS Package Number TLA09ZZA
The dimensions of X1, X2 and X3 are given below
X1 = 1.465mm
X2 = 1.465mm
X3 = 0.600mm

Notes

Notes

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Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
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