NCP4672

Linear Voltage Regulator - Dual, V_{in} and V_{out} Voltage Detector

The NCP4672 is a dual linear voltage regulator with input voltage and output voltage detectors. This part is useful in systems where multiple voltages are required such as for core and I/O. The NCP4672 is very accurate at 2% over full input voltage and full load current. The NCP4672 eliminates the need for external voltage supervision due to the two built in voltage detectors. The voltage detector on the input is set to 7.0 V. The output voltage detector is for channel 1 and is set to 2.9 V. An external capacitor is used to set the duration of this reset signal. Other features include short circuit protection and thermal shutdown protection. The NCP4672 has been designed to work with a 4.7 μF output capacitor having an ESR between 0.1 Ω and 5.0 Ω.

Features

- Accuracy: 2% at Full Voltage and Load
- Excellent Ripple Rejection: 70 dB @ 1 kHz
- Voltage Detector for Input Voltage
- Voltage Detector for Output Voltage
- Programmable Delay of Reset Signal
- Thermal Short Circuit Protection
- This is a Pb−Free Device

Typical Application

- Small Core and I/O Power
- Consumer Equipment
- Measurement Equipment
- Industrial Equipment

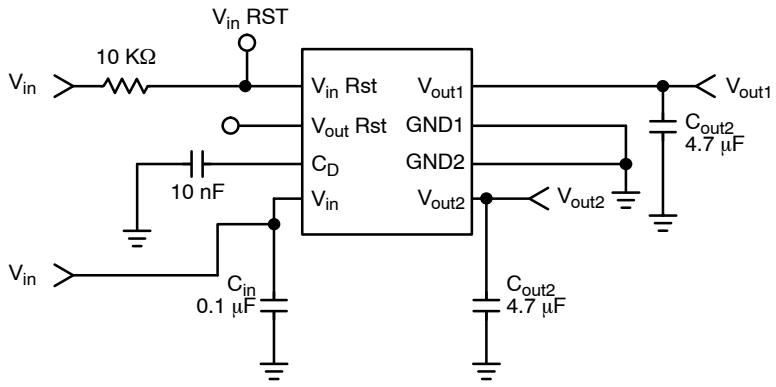


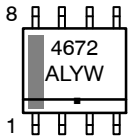
Figure 1. Typical Application Circuit

ON Semiconductor®

http://onsemi.com

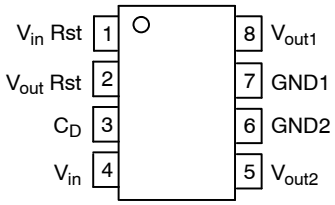
MARKING DIAGRAM

SOIC−8
NB SUFFIX
CASE 751



4672	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP4672DR2G	SOIC−8 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{inmax}	−0.3 ~ 18	V
Output Voltage	V_{out}	−0.3 to V_{in} + 0.3	V
Output Current 1 Output Current 2	$I_{out1max}$ $I_{out2max}$	30 80	mA mA
Output Short Circuit Duration	–	Infinite	–
Power Dissipation and Thermal Characteristics − SOIC−8 Power Dissipation Thermal Resistance, Junction−to−Ambient Minimum Pad Size 200 mm^2 Pad Size (Note 1) Thermal Resistance, Junction−to−Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 190 160 25	 W °C/W °C/W °C/W
Operating Junction Temperature Range	T_{stg}	−40 to 125	°C
Storage Temperature Range	T_{solder}	−55 to 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to Figure 4 for more information.

PIN DESCRIPTION

Pin Number	Symbol	Description
1	$V_{in\ RST}$	Open−collector, active−low output of the input voltage detector with hysteresis. Threshold levels are typical 7.0 V/ 7.35 V at V_{CC} pin.
2	$V_{o\ RST}$	Active−low output of the reset generator. Reset generator is based on sensing of the V_{out1} voltage. Sensing is with hysteresis − threshold levels are typically 2.9 V/ 2.95 V at V_{out1}. Reset is generated at rising edge of the V_{out1} and it's duration is set by external capacitor connected to C_D pin.
3	C_D	Programmable delay of the reset generator. Delay is adjusted by inserting a capacitor between C_D and GND (typically 10 ms for 10 nF capacitor).
4	V_{CC}	Supply Voltage
5	V_{out2}	1.8 V/ 80 mA LDO Regulator Output
6	GND2	Ground for V_{out2} (internally connected with GND1)
7	GND1	Ground for V_{out1} (internally connected with GND2)
8	V_{out1}	3.5 V/30 mA LDO Regulator Output

RECOMMENDED CONDITIONS (T_A = 25°C, C_{in} = 0.1 μF Ceramic, C_{out} = 4.7 μF)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Voltage	V_{in}	3.8	12	16	V
Output Current (where V_{out} remains within accuracy)	I_{out1} I_{out2}	0 0	– –	20 70	mA

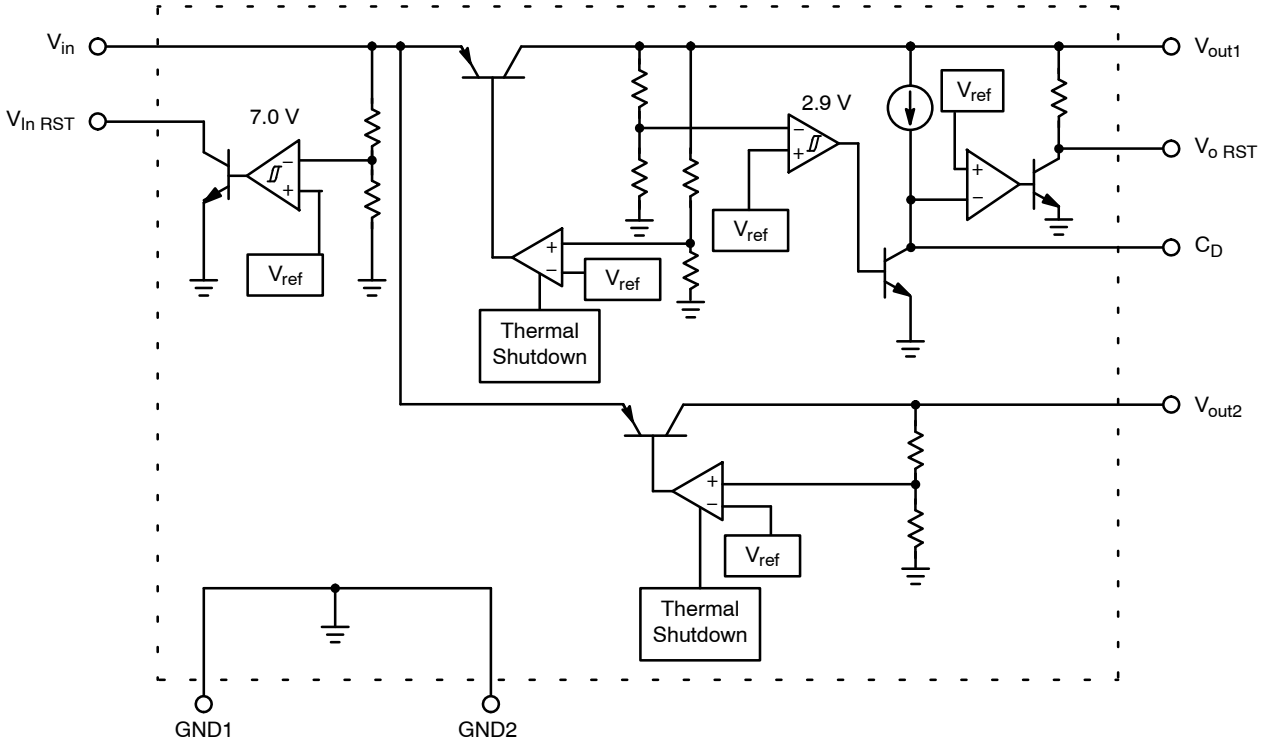

Vin
VIn RST
7.0 V
Vref
2.9 V
Vref
Vref
Thermal Shutdown
Vout1
Vo RST
CD
Vout2
Vref
Thermal Shutdown
GND1
GND2

Figure 1.

ELECTRICAL CHARACTERISTICS (C_{in} = 0.1 μF Ceramic, C_{out} = 4.7 μF with ESR = 0.1 – 5.0 Ω, V_{in} = 12 V, T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage V_{out1} (V_{in} = 4.5 V, I_{out1} = 20 mA) V_{out2} (V_{in} = 4.5 V, I_{out2} = 40 mA)	V_{adj}	 3.43 1.764	 3.5 1.8	 3.57 1.836	V
Line Regulation V_{out1} (V_{in} = 4.5 V , I_{out1} = 20 mA) V_{out2} (V_{in} = 4.5 V to 10 V, I_{out2} = 40 mA)	Reg_{line}	 – –	 3.0 3.0	 30 30	mV
Load Regulation V_{out1} (V_{in} = 4.5 V, I_{out1} = 0.1 mA to 20 mA) V_{out2} (V_{in} = 4.5 V, I_{out2} = 0.1 mA to 70 mA)	Reg_{load}	 – –	 3.0 2.0	 40 40	mV
Dropout Voltage V_{out1} (V_{in} = 3.3 V, I_{out1} = 20 mA)	$V_{in} - V_{out1}$	 –	 150	 300	mV
Ground Pin Current (V_{in} = 8.0 V, I_{out1} = I_{out2} = 0 mA) (V_{in} = 2.7 V, I_{out1} = I_{out2} = 0 mA, Rpu = infinite)	I_{GND}	 – –	 1.0 3.0	 2.0 –	mA
Short Current Limit V_{out1} V_{out2}	I_{SC}	 30 80	 60 150	 – –	mA
Thermal Shutdown		–	165	–	°C
Temperature Coefficient V_{out1} (T_J = –30 to 85°C, V_{in} = 4.5 V, I_{out1} = 20 mA) V_{out2} (T_J = –30 to 85°C, V_{in} = 4.5 V, I_{out2} = 40 mA)	T_C	 – –	 100 100	 – –	ppm/°C
Ripple Rejection (Note 6) V_{out1} (V_{in} = 4.5 V, V_{ripple} = 1.0 V, I_{out1} = 20 mA, 120 Hz) V_{out2} (V_{in} = 4.5 V, V_{ripple} = 1.0 V, I_{out2} = 40 mA, 120 Hz)	R_R	 – –	 65 70	 – –	dB
Output Noise Voltage V_{out1} (V_{in} = 4.5 V, f = 20 Hz – 80 kHz, I_{out1} = 20 mA) V_{out2} (V_{in} = 4.5 V, f = 20 Hz – 80 kHz, I_{out2} = 40 mA)	V_n	 – –	 80 50	 – –	μV_{rms}

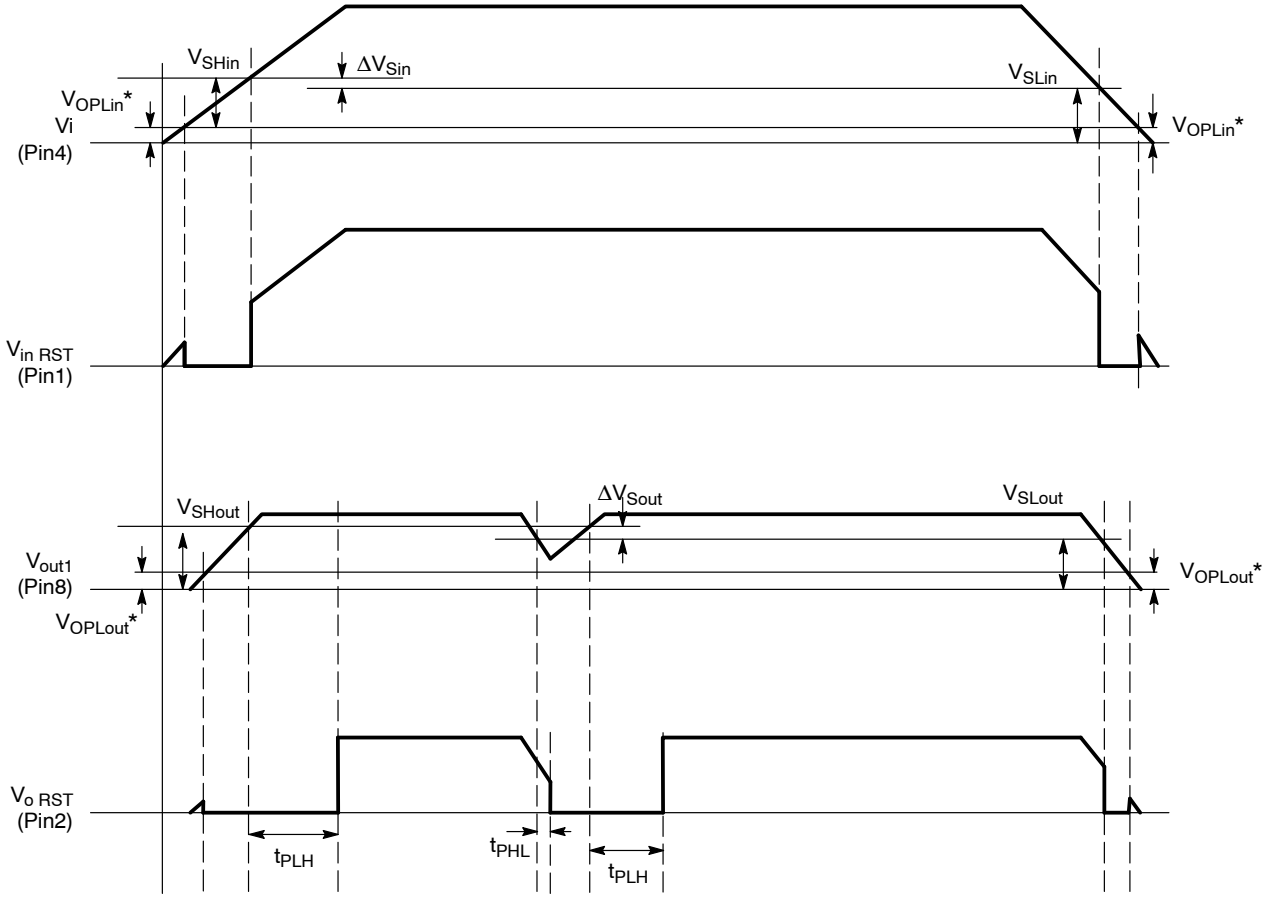
V_{in} Detect

Detecting Voltage L (V_{in} = H to L)	V_{SLin}	6.72	7.0	7.28	V
Detecting Voltage H (V_{in} = L to H)	V_{SHin}	–	7.35	–	V
Hysteresis Voltage (V_{in} = H to L to H)	ΔV_{Sin}	140	350	560	mV
V_{SLin} Temperature Coefficient (T_J = –30°C to +85°C)	V_{Slin} T_C	–	100	–	ppm/°C
Low–Level Output Voltage (V_{in} = 6.0 V, Vt1 = 5.0 V, Rt1 = 10 kΩ) (Note 5) Threshold Operating Voltage (V_{OPLin} = Vt1 = 1.0 V)	V_{OLin1} V_{OLin2}	– –	100 –	200 0.4	mV V

V_{out} Detect

Detecting Voltage L (V_{in} = H to L)	V_{SLout}	2.78	2.9	3.020	V
Detecting Voltage H (V_{in} = L to H)	V_{SHout}	–	2.95	–	V
Hysteresis Voltage (V_{in} = H to L to H)	ΔV_{Sout}	25	50	100	mV
V_{SLin} Temperature Coefficient (T_J = –30°C to +85°C)	V_{SLin} T_C	–	100	–	ppm/°C
Low–Level Output Voltage (V_{out1} = 2.6 V) Threshold Operating Voltage (V_{OPLout} = 0.85 V)	V_{OLout1} V_{OLout2}	– –	100 –	200 0.4	mV V
Reset Delay Time (C_D = 10 nF)	t_{PLH}	5	10	15	ms
"L" Transmission Delay Time (C_D = 10 nF)	t_{PHL}	–	30	90	μs

2. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL–STD–883, Method 3015
   Machine Model Method 200 V.
3. The maximum package power dissipation is: $P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Refer to Figure 3.
6. Guaranteed by design.



*; V_{OPLin} shows theoretical on this chart.
V_{OPLin} spec. must be specified on Pin 1 voltage (0.4 V)

*; V_{OPLout} shows theoretical on this chart.
V_{OPLout} spec. must be specified on Pin 2 voltage (0.4 V)

Figure 2. Dual Regulator Timing

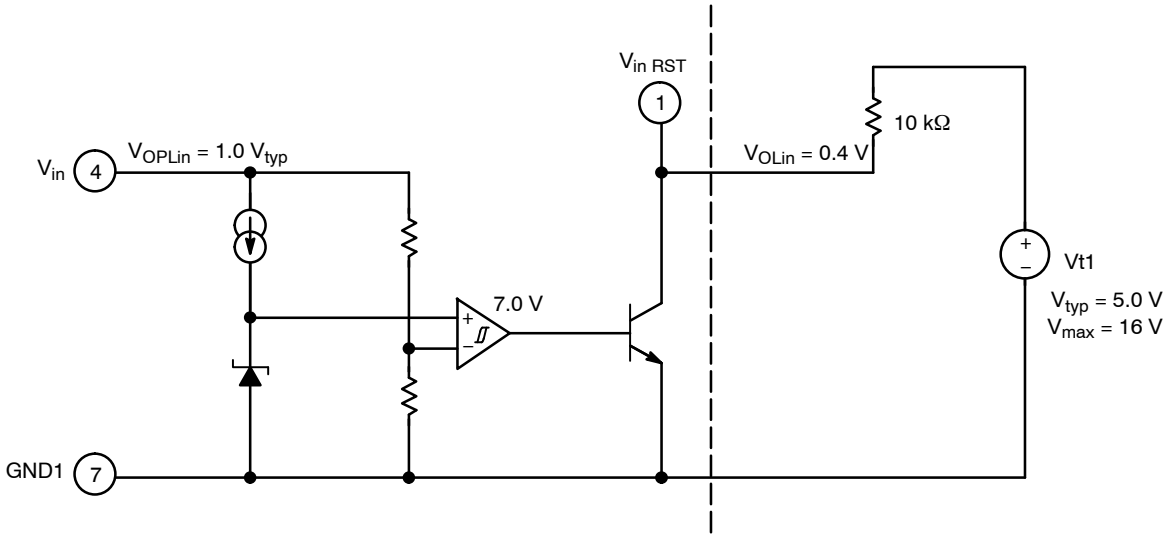


Figure 3. Threshold Operating Voltage V_{OPLin} Under Condition V_{OLin} = 0.4 V

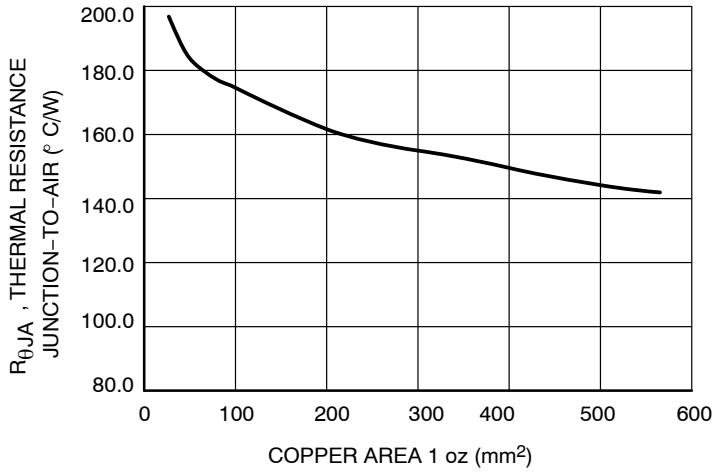


Figure 4. SOP−8 Thermal Resistance versus P.C.B. Copper Area

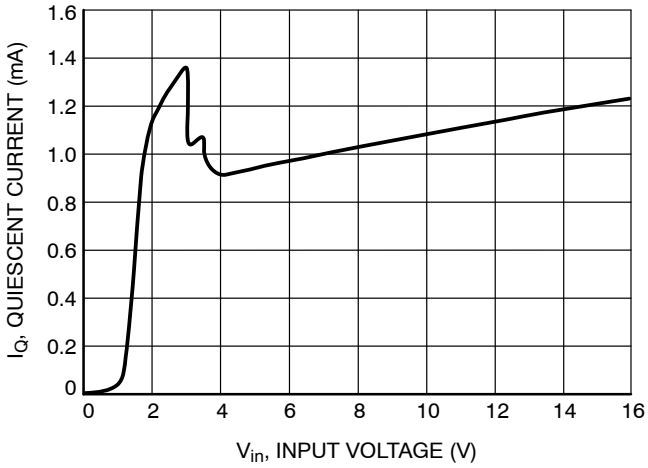


Figure 5. Quiescent Current versus Input Voltage

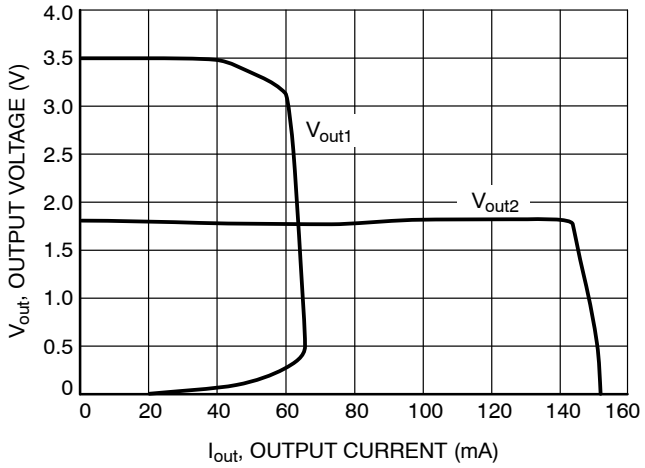


Figure 6. Peak Current Limit

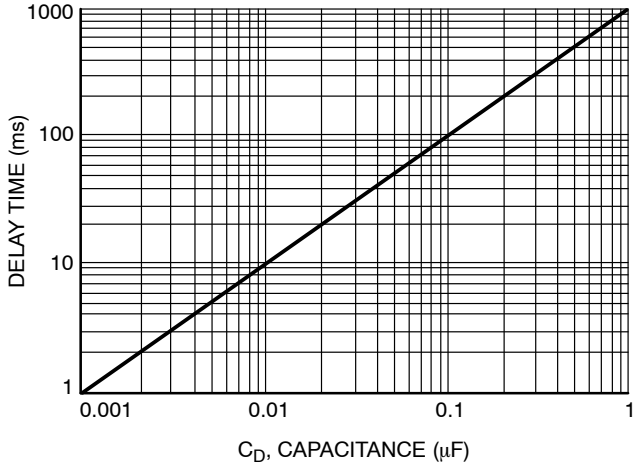


Figure 7. Delay Time versus Capacitance

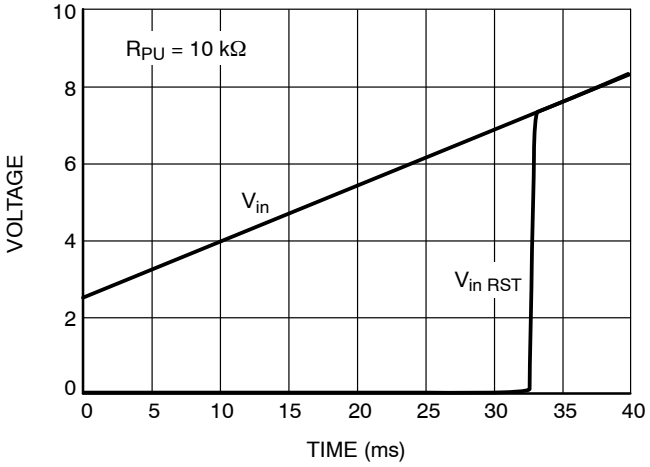


Figure 8. V_{in} and $V_{in\ RST}$ versus Time

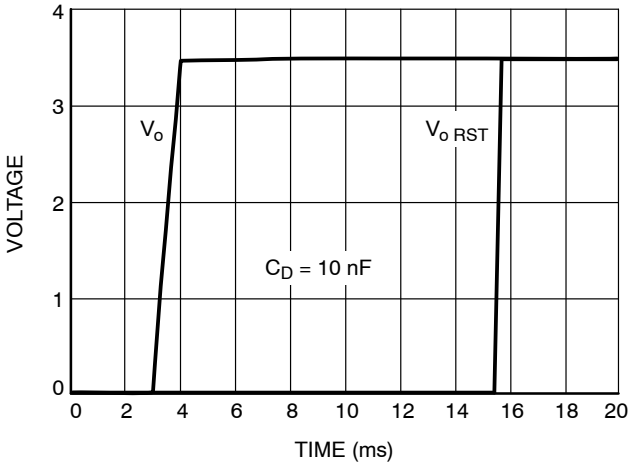


Figure 9. V_o and $V_{o\ RST}$ versus Time

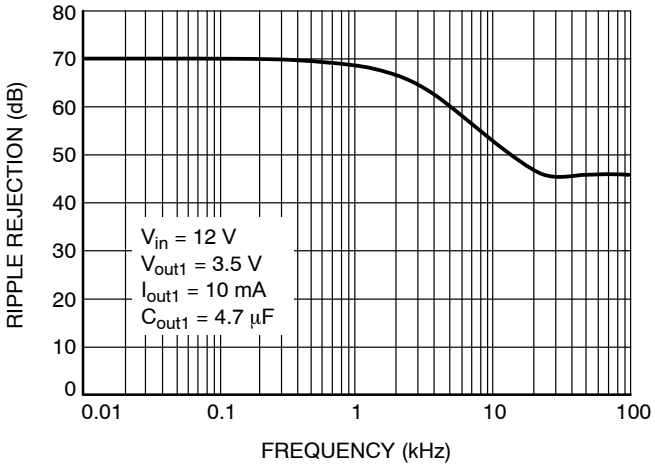


Figure 10. V_{out1} Ripple Rejection

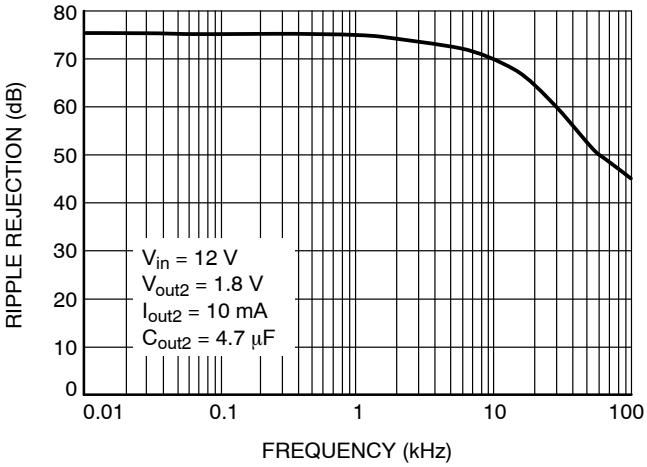


Figure 11. V_{out2} Ripple Rejection

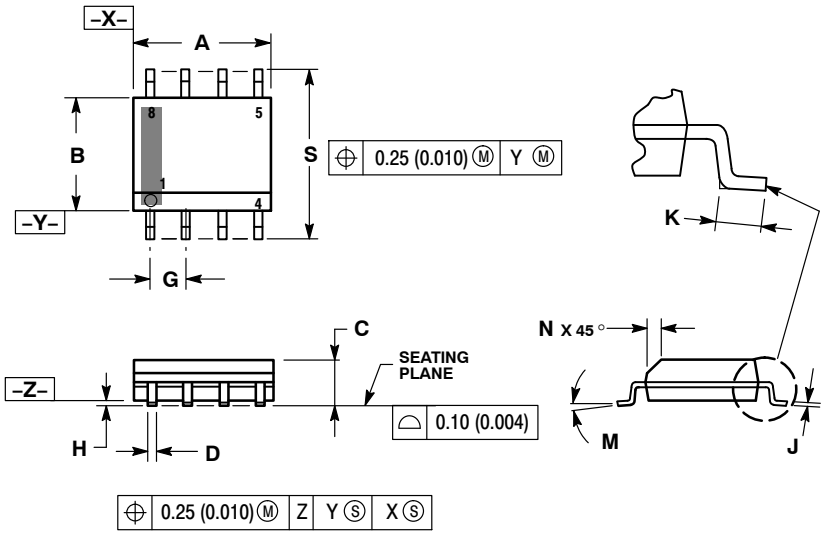
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

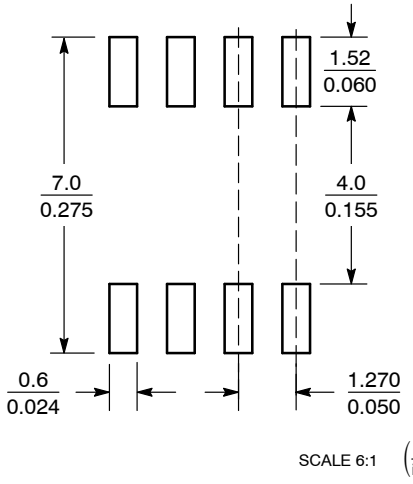
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

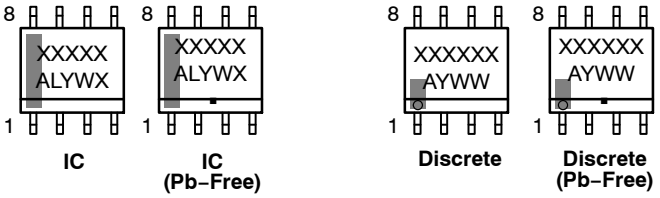
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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