NCP140

LDO Voltage Regulator - Capacitor Free, Low Noise

150 mA

The NCP140 is a 150 mA very low dropout regulator which offers excellent voltage accuracy and clean output voltage for power sensitive application. The NCP140 is very suitable for battery powered application due to very low quiescent current and virtually zero current at disable mode. This device is stable with or without output capacitors and allows minimize footprint and BOM. The XDFN4 package is optimized for use in space constrained applications.

Features

- Stable Operation with or without Capacitors
- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Options: 1.5 V to 5 V
  Contact Factory for Other Voltage Options
- ±1% Typical Accuracy @ 25°C
- Very Low Quiescent Current of Typ. 45 μA
- Standby Current: 0.1 μA
- Very Low Dropout: 125 mV for 3.3 V @ 150 mA
- High PSRR: 55 dB @ 1 kHz
- Available in – XDFN4 – 0.8 mm x 0.8 mm x 0.4 mm Package
  – XDFN4 – 1.0 mm x 1.0 mm x 0.4 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery−powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

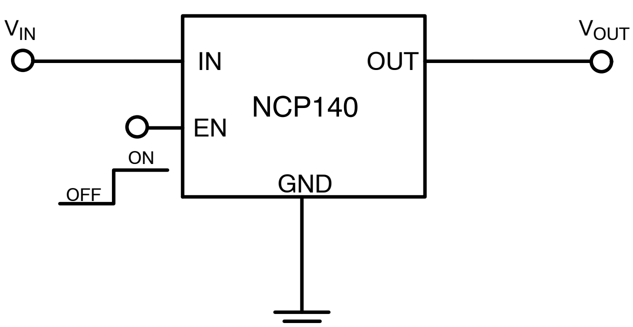

Figure 1. Typical Application Schematic

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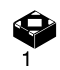
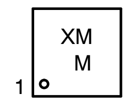
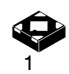
MARKING DIAGRAMS



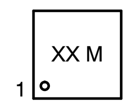
XDFN4, 0.8x0.8
CASE 711BF



X = Specific Device Code
MM = Date Code

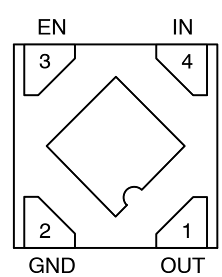


XDFN4, 1.0x1.0
CASE 711AJ



XX = Specific Device Code
M = Date Code

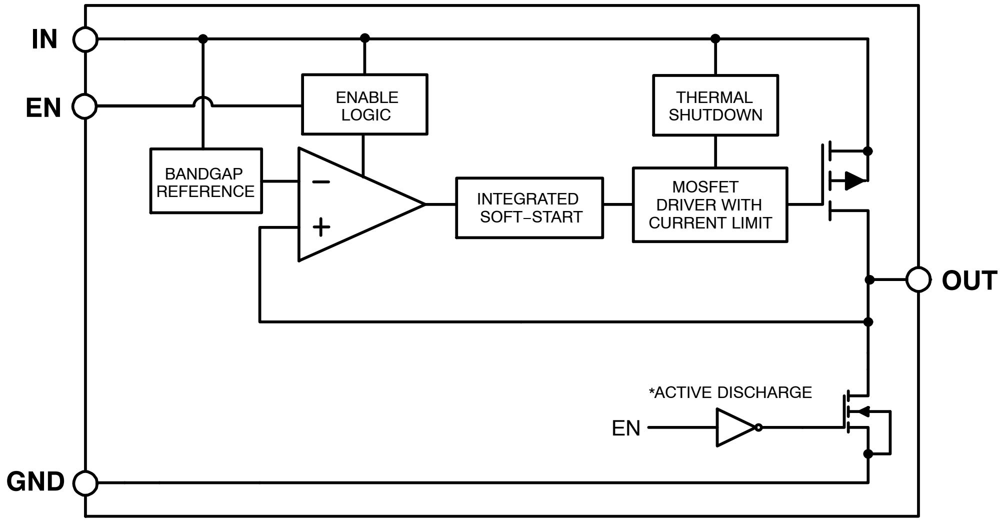
PIN CONNECTIONS



(Bottom View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.



*Active output discharge is available only for NCP140Axxx options.

Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	OUT	Regulated output voltage pin. A small ceramic capacitor can be connected to improve fast load transient.
2	GND	Ground pin
3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	IN	Input pin
−	EPAD	Expose pad must be connect to GND pin as short as possible. Soldered to a large ground copper plane allows for effective heat removal.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V or 6 V	V
Chip Enable Input	V_{CE}	−0.3 V to 6 V	V
Output Short Circuit Duration	t_{SC}	unlimited	s
Maximum Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114
   ESD Machine Model tested per EIA/JESD22−A115
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, XDFN4 0.8 mm x 0.8 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	252	°C/W
Thermal Characteristics, XDFN4 1.0 mm x 1.0 mm Thermal Resistance, Junction−to−Air (Note 3)	$R_{\theta JA}$	265	°C/W

3. Measured according to JEDEC board specification. Detailed description of the board can be found in JESD51−7

ELECTRICAL CHARACTERISTICS $-40°C \le T_J \le 85°C$; $V_{IN} = V_{OUT(NOM)} + 0.5$ V; $I_{OUT} = 1$ mA, $C_{IN} = C_{OUT}$ = none, unless otherwise noted. $V_{EN} = 0.9$ V. Typical values are at $T_J = +25°C$. Min/Max values are for $-40°C \le T_J \le 85°C$ (Note 3)

Parameter	Test Conditions		Symbol	Min	Typ.	Max	Unit
Operating Input Voltage			V_{IN}	1.6		5.5	V
Output Voltage Accuracy	$V_{OUT} \ge 1.8$ V, $T_J = 25°C$		V_{OUT}		±1		%
	$V_{OUT} < 1.8$ V, $T_J = 25°C$				±20		mV
	$V_{OUT} \ge 1.8$ V, $-40°C \le T_J \le 85°C$			−2		+2	%
	$V_{OUT} < 1.8$ V, $-40°C \le T_J \le 85°C$			−50		+50	mV
Line Regulation	$V_{OUT(NOM)} + 0.5 \text{ V} \le V_{IN} \le 5.5$ V		$Line_{Reg}$		1.0	5.0	mV
Load Regulation	I_{OUT} = 0 mA to 150 mA		$Load_{Reg}$		10	30	mV
Dropout Voltage (Note 5)	$I_{OUT} = 150$ mA	$V_{OUT(NOM)} = 1.8$ V	V_{DO}		255	390	mV
		$V_{OUT(NOM)} = 3.3$ V			125	220	
Output Current Limit	$V_{OUT} = 90\%\ V_{OUT(NOM)}$		I_{CL}		230		mA
Short Circuit Current	$V_{OUT} = 0V$		I_{SC}		250		mA
Quiescent Current	$I_{OUT} = 0$ mA		I_Q		45	75	μA
Shutdown Current	$V_{EN} \le 0.4$ V, $V_{IN} = 5.5$ V		I_{DIS}		0.1	1.0	μA
EN Pin Threshold Voltage	EN Input Voltage "H"		V_{ENH}	0.9			V
	EN Input Voltage "L"		V_{ENL}			0.4	
EN Pin Current	$V_{EN} = 5.5$ V		I_{EN}		0.01	1.0	μA
Turn−On Time	$C_{OUT} = 1$ μF, I_{OUT}=150 mA, From assertion of V_{EN} to $V_{OUT} = 98\% V_{OUT(NOM)}$		T_{ON}		100		μs
Power Supply Rejection Ratio	$V_{IN} = 3.5$ V, $V_{OUT(NOM)} = 2.5$ V, $I_{OUT} = 10$ mA	f = 100 Hz	PSRR		62		dB
		f = 1 kHz			55		
Output Noise Voltage	$V_{IN} = 2.3$ V, $V_{OUT(NOM)} = 1.8$ V, $I_{OUT} = 10$ mA f = 100 Hz to 100 kHz		V_N		17		μV_{RMS}
Thermal Shutdown Temperature	Temperature increasing from $T_J = +25°C$		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}		20		°C
Output Discharge Pull−Down	$V_{EN} \le 0.4$ V, A options only		R_{DISCH}		100		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_A = 25°C$. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when V_{OUT} falls 100 mV below $V_{OUT(NOM)}$.

TYPICAL CHARACTERISTICS

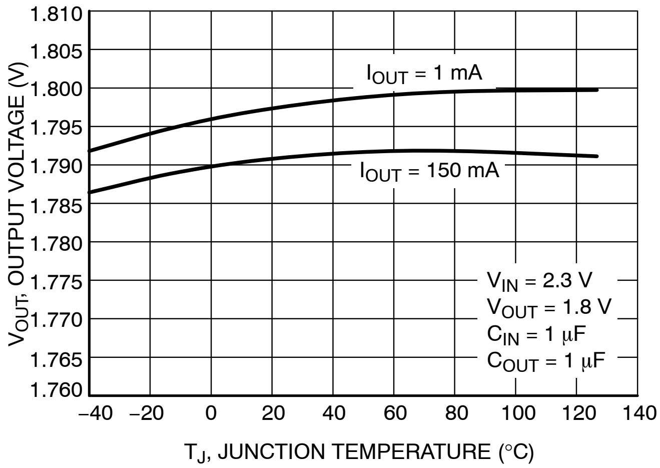


Figure 3. Output Voltage vs. Temperature – V_{OUT} = 1.8 V

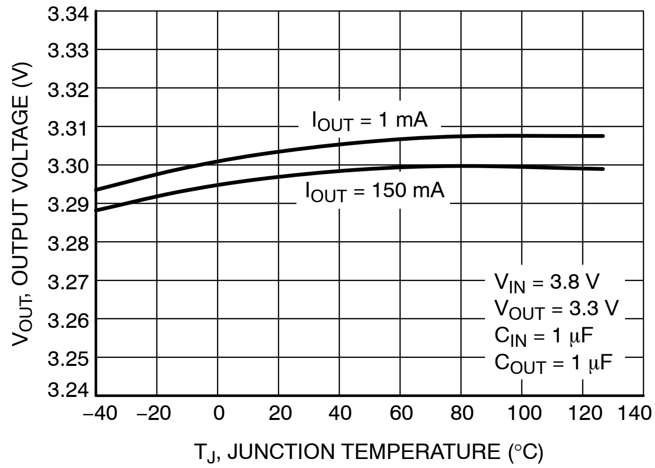


Figure 4. Output Voltage vs. Temperature – V_{OUT} = 3.3 V

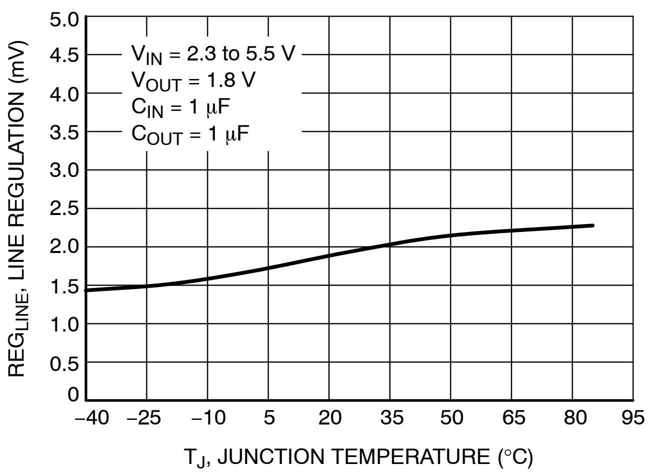


Figure 5. Line Regulation vs. Temperature – V_{OUT} = 1.8 V

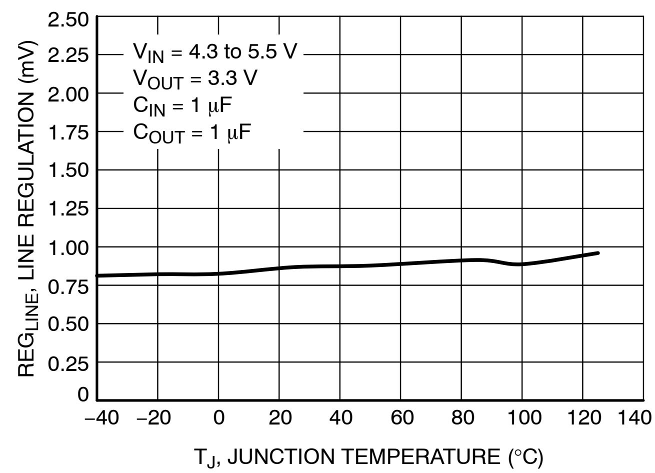


Figure 6. Line Regulation vs. Temperature – V_{OUT} = 3.3 V

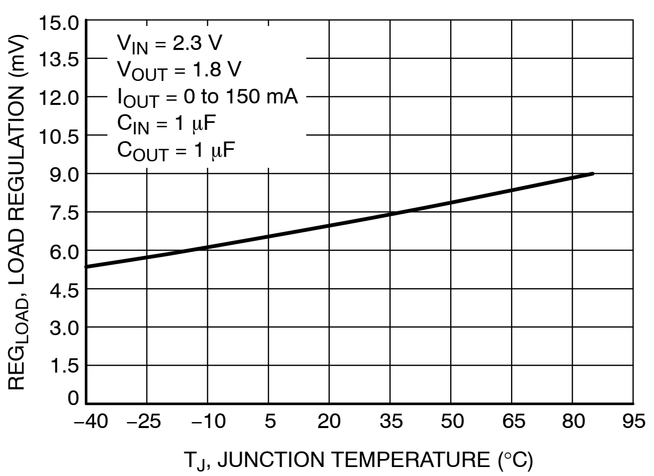


Figure 7. Load Regulation vs. Temperature – V_{OUT} = 1.8 V

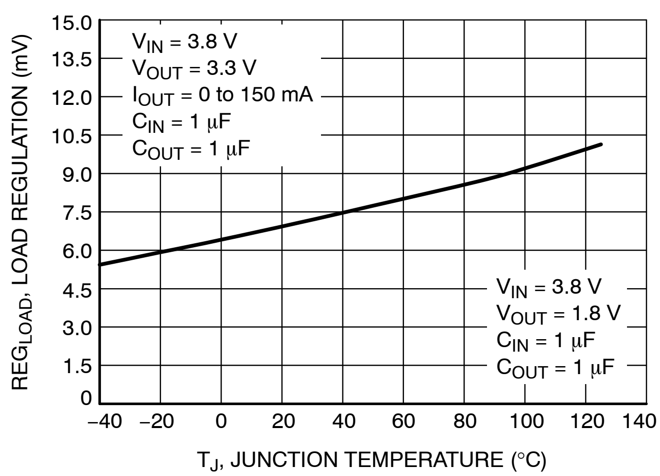


Figure 8. Load Regulation vs. Temperature – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

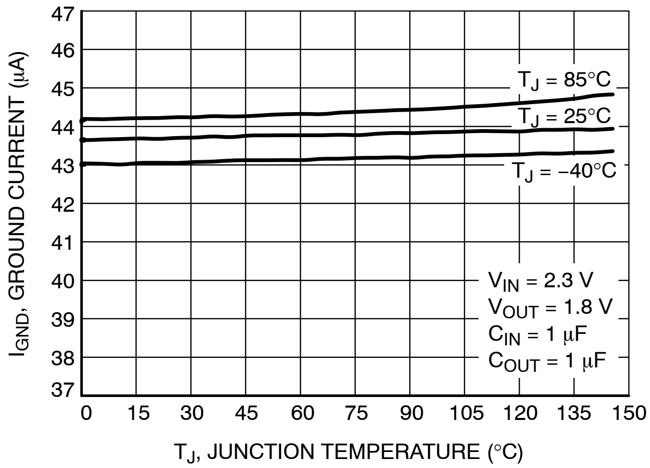


Figure 9. Ground Current vs. Load Current – V_{OUT} = 1.8 V

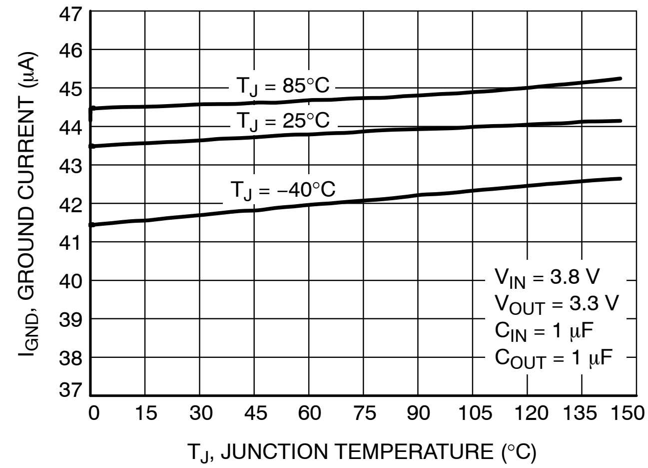


Figure 10. Ground Current vs. Load Current – V_{OUT} = 3.3 V

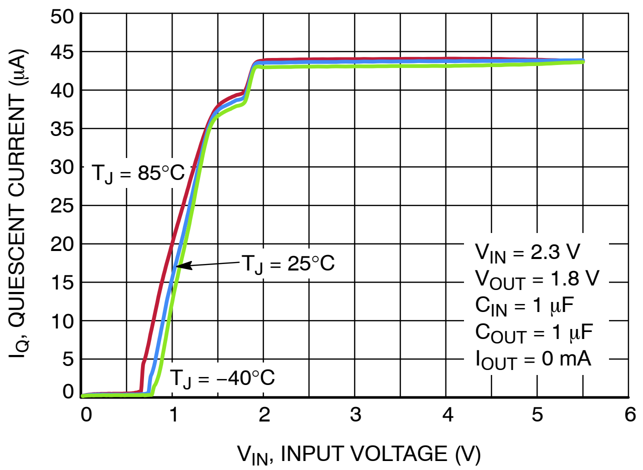


Figure 11. Quiescent Current vs. Input Voltage – V_{OUT} = 1.8 V

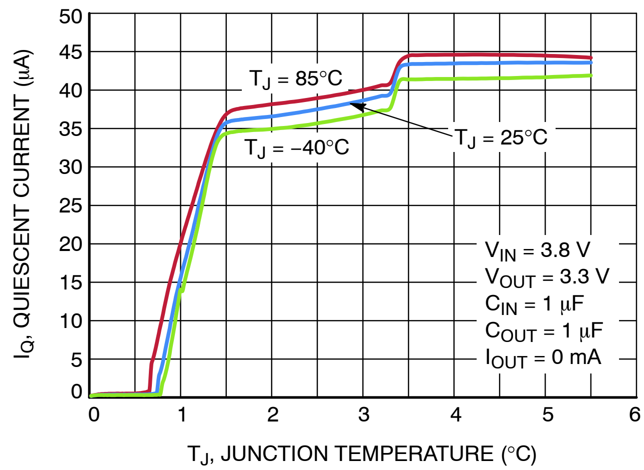


Figure 12. Quiescent Current vs. Input Voltage – V_{OUT} = 3.3 V

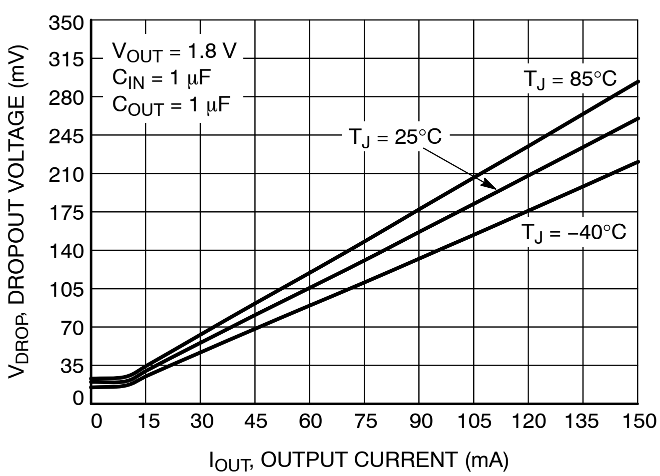


Figure 13. Dropout Voltage vs. Load Current – V_{OUT} = 1.8 V

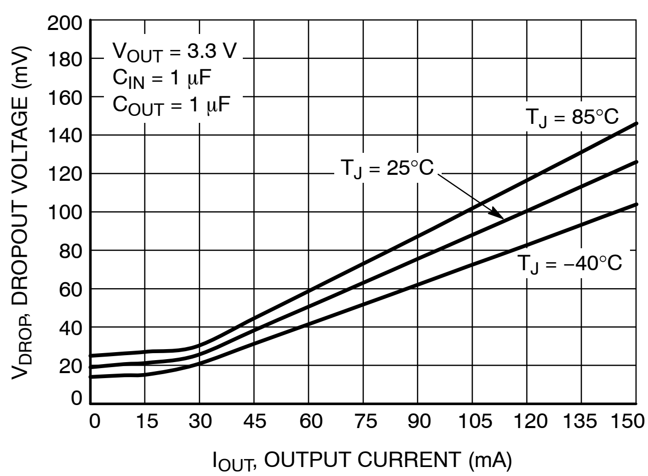


Figure 14. Dropout Voltage vs. Load Current – V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

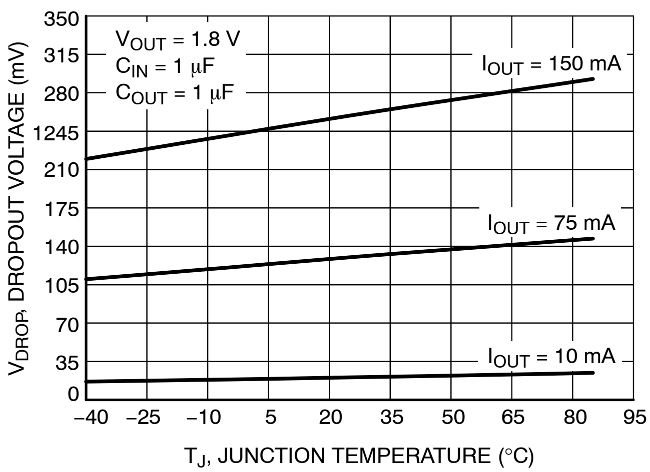


Figure 15. Dropout Voltage vs. Temperature – V_{OUT} = 1.8 V

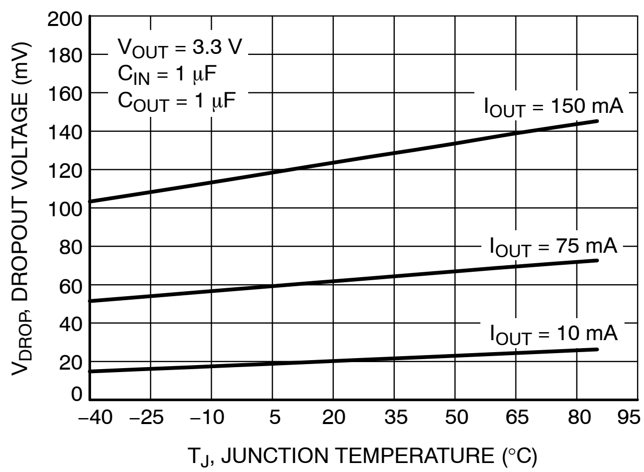


Figure 16. Dropout Voltage vs. Temperature – V_{OUT} = 3.3 V

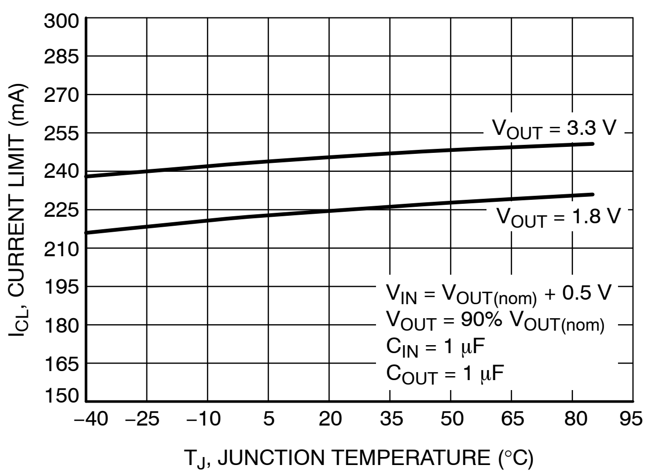


Figure 17. Current Limit vs. Temperature

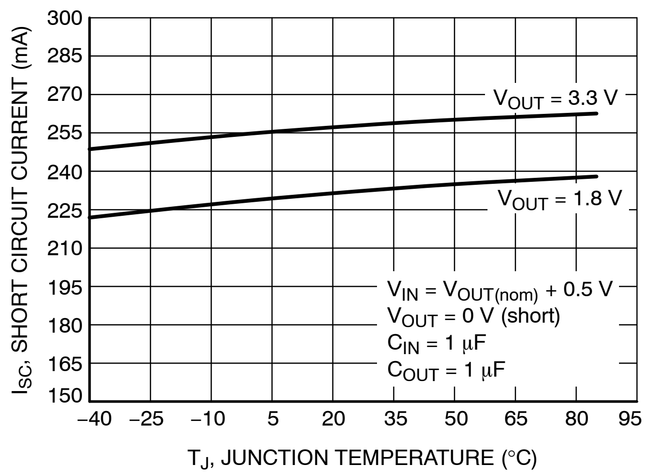


Figure 18. Short Circuit Current vs. Temperature

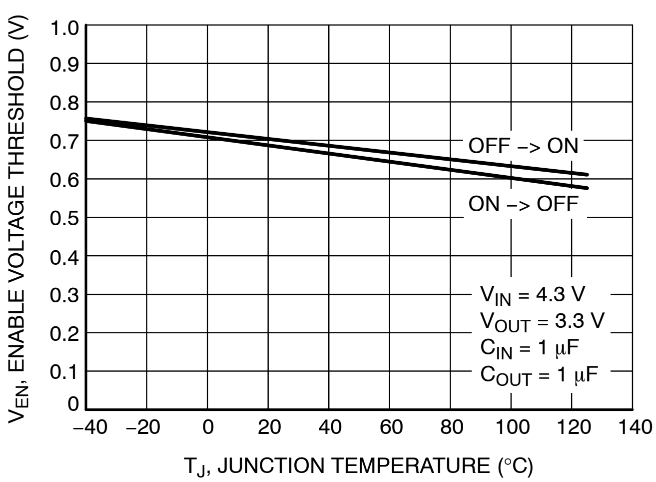


Figure 19. Enable Threshold Voltage vs. Temperature

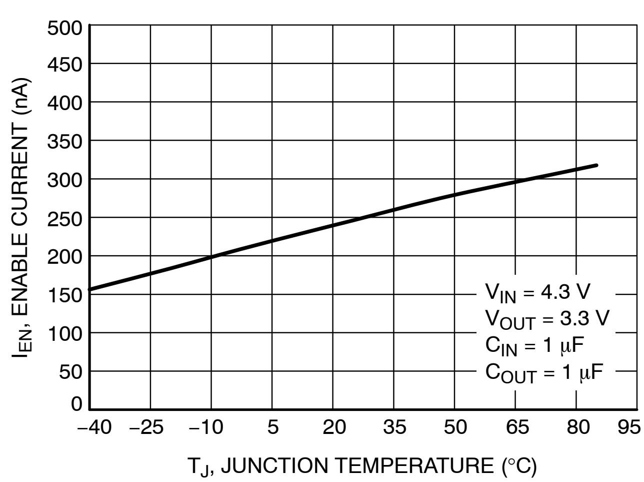


Figure 20. Enable Current vs. Temperature

TYPICAL CHARACTERISTICS

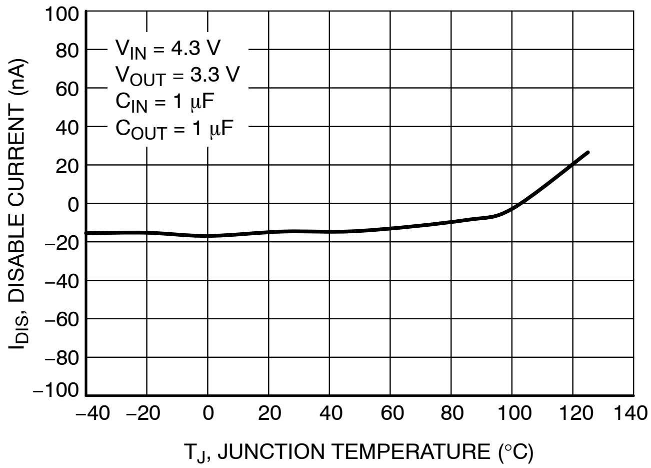


Figure 21. Disable Current vs. Temperature

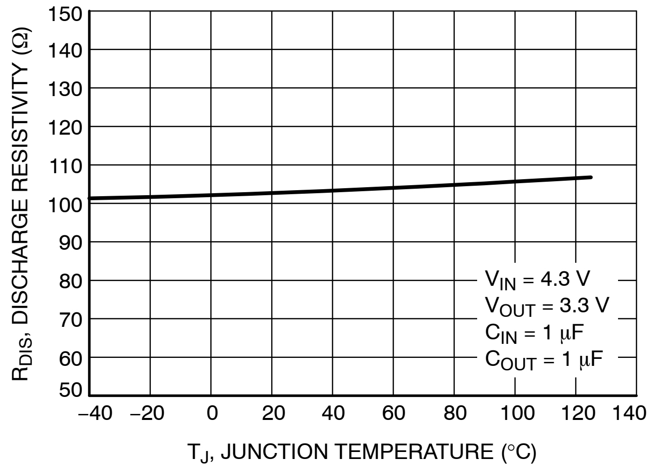


Figure 22. Discharge Resistivity vs. Temperature

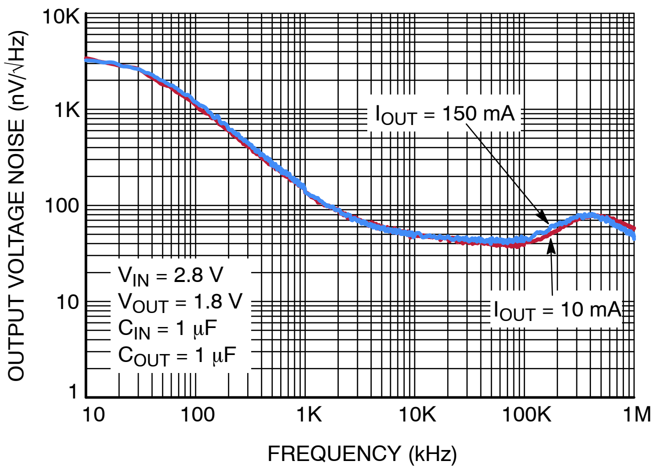


Figure 23. Output Voltage Noise Spectral Density – V_{OUT} = 1.8 V

I_{OUT}	RMS Output Noise (μV)	
	10 Hz – 100 kHz	100 Hz – 100 kHz
10 mA	26.21	17.94
150 mA	27.51	19.11

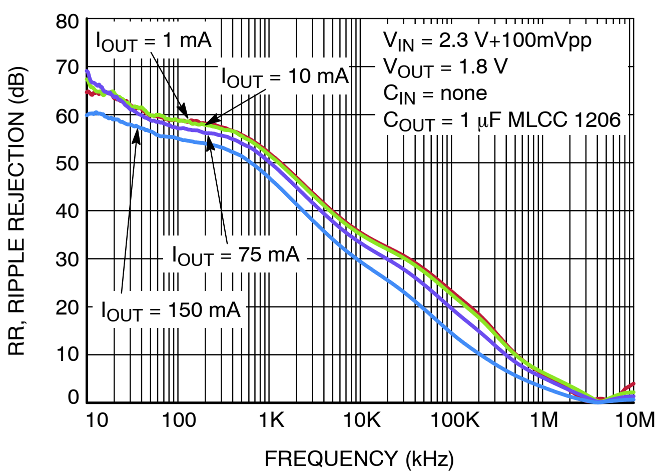


Figure 24. PSRR for Various Output Currents, V_{OUT} = 1.8 V

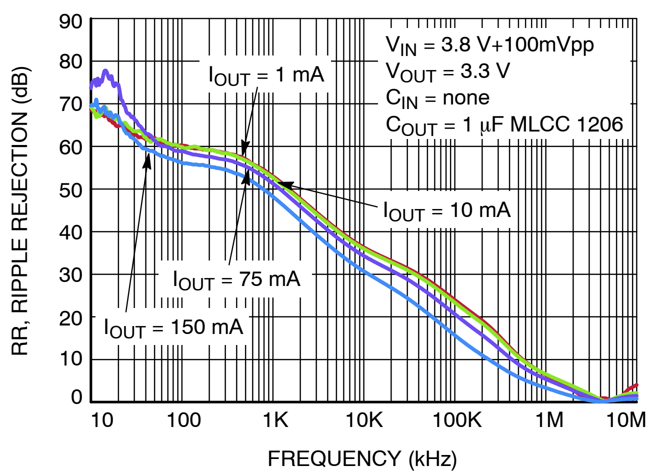


Figure 25. PSRR for Various Output Currents, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

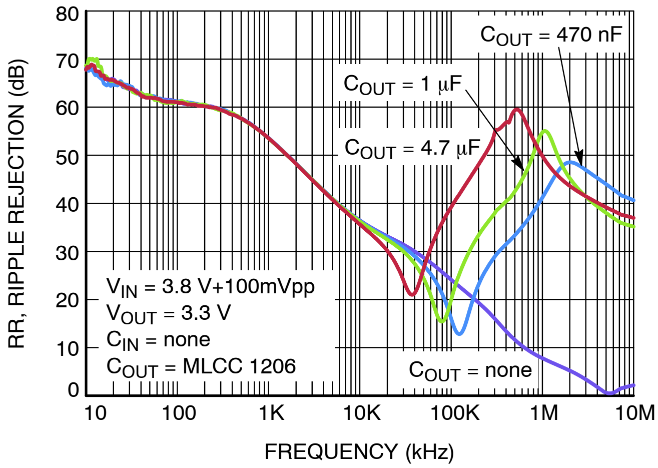


Figure 26. PSRR for Different Output Capacitor, V_{OUT} = 3.3 V

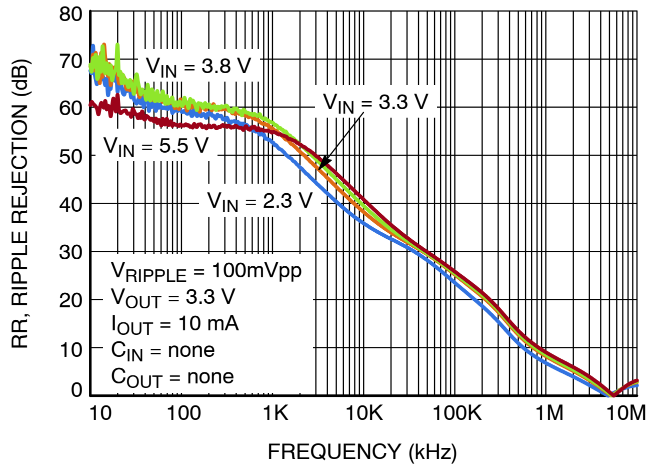


Figure 27. PSRR for Different Output V_{IN}, V_{OUT} = 3.3 V

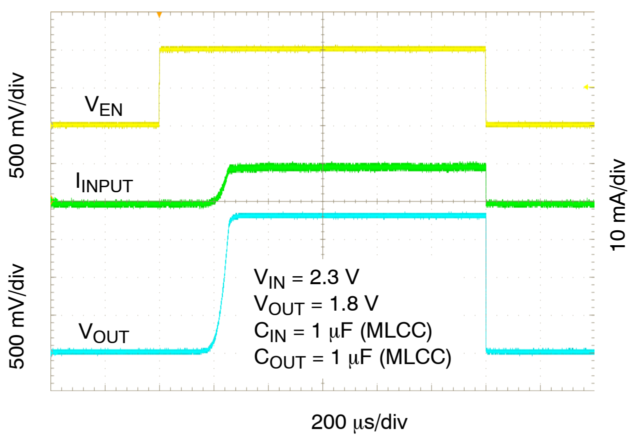


Figure 28. Enable Turn−on Response – C_{OUT} = None, I_{OUT} = 10 mA

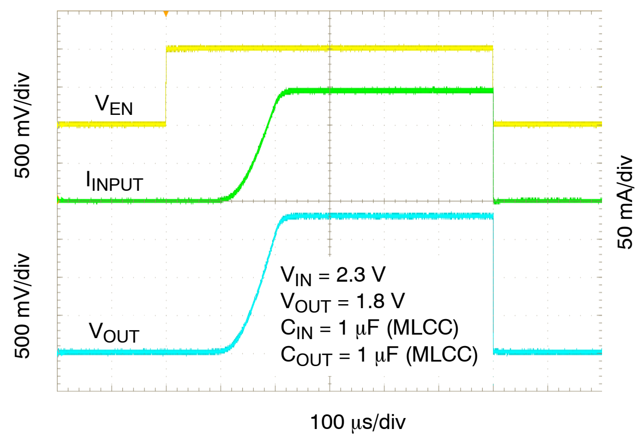


Figure 29. Enable Turn−on Response – C_{OUT} = None, I_{OUT} = 150 mA

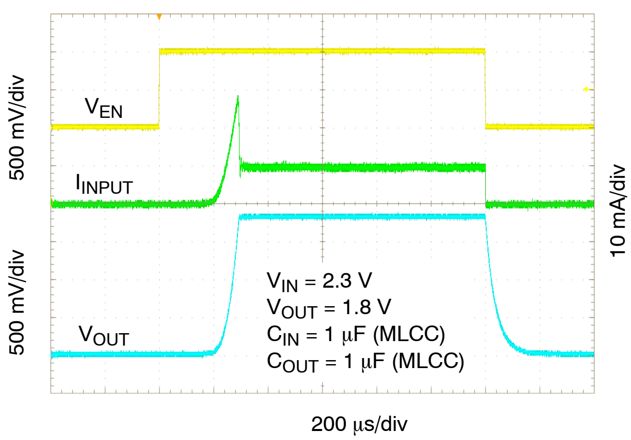


Figure 30. Enable Turn−on Response – C_{OUT} = 470 nF, I_{OUT} = 10 mA

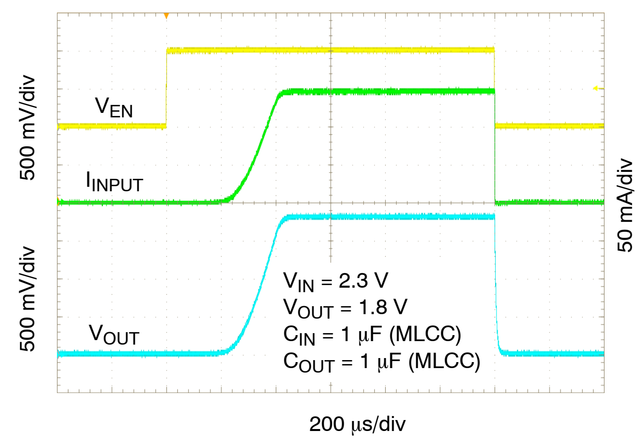


Figure 31. Enable Turn−on Response – C_{OUT} = 470 nF, I_{OUT} = 150 mA

TYPICAL CHARACTERISTICS

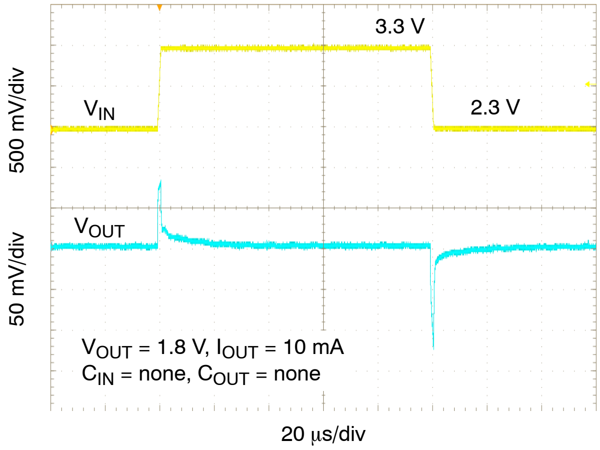


Figure 32. Line Transient Response – C_{OUT} = None

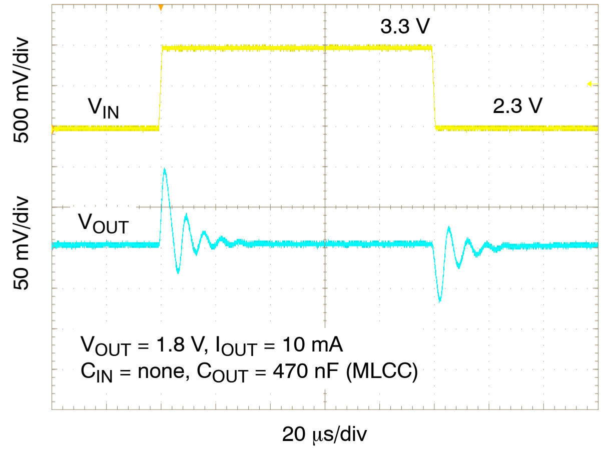


Figure 33. Line Transient Response – C_{OUT} = 470 nF

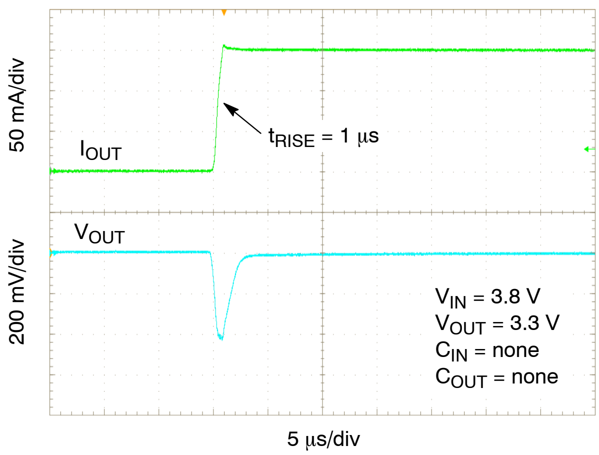


Figure 34. Load Transient Response – 1 mA to 150 mA – C_{OUT} = None

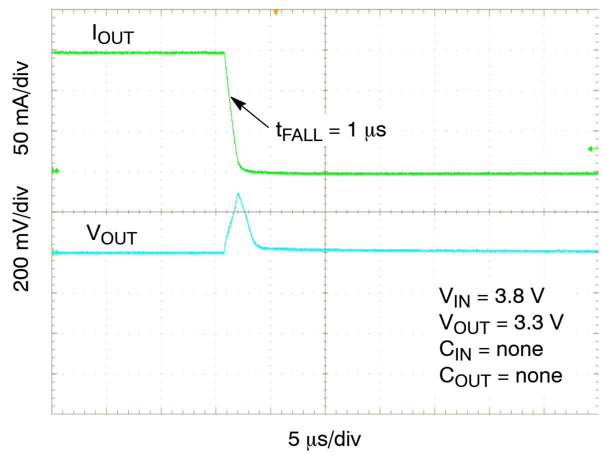


Figure 35. Load Transient Response – 150 mA to 1 mA – C_{OUT} = None

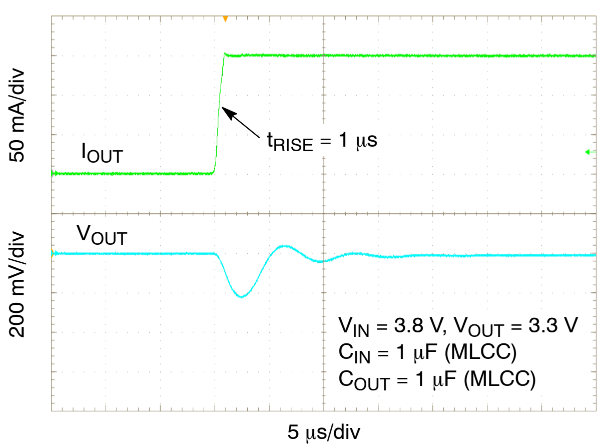


Figure 36. Load Transient Response – 1 mA to 150 mA – C_{OUT} = 1 µF

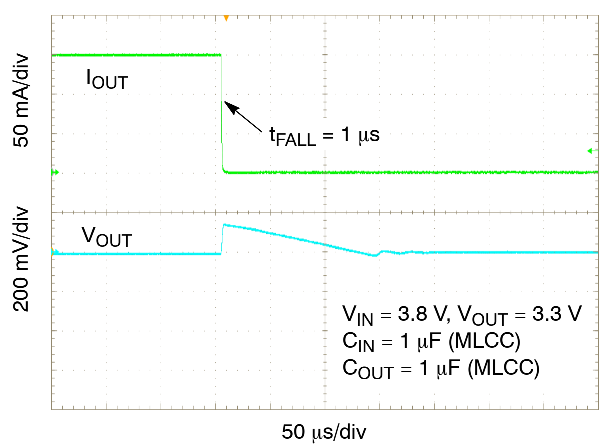


Figure 37. Load Transient Response – 150 mA to 1 mA – C_{OUT} = 1 µF

TYPICAL CHARACTERISTICS

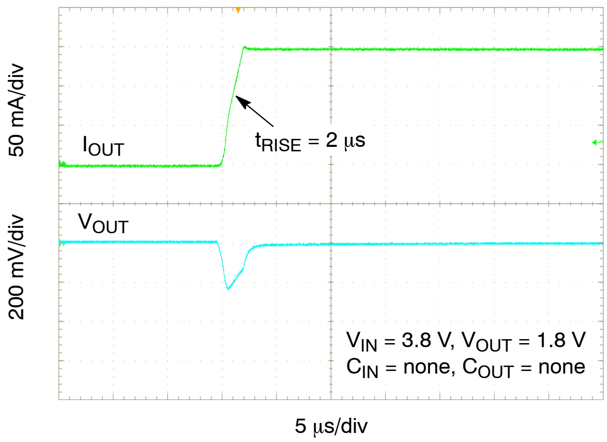


Figure 38. Load Transient Response – 1 mA to 150 mA – t_{RISE} = 2 µs

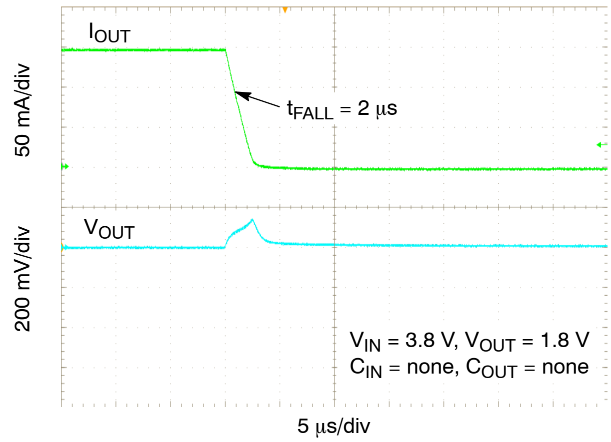


Figure 39. Load Transient Response – 150 mA to 1 mA – t_{FALL} = 2 µs

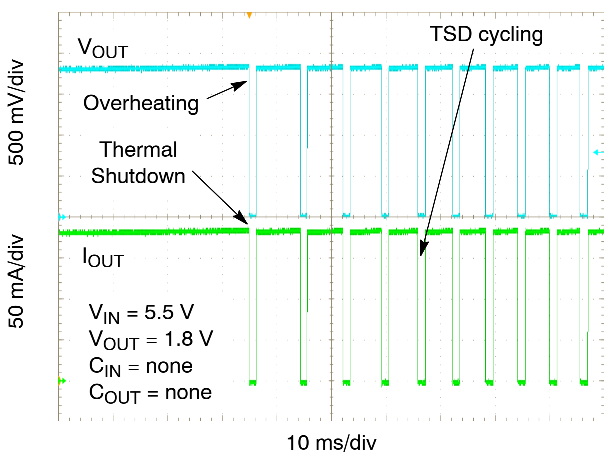


Figure 40. Over Temperature Protection – TSD

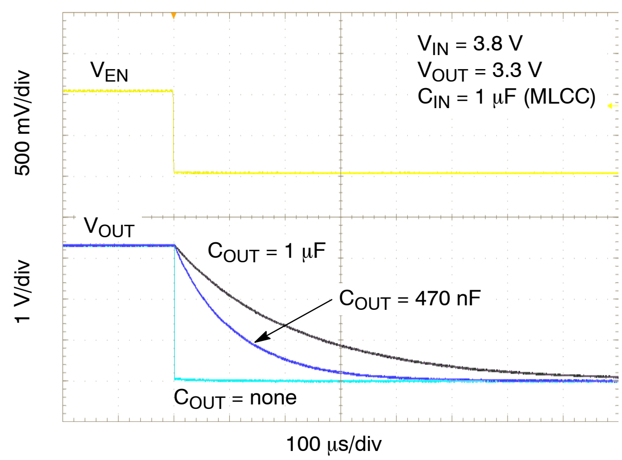


Figure 41. Enable Turn–Off

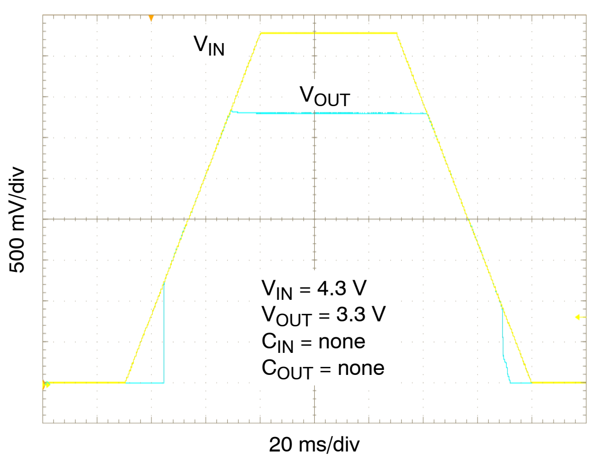


Figure 42. Slow V_{IN} Ramp

APPLICATIONS INFORMATION

General

The NCP140 is high performance low dropout regulator capable of supplying 150 mA and providing very stable output voltage with or without capacitors. The device is designed to remain stable with any type of capacitor or even without input and output capacitor. The NCP140 also offers low quiescent current and very small packages suitable for space constrains application. In connection with no capacitor requirements the regulator is very useful in wearable application, smartphones and everywhere where is high power density required.

Input and Output Capacitor Selection

In spite of the NCP140 is designed as capless device capacitors can be added to improve dynamic behavior such as fast load transient or PSRR. Recommendation for selection input and output capacitor is very similar as for high performance LDO. Low ESR ceramic capacitor is the most beneficial for improvement load transient and PSRR but suitable is almost any type of capacitor. The NCP140 remains stable with electrolytic and tantalum capacitor too.

Enable Operation

The NCP140 uses the EN pin to enable/disable its device and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active (only A option) so that the output voltage V_{OUT} is pulled to GND through a 100 Ω resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCP140 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 100 nA which assures that the device is turned−off when the EN pin is not connected. In the case where the EN function isn't required the EN should be tied directly to IN.

Output Current Limit

Output Current is internally limited within the IC to a typical 230 mA. The NCP140 will source this amount of current measured with a voltage drops on the 90% of the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to approximately 250 mA. The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCP140 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCP140 can handle is given by:

$$P_{D(MAX)} = \frac{\left[85^\circ C - T_A\right]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCP140 for given application conditions can be calculated from the following equation:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

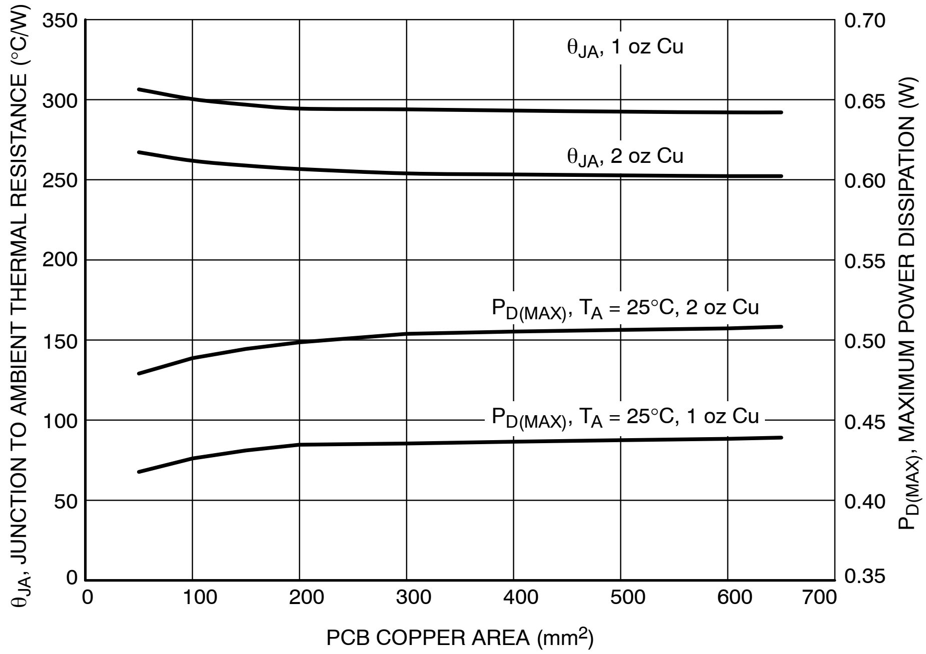


Figure 43. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4− 0.8 x 0.8 mm)

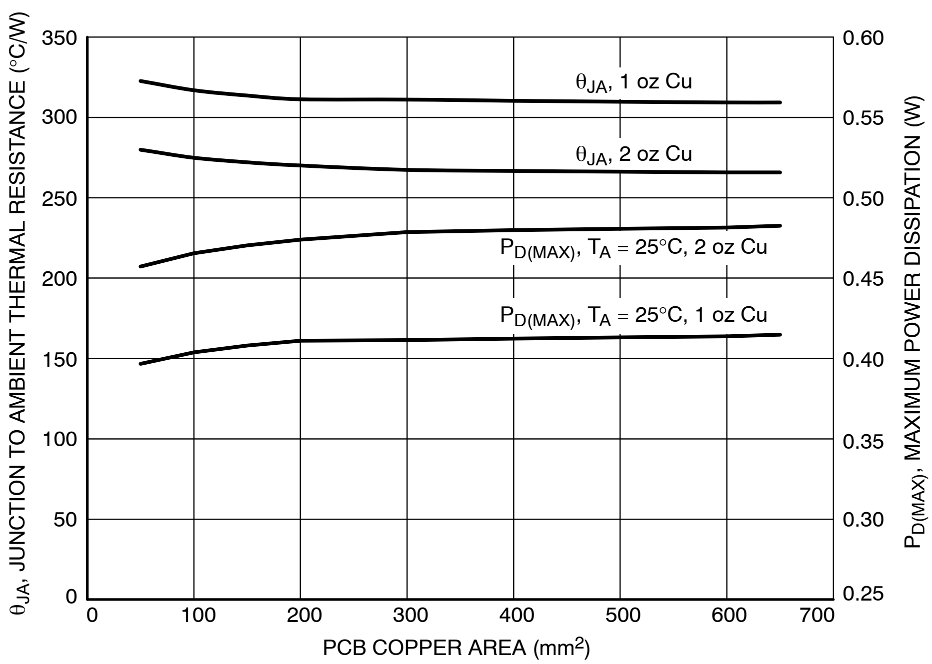


Figure 44. θ_{JA} and $P_{D\ (MAX)}$ vs. Copper Area (XDFN4− 1 x 1 mm)

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

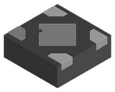
PCB Layout Recommendations

Larger copper area connected to the pins will improve the device thermal resistance and improve maximum power dissipation. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

ORDERING INFORMATION

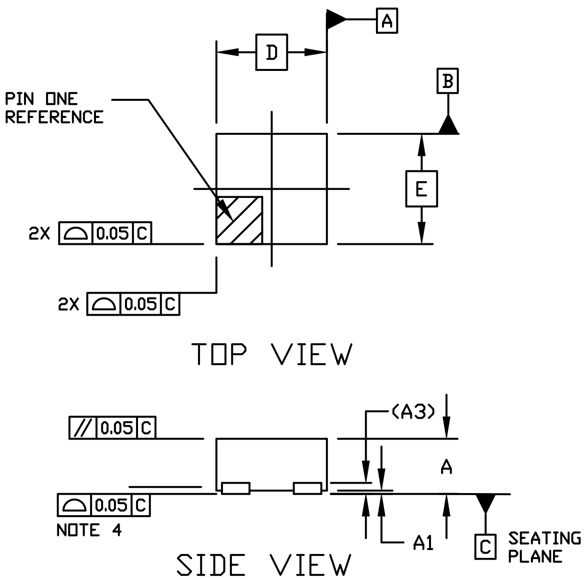
Device	Nominal Output Voltage	Description	Marking	Package	Shipping†
NCP140AMXC180TCG	1.8 V	Active Output Discharge	GA	XDFN4 (Pb−Free) CASE 711BF	3000 / Tape & Reel
NCP140AMXC280TCG	2.8 V		GC		
NCP140AMXC300TCG	3.0 V		GE		
NCP140AMXC330TCG	3.3 V		GD		
NCP140BMXC330TCG	3.3 V	Without Active Output Discharge	G2		
NCP140AMXD180TCG	1.8 V	Active Output Discharge	GA	XDFN4 (Pb−Free) CASE 711AJ	3000 / Tape & Reel
NCP140AMXD280TCG	2.8 V		GC		
NCP140AMXD300TCG	3.0 V		GE		
NCP140AMXD330TCG	3.3 V		GD		
NCP140BMXD330TCG	3.3 V	Without Active Output Discharge	G2		

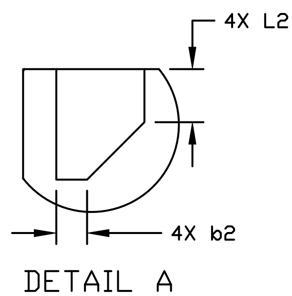
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



XDFN4 1.0x1.0, 0.65P
CASE 711AJ
ISSUE C

DATE 08 MAR 2022

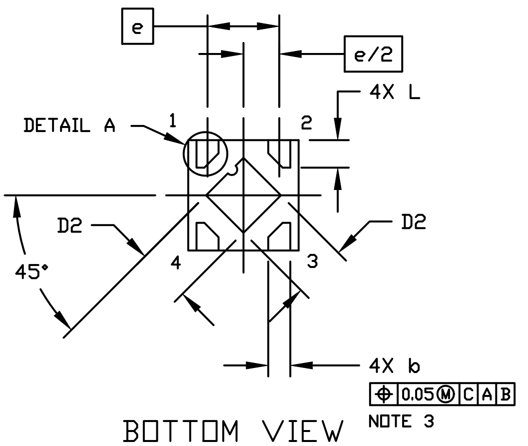


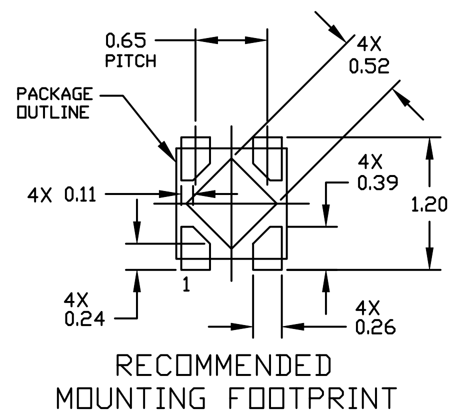


NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.20 FROM THE TERMINAL TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

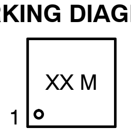
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.33	0.38	0.43
A1	0.00	---	0.05
A3	0.10 REF		
b	0.15	0.20	0.25
b2	0.02	0.07	0.12
D	0.90	1.00	1.10
D2	0.43	0.48	0.53
E	0.90	1.00	1.10
e	0.65 BSC		
L	0.20		0.30
L2	0.07		0.17





* FOR ADDITIONAL INFORMATION ON OUR Pb-FRE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNT TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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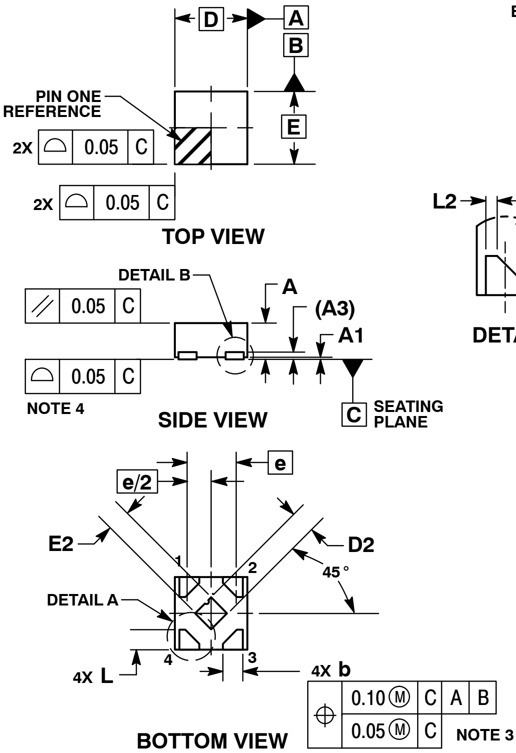
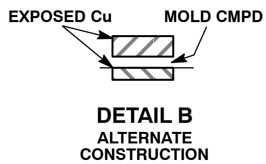
DESCRIPTION:	**XDFN4, 1.0X1.0, 0.65P**	**PAGE 1 OF 1**

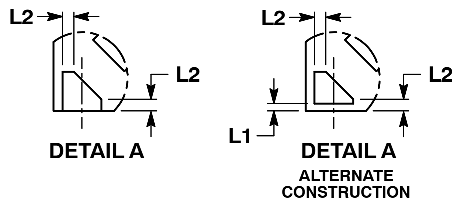
SCALE 4:1

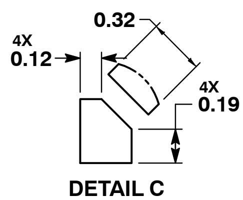
XDFN4 0.8x0.8, 0.48P
CASE 711BF
ISSUE O

DATE 26 FEB 2016





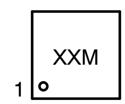




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.33	0.43
A1	0.00	0.05
A3	0.127 REF	
b	0.17	0.27
D	0.80 BSC	
D2	0.20	0.30
E	0.80 BSC	
E2	0.20	0.30
e	0.48 BSC	
L	0.17	0.27
L1	---	0.10
L2	0.06 REF	

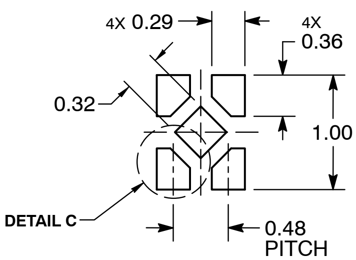
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN4 0.8X0.8, 0.48P	PAGE 1 OF 1

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TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
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