NCP4328

Secondary Side CV/CC Controller

The NCP4328 is a secondary side SMPS controller designed for use in applications which requires constant current and/or constant current regulation.

The NCP4328x consists of two OTA amplifiers for voltage and current loop regulation with precise internal voltage references. Outputs of OTAs are open drain type (OTAs sink current only).

The NCP4328B includes a LED driver pin implemented with an open drain MOSFET driven by a 1 kHz square wave with a 12.5% duty cycle working when VCC is above UVLO for indication purpose.

The NCP4328A is available in TSOP−5 package while the NCP4328B is available in TSOP−6 package.

Features

- Operating Input Voltage Range: 2.5 V to 36.0 V
- Supply current < 100 μA
- ±0.5% Reference Voltage Accuracy (T_J = 25°C)
- Constant Voltage and Constant Current (A versions) Control Loop
- Indication LED PWM Modulated Driver (NCP4328B)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Offline Adapters for Notebooks, Game Stations and Printers
- LED Lightening
- High Power AC−DC Converters for TVs, Set−Top Boxes, Monitors etc.

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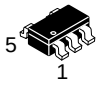
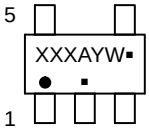
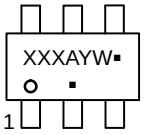
MARKING DIAGRAMS



TSOP−5
SN SUFFIX
CASE 483



TSOP−6
SN SUFFIX
CASE 318G

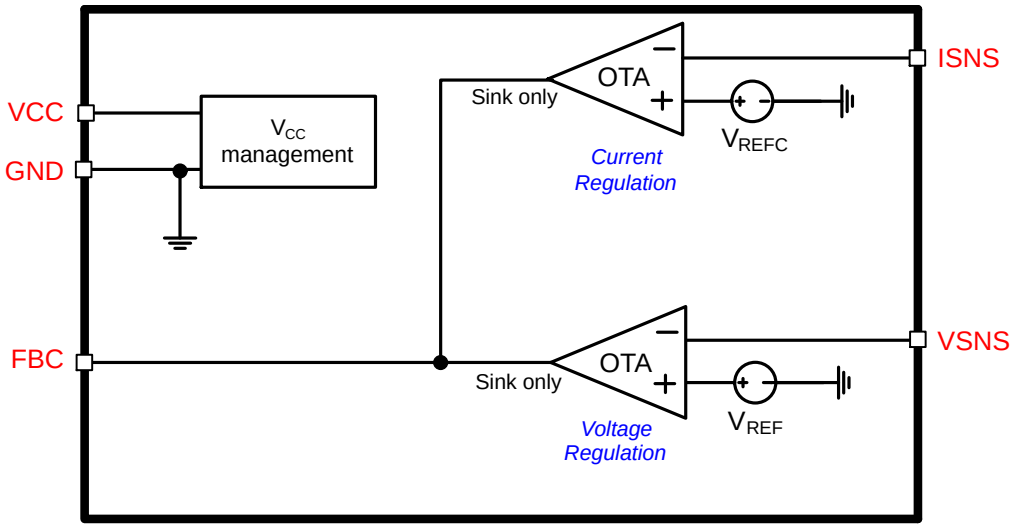


XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

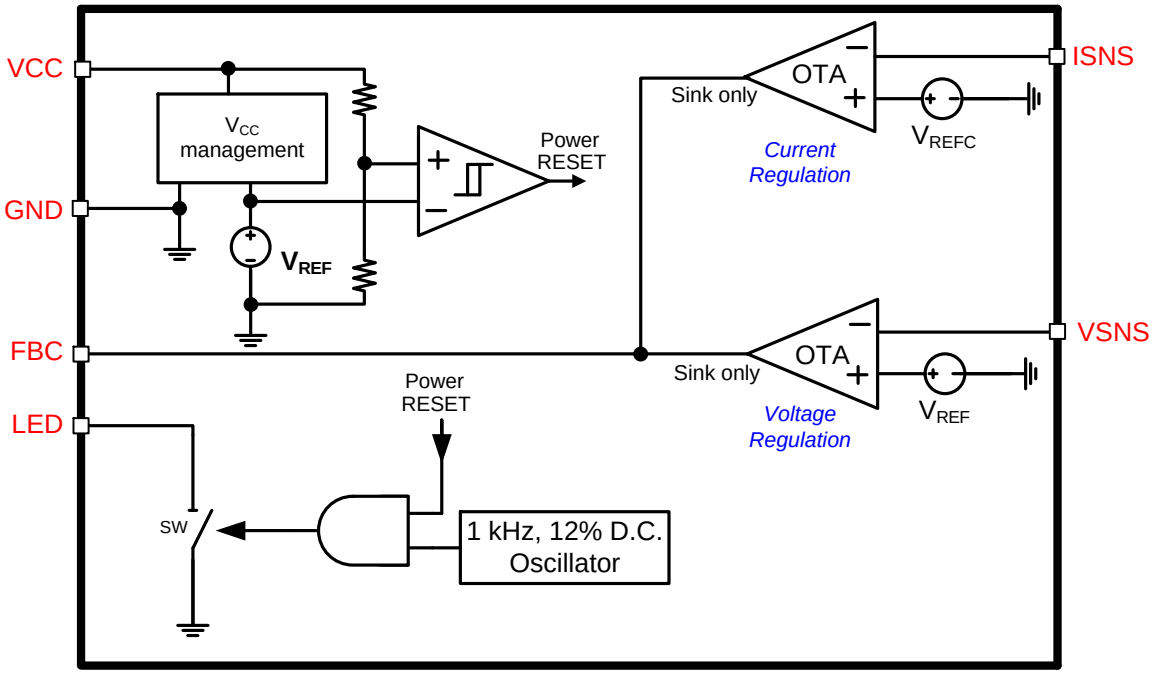
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.



NCP4328A



NCP4328B

Figure 1. Simplified Block Diagrams NCP4328A and NCP4328B

PIN FUNCTION DESCRIPTION

NCP4328A TSOP−5	NCP4328B TSOP−6	Pin Name	Description
1	1	VCC	Supply voltage pin
2	2	GND	Ground
5	6	VSNS	Output voltage sensing pin, connected to output voltage divider
4	4	ISNS	Current sensing input for output current regulation, connect it to shunt resistor in ground branch.
−	5	LED	PWM LED driver output. Connected to LED cathode with current define by external serial resistance
3	3	FBC	Output of current sinking OTA amplifiers driving feedback optocoupler's LED. Connect here compensation networks as well.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	−0.3 to 40.0	V
FBC, LED Voltage	V_{FBC}, V_{LED}	−0.3 to V_{CC} + 0.3	V
VSNS, ISNS Voltage	V_{SNS},V_{ISNS}	−0.3 to 10.0	V
LED Current	I_{LED}	10	mA
Thermal Resistance − Junction−to−Air (Note 1)	$R_{\theta JA}$	315	°C/W
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	250	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 50 mm^2, 1.0 oz. Copper spreader.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114F
   ESD Machine Model tested per JESD22−A115C
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78D.

ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 125°C$; V_{CC} = 15 V; unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum Operating Input Voltage		V_{CC}			36.0	V
VCC UVLO	V_{CC} rising	V_{CCUVLO}	3.3	3.5	3.7	V
	V_{CC} falling		2.3	2.5	2.7	
VCC UVLO Hysteresis		$V_{CCUVLOHYS}$	0.8	1.0		V
Quiescent Current	NCP4328A	I_{CC}		105	130	μA
	NCP4328B			115	140	
VOLTAGE CONTROL LOOP OTA						
Transconductance	Sink current only	gm_V		1		S
Reference Voltage	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 25°C	V_{REF}	1.244	1.250	1.256	V
	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 − 85°C		1.240	1.250	1.264	
	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = −40 − 125°C		1.230	1.250	1.270	
Sink Current Capability	V_{FBC} > 1.5 V	I_{SINKV}	2.5			mA
Inverting Input Bias Current	V_{SNS} = V_{REF}	I_{BIASV}	−100		100	nA
CURRENT CONTROL LOOP OTA						
Transconductance	Sink current only	gm_C		3		S
Reference Voltage	T_J = 25°C	V_{REFC}	61.2	62.5	63.8	mV
	T_J = −20 – 85°C		60.5	62.5	64.5	
	T_J = −40 – 125°C		60.0	62.5	65.0	
Sink Current Capability	V_{FBC} > 1.5 V	I_{SINKC}	2.5			mA
Inverting Input Bias Current	I_{SNS} = V_{REFC}	I_{BIASC}	−100		100	nA
LED DRIVER (NCP4328B Only)						
Switching Frequency		f_{SWLED}		1		kHz
Duty Cycle	(Note 3)	D_{LED}	10.0	12.5	15.0	%
Switch Resistance	I_{LED} = 5 mA	R_{SW}		50		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by design.

TYPICAL CHARACTERISTICS

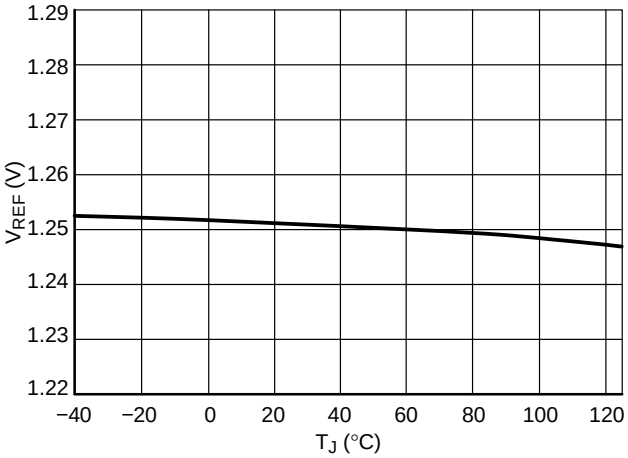


Figure 2. V_{REF} at V_{CC} = 15 V

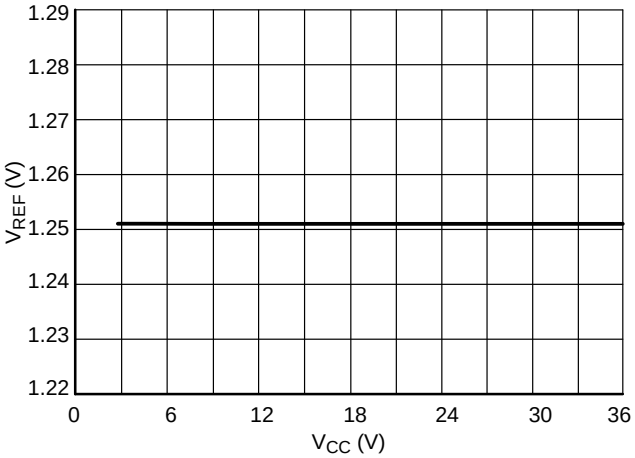


Figure 3. V_{REF} at T_J = 25°C

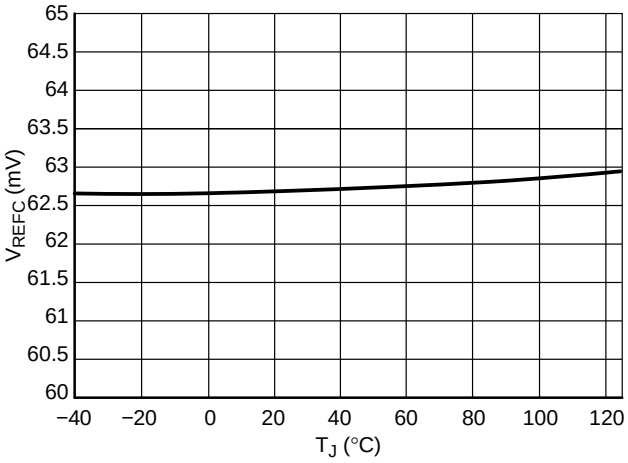


Figure 4. V_{REFC} at V_{CC} = 15 V

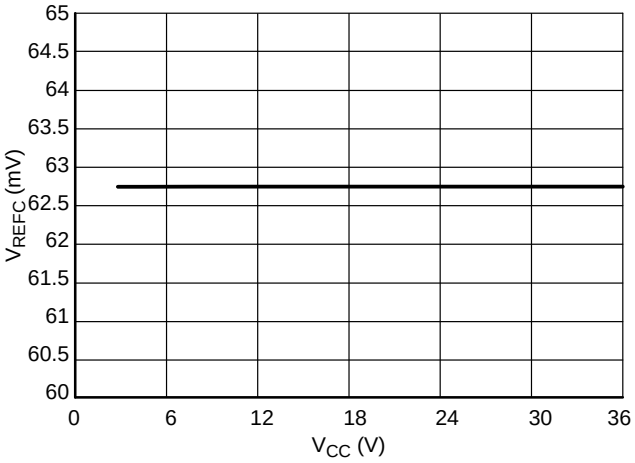


Figure 5. V_{REFC} at T_J = 25°C

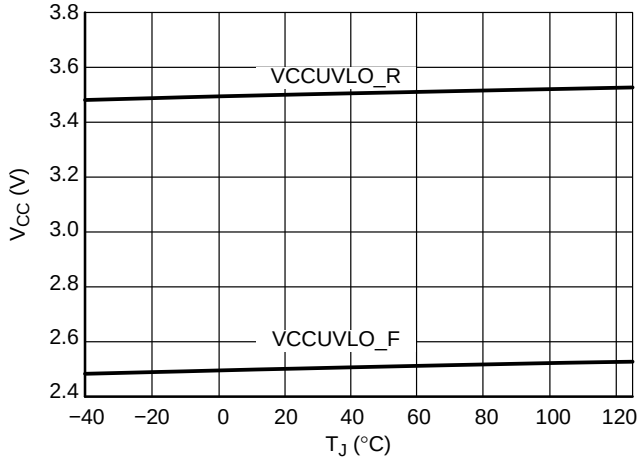


Figure 6. V_{CCUVLO}

TYPICAL CHARACTERISTICS

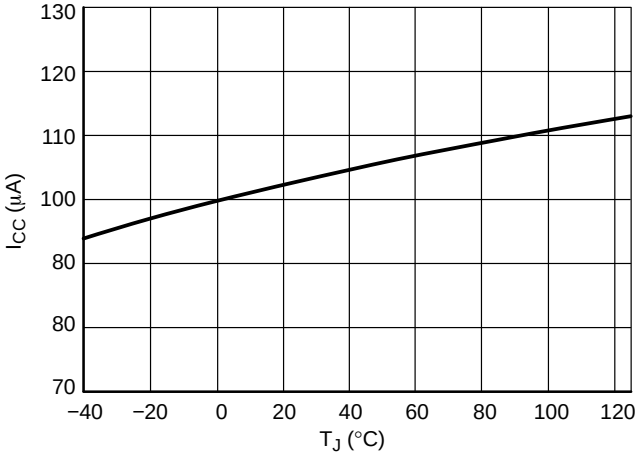


Figure 7. I_{CC} at V_{CC} = 15 V for NCP4328A

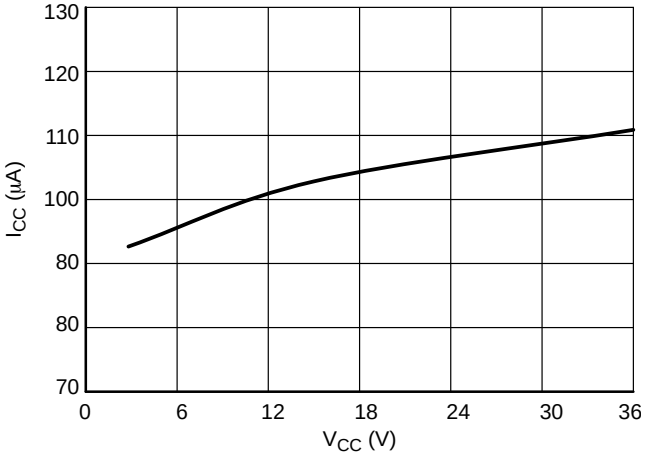


Figure 8. I_{CC} at T_J = 25°C for NCP4328A

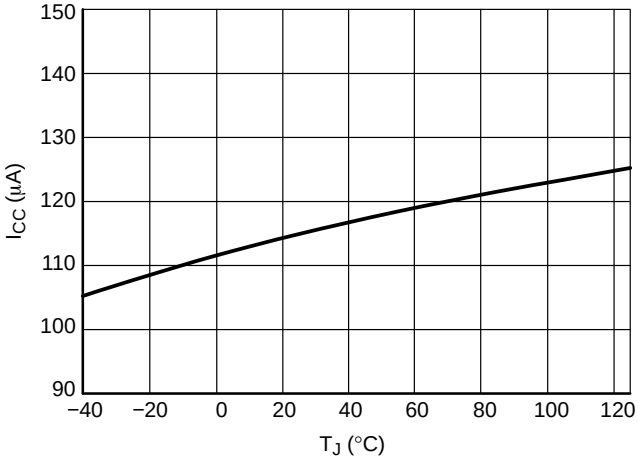


Figure 9. I_{CC} at V_{CC} = 15 V for NCP4328B

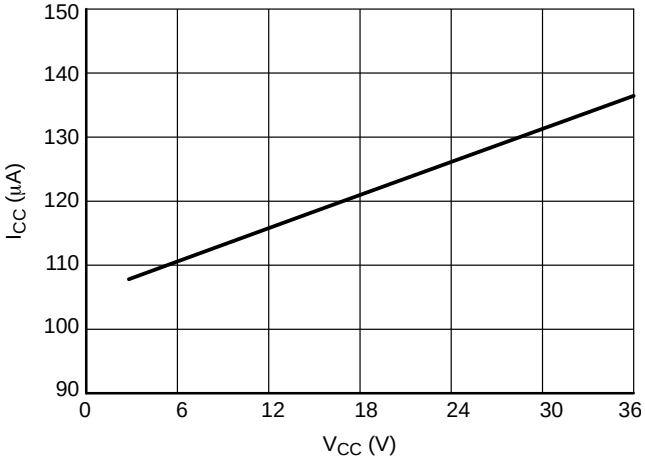


Figure 10. I_{CC} at T_J = 25°C for NCP4328B

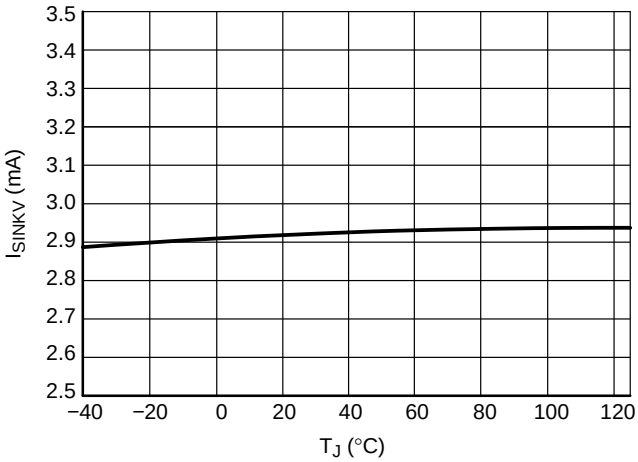


Figure 11. Voltage OTA Current Sink Capability

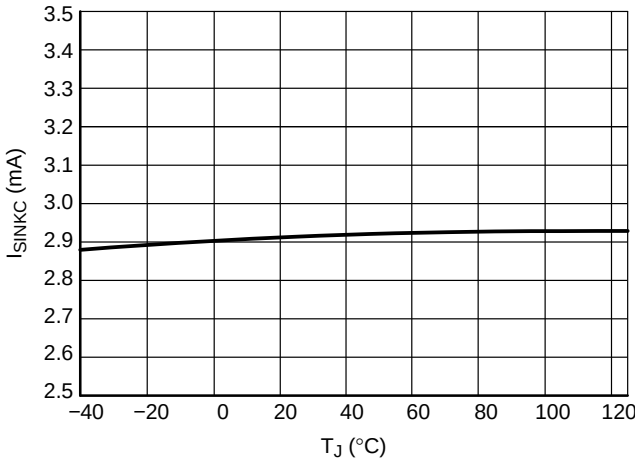


Figure 12. Current OTA Current Sink Capability

TYPICAL CHARACTERISTICS

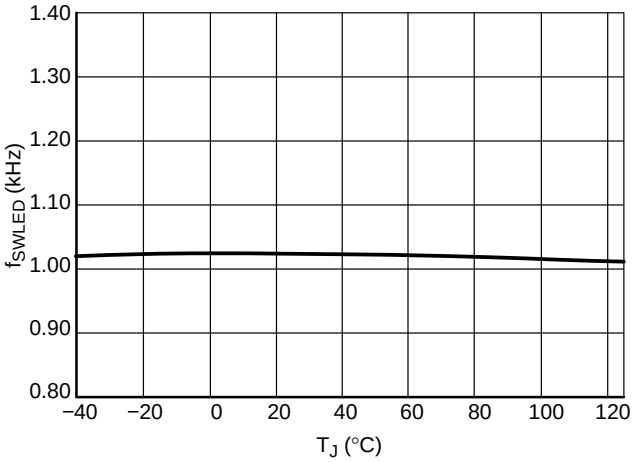


Figure 13. LED Switching Frequency at V_{CC} = 15 V

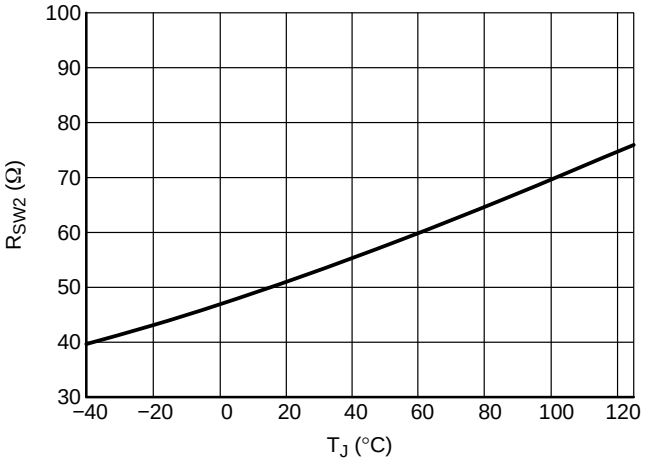


Figure 14. R_{SW} at V_{CC} = 15 V

APPLICATION INFORMATION

Typical application circuit for NCP4328A is shown in Figures 15 and 16 shows typical application circuit for NCP4328B that includes internal LED driver for indication purpose.

Power Supply

The NCP4328 is designed to operate from a single supply up to 36 V. It starts to operate when VCC voltage reaches 3.5 V and stops when VCC voltage drops below 2.5 V. VCC can be supplied by direct connection to the VOUT voltage of the power supply. It is highly recommended to add a RC filter (R1 and C2) in series from VOUT to VCC pin to reduce voltage spikes and drops that are produced at the converter's output capacitors. Recommended values for this filter are 220 Ω and 1 μF.

Voltage Regulation Path

The output voltage is detected on the VSNS pin by the R3 and R4 voltage divider. This voltage is compared with the internal precise voltage reference. The voltage difference is amplified by gm_V of the transconductance amplifier. The amplifier output current is connected to the FBC pin. The compensation network is also connected to this pin to provide frequency compensation for the voltage regulation path. This FBC pin drives regulation optocoupler that provides regulation of primary side. The optocoupler is supplied via direct connection to VOUT line through resistor R2.

Regulation information is transferred through the optocoupler to the primary side controller where its FB pin is usually pulled down to reduce energy transferred to secondary output.

The output voltage can be computed by Equation 1.

$$V_{OUT} = V_{REF}\frac{R3 + R4}{R4} \quad \text{(eq. 1)}$$

Current Regulation

The output current is sensed by the shunt resistor R5 in series with the load. Voltage drop on R5 is compared with internal precise voltage reference V_{REFC} at I_{SNS} transconductance amplifier input.

Voltage difference is amplified by gm_C to output current of amplifier, connected to FBC pin. Compensation network is connected between this pin and ISNS input to provide frequency compensation for current regulation path. Resistor R6 separates compensation network from sense resistor. Compensation network works into low impedance without this resistor that significantly decreases compensation network impact.

Current regulation point is set to current given by Equation 2.

$$I_{OUTLIM} = \frac{V_{REFC}}{R5} \quad \text{(eq. 2)}$$

LED Driver (NCP4328B only)

LED driver is active when VCC is higher than V_{CCMIN}. LED driver consists of an internal power switch controlled by a PWM modulated logic signal and an external current limiting resistor R9. LED current can be computed by Equation 3

$$I_{LED} = \frac{V_{OUT} - V_{F\_LED}}{R9} \quad \text{(eq. 3)}$$

PWM modulation is used to increase efficiency of LED.

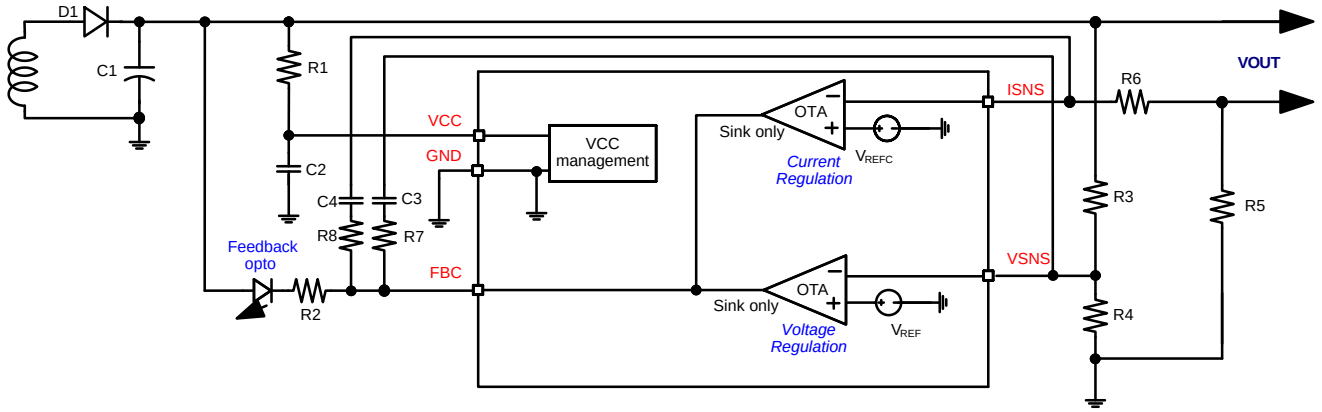


Figure 15. Typical Application Schematic for NCP4328A

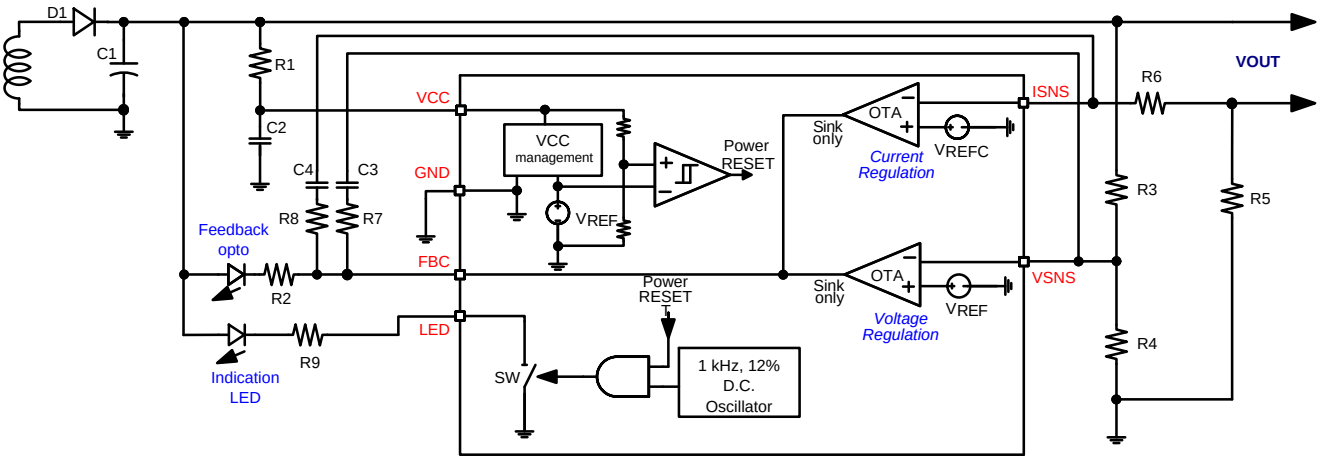


Figure 16. Typical Application Schematic for NCP4328B

ORDERING INFORMATION

Device	Marking	LED Driver	Package	Shipping†
NCP4328ASNT1G	A32	No	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP4328BSNT1G	U32	Yes	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

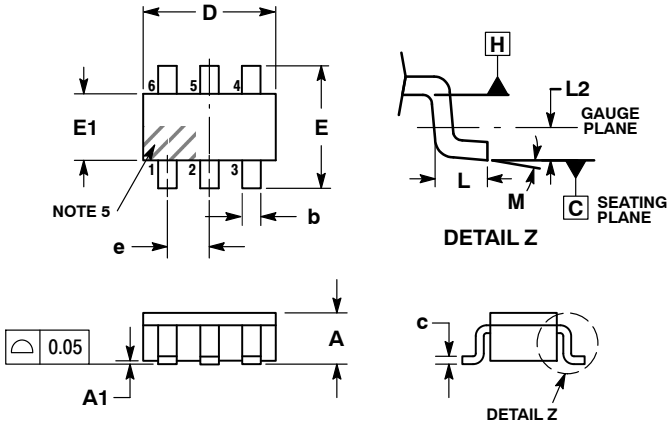
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

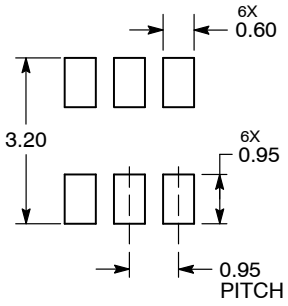
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

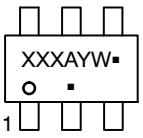
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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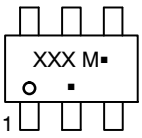


STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

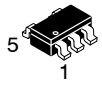
XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

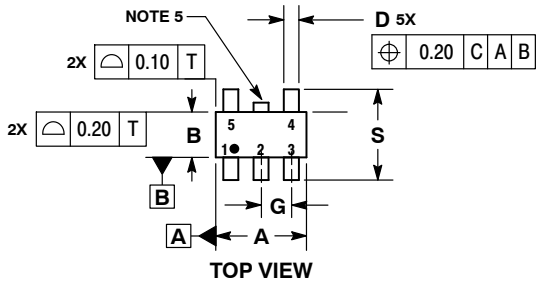
ON Semiconductor®



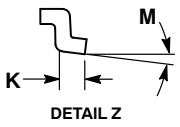
SCALE 2:1

TSOP−5
CASE 483
ISSUE N

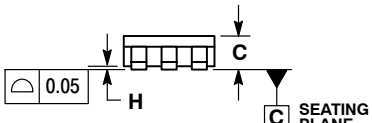
DATE 12 AUG 2020



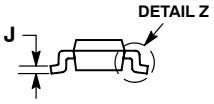
TOP VIEW



DETAIL Z



SIDE VIEW

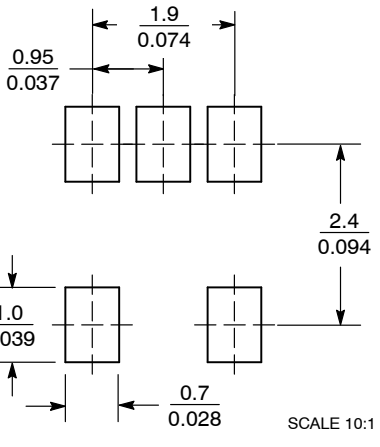


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

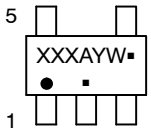
SOLDERING FOOTPRINT*



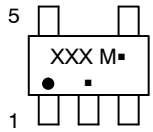
SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



Analog



Discrete/Logic

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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