Buck Converter - High-Efficiency, Synchronous
4 A, 6 A, 2 MHz

NCP1594A, NCP1594B

The NCP1594 is a high−output−current synchronous PWM converter that integrates two N−channel Power MOSFETs. The NCP1594 utilizes externally compensated voltage mode control to provide good transient response, ease of implementation, and excellent loop stability. It regulates input voltages from 2.9 V to 6.0 V down to an output voltage as low as 0.6 V and is able to supply up to 4.0 A of load current (NCP1594A). Please contact factory for NCP1594B which supports 6.0 A load current.

The NCP1594 includes an internal soft−start to limit inrush current. Other features include cycle−by−cycle current limit, 92% max duty cycle, short−circuit protection, and thermal shutdown.

Features

- Wide Input Voltage Range from 2.9 V to 6.0 V
- Nine Preset Output Voltages (0.6 V, 0.7 V, 0.8 V, 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.0 V, and 2.5 V)
- Adjustable Output Voltage Down to 0.6 V
- Adjustable 500 kHz to 2 MHz Switching Frequency
- Externally Adjustable Soft−Start and Able to Start Up with Pre−Biased Output Load
- Selectable Forced PWM with and without Pre−biased Startup
- Compatible with Ceramic, Polymer, and Electrolytic Output Capacitors
- Cycle−by−Cycle Current Limiting
- Hiccup Mode Short−Circuit Protection
- Over Temperature Protection
- This is a 24 Pin 4 x 4 mm 0.5P WQFN Pb−Free Device
- These are Pb−Free Devices

Typical Applications

- Telecom and Networking Power Management
- Computing Power Management
- Datacom Power Management
- Point of Load
- ASIC/CPU/DSP Core and I/O Voltages
- DDR Termination Voltage

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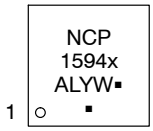
MARKING DIAGRAM

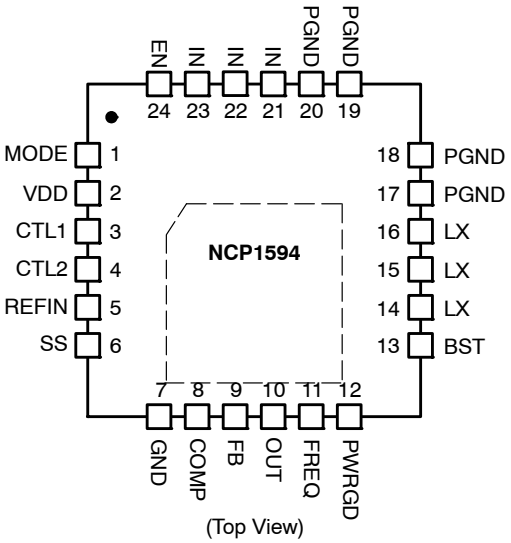
24 PIN WQFN
MT SUFFIX
CASE 510BC



x	= A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1594AMNTXG	WQFN24 (Pb−Free)	4000 / Tape & Reel
NCP1594BMNTXG**	WQFN24 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**This device is End of Life. Please contact sales for additional information and assistance with replacement devices.

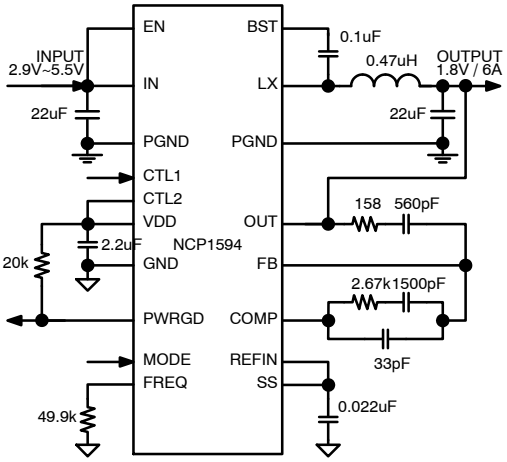


Figure 1. Functional Block Diagram

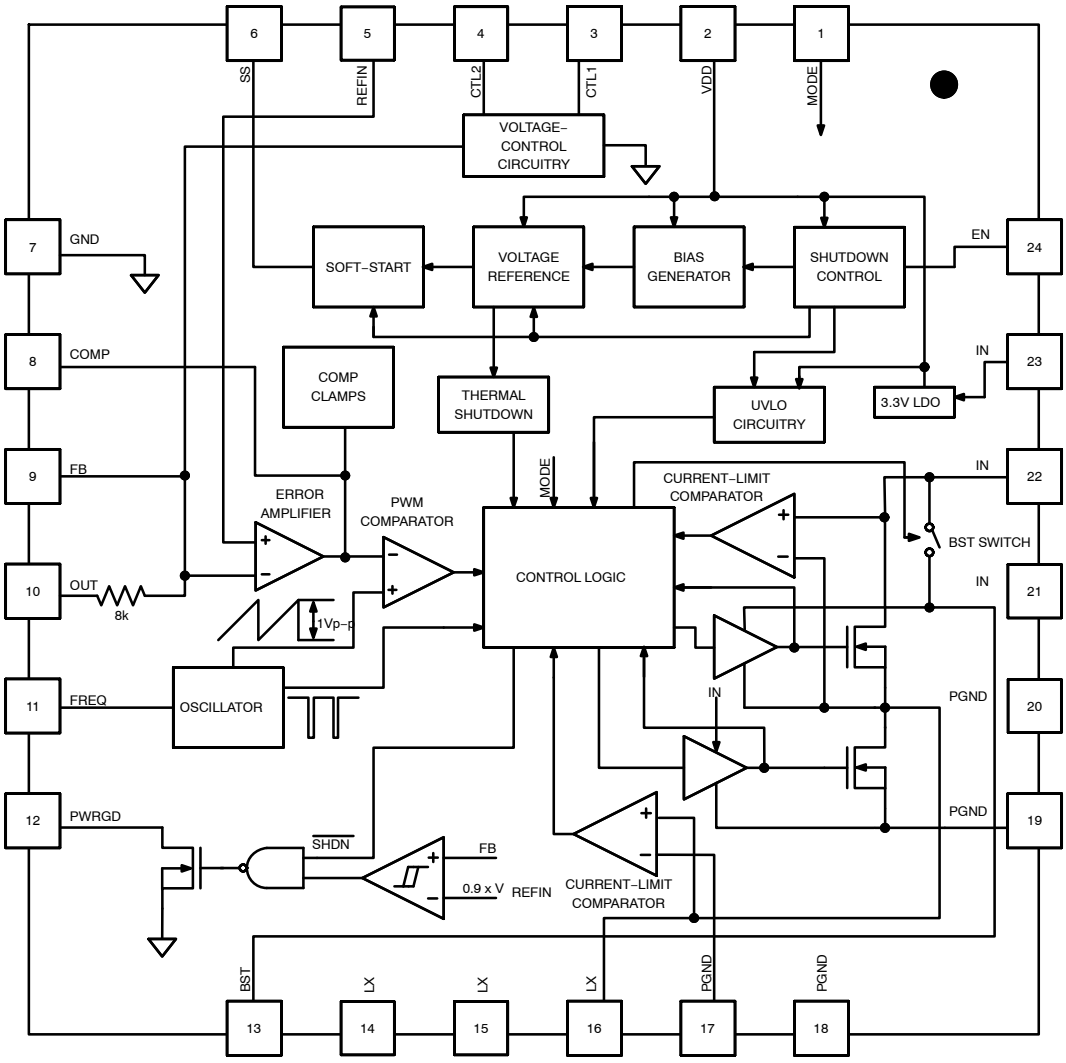


Figure 2. Functional Block Diagram

PIN DESCRIPTION

Pin NO.	Symbol	Descriptions
1	MODE	Mode selection input. Input bias on this pin sets Forced PWM or Forced PWM with pre−biased startup
2	VDD	3.3 V LDO Output. Supply input for the internal analog core. Connect a low−ESR, ceramic capacitor with a minimum value of 2.2 μF from VDD to GND.
3	CTL1	Preset Output−Voltage Selection Inputs. CTL1 and CTL2 set the output voltage to one of nine preset voltages. See Table 1 for details
4	CTL2	
5	REFIN	External Reference Input. Connect REFIN to SS to use the internal 0.6 V reference. Connecting REFIN to an external voltage forces FB to regulate to the voltage applied to REFIN. REFIN is internally pulled to GND when the IC is in shutdown/hiccup mode.
6	SS	Soft−Start Input. Connect a capacitor from SS to GND to set the startup time. Minimum capacitance is 1 nF.
7	GND	Analog Ground Connection. Connect GND and PGND together at one point near the input bypass capacitor return terminal.
8	COMP	Voltage Error−Amplifier Output. Connect the necessary compensation network from COMP to FB and OUT. COMP is internally pulled to GND when the IC is in shutdown/hiccup mode.
9	FB	Feedback Input. Connect FB to the center tap of an external resistive divider from the output to GND to set the output voltage from 0.6 V to 90% of VIN. Connect FB through an RC network to the output when using CTL1 and CTL2 to select any of nine preset voltages.
10	OUT	Output−Voltage Sense. Connect to the converter output. Leave OUT unconnected when an external resistive divider is used.
11	FREQ	Oscillator Frequency Select. Connect a precision resistor from FREQ to GND to select the switching frequency.
12	PWRGD	Open−Drain, Power−Good Output. PWRGD is high impedance when VFB rises above 92.5% (typ) of VREFIN and VREFIN is above 0.54 V. PWRGD is internally pulled low when VFB falls below 90% (typ) of VREFIN or VREFIN is below 0.54 V. PWRGD is internally pulled low when the IC is in shutdown mode, VDD is below the internal UVLO threshold, or the IC is in thermal shutdown.
13	BST	High−Side MOSFET Driver Supply. Internally connected to IN through a P−MOS switch Bypass BST to LX with a 0.1 μF capacitor.
14−16	LX	Inductor Connection. All LX pins are internally shorted together. Connect all LX pins to the switched side of the inductor. LX is high impedance when the IC is in shutdown mode.
17−20	PGND	Power Ground. Connect all PGND pins externally to the power ground plane. Connect all PGND pins together near the IC.
21−23	IN	Input Power Supply. Input supply range is from 2.9 V to 6.0 V. Bypass IN to PGND with a 22 μF ceramic capacitor.
24	EN	Enable Input. Logic input to enable/disable the NCP1594.
—	EP	Exposed Pad. Solder EP to a large contiguous copper plane connected to PGND to optimize thermal performance. Do not use EP as a ground connection for the device.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply to GND	IN,PGND	7 −0.3	V
VDD to GND	V_{DD}	the lower of 7 V or (V_{IN} + 0.3) −0.3	V
COMP, FB, MODE, REFIN, CTL1, CTL2, SS, FREQ to GND		(V_{DD} + 0.3) −0.3	V
OUT, EN to GND		7 −0.3	V
BST to GND	BST	14 −0.3	V
BST to LX	BST,LX	7 −0.3	V
PGND to GND	PGND	0.3 −0.3	V
LX to PGND	LX	the lower of 7 V or (V_{IN} + 0.3) −0.3 the lower of +7 V or (V_{IN} + 1) (t ≤ 50 ns) −1.0 V (t ≤ 50 ns) 8.5 V(t ≤ 10 ns) −2.5 V (t ≤ 10 ns)	V
ILX(rms) (NCP1594A/B)		4/6	A
VDD Output Short Circuit Duration		Continuous	
Converter Output Short Circuit Duration		Continuous	
Continuous Power Dissipation (Note 1)	P_D	2222	mW
Operating Ambient Temperature Range (Note 2)	T_A	−40 to +85	°C
Operating Junction Temperature Range (Note 2)	T_J	−40 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Thermal Characteristics (Note 1)	$R_{\theta JA}$ $R_{\theta JC}$	36 6	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. R_{th_JA} measured on approximately 1x1 in sq of 1 oz. Copper FR−4 or G−10 board.

ELECTRICAL CHARACTERISTICS (V_{IN} = V_{EN} = 5 V, C_{VDD} = 2.2 μF, T_A = T_J = −40°C to 85°C, typical values are at T_A = 25°C, circuit of Figure 1, unless other noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT POWER SUPPLY							
IN Voltage Range	V_{IN}			2.9		6.0	V
IN Supply Current	I_{IN}	F_{SW} = 1 MHz, no load (NCP1594A)	V_{IN} = 3.3 V		4.7	8	mA
			V_{IN} = 5 V		5.0	8.5	
		F_{SW} = 1 MHz, no load (NCP1594B)	V_{IN} = 3.3 V		4.9	8	
			V_{IN} = 5 V		5.2	8.5	
Total Shutdown Current from IN	ISD	V_{IN} = 5 V, V_{EN} = 0 V			10	20	μA
		V_{IN} = V_{DD} = 3.3 V, V_{EN} = 0 V			45		

ELECTRICAL CHARACTERISTICS (V_{IN} = V_{EN} = 5 V, C_{VDD} = 2.2 μF, T_A = T_J = −40°C to 85°C, typical values are at T_A = 25°C, circuit of Figure 1, unless other noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
3.3V LDO (VDD)							
VDD Undervoltage Lockout Threshold	VDD_R	LX starts/stops switching	V_{DD} rising		2.6	2.8	V
	VDD_F		V_{DD} falling	2.35	2.55		V
	TDD		Minimum glitch−width rejection		10		μs
VDD Output Voltage	VDD	V_{IN} = 5 V, IV_{DD} = 0 to 10 mA		3.1	3.3	3.5	V
VDD Dropout	VDD_DRP	V_{IN} = 2.9 V, IV_{DD} = 10 mA				0.08	V
VDD Current Limit	IDD_LMT	V_{IN} = 5 V, V_{DD} = 0 V		25	40		mA
BST							
BST Supply Current	IBST	V_{BST} = V_{IN} = 5 V, V_{LX} = 0 or 5 V, V_{EN} = 0 V			0.025		μA
PWM COMPARATOR							
PWM Comparator Propagation Delay	TD_PWM	10 mV overdrive			20		ns
PWM Peak−to−Peak Ramp Amplitude	RAMP				1		V
PWM Valley Amplitude	RAMP_OS				0.8		V
ERROR AMPLIFIER							
COMP Clamp Voltage, High	COMP_H	V_{IN} = 2.9 V to 5 V, V_{FB} = 0.5 V, V_{REFIN} = 0.6 V			2		V
COMP Clamp Voltage, Low	COMP_L	V_{IN} = 2.9 V to 5 V, V_{FB} = 0.7 V, V_{REFIN} = 0.6 V			0.7		V
COMP Slew Rate	COMP_SL	V_{FB} step from 0.5 V to 0.7 V in 10 ns			1.6		V/μs
COMP Shutdown Resistance	COMP_RS	From COMP to GND, V_{IN} = 3.3 V, V_{COMP} = 100 mV, V_{EN} = V_{SS} = 0 V			6		Ω
Internally Preset Output Voltage Accuracy	VR	VREFIN = VSS, MODE = GND		−1		+1	%
FB Set−Point Value	FB	CTL1 = CTL2 = GND, MODE = GND		0.594	0.6	0.606	V
FB to OUT Resistor	RFB	All VID settings except CTL1 = CTL2 = GND		5.5	8	10.5	kΩ
Open−Loop Voltage Gain	GAIN_EA				115		dB
Error−Amplifier Unity−Gain Bandwidth	BW_EA				28		MHz
Error−Amplifier Common−Mode Input Range	VCOM_EA	V_{DD} = 2.9 V to 3.5 V		0		2	V
Error−Amplifier Maximum Output Current	IMAX_EA	V_{COMP} = 1 V, VREFIN = 0.6 V	V_{FB} = 0.7 V, sinking	1			mA
			V_{FB} = 0.5 V, sourcing	−1			
FB Input Bias Current	IFB	CTL1 = CTL2 = GND			−125		nA
CTL							
CTL Input Bias Current	ICTL	V_{CTL} = 0 V			−7.2		μA
		V_{CTL} = V_{DD}			7.2		

ELECTRICAL CHARACTERISTICS (V_{IN} = V_{EN} = 5 V, C_{VDD} = 2.2 μF, T_A = T_J = −40°C to 85°C, typical values are at T_A = 25°C, circuit of Figure 1, unless other noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
CTL							
CTL Input Threshold	VTH_CTL	Low, falling			0.8		V
		Open			V_{DD}/2		
		High, rising			V_{DD} − 0.8		
Hysteresis	VHS_CTL	All VID transitions			50		mV
REFIN							
REFIN Input Bias Current	IREFIN	VREFIN = 0.6 V			−185		nA
REFIN Offset Voltage	VOS_REFIN	V_{REFIN} = 0.9 V, FB shorted to COMP		−4.5		+4.5	mV
LX (All Pins Combined)							
LX On−Resistance, High Side	Rds_H	I_{LX} = −2 A (NCP1594A)	V_{IN} = V_{BST} − V_{LX} = 3.3 V		42		mΩ
			V_{IN} = V_{BST} − V_{LX} = 5 V		31	54	
		I_{LX} = −2 A (NCP1594B)	V_{IN} = V_{BST} − V_{LX} = 3.3 V		35		mΩ
			V_{IN} = V_{BST} − V_{LX} = 5 V		26	45	
LX On−Resistance, Low Side	Rds_L	I_{LX} = 2 A (NCP1594A)	V_{IN} = 3.3 V		30		mΩ
			V_{IN} = 5 V		24	42	
		I_{LX} = 2 A (NCP1594B)	V_{IN} = 3.3 V		25		mΩ
			V_{IN} = 5 V		20	35	
LX Current−Limit Threshold	ILIM_H	High−side sourcing (NCP1594A)		5.7	7		A
	ILIM_L	Low−side sinking (NCP1594A)			7		
	ILIM_H	High−side sourcing (NCP1594B)		9	11		
	ILIM_L	Low−side sinking (NCP1594B)			11		
LX Leakage Current	ILK_LX	V_{IN} = 5 V, V_{EN} = 0 V	V_{LX} = 0 V		−0.01		μA
			V_{LX} = 5 V		0.01		
LX Switching Frequency	FSW	V_{IN} = 2.9 V to 6.0 V	R_{FREQ} = 49.9 kΩ	0.9	1	1.1	MHz
			R_{FREQ} = 23.6 kΩ	1.8	2	2.2	
Switching Frequency Range	FSW			500		2000	kHz
LX Minimum Off−Time	TOFF_MIN	R_{FREQ} = 49.9 kΩ				78	ns
LX Maximum Duty Cycle	DMAX			92	95		%
LX Minimum Duty Cycle	DMIN	R_{FREQ} = 49.9 kΩ			5	15	%
Average Short−Circuit IN Supply Current	IST	OUT connected to GND, V_{IN} = 5 V (NCP1594A)			0.15		A
		OUT connected to GND, V_{IN} = 5 V (NCP1594B)			0.35		

ELECTRICAL CHARACTERISTICS (V_{IN} = V_{EN} = 5 V, C_{VDD} = 2.2 μF, T_A = T_J = −40°C to 85°C, typical values are at T_A = 25°C, circuit of Figure 1, unless other noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LX (All Pins Combined)						
RMS LX Output Current	IRMS	NCP1594A	4			A
		NCP1594B	6			
ENABLE						
EN Input Logic−Low Threshold	EN_L	EN falling			0.9	V
EN Input Logic−High Threshold	EN_H	EN rising	1.5			V
EN Input Current	IEN	V_{EN} = 0 or 5 V, V_{IN} = 5 V		0.01		μA
MODE						
MODE Input−Logic Threshold	MODE_L	Logic−low, falling		26		%VDD
	MODE_M	Logic V_{DD}/2 or open, rising		50		
	MODE_H	Logic−high, rising		74		
MODE Input−Logic Hysteresis	MODE_HSY	MODE falling		5		%VDD
MODE Input Bias Current	IMODE	MODE = GND		−5		μA
SS						
SS Current	ISS	V_{SS} = 0.45V, V_{REFIN} = 0.6 V, sourcing	6.7	8	9.3	μA
THERMAL SHUTDOWN						
Thermal−Shutdown Threshold	TSD	Rising		150		°C
Thermal−Shutdown Hysteresis	TSD_HSY			25		°C
POWER GOOD (PWRGD)						
Power−Good Threshold Voltage	PG_L	V_{FB} falling, V_{REFIN} = 0.6 V	88	90	92	% VREFIN
	PG_H	V_{FB} rising, V_{REFIN} = 0.6 V		92.5		
Power−Good Edge Deglitch	TPG	V_{FB} rising or falling		48		Clock Cycles
PWRGD Output−Voltage Low	VPG_L	I_{PWRGD} = 4 mA		0.03	0.1	V
PWRGD Leakage Current	ILK_PG	V_{IN} = V_{PWRGD} = 5 V, V_{FB} = 0.7 V, V_{REFIN} = 0.6 V		0.01		μA
HICCUP OVERCURRENT LIMIT						
Current−Limit Startup Blanking	TCBLK			112		Clock Cycles
Autoretry Restart Time	TRST			896		Clock Cycles
FB Hiccup Threshold	VTH_HCP	V_{FB} falling		70		%V_{REFIN}
Hiccup Threshold Blanking Time	TBLK_HCP	V_{FB} falling		28		μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 1. CTL1 AND CTL2 OUTPUT VOLTAGE SELECTION

CTL1	CTL2	V_{OUT} (V)	V_{OUT} (V) When Using External REFIN
GND	GND	0.6	REFIN* or REFIN < V_{OUT} < 0.9 x V_{IN}**
VDD	V_{DD}	0.7	REFIN x (7/6)
GND	Unconnected	0.8	REFIN x (4/3)
GND	V_{DD}	1.0	REFIN x (5/3)
Unconnected	GND	1.2	REFIN x 2
Unconnected	Unconnected	1.5	REFIN x 2.5
Unconnected	V_{DD}	1.8	REFIN x 3
VDD	GND	2.0	REFIN x (10/3)
VDD	Unconnected	2.5	REFIN x (25/6)

*Install an 8.06 kΩresistor at R3 and do not install a resistor at R4 (see Figure 3).
**Install R3 and R4 following the equation in the Compensation Design section.

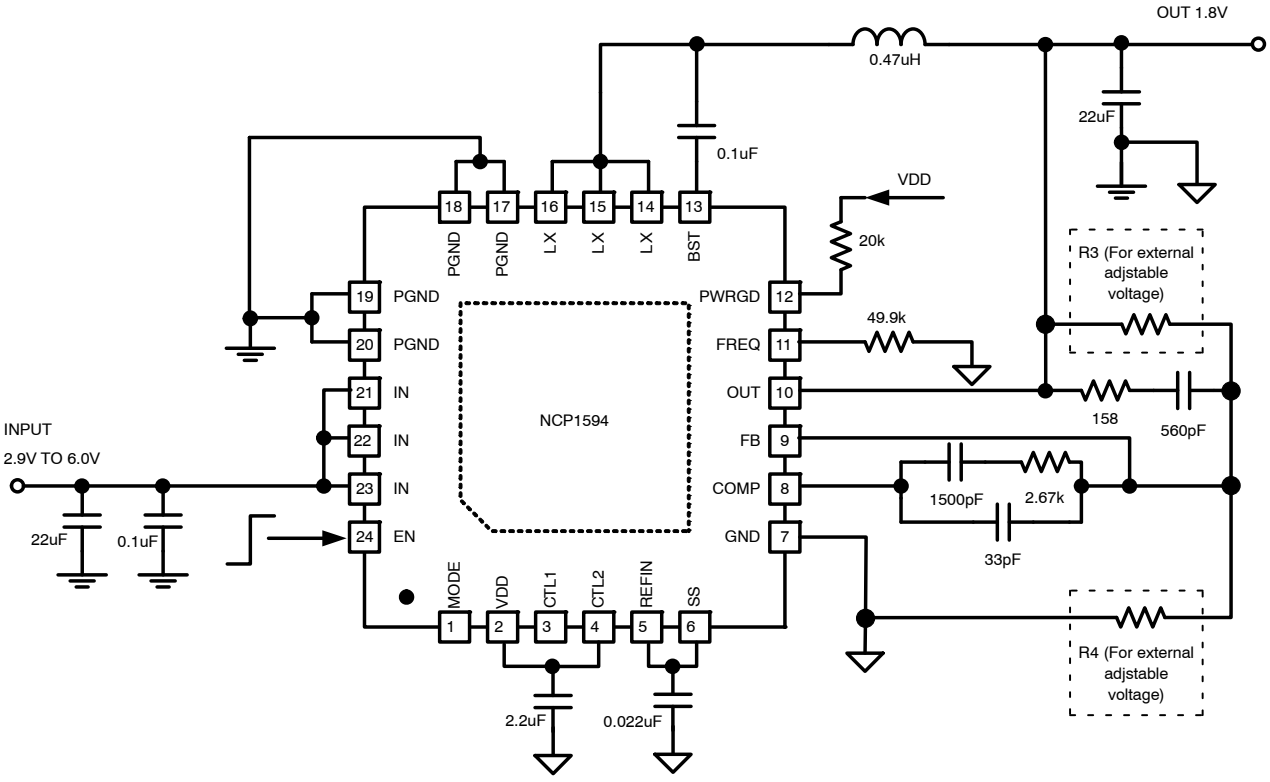


Figure 3. Typical Application Schematic.

DETAILED DESCRIPTION

The NCP1594 high−efficiency, voltage−mode switching regulator delivers up to 4 A of output current. The NCP1594 provides output voltages from 0.6 V to 0.9 x V_{IN} from 2.9 V to 6.0 V input supplies, making it ideal for on−board point−of−load applications. The output voltage accuracy is better than ±1% over load, line, and temperature.

The NCP1594 features a wide switching frequency range, allowing the user to achieve all−ceramic−capacitor designs and fast transient responses (see Figure 1). The high operating frequency minimizes the size of external components. The NCP1594 is available in a small (4 mm x 4 mm), Pb−Free, 24−pin thin QFN package. The REFIN function makes the NCP1594 an ideal candidate for DDR and tracking power supplies. Using internal low−$R_{DS(on)}$ (20 mΩ / 24 mΩ, NCP1594A/B for the low−side n−channel MOSFET and 26 mΩ / 31 mΩ NCP1594A/B for the high−side n−channel MOSFET) maintains high efficiency at both heavy−load and high−switching frequencies.

The NCP1594 employs voltage−mode control architecture with a high bandwidth (28 MHz) error amplifier. The voltage−mode control architecture allows up to 2 MHz switching frequency, reducing board area. The op−amp voltage−error amplifier works with type III compensation to fully utilize the bandwidth of the high−frequency switching to obtain fast transient response. Adjustable soft−start time provides flexibilities to minimize input startup inrush current. An open−drain, power−good (PWRGD) output goes high when V_{FB} reaches 92.5% of V_{REFIN} and V_{REFIN} is greater than 0.54 V.

The NCP1594 provides options for regular PWM, or PWM mode with monotonic startup into prebiased output.

Controller

The controller logic block determines the duty cycle of the high−side MOSFET under different line, load, and temperature conditions. Under normal operation, where the current−limit and temperature protection are not triggered, the controller logic block takes the output from the PWM comparator and generates the driver signals for both high−side and low−side MOSFETs. The break−before−make logic and the timing for charging the bootstrap capacitors are calculated by the controller logic block. The error signal from the voltage−error amplifier is compared with the ramp signal generated by the oscillator at the PWM comparator and, thus, the required PWM signal is produced. The high−side switch is turned on at the beginning of the oscillator cycle and turns off when the ramp voltage exceeds the VCOMP signal or the current−limit threshold is exceeded. The low−side switch is then turned on for the remainder of the oscillator cycle.

Current Limit

The internal, high−side MOSFET has a typical 7 A peak current−limit threshold for the NCP1594A and 11 A for the NCP1594B. When current flowing out of LX exceeds this limit, the high−side MOSFET turns off and the synchronous rectifier turns on. The synchronous rectifier remains on until the inductor current falls below the low−side current limit. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. The NCP1594 uses a hiccup mode to prevent overheating during short−circuit output conditions.

During current limit, if V_{FB} drops below 70% of V_{REFIN} and stays below this level for 12 μs or more, the NCP1594 enters hiccup mode. The high−side MOSFET and the synchronous rectifier are turned off and both COMP and REFIN are internally pulled low. If REFIN and SS are connected together, both are pulled low. The part remains in this state for 896 clock cycles and then attempts to restart for 112 clock cycles. If the fault causing current limit has cleared, the part resumes normal operation. Otherwise, the part reenters hiccup mode again.

Soft−Start and REFIN

The NCP1594 utilizes an adjustable soft−start function to limit inrush current during startup. An 8 μA (typ) current source charges an external capacitor connected to SS. The soft−start time is adjusted by the value of the external capacitor from SS to GND. The required capacitance value is determined as:

$$C = \frac{8\ \mu A \times t_{SS}}{0.6\ V} \qquad \text{(eq. 1)}$$

where t_{SS} is the required soft−start time in seconds. The NCP1594 also features an external reference input (REFIN). The IC regulates FB to the voltage applied to REFIN. The internal soft−start is not available when using an external reference. A method of soft−start when using an external reference is shown in Figure 2. Connect REFIN to SS to use the internal 0.6 V reference. Use a capacitor of 1 nF minimum value at SS.

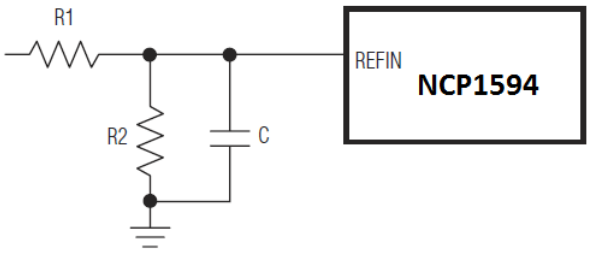


Figure 4. Soft−start with External Reference

Undervoltage Lockout (UVLO)

The UVLO circuitry inhibits switching when V_{DD} is below 2.55 V (typ). Once V_{DD} rises above 2.6 V (typ), UVLO clears and the soft−start function activates. A 50 mV hysteresis is built in for glitch immunity.

Bootstrap (BST)

The gate−drive voltage for the high−side, n−channel switch is generated by a flying−capacitor boost circuit. The capacitor between BST and LX is charged from the VIN supply while the low−side MOSFET is on. When the low−side MOSFET is switched off, the voltage of the capacitor is stacked above LX to provide the necessary turn−on voltage for the high−side internal MOSFET.

Frequency Select (FREQ)

The switching frequency is resistor programmable from 500 kHz to 2 MHz. Set the switching frequency of the IC with a resistor (R_{FREQ}) connected from FREQ to GND. R_{FREQ} is calculated as:

$$R_{FREQ} = \frac{50\ k\Omega}{0.95\ \mu s} \times \left(\frac{1}{f_S} - 0.05\ \mu s\right) \quad \text{(eq. 2)}$$

Where fS is the desired switching frequency in Hertz.

Power−Good Output (PWRGD)

PWRGD is an open−drain output that goes high impedance when V_{FB} is above 0.925 x V_{REFIN} and V_{REFIN} is above 0.54 V for at least 48 clock cycles. PWRGD pulls low when V_{FB} is below 90% of V_{REFIN} or V_{REFIN} is below 0.54 V for at least 48 clock cycles. PWRGD is low when the IC is in shutdown mode, V_{DD} is below the internal UVLO threshold, or the IC is in thermal shutdown mode.

Programming the Output Voltage (CTL1, CTL2)

As shown in Table 1, the output voltage is pin programmable by the logic states of C_{TL1} and C_{TL2}. C_{TL1} and C_{TL2} are trilevel inputs: V_{DD}, unconnected, and GND. An 8.06 kΩ resistor must be connected between V_{OUT} and FB when CTL1 and CTL2 are connected to GND. The logic states of CTL1 and CTL2 should be programmed only before power−up. Once the part is enabled, CTL1 and CTL2 should not be changed. If the output voltage needs to be reprogrammed, cycle power or EN and reprogram before enabling. The output voltage can be programmed continuously from 0.6 V to 90% of V_{IN} by using a resistor−divider network from V_{OUT} to FB to GND as shown in Figure 3a. CTL1 and CTL2 must be connected to GND.

Shutdown Mode

Drive EN to GND to shut down the IC and reduce quiescent current to 10 μA (typ). During shutdown, the LX is high impedance. Drive EN high to enable the NCP1594.

Thermal Protection

Thermal−overload protection limits total power dissipation in the device. When the junction temperature exceeds T_J = +165°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C, causing a pulsed output during continuous overload conditions. The soft−start sequence begins after recovery from a thermal−shutdown condition.

APPLICATIONS INFORMATION

IN and VDD Decoupling

To decrease the noise effects due to the high switching frequency and maximize the output accuracy of the NCP1594, decouple IN with a 22 μF capacitor from IN to PGND. Also, decouple VDD with a 2.2 μF low−ESR ceramic capacitor from VDD to GND. Place these capacitors as close as possible to the IC.

Inductor Selection

Choose an inductor with the following equation:

$$L = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right)}{f_S \times V_{IN} \times LIR \times I_{OUT(MAX)}} \quad \text{(eq. 3)}$$

where LIR is the ratio of the inductor ripple current to full load current at the minimum duty cycle. Choose LIR between 20% to 40% for best performance and stability. Use an inductor with the lowest possible DC resistance that fits in the allotted dimensions. Powdered iron ferrite core types are often the best choice for performance. With any core material, the core must be large enough not to saturate at the current limit of the NCP1594.

Output−Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage−rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC−DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output−voltage ripple due to the output capacitance, ESR, and ESL:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad \text{(eq. 4)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{I_{P-P}}{8 \times \times C_{OUT} \times f_S} \quad \text{(eq. 5)}$$

$$V_{RIPPLE(ESR)} = I_{P-} \times ESR \quad \text{(eq. 6)}$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-}}{t_{ON}} \times ESR \quad \text{(eq. 7)}$$

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{ON}} \times ESL \quad \text{(eq. 8)}$$

or

$$V_{RIPPLE(ESL)} = \frac{I_{P-P}}{t_{OFF}} \times ESL$$

or whichever is larger.

The peak−to−peak inductor current (I_{P-P}) is:

$$I_{P-P} = \frac{V_{IN} - V_{OUT}}{f_S \times L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 9)}$$

Use these equations for initial output−capacitor selection.

Determine final values by testing a prototype or an evaluation circuit. A smaller ripple current results in less output−voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output−voltage ripple decreases with larger inductance. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

Load−transient response depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to its predetermined value. The controller response time depends on the closed−loop bandwidth. A higher bandwidth yields a faster response time, preventing the output from deviating further from its regulating value. See the Compensation Design section for more details.

Input−Capacitor Selection

The input capacitor reduces the current peaks drawn from the input power supply and reduces switching noise in the IC. The total input capacitance must be equal or greater than the value given by the following equation to keep the input−ripple voltage within specification and minimize the high−frequency ripple current being fed back to the input source:

$$C_{IN\_MIN} = \frac{D \times T_S \times I_{OUT}}{V_{IN-RIPPLE}} \quad \text{(eq. 10)}$$

voltage across the input capacitors and is recommended to be less than 2% of the minimum input voltage. D is the duty cycle (V_{OUT}/V_{IN}) and T_S is the switching period ($1/f_S$).

The impedance of the input capacitor at the switching frequency should be less than that of the input source so high−frequency switching currents do not pass through the input source, but are instead shunted through the input capacitor. The input capacitor must meet the ripple current requirement imposed by the switching currents. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad \text{(eq. 11)}$$

Where I_{RIPPLE} is the RMS ripple current.

Compensation Design

The power transfer function consists of one double pole and one zero. The double pole is introduced by the inductor L and the output capacitor CO. The ESR of the output capacitor determines the zero. The double pole and zero frequencies are given as follows:

$$f_{P1\_LC} = f_{P2\_LC} = \frac{1}{2\pi \times \sqrt{L \times C_O \times \left(\frac{R_O + ESR}{R_O + R_L}\right)}} \quad \text{(eq. 12)}$$

$$f_{Z\_ESR} = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(eq. 13)}$$

where RL is equal to the sum of the output inductor's DCR (DC resistance) and the internal switch resistance, $R_{DS(on)}$. A typical value for $R_{DS(on)}$ is 20 mΩ (low−side MOSFET) and 26 mΩ (high−side MOSFET). RO is the output load resistance, which is equal to the rated output voltage divided by the rated output current. ESR is the total equivalent series resistance of the output capacitor. If there is more than one output capacitor of the same type in parallel, the value of the ESR in the above equation is equal to that of the ESR of a single output capacitor divided by the total number of output capacitors.

The high switching frequency range of the NCP1594 allows the use of ceramic output capacitors. Since the ESR of ceramic capacitors is typically very low, the frequency of the associated transfer function zero is higher than the unity−gain crossover frequency, f_C, and the zero cannot be used to compensate for the double pole created by the output filtering inductor and capacitor. The double pole produces a gain drop of 40 dB/decade and a phase shift of 180°. The compensation network error amplifier must compensate for this gain drop and phase shift to achieve a stable high−bandwidth closed−loop system. Therefore, use type III compensation as shown in Figures 3 and 4. Type III compensation possesses three poles and two zeros with the first pole, f_{P1_EA}, located at zero frequency (DC). Locations of other poles and zeros of the type III compensation are given by:

$$f_{Z1\_EA} = \frac{1}{2\pi \times R1 \times C1} \quad \text{(eq. 14)}$$

$$f_{Z2\_EA} = \frac{1}{2\pi \times R3 \times C3} \quad \text{(eq. 15)}$$

$$f_{P3\_EA} = \frac{1}{2\pi \times R1 \times C2} \quad \text{(eq. 16)}$$

$$f_{P2\_EA} = \frac{1}{2\pi \times R2 \times C3} \quad \text{(eq. 17)}$$

The above equations are based on the assumptions that C1 >> C2 and R3 >> R2 are true in most applications. Placements of these poles and zeros are determined by the frequencies of the double pole and ESR zero of the power transfer function. It is also a function of the desired close−loop bandwidth. The following section outlines the step−by−step design procedure to calculate the required compensation components for the NCP1594. When the output voltage of the NCP1594 is programmed to a preset voltage, R3 is internal to the IC and R4 does not exist (Figure 3b).

When externally programming the NCP1594 (Figure 3a), the output voltage is determined by:

$$R4 = \frac{0.6 \times R3}{(V_{OUT} - 0.6)} \left(\text{for } V_{OUT} > 0.6\ V\right) \quad \text{(eq. 18)}$$

or:

$$R4 = \frac{(V_{REFIN} \times R3)}{(V_{OUT} - V_{REFIN})} \quad \text{(eq. 19)}$$

if using and external V_{REFIN}, and $V_{OUT} > V_{REFIN}$.

For a 0.6 V output, or for $V_{OUT} = V_{REFIN}$, connect an 8.06 kΩ resistor from FB to V_{OUT}. The zero−cross frequency of the close−loop, fC, should be between 10% and 20% of the switching frequency, f_S. A higher zero cross frequency results in faster transient response. Once fC is chosen, C1 is calculated from the following equation:

$$C1 = \frac{1.5625 \times \frac{V_{IN}}{V_{P-P}}}{2 \times \pi \times R3 \times \left(1 + \frac{R_L}{R_O}\right) \times f_C} \quad \text{(eq. 20)}$$

where $V_{P−P}$ is the ramp peak−to−peak voltage (1 V typ). Due to the underdamped nature of the output LC double pole, set the two zero frequencies of the type III compensation less than the LC double−pole frequency to provide adequate phase boost. Set the two zero frequencies to 80% of the LC double−pole frequency.

Hence:

$$R1 = \frac{1}{0.8 \times C1} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}} \quad \text{(eq. 21)}$$

$$C3 = \frac{1}{0.8 \times R3} \times \sqrt{\frac{L \times C_O \times (R_O + ESR)}{R_L + R_O}} \quad \text{(eq. 22)}$$

$$R2 = \frac{C_O \times ESR}{C3} \quad \text{(eq. 23)}$$

Set the third compensation pole at half of the switching frequency. Calculate C2 as follows:

$$C2 = \frac{1}{\pi \times R1 \times f_S} \quad \text{(eq. 24)}$$

The above equations (Equation 12 − 24) provide application compensation when the zero−cross frequency is significantly higher than the double−pole frequency. When the zero−cross frequency is near the double−pole frequency, the actual zero cross frequency is higher than the calculated frequency. In this case, lowering the value of R1 reduces the zero cross frequency. Also, set the third pole of the type III compensation close to the switching frequency if the zero−cross frequency is above 200 kHz to boost the phase margin. The recommended range for R3 is 2 kΩ to 10 kΩ. Note that the loop compensation remains unchanged if only R4's resistance is altered to set different outputs.

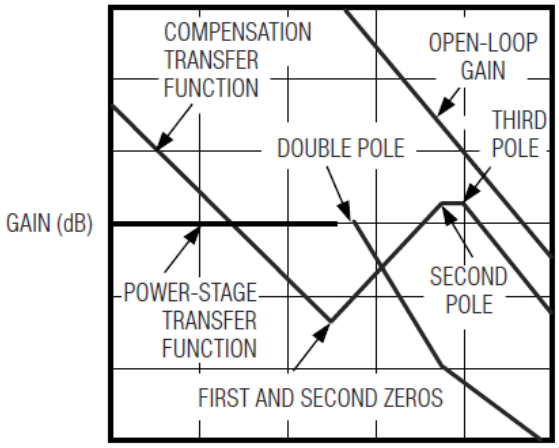


Figure 5. Type 3 Compensation

MODE SELECTION

The NCP1594 features a mode selection input (MODE) that enables users to select a functional mode for the device (See Table 2).

Forced−PWM Mode

Connect MODE to GND to select forced−PWM mode. In forced−PWM mode, the NCP1594 operates at a constant switching frequency (set by the resistor at FREQ terminal) with no pulse skipping. PWM operation starts after a brief settling time when EN goes high. The low side switch turns on first, charging the bootstrap capacitor to provide the gate−drive voltage for the high side switch. The low−side switch turns off either at the end of the clock period or once the low−side switch sinks 0.875 A/1.35 A (NCP1594A/NCP1594B respectively) current (typ), whichever occurs first. If the low−side switch is turned off before the end of the clock period, the high−side switch is turned on for the remaining part of the time interval until the inductor current reaches 0.58A/0.9A

(NCP1594A/NCP1594B respectively), or the end of clock cycle is encountered.

Starting from the first PWM activity, the sink current threshold is increased through an internal 4−step DAC to reach the current limit of 7 A/11 A (NCP1594A/NCP1594B respectively), after 128 clock periods. This is done to help a smooth recovery of the regulated voltage even in the case of an accidental prebiased output with the forced−PWM mode selection.

Soft−Starting Into a Prebiased Output Mode (Monotonic Startup)

When MODE is left unconnected or biased to $V_{DD}/2$, the NCP1594 soft−starts into a prebiased output without discharging the output capacitor. This type of operation is also termed monotonic startup. See the Starting Into Prebiased Output waveforms in the Typical Operating Characteristics section for an example.

In monotonic startup mode, both low−side and high side switches remain off to avoid discharging the prebiased output. PWM operation starts when the FB voltage crosses the SS voltage. As in forced−PWM mode, the PWM activity starts with the low−side switch turning on first to build the bootstrap capacitor charge.

The NCP1594 is also able to start into prebiased with the output above the nominal set point without abruptly discharging the output, thanks to the sink current control of the low−side switch through a 4−step DAC in 128 clock cycles. Monotonic startup mode automatically switches to forced−PWM mode 4096 clock cycles delay after the voltage at FB increases above 92.5% of VREFIN. The additional delay prevents an early transition from monotonic startup to forced−PWM mode during soft−start when a prolonged time constant external REFIN voltage is applied.

The maximum allowed soft−start time is 2ms when an external reference is applied at REFIN in the case of starting up into prebiased output.

Table 2. MODE SELECTION

Mode Connection	Operation Mode
GND	Forced PWM
Unconnected or VDD/2	Forced PWM. Soft−start into a prebiased output (monotonic startup)

PCB Layout Considerations and Thermal Performance

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the NCP1594 EV kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

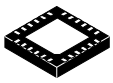
1. Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
2. Place capacitors on VDD, IN, and SS as close as possible to the IC and its corresponding pin using direct traces. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
3. Keep the high−current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4. Connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long−term reliability.
5. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.
6. Route high−speed switching nodes, such as LX, away from sensitive analog areas (FB, COMP).

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

WQFN24, 4x4, 0.5P
CASE 510BP
ISSUE O

DATE 03 FEB 2016



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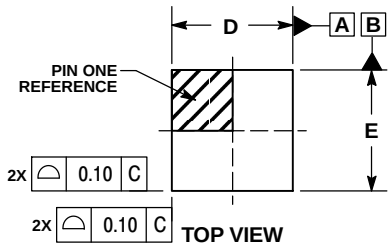
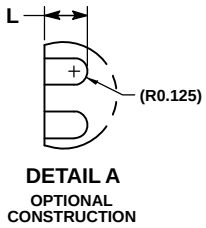
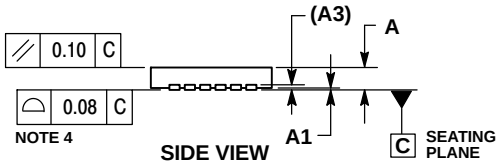
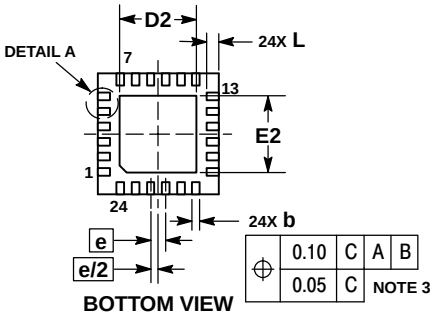




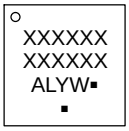
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.90	4.10
D2	2.44	2.64
E	3.90	4.10
E2	2.44	2.64
e	0.50 BSC	
L	0.30	0.50





GENERIC MARKING DIAGRAM*

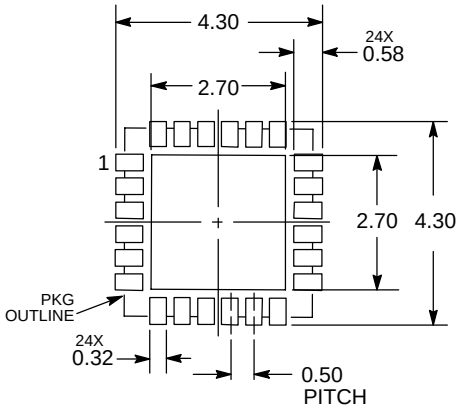


XXXXXX= Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ISSUE	REVISION	DATE
O	THIS IS A CUSTOM VERSION OF CASE 510BC TO MEET CUSTOMER'S SPECIAL REQUIREMENT OF LEAD CONSTRUCTION OPTION. REQ. BY J. LIU.	03 FEB 2016

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