Datasheet

RL78/G23

RENESAS MCU

R01DS0395EJ0110
Rev.1.10
Nov 18, 2021

<R> True low-power platform, 41-µA/MHz operating current, 210-nA holding current for 4 KB of RAM, up to 768-KB code flash memory and 48-KB RAM, Capacitive sensing unit, from 30 to 128 pins, 1.6-5.5 V

1. Outline

1.1 Features

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
  High-speed wakeup from the STOP mode is possible.
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 µs @ 32 MHz operation with the high-speed on-chip oscillator clock) to ultra-low speed (30.5 µs @ 32.768 kHz operation with the subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 12 to 48 KB

Code flash memory

- Code flash memory: 96 to 768 KB
- Block size: 2 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debugging
- Self-programming
  (with boot swapping and flash shield window)

Data flash memory

- Data flash memory: 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, or 1 MHz
- High accuracy: ±1.0% (V_{DD} = 1.8 to 5.5 V,
  T_A = -20 to +85°C)

<R> Middle-speed on-chip oscillator

- Select from 4 MHz, 2 MHz, or 1 MHz
  (with adjustability)

Low-speed on-chip oscillator

- 32.768 kHz (typ.) (with adjustability)

Operating ambient temperature

- T_A = -40 to +85°C (2D: Consumer applications)
- T_A = -40 to +105°C (3C: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detectors (LVD0 and LVD1)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

SNOOZE mode sequencer (SMS)

- Calculations and comparison of values by the commands for use in processing by the sequencer can realize intermittent operations where the RL78/G23 does not have to return to normal operation.
- Sequentially handling a total of 32 processes with the use of desired commands from among 21 different ones
- The SNOOZE mode sequencer offers operation with low power consumption without using the CPU, flash memory, and RAM.

Logic and event link controller (ELCL)

- Event signals can be set up between specified peripheral functions.
- The signals can be generated by the input of multiple event signals to the logic circuit.
- Flip-flop circuits are incorporated to handle setting and resetting functions.

Serial interface

- Simplified SPI (CSI[Note 1]): 3 to 8 channels
- UART/UART (LIN-bus supported)/UARTA: 3 to 6 channels
- I^{2}C/Simplified I^{2}C: 4 to 10 channels

Remote control signal receiver

- 1 channel
- Matching of 4 waveform patterns (header, data 0, data 1, and special data)

Timers

- 16-bit timer: 8 to 16 channels
- <R> 32-bit interval timer: 1 channel in 32-bit counter mode
  2 channels in 16-bit counter mode
  4 channels in 8-bit counter mode
- Realtime clock: 1 channel (counting of one second to 99 years, alarm interrupt, and clock correction)
- Watchdog timer: 1 channel (operates with the dedicated low-speed on-chip oscillator clock)

A/D converter

- 8-/10-/12-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 8 to 26 channels
- Internal reference voltage (1.48 V) and temperature sensor

D/A converter

- 8-bit resolution D/A converter (V_{DD} = 1.6 to 5.5 V)
- Analog output: 2 channels
- Output voltage: 0 V to V_{DD}
- Realtime output function

Comparator

- 2 channels
- Operating modes: Comparator high-speed mode and comparator low-speed mode
- The external reference voltage and the internal reference voltage or D/A converter output are selectable as the reference voltage.

Capacitive sensing unit

- CTSU2L operating voltage condition: V_{DD} = 1.8 to 5.5 V
- Self-capacitance method: A single pin configures a single key, supporting up to 32 keys
- Mutual capacitance method: Matrix configuration with 8 × 8 pins, supporting up to 64 keys

Input/output port pins

- Number of port pins:
  26 to 120 (N-ch open drain I/O [withstand voltage of 6 V]: 2 to 4, N-ch open drain I/O [V_{DD} withstand voltage[Note 2]/EV_{DD} withstand voltage[Note 3]]: 10 to 33, output current control pins: 6 to 8)
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

Others

- BCD (binary-coded decimal) correction circuit
- Key interrupt input
- Clock output/buzzer output controller

Note 1. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Note 2. This applies to the 30- to 52-pin products.

Note 3. This applies to the 64- to 128-pin products.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

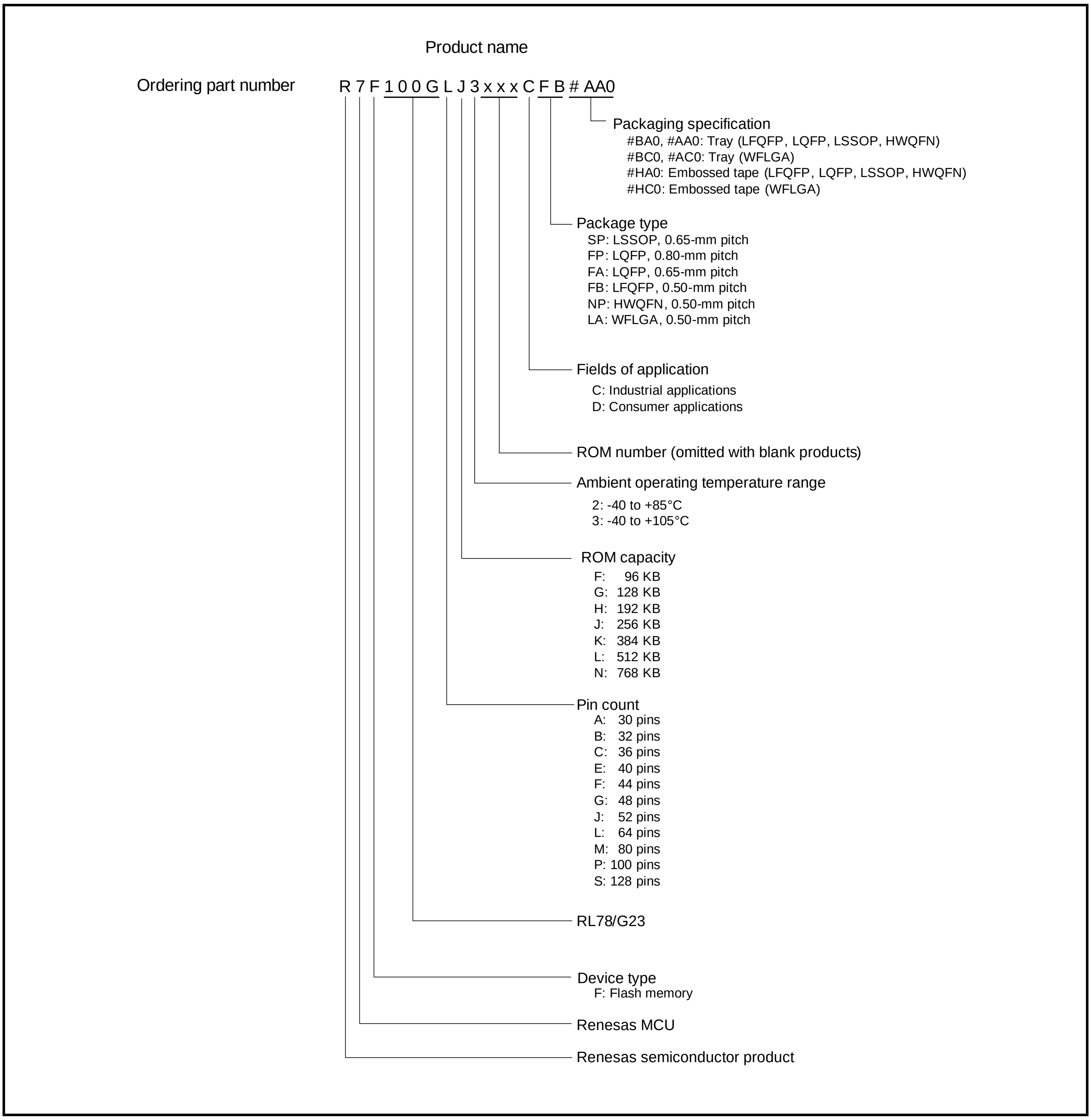
O ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G23					
			30 pins	32 pins	36 pins	40 pins	44 pins	48 pins
768 KB	8 KB	48 KB	—	—	—	—	R7F100GFN	R7F100GGN
512 KB	8 KB	48 KB	—	—	—	—	R7F100GFL	R7F100GGL
384 KB	8 KB	32 KB	—	—	—	—	R7F100GFK	R7F100GGK
256 KB	8 KB	24 KB	R7F100GAJ	R7F100GBJ	R7F100GCJ	R7F100GEJ	R7F100GFJ	R7F100GGJ
192 KB	8 KB	20 KB	R7F100GAH	R7F100GBH	R7F100GCH	R7F100GEH	R7F100GFH	R7F100GGH
128 KB	8 KB	16 KB	R7F100GAG	R7F100GBG	R7F100GCG	R7F100GEG	R7F100GFG	R7F100GGG
96 KB	8 KB	12 KB	R7F100GAF	R7F100GBF	R7F100GCF	R7F100GEF	R7F100GFF	R7F100GGF

Flash ROM	Data flash	RAM	RL78/G23				
			52 pins	64 pins	80 pins	100 pins	128 pins
768 KB	8 KB	48 KB	R7F100GJN	R7F100GLN	R7F100GMN	R7F100GPN	R7F100GSN
512 KB	8 KB	48 KB	R7F100GJL	R7F100GLL	R7F100GML	R7F100GPL	R7F100GSL
384 KB	8 KB	32 KB	R7F100GJK	R7F100GLK	R7F100GMK	R7F100GPK	R7F100GSK
256 KB	8 KB	24 KB	R7F100GJJ	R7F100GLJ	R7F100GMJ	R7F100GPJ	R7F100GSJ
192 KB	8 KB	20 KB	R7F100GJH	R7F100GLH	R7F100GMH	R7F100GPH	—
128 KB	8 KB	16 KB	R7F100GJG	R7F100GLG	R7F100GMG	R7F100GPG	—
96 KB	8 KB	12 KB	R7F100GJF	R7F100GLF	—	—	—

1.2 List of Part Numbers

<R> Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23



Product name

Ordering part number R 7 F 1 0 0 G L J 3 x x x C F B # AA0

Packaging specification
#BA0, #AA0: Tray (LFQFP, LQFP, LSSOP, HWQFN)
#BC0, #AC0: Tray (WFLGA)
#HA0: Embossed tape (LFQFP, LQFP, LSSOP, HWQFN)
#HC0: Embossed tape (WFLGA)

Package type
SP: LSSOP, 0.65-mm pitch
FP: LQFP, 0.80-mm pitch
FA: LQFP, 0.65-mm pitch
FB: LFQFP, 0.50-mm pitch
NP: HWQFN, 0.50-mm pitch
LA: WFLGA, 0.50-mm pitch

Fields of application
C: Industrial applications
D: Consumer applications

ROM number (omitted with blank products)

Ambient operating temperature range
2: -40 to +85°C
3: -40 to +105°C

ROM capacity
F: 96 KB
G: 128 KB
H: 192 KB
J: 256 KB
K: 384 KB
L: 512 KB
N: 768 KB

Pin count
A: 30 pins
B: 32 pins
C: 36 pins
E: 40 pins
F: 44 pins
G: 48 pins
J: 52 pins
L: 64 pins
M: 80 pins
P: 100 pins
S: 128 pins

RL78/G23

Device type
F: Flash memory

Renesas MCU

Renesas semiconductor product

Table 1 - 1 List of Ordering Part Numbers (1/3)

Pin count	Package	Fields of Application **Note 1**	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)	C	R7F100GAF3CSP, R7F100GAG3CSP, R7F100GAH3CSP, R7F100GAJ3CSP	#AA0, #BA0 #HA0	PLSP0030JB-B
		D	R7F100GAF2DSP, R7F100GAG2DSP, R7F100GAH2DSP, R7F100GAJ2DSP		
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch)	C	R7F100GBF3CNP, R7F100GBG3CNP, R7F100GBH3CNP, R7F100GBJ3CNP	#AA0, #BA0 #HA0	PWQN0032KE-A
		D	R7F100GBF2DNP, R7F100GBG2DNP, R7F100GBH2DNP, R7F100GBJ2DNP		
32 pins	32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)	C	R7F100GBF3CFP, R7F100GBG3CFP, R7F100GBH3CFP, R7F100GBJ3CFP	#AA0, #BA0 #HA0	PLQP0032GB-A
		D	R7F100GBF2DFP, R7F100GBG2DFP, R7F100GBH2DFP, R7F100GBJ2DFP		
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)	C	R7F100GCF3CLA, R7F100GCG3CLA, R7F100GCH3CLA, R7F100GCJ3CLA	#BC0, #AC0 #HC0	**Note 2**
		D	R7F100GCF2DLA, R7F100GCG2DLA, R7F100GCH2DLA, R7F100GCJ2DLA		
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)	C	R7F100GEF3CNP, R7F100GEG3CNP, R7F100GEH3CNP, R7F100GEJ3CNP	#AA0, #BA0 #HA0	PWQN0040KD-A
		D	R7F100GEF2DNP, R7F100GEG2DNP, R7F100GEH2DNP, R7F100GEJ2DNP		
44 pins	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	C	R7F100GFF3CFP, R7F100GFG3CFP, R7F100GFH3CFP, R7F100GFJ3CFP, R7F100GFK3CFP, R7F100GFL3CFP, R7F100GFN3CFP	#AA0, #BA0 #HA0	PLQP0044GC-A
		D	R7F100GFF2DFP, R7F100GFG2DFP, R7F100GFH2DFP, R7F100GFJ2DFP, R7F100GFK2DFP, R7F100GFL2DFP, R7F100GFN2DFP		
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	C	R7F100GGF3CFB, R7F100GGG3CFB, R7F100GGH3CFB, R7F100GGJ3CFB, R7F100GGK3CFB, R7F100GGL3CFB, R7F100GGN3CFB	#AA0, #BA0 #HA0	PLQP00048KB-B
		D	R7F100GGF2DFB, R7F100GGG2DFB, R7F100GGH2DFB, R7F100GGJ2DFB, R7F100GGK2DFB, R7F100GGL2DFB, R7F100GGN2DFB		
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)	C	R7F100GGF3CNP, R7F100GGG3CNP, R7F100GGH3CNP, R7F100GGJ3CNP, R7F100GGK3CNP, R7F100GGL3CNP, R7F100GGN3CNP	#AA0, #BA0 #HA0	PWQN0048KC-A
		D	R7F100GGF2DNP, R7F100GGG2DNP, R7F100GGH2DNP, R7F100GGJ2DNP, R7F100GGK2DNP, R7F100GGL2DNP, R7F100GGN2DNP		

Table 1 - 1 List of Ordering Part Numbers (2/3)

Pin count	Package	Fields of Application **Note 1**	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)	C	R7F100GJF3CFA, R7F100GJG3CFA, R7F100GJH3CFA, R7F100GJJ3CFA, R7F100GJK3CFA, R7F100GJL3CFA, R7F100GJN3CFA	#AA0, #BA0 #HA0	PLQP0052JA-A
		D	R7F100GJF2DFA, R7F100GJG2DFA, R7F100GJH2DFA, R7F100GJJ2DFA, R7F100GJK2DFA, R7F100GJL2DFA, R7F100GJN2DFA		
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)	C	R7F100GLF3CFA, R7F100GLG3CFA, R7F100GLH3CFA, R7F100GLJ3CFA, R7F100GLK3CFA, R7F100GLL3CFA, R7F100GLN3CFA	#AA0, #BA0 #HA0	PLQP0064JA-A
		D	R7F100GLF2DFA, R7F100GLG2DFA, R7F100GLH2DFA, R7F100GLJ2DFA, R7F100GLK2DFA, R7F100GLL2DFA, R7F100GLN2DFA		
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)	C	R7F100GLF3CFB, R7F100GLG3CFB, R7F100GLH3CFB, R7F100GLJ3CFB, R7F100GLK3CFB, R7F100GLL3CFB, R7F100GLN3CFB	#AA0, #BA0 #HA0	PLQP0064KB-C
		D	R7F100GLF2DFB, R7F100GLG2DFB, R7F100GLH2DFB, R7F100GLJ2DFB, R7F100GLK2DFB, R7F100GLL2DFB, R7F100GLN2DFB		
64 pins	64-pin plastic WFLGA (5 × 5 mm, 0.50-mm pitch)	C	R7F100GLF3CLA, R7F100GLG3CLA, R7F100GLH3CLA, R7F100GLJ3CLA, R7F100GLK3CLA, R7F100GLL3CLA, R7F100GLN3CLA	#BC0, #AC0 #HC0	**Note 3**
		D	R7F100GLF2DLA, R7F100GLG2DLA, R7F100GLH2DLA, R7F100GLJ2DLA, R7F100GLK2DLA, R7F100GLL2DLA, R7F100GLN2DLA		
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)	C	R7F100GMG3CFA, R7F100GMH3CFA, R7F100GMJ3CFA, R7F100GMK3CFA, R7F100GML3CFA, R7F100GMN3CFA	#AA0, #BA0 #HA0	PLQP0080JA-B
		D	R7F100GMG2DFA, R7F100GMH2DFA, R7F100GMJ2DFA, R7F100GMK2DFA, R7F100GML2DFA, R7F100GMN2DFA		
80 pins	80-pin plastic LFQFP (12 × 12 mm, 0.50-mm pitch)	C	R7F100GMG3CFB, R7F100GMH3CFB, R7F100GMJ3CFB, R7F100GMK3CFB, R7F100GML3CFB, R7F100GMN3CFB	#AA0, #BA0 #HA0	PLQP0080KB-B
		D	R7F100GMG2DFB, R7F100GMH2DFB, R7F100GMJ2DFB, R7F100GMK2DFB, R7F100GML2DFB, R7F100GMN2DFB		
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.50-mm pitch)	C	R7F100GPG3CFB, R7F100GPH3CFB, R7F100GPJ3CFB, R7F100GPK3CFB, R7F100GPL3CFB, R7F100GPN3CFB	#AA0, #BA0 #HA0	PLQP0100KB-B
		D	R7F100GPG2DFB, R7F100GPH2DFB, R7F100GPJ2DFB, R7F100GPK2DFB, R7F100GPL2DFB, R7F100GPN2DFB		

Table 1 - 1 List of Ordering Part Numbers (3/3)

Pin count	Package	Fields of Application Note 1	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
100 pins	100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)	C	R7F100GPG3CFA, R7F100GPH3CFA, R7F100GPJ3CFA, R7F100GPK3CFA, R7F100GPL3CFA, R7F100GPN3CFA	#AA0, #BA0 #HA0	PLQP0100JC-A
		D	R7F100GPG2DFA, R7F100GPH2DFA, R7F100GPJ2DFA, R7F100GPK2DFA, R7F100GPL2DFA, R7F100GPN2DFA		
128 pins	128-pin plastic LFQFP (14 × 20 mm, 0.50-mm pitch)	C	R7F100GSJ3CFB, R7F100GSK3CFB, R7F100GSL3CFB, R7F100GSN3CFB	#AA0, #BA0 #HA0	PLQP0128KD-A
		D	R7F100GSJ2DFB, R7F100GSK2DFB, R7F100GSL2DFB, R7F100GSN2DFB		

Note 1. For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23**.

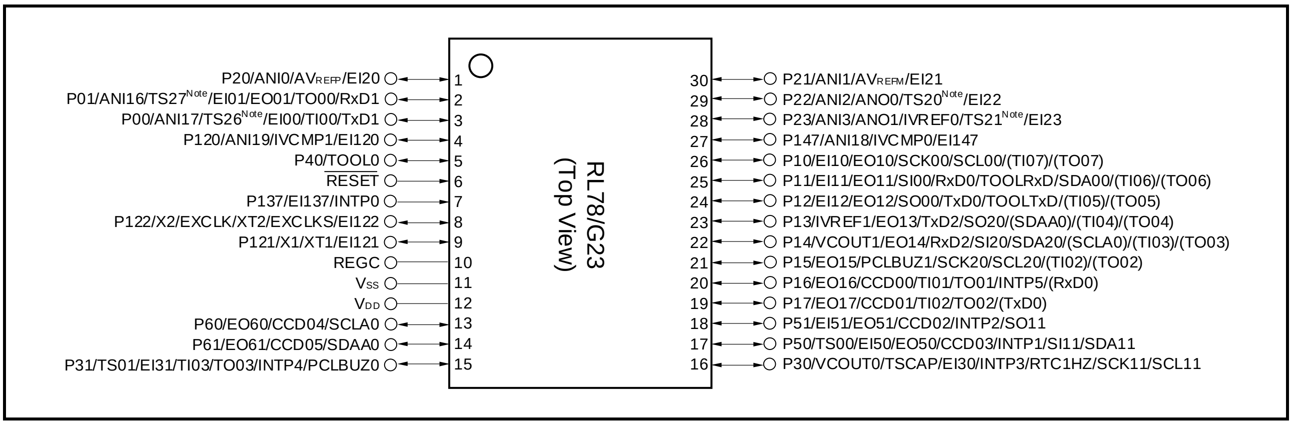
Note 2. The 36-pin plastic WFLGA products are in planning. Contact a Renesas Electronics sales office for details.

Note 3. The 64-pin plastic WFLGA products are in planning. Contact a Renesas Electronics sales office for details.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)


P20/ANI0/AV$_{REFP}$/EI20 1
P01/ANI16/TS27[Note]/EI01/EO01/TO00/RxD1 2
P00/ANI17/TS26[Note]/EI00/TI00/TxD1 3
P120/ANI19/IVCMP1/EI120 4
P40/TOOL0 5
$\overline{\text{RESET}}$ 6
P137/EI137/INTP0 7
P122/X2/EXCLK/XT2/EXCLKS/EI122 8
P121/X1/XT1/EI121 9
REGC 10
V$_{SS}$ 11
V$_{DD}$ 12
P60/EO60/CCD04/SCLA0 13
P61/EO61/CCD05/SDAA0 14
P31/TS01/EI31/TI03/TO03/INTP4/PCLBUZ0 15
RL78/G23
(Top View)
30 P21/ANI1/AV$_{REFM}$/EI21
29 P22/ANI2/ANO0/TS20[Note]/EI22
28 P23/ANI3/ANO1/IVREF0/TS21[Note]/EI23
27 P147/ANI18/IVCMP0/EI147
26 P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
25 P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
24 P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
23 P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
22 P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
21 P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
20 P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
19 P17/EO17/CCD01/TI02/TO02/(TxD0)
18 P51/EI51/EO51/CCD02/INTP2/SO11
17 P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
16 P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11

Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

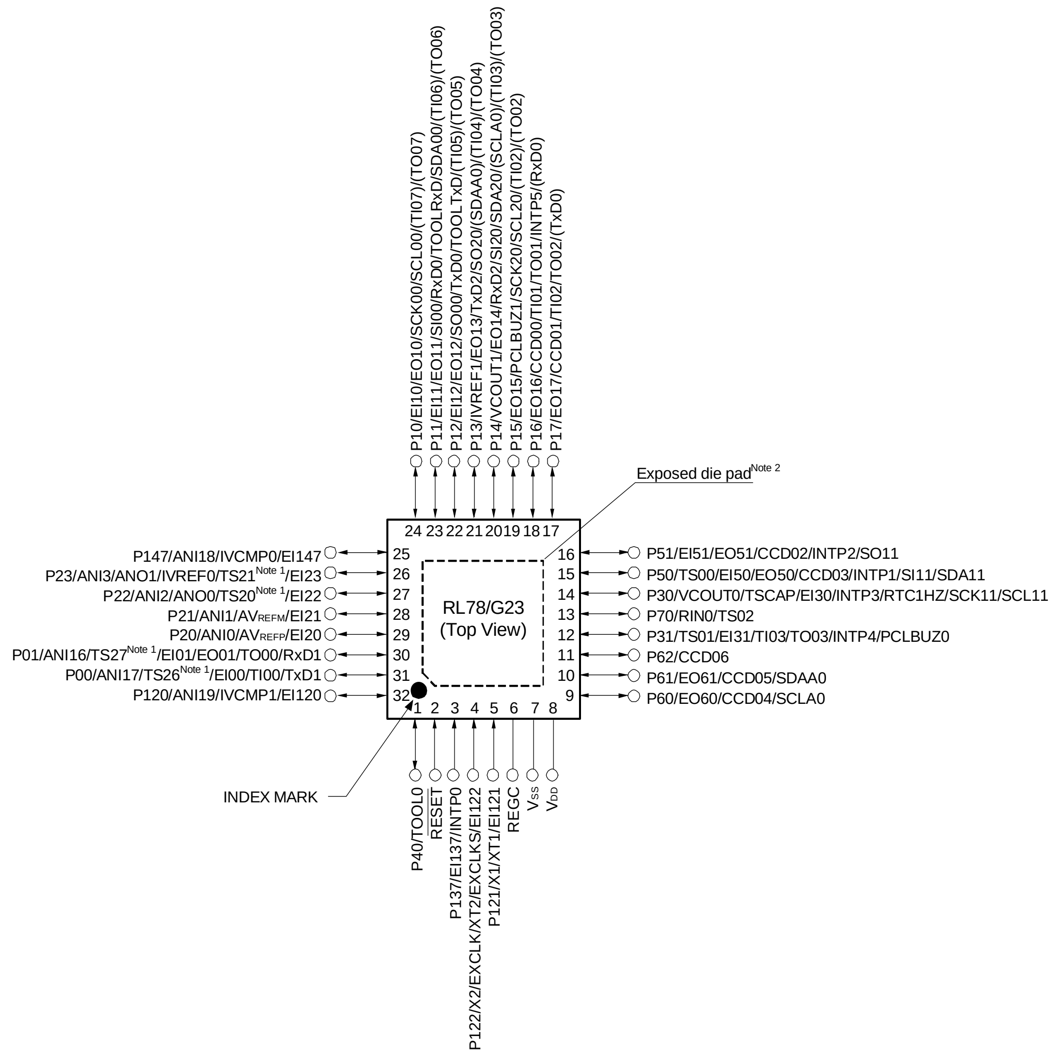
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)
- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)


P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
P17/EO17/CCD01/TI02/TO02/(TxD0)
24 23 22 21 20 19 18 17
Exposed die pad Note 2
P147/ANI18/IVCMP0/EI147
P23/ANI3/ANO1/IVREF0/TS21 Note 1/EI23
P22/ANI2/ANO0/TS20 Note 1/EI22
P21/ANI1/AVREFM/EI21
P20/ANI0/AVREFP/EI20
P01/ANI16/TS27 Note 1/EI01/EO01/TO00/RxD1
P00/ANI17/TS26 Note 1/EI00/TI00/TxD1
P120/ANI19/IVCMP1/EI120
25 26 27 28 29 30 31 32
RL78/G23
(Top View)
16 15 14 13 12 11 10 9
P51/EI51/EO51/CCD02/INTP2/SO11
P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11
P70/RIN0/TS02
P31/TS01/EI31/TI03/TO03/INTP4/PCLBUZ0
P62/CCD06
P61/EO61/CCD05/SDAA0
P60/EO60/CCD04/SCLA0
1 2 3 4 5 6 7 8
INDEX MARK
P40/TOOL0
RESET
P137/EI137/INTP0
P122/X2/EXCLK/XT2/EXCLKS/EI122
P121/X1/XT1/EI121
REGC
VSS
VDD

Note 1. Not present in products with 128 or fewer Kbytes of code flash memory.

Note 2. The 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch) products do not have an exposed die pad.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

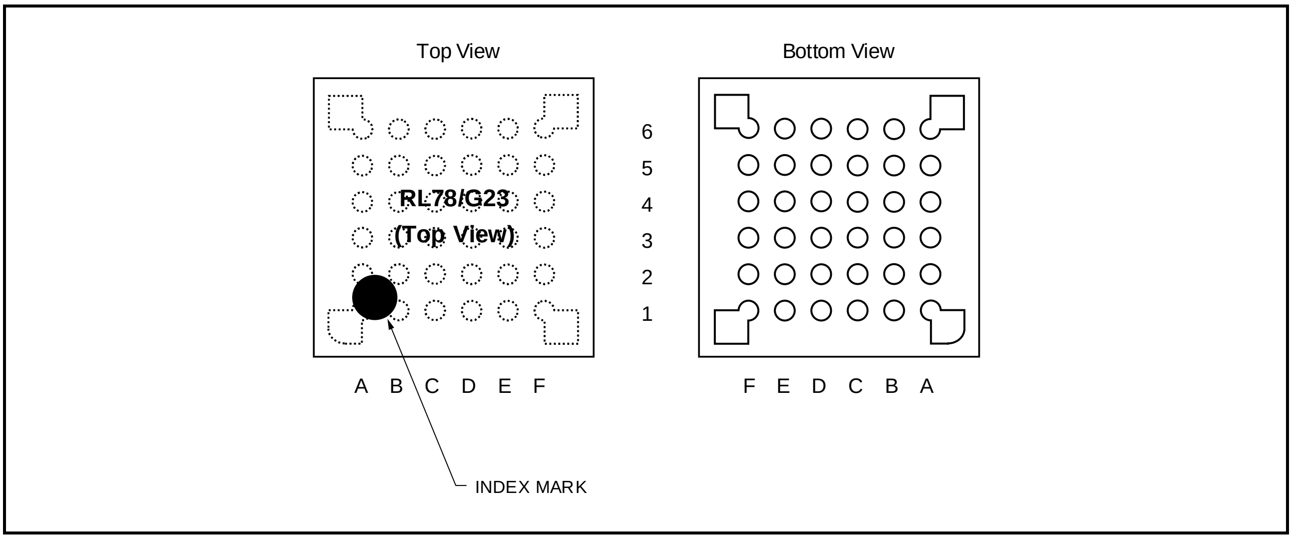
Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)



	A	B	C	D	E	F
6	P60/EO60/CCD04/SCLA0	VDD	P121/X1/XT1/EI121	P122/X2/EXCLK/XT2/EXCLKS/EI122	P137/EI137/INTP0	P40/TOOL0
5	P62/CCD06	P61/EO61/CCD05/SDAA0	VSS	REGC	$\overline{\text{RESET}}$	P120/ANI19/IVCMP1/EI120
4	P72/TS04/SO21/TxDA0	P71/TS03/SI21/SDA21/RxDA0	P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)	P31/TS01/EI31/TI03/TO03/INTP4/PCLBUZ0	P00/TS26[Note]/EI00/TI00/TxD1	P01/TS27[Note]/EI01/EO01/TO00/RxD1
3	P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11	P70/TS02/RIN0/SCK21/SCL21	P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)	P22/ANI2/ANO0/TS20[Note]/EI22	P20/ANI0/AVREFP/EI20	P21/ANI1/AVREFM/EI21
2	P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11	P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)	P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)	P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)	P24/ANI4/TS22[Note]	P23/ANI3/ANO1/IVREF0/TS21[Note]/EI23
1	P51/EI51/EO51/CCD02/INTP2/SO11	P17/EO17/CCD01/TI02/TO02/(TxD0)	P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)	P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)	P147/ANI18/IVCMP0/EI147	P25/ANI5/TS23[Note]

Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

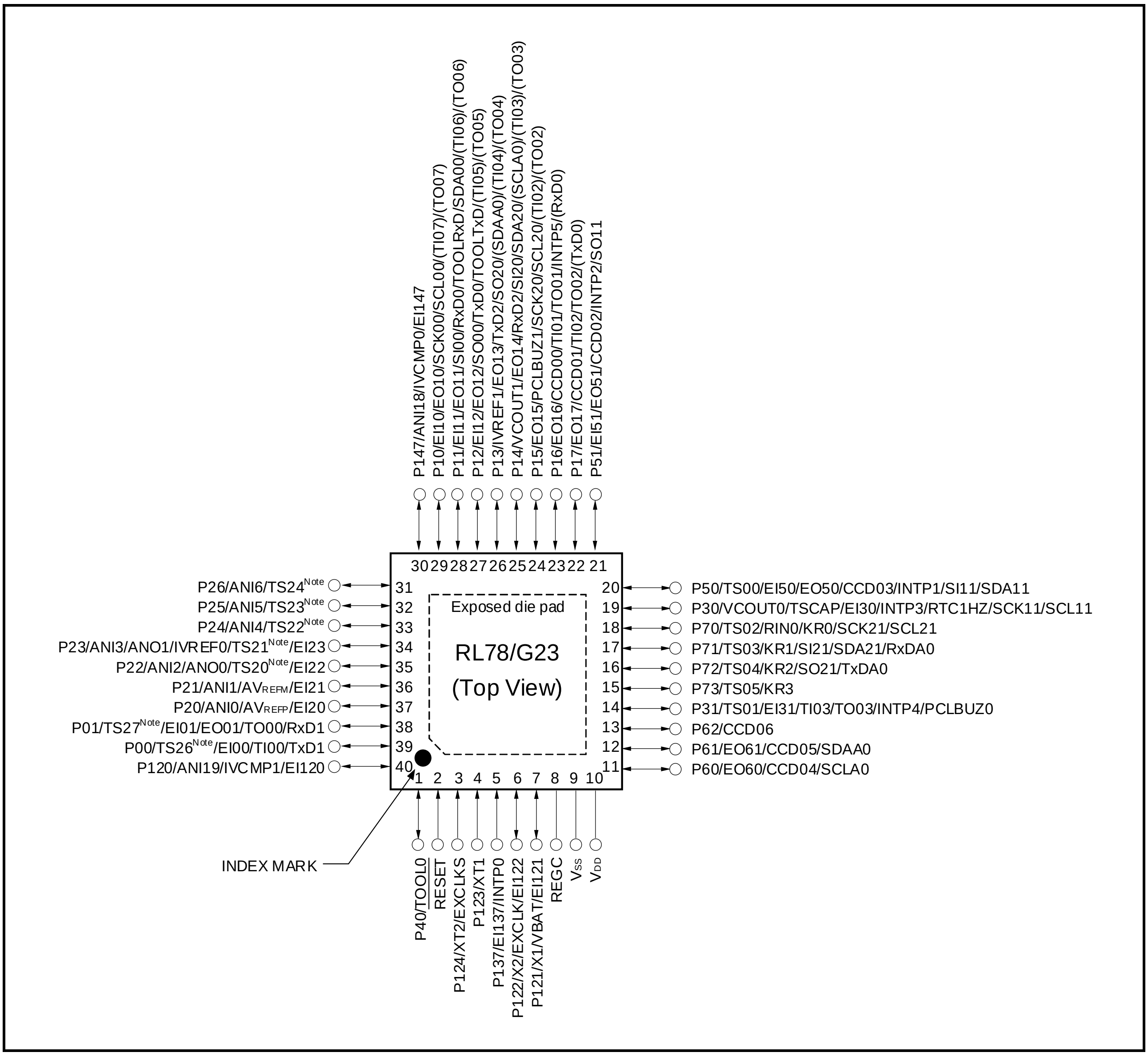
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.4 40-pin products

<R>

- 40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)


P147/ANI18/IVCMP0/EI147
P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
P17/EO17/CCD01/TI02/TO02/(TxD0)
P51/EI51/EO51/CCD02/INTP2/SO11
30 29 28 27 26 25 24 23 22 21
P26/ANI6/TS24$^{\text{Note}}$ 31
P25/ANI5/TS23$^{\text{Note}}$ 32
P24/ANI4/TS22$^{\text{Note}}$ 33
P23/ANI3/ANO1/IVREF0/TS21$^{\text{Note}}$/EI23 34
P22/ANI2/ANO0/TS20$^{\text{Note}}$/EI22 35
P21/ANI1/AV$_{\text{REFM}}$/EI21 36
P20/ANI0/AV$_{\text{REFP}}$/EI20 37
P01/TS27$^{\text{Note}}$/EI01/EO01/TO00/RxD1 38
P00/TS26$^{\text{Note}}$/EI00/TI00/TxD1 39
P120/ANI19/IVCMP1/EI120 40
Exposed die pad
RL78/G23
(Top View)
20 P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
19 P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11
18 P70/TS02/RIN0/KR0/SCK21/SCL21
17 P71/TS03/KR1/SI21/SDA21/RxDA0
16 P72/TS04/KR2/SO21/TxDA0
15 P73/TS05/KR3
14 P31/TS01/EI31/TI03/TO03/INTP4/PCLBUZ0
13 P62/CCD06
12 P61/EO61/CCD05/SDAA0
11 P60/EO60/CCD04/SCLA0
1 2 3 4 5 6 7 8 9 10
INDEX MARK
P40/$\overline{\text{TOOL0}}$
$\overline{\text{RESET}}$
P124/XT2/EXCLKS
P123/XT1
P137/EI137/INTP0
P122/X2/EXCLK/EI122
P121/X1/VBAT/EI121
REGC
V$_{\text{SS}}$
V$_{\text{DD}}$

Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

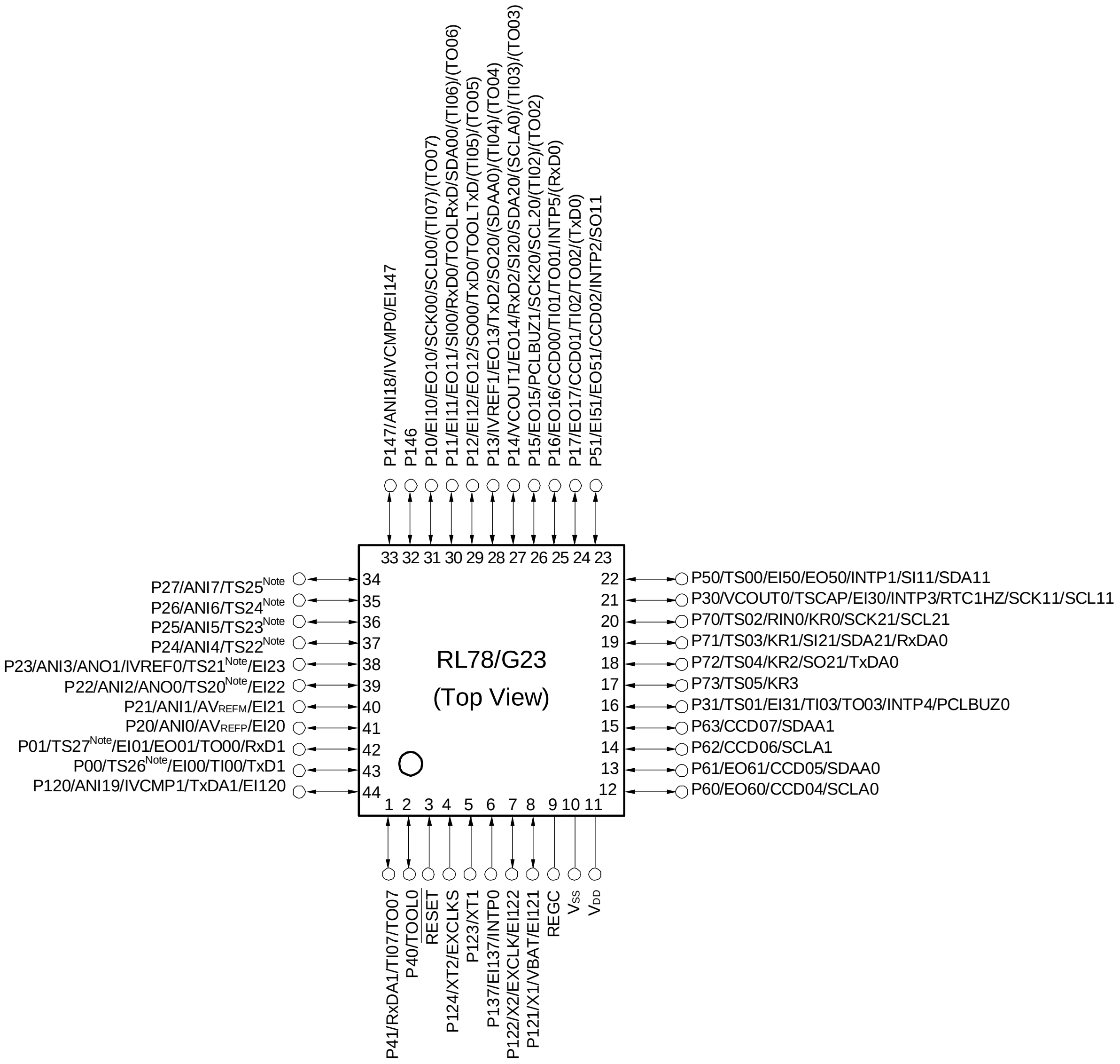
Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to Vss.

1.3.5 44-pin products

<R>

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)


P147/ANI18/IVCMP0/EI147
P146
P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
P17/EO17/CCD01/TI02/TO02/(TxD0)
P51/EI51/EO51/CCD02/INTP2/SO11
33 32 31 30 29 28 27 26 25 24 23
P27/ANI7/TS25Note
P26/ANI6/TS24Note
P25/ANI5/TS23Note
P24/ANI4/TS22Note
P23/ANI3/ANO1/IVREF0/TS21Note/EI23
P22/ANI2/ANO0/TS20Note/EI22
P21/ANI1/AVREFM/EI21
P20/ANI0/AVREFP/EI20
P01/TS27Note/EI01/EO01/TO00/RxD1
P00/TS26Note/EI00/TI00/TxD1
P120/ANI19/IVCMP1/TxDA1/EI120
34 35 36 37 38 39 40 41 42 43 44
RL78/G23
(Top View)
22 21 20 19 18 17 16 15 14 13 12
P50/TS00/EI50/EO50/INTP1/SI11/SDA11
P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11
P70/TS02/RIN0/KR0/SCK21/SCL21
P71/TS03/KR1/SI21/SDA21/RxDA0
P72/TS04/KR2/SO21/TxDA0
P73/TS05/KR3
P31/TS01/EI31/TI03/TO03/INTP4/PCLBUZ0
P63/CCD07/SDAA1
P62/CCD06/SCLA1
P61/EO61/CCD05/SDAA0
P60/EO60/CCD04/SCLA0
1 2 3 4 5 6 7 8 9 10 11
P41/RxDA1/TI07/TO07
P40/TOOL0
RESET
P124/XT2/EXCLKS
P123/XT1
P137/EI137/INTP0
P122/X2/EXCLK/EI122
P121/X1/VBAT/EI121
REGC
VSS
VDD

Note Not present in products with 128 or fewer Kbytes of code flash memory.

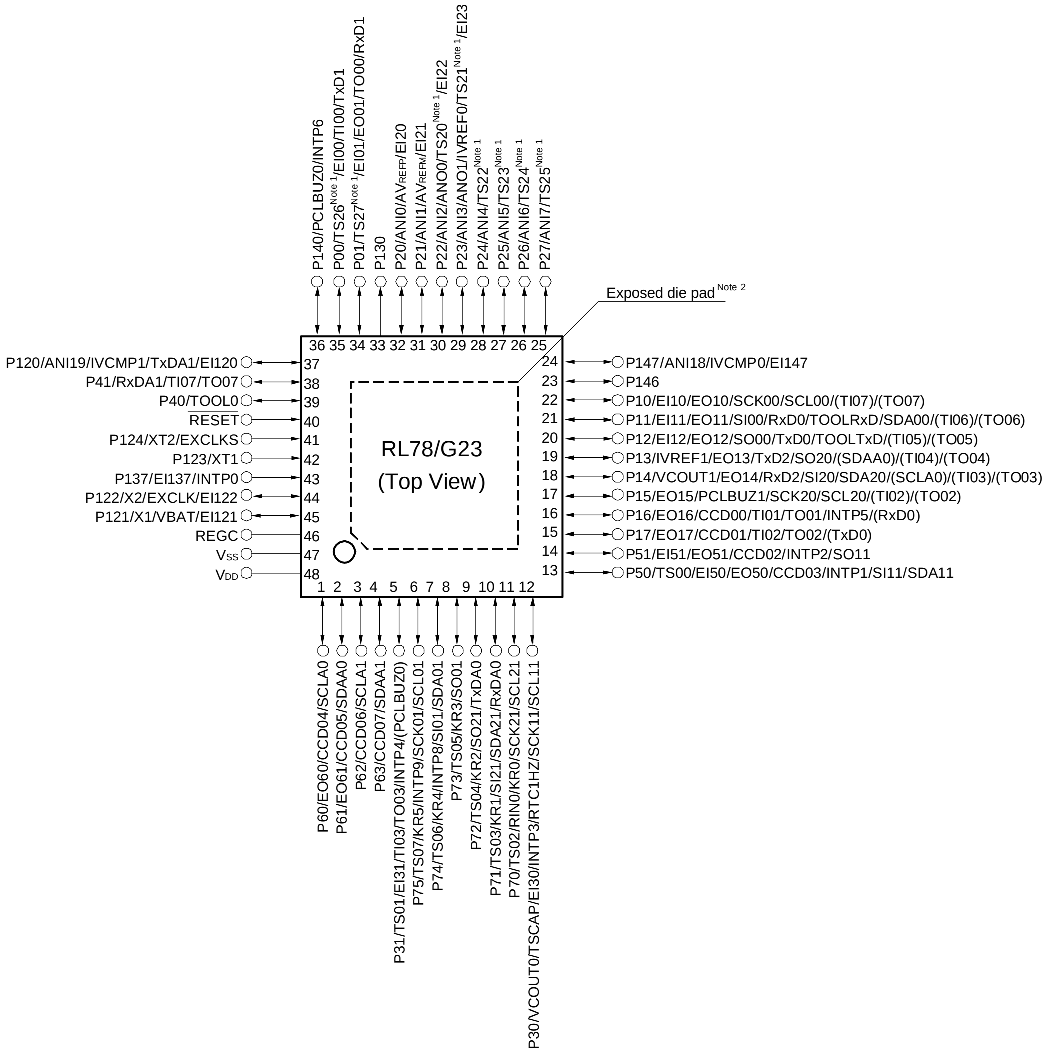
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)


P140/PCLBUZ0/INTP6
P00/TS26^Note 1/EI00/TI00/TxD1
P01/TS27^Note 1/EI01/EO01/TO00/RxD1
P130
P20/ANI0/AVREFP/EI20
P21/ANI1/AVREFM/EI21
P22/ANI2/ANO0/TS20^Note 1/EI22
P23/ANI3/ANO1/IVREF0/TS21^Note 1/EI23
P24/ANI4/TS22^Note 1
P25/ANI5/TS23^Note 1
P26/ANI6/TS24^Note 1
P27/ANI7/TS25^Note 1
Exposed die pad^Note 2
36 35 34 33 32 31 30 29 28 27 26 25
P120/ANI19/IVCMP1/TxDA1/EI120 37
P41/RxDA1/TI07/TO07 38
P40/TOOL0 39
RESET 40
P124/XT2/EXCLKS 41
P123/XT1 42
P137/EI137/INTP0 43
P122/X2/EXCLK/EI122 44
P121/X1/VBAT/EI121 45
REGC 46
VSS 47
VDD 48
RL78/G23
(Top View)
24 P147/ANI18/IVCMP0/EI147
23 P146
22 P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
21 P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
20 P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
19 P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
18 P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
17 P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
16 P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
15 P17/EO17/CCD01/TI02/TO02/(TxD0)
14 P51/EI51/EO51/CCD02/INTP2/SO11
13 P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
1 2 3 4 5 6 7 8 9 10 11 12
P60/EO60/CCD04/SCLA0
P61/EO61/CCD05/SDAA0
P62/CCD06/SCLA1
P63/CCD07/SDAA1
P31/TS01/EI31/TI03/TO03/INTP4/(PCLBUZ0)
P75/TS07/KR5/INTP9/SCK01/SCL01
P74/TS06/KR4/INTP8/SI01/SDA01
P73/TS05/KR3/SO01
P72/TS04/KR2/SO21/TxDA0
P71/TS03/KR1/SI21/SDA21/RxDA0
P70/TS02/RIN0/KR0/SCK21/SCL21
P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11

Note 1. Not present in products with 128 or fewer Kbytes of code flash memory.

<R> **Note 2.** The 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

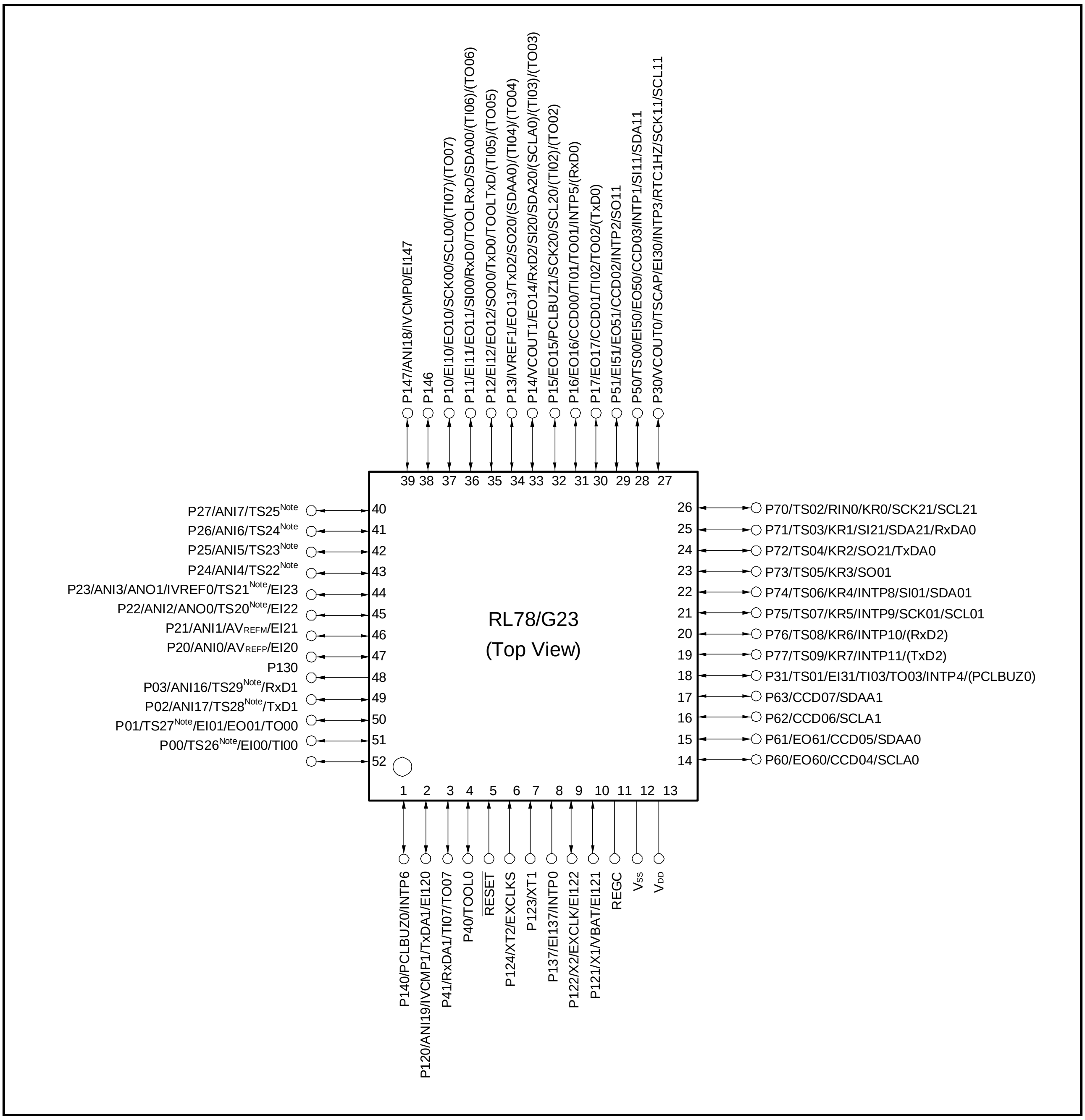
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

<R> **Remark 3.** It is recommended to connect an exposed die pad to VSS.

1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)


P147/ANI18/IVCMP0/EI147
P146
P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/EI12/EO12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/EO15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
P16/EO16/CCD00/TI01/TO01/INTP5/(RxD0)
P17/EO17/CCD01/TI02/TO02/(TxD0)
P51/EI51/EO51/CCD02/INTP2/SO11
P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11
39 38 37 36 35 34 33 32 31 30 29 28 27
P27/ANI7/TS25$^{\text{Note}}$ 40
P26/ANI6/TS24$^{\text{Note}}$ 41
P25/ANI5/TS23$^{\text{Note}}$ 42
P24/ANI4/TS22$^{\text{Note}}$ 43
P23/ANI3/ANO1/IVREF0/TS21$^{\text{Note}}$/EI23 44
P22/ANI2/ANO0/TS20$^{\text{Note}}$/EI22 45
P21/ANI1/AV$_{\text{REFM}}$/EI21 46
P20/ANI0/AV$_{\text{REFP}}$/EI20 47
P130 48
P03/ANI16/TS29$^{\text{Note}}$/RxD1 49
P02/ANI17/TS28$^{\text{Note}}$/TxD1 50
P01/TS27$^{\text{Note}}$/EI01/EO01/TO00 51
P00/TS26$^{\text{Note}}$/EI00/TI00 52
RL78/G23
(Top View)
26 P70/TS02/RIN0/KR0/SCK21/SCL21
25 P71/TS03/KR1/SI21/SDA21/RxDA0
24 P72/TS04/KR2/SO21/TxDA0
23 P73/TS05/KR3/SO01
22 P74/TS06/KR4/INTP8/SI01/SDA01
21 P75/TS07/KR5/INTP9/SCK01/SCL01
20 P76/TS08/KR6/INTP10/(RxD2)
19 P77/TS09/KR7/INTP11/(TxD2)
18 P31/TS01/EI31/TI03/TO03/INTP4/(PCLBUZ0)
17 P63/CCD07/SDAA1
16 P62/CCD06/SCLA1
15 P61/EO61/CCD05/SDAA0
14 P60/EO60/CCD04/SCLA0
1 2 3 4 5 6 7 8 9 10 11 12 13
P140/PCLBUZ0/INTP6
P120/ANI19/IVCMP1/TxDA1/EI120
P41/RxDA1/TI07/TO07
P40/TOOL0
RESET
P124/XT2/EXCLKS
P123/XT1
P137/EI137/INTP0
P122/X2/EXCLK/EI122
P121/X1/VBAT/EI121
REGC
V$_{\text{SS}}$
V$_{\text{DD}}$

Note Not present in products with 128 or fewer Kbytes of code flash memory.

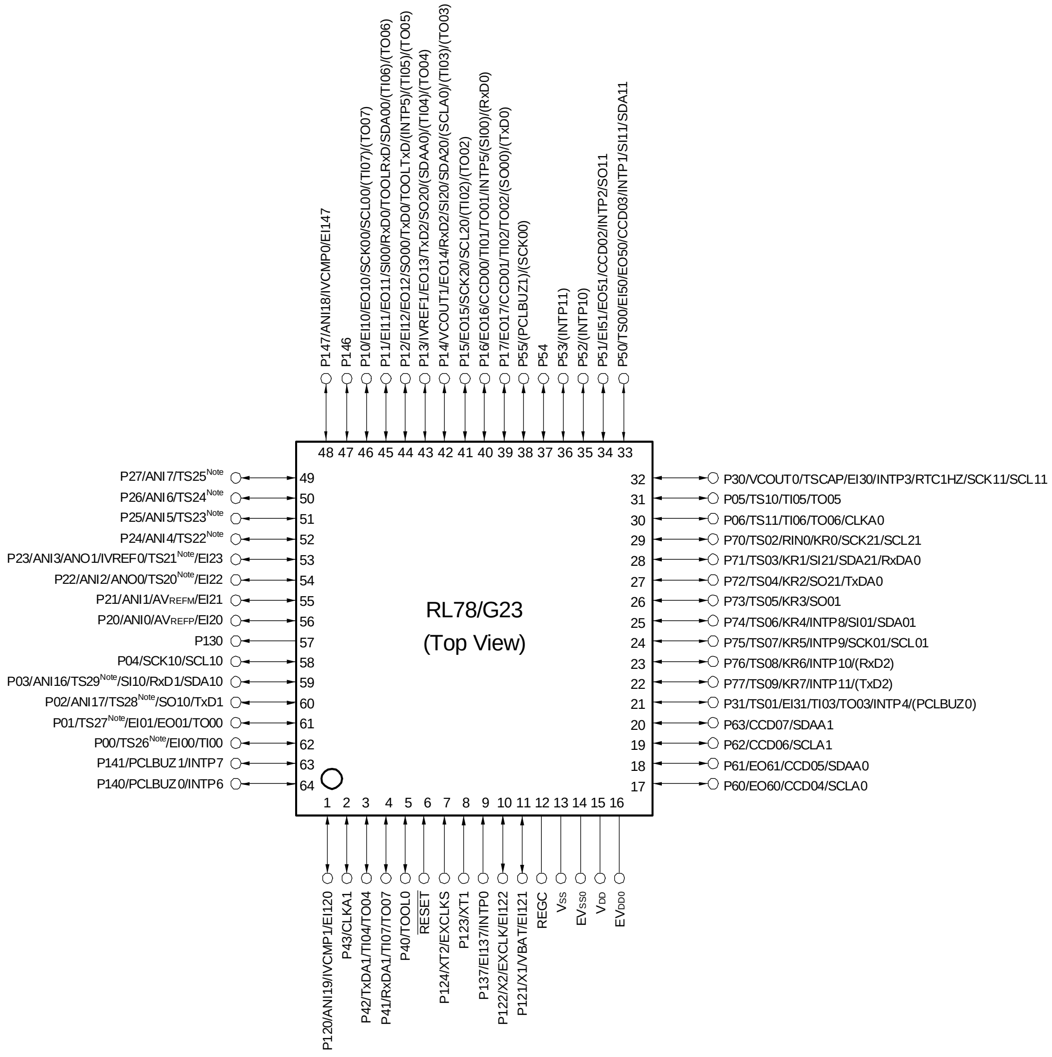
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.8 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)


P147/ANI18/IVCMP0/EI147
P146
P10/EI10/EO10/SCK00/SCL00/(TI07)/(TO07)
P11/EI11/EO11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/EI12/EO12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)
P13/IVREF1/EO13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/VCOUT1/EO14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/EO15/SCK20/SCL20/(TI02)/(TO02)
P16/EO16/CCD00/TI01/TO01/INTP5/(SI00)/(RxD0)
P17/EO17/CCD01/TI02/TO02/(SO00)/(TxD0)
P55/(PCLBUZ1)/(SCK00)
P54
P53/(INTP11)
P52/(INTP10)
P51/EI51/EO51/CCD02/INTP2/SO11
P50/TS00/EI50/EO50/CCD03/INTP1/SI11/SDA11
48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
P27/ANI7/TS25Note 49
P26/ANI6/TS24Note 50
P25/ANI5/TS23Note 51
P24/ANI4/TS22Note 52
P23/ANI3/ANO1/IVREF0/TS21Note/EI23 53
P22/ANI2/ANO0/TS20Note/EI22 54
P21/ANI1/AV_{REFM}/EI21 55
P20/ANI0/AV_{REFP}/EI20 56
P130 57
P04/SCK10/SCL10 58
P03/ANI16/TS29Note/SI10/RxD1/SDA10 59
P02/ANI17/TS28Note/SO10/TxD1 60
P01/TS27Note/EI01/EO01/TO00 61
P00/TS26Note/EI00/TI00 62
P141/PCLBUZ1/INTP7 63
P140/PCLBUZ0/INTP6 64
RL78/G23
(Top View)
32 P30/VCOUT0/TSCAP/EI30/INTP3/RTC1HZ/SCK11/SCL11
31 P05/TS10/TI05/TO05
30 P06/TS11/TI06/TO06/CLKA0
29 P70/TS02/RIN0/KR0/SCK21/SCL21
28 P71/TS03/KR1/SI21/SDA21/RxDA0
27 P72/TS04/KR2/SO21/TxDA0
26 P73/TS05/KR3/SO01
25 P74/TS06/KR4/INTP8/SI01/SDA01
24 P75/TS07/KR5/INTP9/SCK01/SCL01
23 P76/TS08/KR6/INTP10/(RxD2)
22 P77/TS09/KR7/INTP11/(TxD2)
21 P31/TS01/EI31/TI03/TO03/INTP4/(PCLBUZ0)
20 P63/CCD07/SDAA1
19 P62/CCD06/SCLA1
18 P61/EO61/CCD05/SDAA0
17 P60/EO60/CCD04/SCLA0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
P120/ANI19/IVCMP1/EI120
P43/CLKA1
P42/TxDA1/TI04/TO04
P41/RxDA1/TI07/TO07
P40/TOOL0
$\overline{\text{RESET}}$
P124/XT2/EXCLKS
P123/XT1
P137/EI137/INTP0
P122/X2/EXCLK/EI122
P121/X1/VBAT/EI121
REGC
V_{SS}
EV_{SS0}
V_{DD}
EV_{DD0}

Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution 1. Connect the EV_{SS0} pin to the same ground as the V_{SS} pin.

Caution 2. Make sure that the voltage on the V_{DD} pin is no less than that on the EV_{DD0} pin.

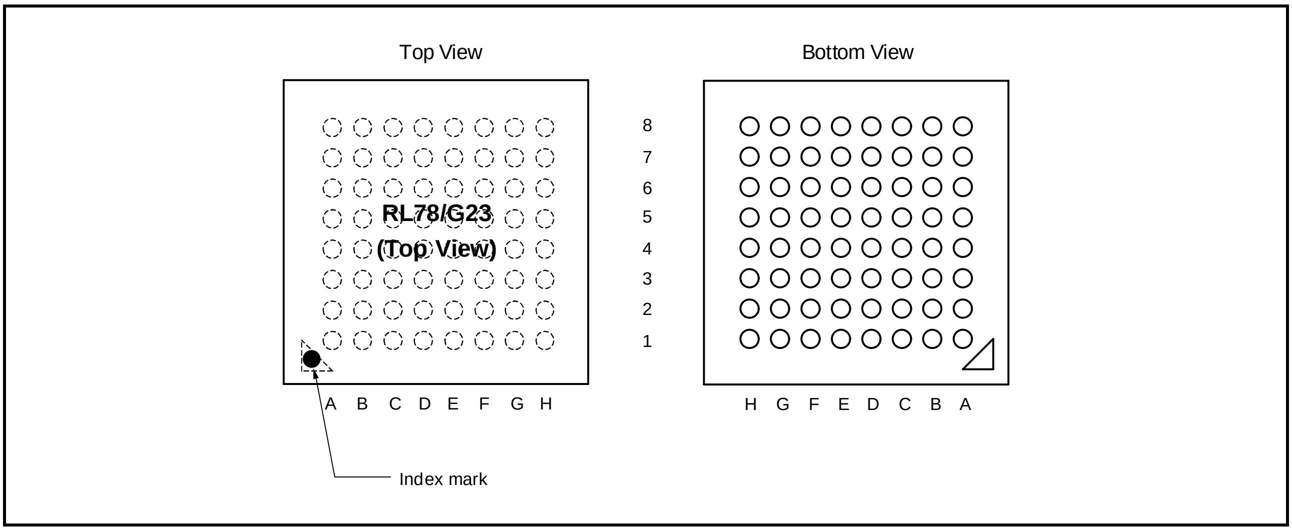
Caution 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

- 64-pin plastic WFLGA (5 × 5 mm, 0.50-mm pitch)



	A	B	C	D	E	F	G	H
8	EVDD0	EVSS0	P121/X1/EI121/VBAT	P122/X2/EXCLK/EI122	P137/INTP0/EI137	P123/XT1	P124/XT2/EXCLKS	P120/ANI19/IVCMP1/EI120
7	P60/CCD04/SCLA0/EO60	VDD	VSS	REGC	$\overline{\text{RESET}}$	P01/TS27$^{\text{Note}}$/EI01/EO01/TO00	P00/TS26$^{\text{Note}}$/EI00/TI00	P140/PCLBUZ0/INTP6
6	P61/CCD05/SDAA0/EO61	P62/CCD06/SCLA1	P63/CCD07/SDAA1	P40/TOOL0	P41/TI07/TO07/RxDA1	P43/CLKA1	P02/ANI17/TS28$^{\text{Note}}$/SO10/TxD1	P141/PCLBUZ1/INTP7
5	P77/KR7/TS09/INTP11/(TxD2)	P31/TI03/TO03/INTP4/TS01/EI31/(PCLBUZ0)	P53/(INTP11)	P42/TI04/TO04/TxDA1	P03/ANI16/TS29$^{\text{Note}}$/SI10/RxD1/SDA10	P04/SCK10/SCL10	P130	P20/ANI0/AVREFP/EI20
4	P75/KR5/TS07/INTP9/SCK01/SCL01	P76/KR6/TS08/INTP10/(RxD2)	P52/(INTP10)	P54	P16/CCD00/TI01/TO01/INTP5/EO16/(SI00)/(RxD0)	P21/ANI1/AVREFM/EI21	P22/ANI2/ANO0/EI22/TS20$^{\text{Note}}$	P23/ANI3/ANO1/IVREF0/EI23/TS21$^{\text{Note}}$
3	P70/KR0/TS02/RIN0/SCK21/SCL21	P73/KR3/TS05/SO01	P74/KR4/TS06/INTP8/SI01/SDA01	P17/CCD01/TI02/TO02/EO17/(SO00)/(TxD0)	P15/SCK20/SCL20/EO15/(TI02)/(TO02)	P12/SO00/TxD0/TOOLTxD/EI12/EO12/(INTP5)/(TI05)/(TO05)	P24/ANI4/TS22$^{\text{Note}}$	P26/ANI6/TS24$^{\text{Note}}$
2	P30/INTP3/TSCAP/RTC1HZ/EI30/VCOUT0/SCK11/SCL11	P72/KR2/TS04/SO21/TxDA0	P71/KR1/TS03/SI21/SDA21/RxDA0	P06/TS11/TI06/TO06/CLKA0	P14/RxD2/SI20/SDA20/VCOUT1/EO14/(SCLA0)/(TI03)/(TO03)	P11/SI00/RxD0/TOOLRxD/SDA00/EI11/EO11/(TI06)/(TO06)	P25/ANI5/TS23$^{\text{Note}}$	P27/ANI7/TS25$^{\text{Note}}$
1	P05/TS10/TI05/TO05	P50/CCD03/TS00/EI50/EO50/INTP1/SI11/SDA11	P51/CCD02/EI51/EO51/INTP2/SO11	P55/(PCLBUZ1)/(SCK00)	P13/TxD2/SO20/IVREF1/EO13/(SDAA0)/(TI04)/(TO04)	P10/SCK00/SCL00/EI10/EO10/(TI07)/(TO07)	P146	P147/ANI18/EI147/IVCMP0

Note Not present in products with 128 or fewer Kbytes of code flash memory.

(Cautions and Remarks are listed on the next page.)

Caution 1. Connect the EV_{SS0} pin to the same ground as the V_{SS} pin.

Caution 2. Make sure that the voltage on the V_{DD} pin is no less than that on the EV_{DD0} pin.

Caution 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

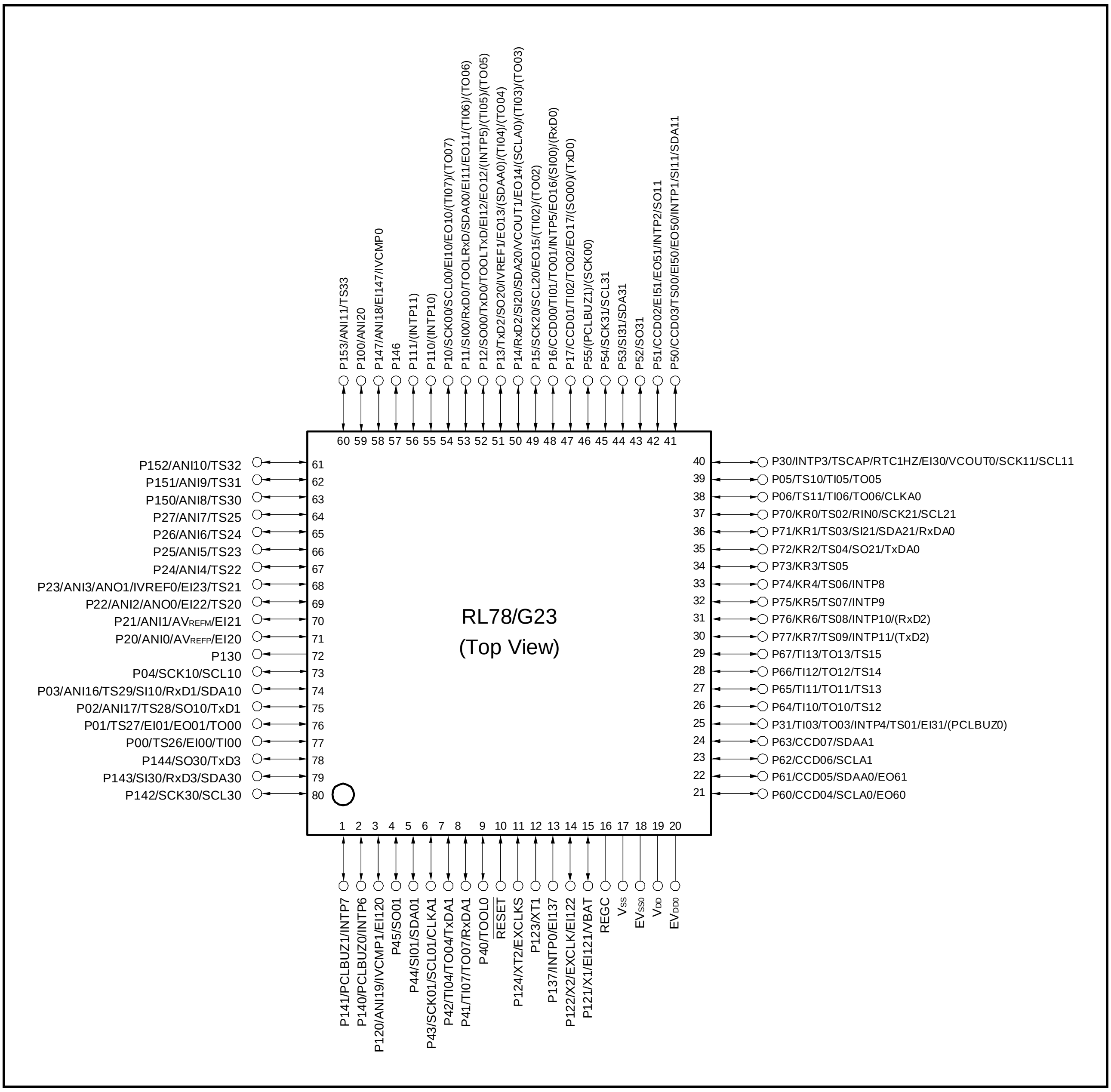
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.50-mm pitch)


RL78/G23
(Top View)
1 P141/PCLBUZ1/INTP7
2 P140/PCLBUZ0/INTP6
3 P120/ANI19/IVCMP1/EI120
4 P45/SO01
5 P44/SI01/SDA01
6 P43/SCK01/SCL01/CLKA1
7 P42/TI04/TO04/TxDA1
8 P41/TI07/TO07/RxDA1
9 P40/TOOL0
10 RESET
11 P124/XT2/EXCLKS
12 P123/XT1
13 P137/INTP0/EI137
14 P122/X2/EXCLK/EI122
15 P121/X1/EI121/VBAT
16 REGC
17 VSS
18 EVSS0
19 VDD
20 EVDD0
21 P60/CCD04/SCLA0/EO60
22 P61/CCD05/SDAA0/EO61
23 P62/CCD06/SCLA1
24 P63/CCD07/SDAA1
25 P31/TI03/TO03/INTP4/TS01/EI31/(PCLBUZ0)
26 P64/TI10/TO10/TS12
27 P65/TI11/TO11/TS13
28 P66/TI12/TO12/TS14
29 P67/TI13/TO13/TS15
30 P77/KR7/TS09/INTP11/(TxD2)
31 P76/KR6/TS08/INTP10/(RxD2)
32 P75/KR5/TS07/INTP9
33 P74/KR4/TS06/INTP8
34 P73/KR3/TS05
35 P72/KR2/TS04/SO21/TxDA0
36 P71/KR1/TS03/SI21/SDA21/RxDA0
37 P70/KR0/TS02/RIN0/SCK21/SCL21
38 P06/TS11/TI06/TO06/CLKA0
39 P05/TS10/TI05/TO05
40 P30/INTP3/TSCAP/RTC1HZ/EI30/VCOUT0/SCK11/SCL11
41 P50/CCD03/TS00/EI50/EO50/INTP1/SI11/SDA11
42 P51/CCD02/EI51/EO51/INTP2/SO11
43 P52/SO31
44 P53/SI31/SDA31
45 P54/SCK31/SCL31
46 P55/(PCLBUZ1)/(SCK00)
47 P17/CCD01/TI02/TO02/EO17/(SO00)/(TxD0)
48 P16/CCD00/TI01/TO01/INTP5/EO16/(SI00)/(RxD0)
49 P15/SCK20/SCL20/EO15/(TI02)/(TO02)
50 P14/RxD2/SI20/SDA20/VCOUT1/EO14/(SCLA0)/(TI03)/(TO03)
51 P13/TxD2/SO20/IVREF1/EO13/(SDAA0)/(TI04)/(TO04)
52 P12/SO00/TxD0/TOOLTxD/EI12/EO12/(INTP5)/(TI05)/(TO05)
53 P11/SI00/RxD0/TOOLRxD/SDA00/EI11/EO11/(TI06)/(TO06)
54 P10/SCK00/SCL00/EI10/EO10/(TI07)/(TO07)
55 P110/(INTP10)
56 P111/(INTP11)
57 P146
58 P147/ANI18/EI147/IVCMP0
59 P100/ANI20
60 P153/ANI11/TS33
61 P152/ANI10/TS32
62 P151/ANI9/TS31
63 P150/ANI8/TS30
64 P27/ANI7/TS25
65 P26/ANI6/TS24
66 P25/ANI5/TS23
67 P24/ANI4/TS22
68 P23/ANI3/ANO1/IVREF0/EI23/TS21
69 P22/ANI2/ANO0/EI22/TS20
70 P21/ANI1/AVREFM/EI21
71 P20/ANI0/AVREFP/EI20
72 P130
73 P04/SCK10/SCL10
74 P03/ANI16/TS29/SI10/RxD1/SDA10
75 P02/ANI17/TS28/SO10/TxD1
76 P01/TS27/EI01/EO01/TO00
77 P00/TS26/EI00/TI00
78 P144/SO30/TxD3
79 P143/SI30/RxD3/SDA30
80 P142/SCK30/SCL30

Caution 1. Connect the EVSS0 pin to the same ground as the Vss pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 pin.

Caution 3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

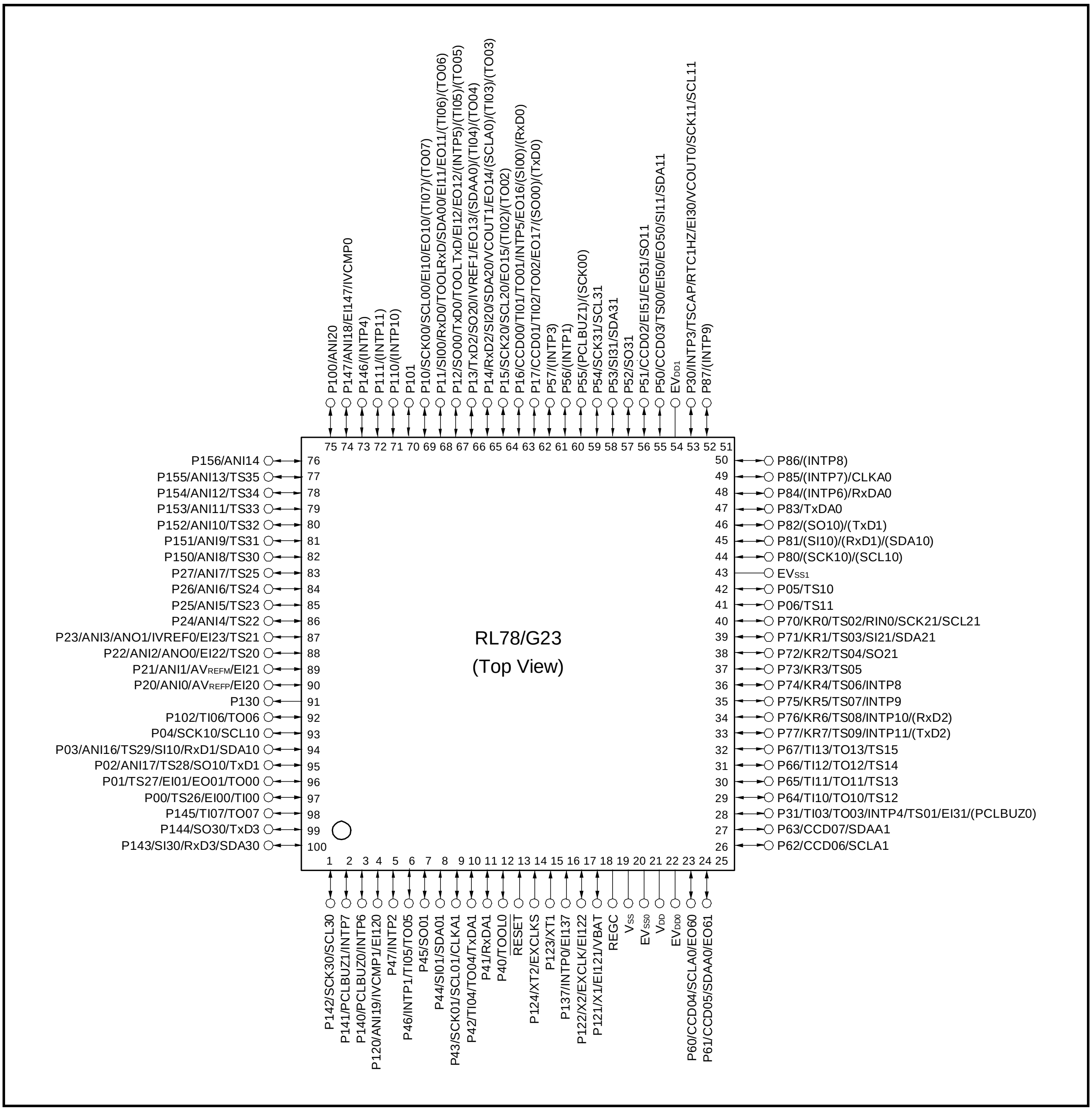
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.10 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.50-mm pitch)


P100/ANI20
P147/ANI18/EI147/IVCMP0
P146/(INTP4)
P111/(INTP11)
P110/(INTP10)
P101
P10/SCK00/SCL00/EI10/EO10/(TI07)/(TO07)
P11/SI00/RxD0/TOOLRxD/SDA00/EI11/EO11/(TI06)/(TO06)
P12/SO00/TxD0/TOOLTxD/EI12/EO12/(INTP5)/(TI05)/(TO05)
P13/TxD2/SO20/IVREF1/EO13/(SDAA0)/(TI04)/(TO04)
P14/RxD2/SI20/SDA20/VCOUT1/EO14/(SCLA0)/(TI03)/(TO03)
P15/SCK20/SCL20/EO15/(TI02)/(TO02)
P16/CCD00/TI01/TO01/INTP5/EO16/(SI00)/(RxD0)
P17/CCD01/TI02/TO02/EO17/(SO00)/(TxD0)
P57/(INTP3)
P56/(INTP1)
P55/(PCLBUZ1)/(SCK00)
P54/SCK31/SCL31
P53/SI31/SDA31
P52/SO31
P51/CCD02/EI51/EO51/SO11
P50/CCD03/TS00/EI50/EO50/SI11/SDA11
EVDD1
P30/INTP3/TSCAP/RTC1HZ/EI30/VCOUT0/SCK11/SCL11
P87/(INTP9)
P156/ANI14
P155/ANI13/TS35
P154/ANI12/TS34
P153/ANI11/TS33
P152/ANI10/TS32
P151/ANI9/TS31
P150/ANI8/TS30
P27/ANI7/TS25
P26/ANI6/TS24
P25/ANI5/TS23
P24/ANI4/TS22
P23/ANI3/ANO1/IVREF0/EI23/TS21
P22/ANI2/ANO0/EI22/TS20
P21/ANI1/AVREFM/EI21
P20/ANI0/AVREFP/EI20
P130
P102/TI06/TO06
P04/SCK10/SCL10
P03/ANI16/TS29/SI10/RxD1/SDA10
P02/ANI17/TS28/SO10/TxD1
P01/TS27/EI01/EO01/TO00
P00/TS26/EI00/TI00
P145/TI07/TO07
P144/SO30/TxD3
P143/SI30/RxD3/SDA30
RL78/G23
(Top View)
P86/(INTP8)
P85/(INTP7)/CLKA0
P84/(INTP6)/RxDA0
P83/TxDA0
P82/(SO10)/(TxD1)
P81/(SI10)/(RxD1)/(SDA10)
P80/(SCK10)/(SCL10)
EVSS1
P05/TS10
P06/TS11
P70/KR0/TS02/RIN0/SCK21/SCL21
P71/KR1/TS03/SI21/SDA21
P72/KR2/TS04/SO21
P73/KR3/TS05
P74/KR4/TS06/INTP8
P75/KR5/TS07/INTP9
P76/KR6/TS08/INTP10/(RxD2)
P77/KR7/TS09/INTP11/(TxD2)
P67/TI13/TO13/TS15
P66/TI12/TO12/TS14
P65/TI11/TO11/TS13
P64/TI10/TO10/TS12
P31/TI03/TO03/INTP4/TS01/EI31/(PCLBUZ0)
P63/CCD07/SDAA1
P62/CCD06/SCLA1
P142/SCK30/SCL30
P141/PCLBUZ1/INTP7
P140/PCLBUZ0/INTP6
P120/ANI19/IVCMP1/EI120
P47/INTP2
P46/INTP1/TI05/TO05
P45/SO01
P44/SI01/SDA01
P43/SCK01/SCL01/CLKA1
P42/TI04/TO04/TxDA1
P41/RxDA1
P40/TOOL0
RESET
P124/XT2/EXCLKS
P123/XT1
P137/INTP0/EI137
P122/X2/EXCLK/EI122
P121/X1/EI121/VBAT
REGC
VSS
EVSS0
VDD
EVDD0
P60/CCD04/SCLA0/EO60
P61/CCD05/SDAA0/EO61

Caution 1. Connect the EVSS0 and EVSS1 pins to the same ground as the VSS pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 and EVDD1 pins. Also make sure that the voltage on the EVDD0 is the same as that on the EVDD1 pin.

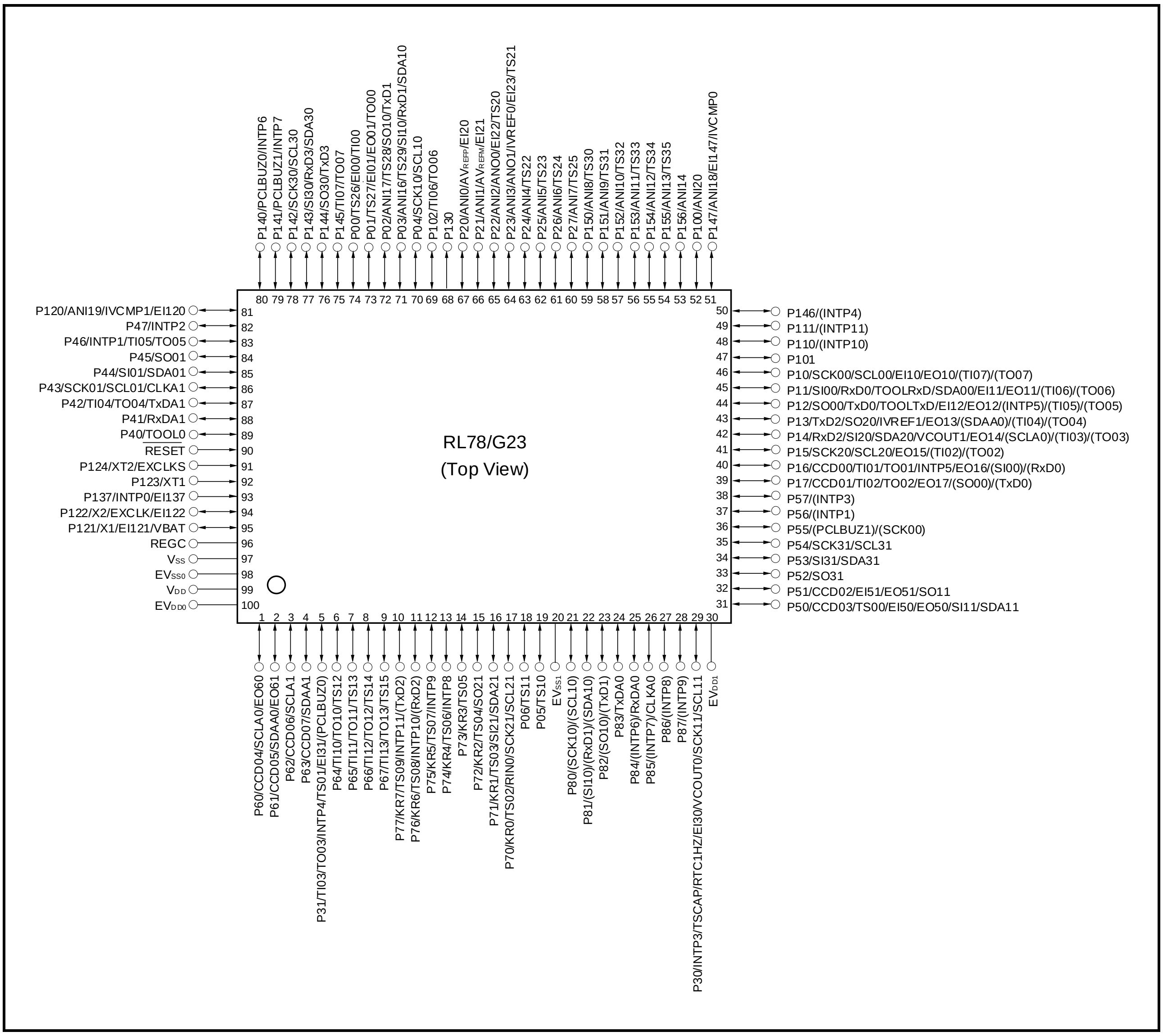
Caution 3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0, and EVDD1 pins and connect the VSS, EVSS0, and EVSS1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

- 100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)


RL78/G23
(Top View)
P60/CCD04/SCLA0/EO60
P61/CCD05/SDAA0/EO61
P62/CCD06/SCLA1
P63/CCD07/SDAA1
P31/TI03/TO03/INTP4/TS01/EI31/(PCLBUZ0)
P64/TI10/TO10/TS12
P65/TI11/TO11/TS13
P66/TI12/TO12/TS14
P67/TI13/TO13/TS15
P77/KR7/TS09/INTP11/(TxD2)
P76/KR6/TS08/INTP10/(RxD2)
P75/KR5/TS07/INTP9
P74/KR4/TS06/INTP8
P73/KR3/TS05
P72/KR2/TS04/SO21
P71/KR1/TS03/SI21/SDA21
P70/KR0/TS02/RIN0/SCK21/SCL21
P06/TS11
P05/TS10
EVSS1
P80/(SCK10)/(SCL10)
P81/(SI10)/(RxD1)/(SDA10)
P82/(SO10)/(TxD1)
P83/TxDA0
P84/(INTP6)/RxDA0
P85/(INTP7)/CLKA0
P86/(INTP8)
P87/(INTP9)
P30/INTP3/TSCAP/RTC1HZ/EI30/VCOUT0/SCK11/SCL11
EVDD1
P50/CCD03/TS00/EI50/EO50/SI11/SDA11
P51/CCD02/EI51/EO51/SO11
P52/SO31
P53/SI31/SDA31
P54/SCK31/SCL31
P55/(PCLBUZ1)/(SCK00)
P56/(INTP1)
P57/(INTP3)
P17/CCD01/TI02/TO02/EO17/(SO00)/(TxD0)
P16/CCD00/TI01/TO01/INTP5/EO16/(SI00)/(RxD0)
P15/SCK20/SCL20/EO15/(TI02)/(TO02)
P14/RxD2/SI20/SDA20/VCOUT1/EO14/(SCLA0)/(TI03)/(TO03)
P13/TxD2/SO20/IVREF1/EO13/(SDAA0)/(TI04)/(TO04)
P12/SO00/TxD0/TOOLTxD/EI12/EO12/(INTP5)/(TI05)/(TO05)
P11/SI00/RxD0/TOOLRxD/SDA00/EI11/EO11/(TI06)/(TO06)
P10/SCK00/SCL00/EI10/EO10/(TI07)/(TO07)
P101
P110/(INTP10)
P111/(INTP11)
P146/(INTP4)
P147/ANI18/EI147/IVCMP0
P100/ANI20
P156/ANI14
P155/ANI13/TS35
P154/ANI12/TS34
P153/ANI11/TS33
P152/ANI10/TS32
P151/ANI9/TS31
P150/ANI8/TS30
P27/ANI7/TS25
P26/ANI6/TS24
P25/ANI5/TS23
P24/ANI4/TS22
P23/ANI3/ANO1/IVREF0/EI23/TS21
P22/ANI2/ANO0/EI22/TS20
P21/ANI1/AVREFM/EI21
P20/ANI0/AVREFP/EI20
P130
P102/TI06/TO06
P04/SCK10/SCL10
P03/ANI16/TS29/SI10/RxD1/SDA10
P02/ANI17/TS28/SO10/TxD1
P01/TS27/EI01/EO01/TO00
P00/TS26/EI00/TI00
P145/TI07/TO07
P144/SO30/TxD3
P143/SI30/RxD3/SDA30
P142/SCK30/SCL30
P141/PCLBUZ1/INTP7
P140/PCLBUZ0/INTP6
P120/ANI19/IVCMP1/EI120
P47/INTP2
P46/INTP1/TI05/TO05
P45/SO01
P44/SI01/SDA01
P43/SCK01/SCL01/CLKA1
P42/TI04/TO04/TxDA1
P41/RxDA1
P40/TOOL0
RESET
P124/XT2/EXCLKS
P123/XT1
P137/INTP0/EI137
P122/X2/EXCLK/EI122
P121/X1/EI121/VBAT
REGC
VSS
EVSS0
VDD
EVDD0

Caution 1. Connect the EVSS0 and EVSS1 pins to the same ground as the VSS pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 and EVDD1 pins. Also make sure that the voltage on the EVDD0 is the same as that on the EVDD1 pin.

Caution 3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

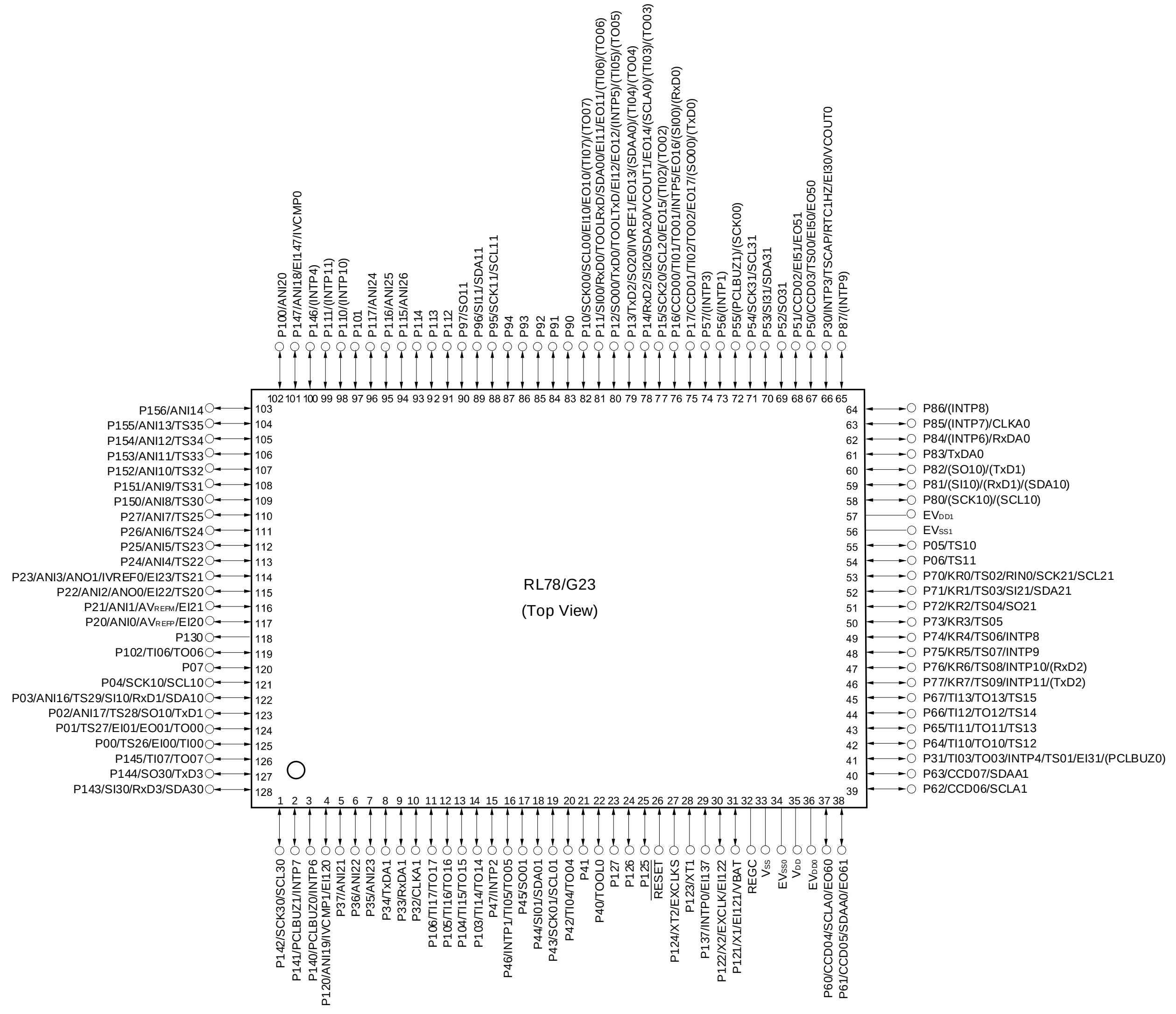
Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0, and EVDD1 pins and connect the VSS, EVSS0, and EVSS1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

1.3.11 128-pin products

- 128-pin plastic LFQFP (14 × 20 mm, 0.50-mm pitch)


RL78/G23
(Top View)
P100/ANI20
P147/ANI18/EI147/IVCMP0
P146/(INTP4)
P111/(INTP11)
P110/(INTP10)
P101
P117/ANI24
P116/ANI25
P115/ANI26
P114
P113
P112
P97/SO11
P96/SI11/SDA11
P95/SCK11/SCL11
P94
P93
P92
P91
P90
P10/SCK00/SCL00/EI10/EO10/(TI07)/(TO07)
P11/SI00/RxD0/TOOLRxD/SDA00/EI11/EO11/(TI06)/(TO06)
P12/SO00/TxD0/TOOLTxD/EI12/EO12/(INTP5)/(TI05)/(TO05)
P13/TxD2/SO20/IVREF1/EO13/(SDAA0)/(TI04)/(TO04)
P14/RxD2/SI20/SDA20/VCOUT1/EO14/(SCLA0)/(TI03)/(TO03)
P15/SCK20/SCL20/EO15/(TI02)/(TO02)
P16/CCD00/TI01/TO01/INTP5/EO16/(SI00)/(RxD0)
P17/CCD01/TI02/TO02/EO17/(SO00)/(TxD0)
P57/(INTP3)
P56/(INTP1)
P55/(PCLBUZ1)/(SCK00)
P54/SCK31/SCL31
P53/SI31/SDA31
P52/SO31
P51/CCD02/EI51/EO51
P50/CCD03/TS00/EI50/EO50
P30/INTP3/TSCAP/RTC1HZ/EI30/VCOUT0
P87/(INTP9)
102 101 100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65
P156/ANI14 103
P155/ANI13/TS35 104
P154/ANI12/TS34 105
P153/ANI11/TS33 106
P152/ANI10/TS32 107
P151/ANI9/TS31 108
P150/ANI8/TS30 109
P27/ANI7/TS25 110
P26/ANI6/TS24 111
P25/ANI5/TS23 112
P24/ANI4/TS22 113
P23/ANI3/ANO1/IVREF0/EI23/TS21 114
P22/ANI2/ANO0/EI22/TS20 115
P21/ANI1/AVREFM/EI21 116
P20/ANI0/AVREFP/EI20 117
P130 118
P102/TI06/TO06 119
P07 120
P04/SCK10/SCL10 121
P03/ANI16/TS29/SI10/RxD1/SDA10 122
P02/ANI17/TS28/SO10/TxD1 123
P01/TS27/EI01/EO01/TO00 124
P00/TS26/EI00/TI00 125
P145/TI07/TO07 126
P144/SO30/TxD3 127
P143/SI30/RxD3/SDA30 128
64 P86/(INTP8)
63 P85/(INTP7)/CLKA0
62 P84/(INTP6)/RxDA0
61 P83/TxDA0
60 P82/(SO10)/(TxD1)
59 P81/(SI10)/(RxD1)/(SDA10)
58 P80/(SCK10)/(SCL10)
57 EVDD1
56 EVSS1
55 P05/TS10
54 P06/TS11
53 P70/KR0/TS02/RIN0/SCK21/SCL21
52 P71/KR1/TS03/SI21/SDA21
51 P72/KR2/TS04/SO21
50 P73/KR3/TS05
49 P74/KR4/TS06/INTP8
48 P75/KR5/TS07/INTP9
47 P76/KR6/TS08/INTP10/(RxD2)
46 P77/KR7/TS09/INTP11/(TxD2)
45 P67/TI13/TO13/TS15
44 P66/TI12/TO12/TS14
43 P65/TI11/TO11/TS13
42 P64/TI10/TO10/TS12
41 P31/TI03/TO03/INTP4/TS01/EI31/(PCLBUZ0)
40 P63/CCD07/SDAA1
39 P62/CCD06/SCLA1
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38
P142/SCK30/SCL30
P141/PCLBUZ1/INTP7
P140/PCLBUZ0/INTP6
P120/ANI19/IVCMP1/EI120
P37/ANI21
P36/ANI22
P35/ANI23
P34/TxDA1
P33/RxDA1
P32/CLKA1
P106/TI17/TO17
P105/TI16/TO16
P104/TI15/TO15
P103/TI14/TO14
P47/INTP2
P46/INTP1/TI05/TO05
P45/SO01
P44/SI01/SDA01
P43/SCK01/SCL01
P42/TI04/TO04
P41
P40/TOOL0
P127
P126
P125/RESET
P124/XT2/EXCLKS
P123/XT1
P137/INTP0/EI137
P122/X2/EXCLK/EI122
P121/X1/EI121/VBAT
REGC
VSS
EVSS0
VDD
EVDD0
P60/CCD04/SCLA0/EO60
P61/CCD05/SDAA0/EO61

Caution 1. Connect the EVSS0 and EVSS1 pins to the same ground as the VSS pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 and EVDD1 pins. Also make sure that the voltage on the EVDD0 is the same as that on the EVDD1 pin.

Caution 3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0, and EVDD1 pins and connect the VSS, EVSS0, and EVSS1 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) (1/2)** in the RL78/G23 User's Manual.

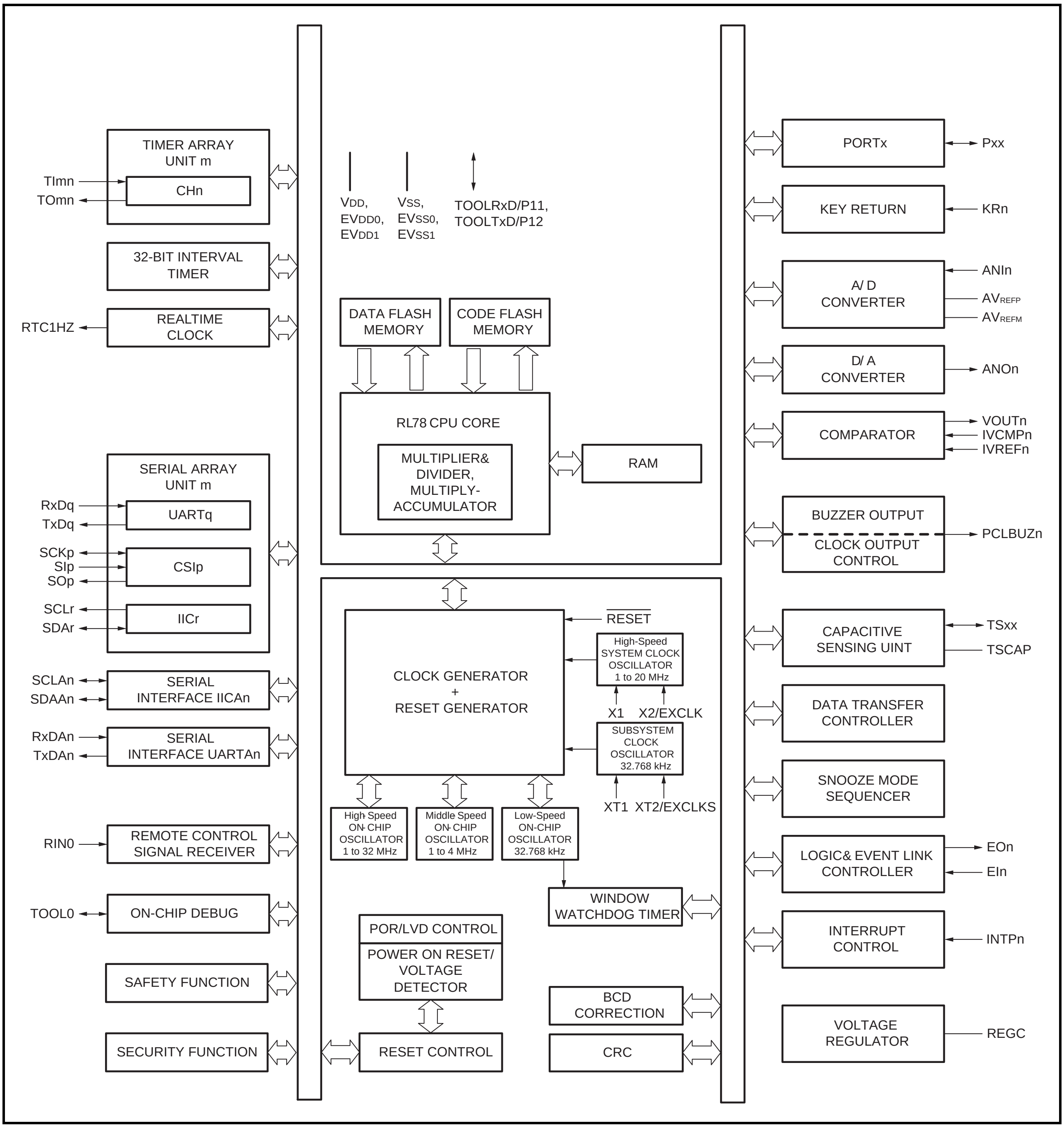
1.4 Pin Identification

ANI0 to ANI14, ANI16 to ANI26:	Analog input
ANO0, ANO1:	Analog output
AVREFM:	Analog reference voltage minus
AVREFP:	Analog reference voltage plus
CCD00 to CCD07:	Controlled current drive output
CLKA0, CLKA1:	Asynchronous serial clock output
EI00, EI01, EI10 to EI12, EI20 to EI23, EI30, EI31, EI50, EI51, EI120 to EI122, EI137, EI147:	Logic & event link controller input
EO01, EO10 to EO17, EO50, EO51, EO60, EO61:	Logic & event link controller output
EVDD0, EVDD1:	Power supply for port
EVSS0, EVSS1:	Ground for port
EXCLK:	External clock input (main system clock)
EXCLKS:	External clock input (subsystem clock)
INTP0 to INTP11:	Interrupt request from Peripheral
IVCMP0, IVCMP1:	Comparator input
IVREF0, IVREF1:	Comparator reference input
KR0 to KR7:	Key return
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P97:	Port 9
P100 to P106:	Port 10
P110 to P117:	Port 11
P120 to P127:	Port 12
P130, P137:	Port 13
P140 to P147:	Port 14
P150 to P156:	Port 15

PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer Output
REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RIN0:	IR remote controller input
RTC1HZ:	Realtime clock correction clock (1 Hz) Output
RxD0 to RxD3, RxDA0, RxDA1:	Receive data
SCLA0, SCLA1, SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, SCK30, SCK31:	Serial clock input/output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21, SCL30, SCL31:	Serial clock output
SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31:	Serial data output
TSCAP:	Touch sensor capacitance
TI00 to TI07, TI10 to TI17:	Timer input
TO00 to TO07, TO10 to TO17:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TS00 to TS15, TS20 to TS35:	Capacitive sensor
TxD0 to TxD3, TxDA0, TxDA1:	Transmit data
VBAT:	Battery backup power supply
VCOUT0, VCOUT1:	Comparator output
VDD:	Power supply
VSS:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

1.5 Block Diagram

<R>


TIMER ARRAY UNIT m
CHn
TImn
TOmn
32-BIT INTERVAL TIMER
REALTIME CLOCK
RTC1HZ
SERIAL ARRAY UNIT m
UARTq
CSIp
IICr
RxDq
TxDq
SCKp
SIp
SOp
SCLr
SDAr
SCLAn
SDAAn
SERIAL INTERFACE IICAn
RxDAn
TxDAn
SERIAL INTERFACE UARTAn
RIN0
REMOTE CONTROL SIGNAL RECEIVER
TOOL0
ON-CHIP DEBUG
SAFETY FUNCTION
SECURITY FUNCTION
VDD, EVDD0, EVDD1
VSS, EVSS0, EVSS1
TOOLRxD/P11, TOOLTxD/P12
DATA FLASH MEMORY
CODE FLASH MEMORY
RL78 CPU CORE
MULTIPLIER& DIVIDER, MULTIPLY-ACCUMULATOR
RAM
CLOCK GENERATOR + RESET GENERATOR
RESET
High-Speed SYSTEM CLOCK OSCILLATOR 1 to 20 MHz
X1
X2/EXCLK
SUBSYSTEM CLOCK OSCILLATOR 32.768 kHz
XT1
XT2/EXCLKS
High-Speed ON-CHIP OSCILLATOR 1 to 32 MHz
Middle Speed ON-CHIP OSCILLATOR 1 to 4 MHz
Low-Speed ON-CHIP OSCILLATOR 32.768 kHz
WINDOW WATCHDOG TIMER
POR/LVD CONTROL
POWER ON RESET/ VOLTAGE DETECTOR
RESET CONTROL
BCD CORRECTION
CRC
PORTx
Pxx
KEY RETURN
KRn
A/ D CONVERTER
ANIn
AVREFP
AVREFM
D/ A CONVERTER
ANOn
COMPARATOR
VOUTn
IVCMPn
IVREFn
BUZZER OUTPUT
CLOCK OUTPUT CONTROL
PCLBUZn
CAPACITIVE SENSING UINT
TSxx
TSCAP
DATA TRANSFER CONTROLLER
SNOOZE MODE SEQUENCER
LOGIC& EVENT LINK CONTROLLER
EOn
EIn
INTERRUPT CONTROL
INTPn
VOLTAGE REGULATOR
REGC

Caution 1. 32- to 128-pin products incorporate the remote control signal receiver.

Caution 2. 36- to 128-pin products incorporate the serial interface UARTA.

Caution 3. 40- to 128-pin products incorporate the key return function.

Remark m: Unit number, n: Channel number, p: CSI number, q: UART number, r: Simplified I^{2}C number, xx: Port number

1.6 Outline of Functions

[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Caution This outline describes the functions at the time when peripheral I/O redirection register (PIOR) is set to 00H.

(1/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Code flash memory		96 to 256 KB	96 to 256 KB	96 to 256 KB	96 to 256 KB	96 to 768 KB	96 to 768 KB
Data flash memory		8 KB	8 KB	8 KB	8 KB	8 KB	8 KB
RAM		12 to 24 KB	12 to 24 KB	12 to 24 KB	12 to 24 KB	12 to 48 KB	12 to 48 KB
Address space		1 MB					
<R> CPU/ peripheral hardware clock frequency (f_{CLK})	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz$^{\text{Note 1}}$ (V_{DD} = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (V_{DD} = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz$^{\text{Note 1}}$ (V_{DD} = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz$^{\text{Note 2}}$ (V_{DD} = 1.6 to 5.5 V)					
	Subsystem clock	SUB mode: 32.768 kHz (V_{DD} = 1.6 to 5.5 V)					
Main system clock	High-speed system clock (f_{MX})	1 to 20 MHz					
	High-speed on-chip oscillator clock (f_{IH})	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz 24 MHz, 32 MHz					
	Middle-speed on-chip oscillator clock (f_{IM})	1 MHz, 2 MHz, 4 MHz					
Subsystem clock	Subsystem clock X (f_{SX})	32.768 kHz (V_{DD} = 2.4 to 5.5 V)			32.768 kHz (V_{DD} = 1.6 to 5.5 V)		
	Low-speed on-chip oscillator clock (f_{IL})	32.768 kHz (typ.)					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (f_{IH}))					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.					
I/O port	Total number of pins	26	28	32	36	40	44
	CMOS I/O	23 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)	24 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)	28 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	30 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	33 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V_{DD} withstand voltage]: 13)
	CMOS input	1	1	1	3	3	3
	CMOS output	—	—	—	—	—	1
	N-ch open drain I/O (withstand voltage: 6 V)	2	3	3	3	4	4
<R>	Output current control port	6	7	7	7	7	8

(2/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	Realtime clock (RTC)	1 channel					
<R>	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode					
	Timer output	4 channels (PWM outputs: 3[Note 3]), 8 channels (PWM outputs: 7[Note 3])[Note 4]				5 channels (PWM outputs: 4[Note 3]), 8 channels (PWM outputs: 7[Note 3])[Note 4]	
	RTC output	1 channel					
Clock output/buzzer output		2					
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (f_{MAIN})) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (f_{SXP}))					
8-/10-/12-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels	10 channels	10 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[30- and 32-pin products] • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-, 40-, and 44-pin products] • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin products] • Simplified SPI (CSI): 2 channels/simplified I^2C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I^2C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel					
	UARTA	—		1 channel	1 channel	2 channels	2 channels
	I^2C bus	1 channel	1 channel	1 channel	1 channel	2 channels	2 channels
Remote control signal receiver		—	1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources	30 sources	32 sources	33 sources	35 sources	36 sources
Logic and event link controller (ELCL)		1					
SNOOZE mode sequencer (SMS)		1					
<R> Capacitive sensing unit	ROM size: 96 to 128 KB	2	3	5	6	6	8
	ROM size: 192 to 768 KB	6	7	11	13	14	16
Vectored interrupt sources	Internal	31	32	35	35	39	39
	External	6	6	6	7	7	10
Key interrupt		—	—	—	4	4	6

(3/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution[Note 5] • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)					
<R> Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)					
	LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)					
On-chip debugging		Available (tracing supported)					
Power supply voltage		V_{DD} = 1.6 to 5.5 V (2D: Consumer applications), V_{DD} = 1.8 to 5.5 V (3C: Industrial applications)					
Operating ambient temperature		T_A = -40 to +85°C (2D: Consumer applications), T_A = -40 to +105°C (3C: Industrial applications)					

Note 1. Overwrite the flash memory during operation at 2 MHz or a lower frequency.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G23 User's Manual.

Note 4. This applies when the setting of the PIOR0 bit is 1.

Note 5. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the in-circuit emulator or on-chip debugging emulator.

[52-, 64-, 80-, 100-, and 128-pin products]

Caution This outline describes the functions at the time when peripheral I/O redirection register (PIOR) is set to 00H.

(1/3)

Item		52-pin	64-pin	80-pin	100-pin	128-pin
		R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
Code flash memory		96 to 768 KB	96 to 768 KB	128 to 768 KB	128 to 768 KB	256 to 768 KB
Data flash memory		8 KB	8 KB	8 KB	8 KB	8 KB
RAM		12 to 48 KB	12 to 48 KB	16 to 48 KB	16 to 48 KB	24 to 48 KB
Address space		1 MB				
<R> CPU/ peripheral hardware clock frequency (f_{CLK})	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (V_{DD} = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz[Note 1] (V_{DD} = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (V_{DD} = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz[Note 1] (V_{DD} = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz[Note 2] (V_{DD} = 1.6 to 5.5 V)				
	Subsystem clock	SUB mode: 32.768 kHz (V_{DD} = 1.6 to 5.5 V)				
Main system clock	High-speed system clock (f_{MX})	1 to 20 MHz				
	High-speed on-chip oscillator clock (f_{IH})	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz 24 MHz, 32 MHz				
	Middle-speed on-chip oscillator clock (f_{IM})	1 MHz, 2 MHz, 4 MHz				
Subsystem clock	Subsystem clock X (f_{SX})	32.768 kHz (V_{DD} = 1.6 to 5.5 V)				
	Low-speed on-chip oscillator clock (f_{IL})	32.768 kHz (typ.)				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (f_{IH}))				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.				
I/O port	Total number of pins	48	58	74	92	120
	CMOS I/O	40 (N-ch open drain I/O [V_{DD} withstand voltage]: 15)	50 (N-ch open drain I/O [EV_{DD} withstand voltage]: 22[Note 6]/ 18[Note 7])	66 (N-ch open drain I/O [EV_{DD} withstand voltage]: 27)	84 (N-ch open drain I/O [EV_{DD} withstand voltage]: 31)	112 (N-ch open drain I/O [EV_{DD} withstand voltage]: 33)
	CMOS input	3	3	3	3	3
	CMOS output	1	1	1	1	1
	N-ch open drain I/O (withstand voltage: 6 V)	4	4	4	4	4
	Output current control port	8	8	8	8	8

(2/3)

Item		52-pin	64-pin	80-pin	100-pin	128-pin
		R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
Timers	16-bit timer	8 channels		12 channels		16 channels
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	<R> 32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode				
	Timer output	5 channels (PWM outputs: 4[Note 3]), 8 channels (PWM outputs: 7[Note 3])[Note 4]	8 channels (PWM outputs: 7[Note 3])	12 channels (PWM outputs: 10[Note 3])		16 channels (PWM outputs: 14[Note 3])
	RTC output	1 channel				
Clock output/buzzer output		2	2	2	2	2
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (f$_{MAIN}$)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (f$_{SXP}$))				
8-/10-/12-bit resolution A/D converter		12 channels	12 channels	17 channels	20 channels	26 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[52-pin products] • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I^{2}C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART (UART supporting LIN-bus): 1 channel [80-, 100-, and 128-pin products] • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified SPI (CSI): 2 channels/simplified I^{2}C: 2 channels/UART: 1 channel				
	UARTA	2 channels	2 channels	2 channels	2 channels	2 channels
	I^{2}C bus	2 channels	2 channels	2 channels	2 channels	2 channels
Remote control signal receiver		1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		36 sources	37 sources	39 sources		
Logic and event link controller (ELCL)		1				
SNOOZE mode sequencer (SMS)		1				

(3/3)

	Item		52-pin	64-pin	80-pin	100-pin	128-pin
			R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
<R>	Capacitive sensing unit	ROM size: 96 to 128 KB	10	12	30	32	32
		ROM size: 192 to 768 KB	20	22	30	32	32
	Vectored interrupt sources	Internal	39	39	44	44	48
		External	12	13	13	13	13
	Key interrupt		8	8	8	8	8
	Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution[Note 5] • Internal reset by RAM parity error • Internal reset by illegal-memory access				
	Power-on-reset circuit		Detection voltage • 1.50 V (typ.)				
<R>	Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)				
		LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)				
	On-chip debugging		Available (tracing supported)				
	Power supply voltage		V_{DD} = 1.6 to 5.5 V (2D: Consumer applications), V_{DD} = 1.8 to 5.5 V (3C: Industrial applications)				
	Operating ambient temperature		T_A = -40 to +85°C (2D: Consumer applications), T_A = -40 to +105°C (3C: Industrial applications)				

Note 1. Overwrite the flash memory during operation at 2 MHz or a lower frequency.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G23 User's Manual.

Note 4. This applies when the setting of the PIOR0 bit is 1.

Note 5. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the in-circuit emulator or on-chip debugging emulator.

Note 6. This only applies to the products with 96- and 128-Kbyte flash memory.

Note 7. This only applies to the products with 192- to 768-Kbyte flash memory.

2. Electrical Characteristics T_A = -40 to +105°C

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (1/2)

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.1 and -0.3 to V_{DD} + 0.3[Note 1]	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3[Note 2]	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V_{DD} + 0.3[Note 2]	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV_{DD0} + 0.3 and -0.3 to V_{DD} + 0.3[Note 2]	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to V_{DD} + 0.3[Note 2]	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to EV_{DD0} + 0.3 and -0.3 to AV_{REFP} + 0.3 [Notes 2, 3]	V
	V_{AI2}	ANI0 to ANI14	-0.3 to V_{DD} + 0.3 and -0.3 to AV_{REFP} + 0.3 [Notes 2, 3]	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AV_{REFP} + 0.3.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. AV_{REFP} refers to the positive reference voltage of the A/D converter.

Remark 3. The reference voltage is V_{SS}.

Absolute Maximum Ratings (2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121 to P124, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40[Note]	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121 to P124, P150 to P156	1	mA
		Total of all pins		5	mA
Ambient operating temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note The rating for the following port pins is 80 mA when I_{OL1} = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P110 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- <R> Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.2 Characteristics of the Oscillators

2.2.1 Characteristics of the X1 and XT1 oscillators

<R> (T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V (30- to 36-pin products), 1.6 V ≤ V_{DD} ≤ 5.5 V (40- to 128-pin products), V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time **Note**	Ceramic resonator/ crystal resonator		0.05		1	µs
XT1 clock oscillation frequency (f_{XT})**Note**	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

2.2.2 Characteristics of the On-chip Oscillators

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f_{IH}				1		32	MHz
High-speed on-chip oscillator clock frequency accuracy[Note 1]		HIPREC = 1	+85 to +105°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-2.0		+2.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ V_{DD} ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ V_{DD} ≤ 5.5 V	-5.5		+5.5	%
		HIPREC = 0[Note 4]			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%
Middle-speed on-chip oscillator clock frequency[Note 2]	f_{IM}				1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy[Note 1]					-12		+12	%
Middle-speed on-chip oscillator clock correction resolution						0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient							±0.17 **Note 3**	%/°C
Low-speed on-chip oscillator clock frequency[Note 2]	f_{IL}					32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy[Note 1]					-15		+15	%
Low-speed on-chip oscillator clock correction resolution						0.3		%
Low-speed on-chip oscillator frequency temperature coefficient							±0.21 **Note 3**	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 3. Guaranteed by characterization results.

Note 4. The listed condition applies when the setting of the FRQSEL3 bit is 1.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current **Note 1**	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-10.0 **Note 2**	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70%**Note 3**)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-55.0 **Note 4**	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70%**Note 3**)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-80.0 **Note 5**	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70%**Note 3**)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-135.0 **Note 6**	mA
	I_{OH2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0 **Note 2**	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0 **Note 2**	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0 **Note 2**	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5 **Note 2**	mA
		Total of all pins (when duty ≤ 70%**Note 3**)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EV_{DD0}, EV_{DD1}, or V_{DD} pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

•Total output current from the listed pins = (I_{OH} × 0.7)/(n × 0.01)
Example when n = 80% and I_{OH} = -10.0 mA
Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) ≅ -8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

(Notes, Caution, and Remark continue on the next page.)

<R> **Note 4.** The maximum value is -30 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

<R> **Note 5.** The maximum value is -50 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

<R> **Note 6.** The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of -40°C to 85°C and of 85°C to 105°C.

Caution The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.

P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current[Note 1]	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 **Notes 2, 3**	mA
		Per pin for P60 to P63				15.0 **Note 2**	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70%[Note 4])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			70.0 **Note 5**	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70%[Note 4])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			80.0 **Note 5**	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70%[Note 4])				150.0 **Note 6**	mA
	I_{OL2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5[Note 2]	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5[Note 2]	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6[Note 2]	mA
			1.6 V ≤ V_{DD} < 1.8 V			0.4[Note 2]	mA
		Total of all pins (when duty ≤ 70%[Note 4])	4.0 V ≤ V_{DD} ≤ 5.5 V			20	mA
			2.7 V ≤ V_{DD} < 4.0 V			20	mA
			1.8 V ≤ V_{DD} < 2.7 V			15	mA
			1.6 V ≤ V_{DD} < 1.8 V			10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EV_{SS0}, EV_{SS1}, or V_{SS} pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The maximum rating for the following port pins is 40 mA when I_{OL1} = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- <R> Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

(Notes and Remark continue on the next page.)

Note 4. The listed currents apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

•Total output current from the listed pins = (I_{OL} × 0.7)/(n × 0.01)
Example when n = 80% and I_{OL} = 10.0 mA
Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

<R> **Note 5.** The maximum value is 40 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

<R> **Note 6.** The maximum value is 80 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of 85°C to 105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	2.2		EV_{DD0}	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156		0.7 V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63		0.7 EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV_{DD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P156		0		0.3 V_{DD}	V
	V_{IL4}	P60 to P63		0		0.3 EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0}, even in the N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -10.0 mA	EV_{DD0} - 1.5			V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -3.0 mA	EV_{DD0} - 0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -2.0 mA	EV_{DD0} - 0.6			V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = -1.5 mA	EV_{DD0} - 0.5			V
			1.6 V ≤ EV_{DD0} < 5.5 V, I_{OH1} = -1.0 mA	EV_{DD0} - 0.5			V
	V_{OH2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OH2} = -1.0 mA	V_{DD} - 0.5			V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OH2} = -0.5 mA	V_{DD} - 0.5			V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high-level signals in the N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (5/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 20.0 mA			1.3	V
				I_{OL1} = 40.0 mA^{Note}			1.3	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 8.5 mA			0.7	V
				I_{OL1} = 17.0 mA^{Note}			0.7	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 3.0 mA			0.6	V
				I_{OL1} = 6.0 mA^{Note}			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 1.5 mA			0.4	V
				I_{OL1} = 3.0 mA^{Note}			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.6 mA			0.4	V
				I_{OL1} = 1.2 mA^{Note}			0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	I_{OL1} = 0.3 mA			0.4	V
				I_{OL1} = 0.6 mA^{Note}			0.4	V
	V_{OL2}	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 8.5 mA				0.7	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL2} = 1.5 mA				0.5	V
			1.8 V ≤ V_{DD} < 2.7 V, I_{OL2} = 0.6 mA				0.4	V
			1.6 V ≤ V_{DD} < 1.8 V, I_{OL2} = 0.4 mA				0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA				2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA				0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA				0.4	V
			1.8 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA				0.4	V
			1.6 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 1.0 mA				0.4	V

Note This setting applies to the following port pins.

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17, P51, and P70 of the 30- to 52-pin package products

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (6/7)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Output current[Note]	$CCDI_{OL}$	P16, P17, P50, P51 P60 to P63	CCSm = 01H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ EV_{DD0} < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ EV_{DD0} < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ EV_{DD0} < 4.0 V	6.0	9.1	12.1	mA
		P60 to P63	CCSm = 04H	4.0 V ≤ EV_{DD0} ≤ 5.5 V	10.2	15.0	19.8	mA
				3.3 V ≤ EV_{DD0} < 4.0 V	9.4	13.8	18.2	mA

Note The listed currents apply when the output current control function is enabled.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (7/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{DD0}			0.5	µA
	I_{LIH2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{DD}			0.5	µA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}			0.5	µA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV_{SS0}			0.5	µA
	I_{LIL2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	V_I = V_{SS}			0.5	µA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}			0.5	µA
On-chip pll-up resistance	R_U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120 to P122, P125 to P127, P140 to P147	V_I = EV_{SS0}, In input port	10	20	100	kΩ

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Supply current characteristics

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 2**	Basic operation	V_{DD} = 5.0 V		1.3	—	mA
						V_{DD} = 1.8 V		1.3	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		2.3	3.8	mA
						V_{DD} = 1.8 V		2.3	3.8	
				f_{IH} = 16 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		1.7	2.7	mA
						V_{DD} = 1.8 V		1.7	2.7	
				f_{IM} = 4 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		0.4	0.7	mA
						V_{DD} = 1.6 V		0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		200	325	μA
						V_{DD} = 1.6 V		200	325	
				f_{IM} = 1 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		112	178	μA
						V_{DD} = 1.6 V		111	176	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.8	3.0	mA
						V_{DD} = 1.8 V		1.7	3.0	
				f_{MX} = 20 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	
				f_{MX} = 10 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.6	mA
						V_{DD} = 1.8 V		0.9	1.6	
				f_{MX} = 10 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.7	mA
						V_{DD} = 1.8 V		1.0	1.7	
				f_{MX} = 8 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(Note and Remarks are listed on the next page.)

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz **Note 2**, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.2	5.5	μA
						T_A = +25°C		3.5	5.8	
						T_A = +50°C		3.8	8.5	
						T_A = +70°C		4.4	13.8	
						T_A = +85°C		5.3	22.1	
						T_A = +105°C		7.7	40.9	
				f_{SUB} = 32.768 kHz **Note 3**, Square wave input	Normal operation	T_A = -40°C		3.2	5.6	μA
						T_A = +25°C		3.4	5.7	
						T_A = +50°C		3.7	8.5	
						T_A = +70°C		4.3	13.7	
						T_A = +85°C		5.2	21.4	
						T_A = +105°C		7.6	39.0	
				f_{SUB} = 32.768 kHz **Note 3**, Resonator connection	Normal operation	T_A = -40°C		3.2	5.2	μA
						T_A = +25°C		3.4	5.4	
						T_A = +50°C		3.7	7.7	
						T_A = +70°C		4.3	13.4	
						T_A = +85°C		5.2	20.9	
						T_A = +105°C		7.7	38.5	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

<R> (TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current[Note 1]	IDD2[Note 2]	HALT mode	HS (high-speed main) mode	fIH = 32 MHz[Note 3]	VDD = 5.0 V		0.54	1.93	mA
					VDD = 1.8 V		0.53	1.92	
			LS (low-speed main) mode	fIH = 24 MHz[Note 3]	VDD = 5.0 V		0.45	1.50	mA
					VDD = 1.8 V		0.44	1.49	
				fIH = 16 MHz[Note 3]	VDD = 5.0 V		0.45	1.19	mA
					VDD = 1.8 V		0.44	1.18	
				fIM = 4 MHz[Note 4]	VDD = 5.0 V		0.08	0.26	mA
					VDD = 1.6 V		0.08	0.26	
			LP (low-power main) mode	fIM = 2 MHz[Note 4]	VDD = 5.0 V		33	120	µA
					VDD = 1.6 V		33	120	
				fIM = 1 MHz[Note 4]	VDD = 5.0 V		29	76	µA
					VDD = 1.6 V		28	74	
			HS (high-speed main) mode	fMX = 20 MHz[Note 5], Square wave input	VDD = 5.0 V		0.22	1.07	mA
					VDD = 1.8 V		0.19	1.03	
			LS (low-speed main) mode	fMX = 20 MHz[Note 5], Square wave input	VDD = 5.0 V		0.22	1.07	mA
					VDD = 1.8 V		0.19	1.03	
				fMX = 20 MHz[Note 5], Resonator connection	VDD = 5.0 V		0.40	1.28	mA
					VDD = 1.8 V		0.39	1.27	
				fMX = 10 MHz[Note 5], Square wave input	VDD = 5.0 V		0.14	0.57	mA
					VDD = 1.8 V		0.12	0.54	
				fMX = 10 MHz[Note 5], Resonator connection	VDD = 5.0 V		0.24	0.69	mA
					VDD = 1.8 V		0.23	0.68	
				fMX = 8 MHz[Note 5], Square wave input	VDD = 5.0 V		0.12	0.47	mA
					VDD = 1.8 V		0.10	0.44	
				fMX = 8 MHz[Note 5], Resonator connection	VDD = 5.0 V		0.21	0.58	mA
					VDD = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz**Note 3**, Low-speed on-chip oscillator operation	T_A = -40°C		0.53	2.31	μA
					T_A = +25°C		0.65	2.38	
					T_A = +50°C		0.80	4.95	
					T_A = +70°C		1.17	9.97	
					T_A = +85°C		1.78	17.96	
					T_A = +105°C		4.41	37.71	
				f_{SUB} = 32.768 kHz, Square wave input **Note 4**	T_A = -40°C		0.20	1.97	μA
					T_A = +25°C		0.29	2.00	
					T_A = +50°C		0.54	5.33	
					T_A = +70°C		0.99	10.94	
					T_A = +85°C		1.70	19.62	
					T_A = +105°C		4.10	41.82	
				f_{SUB} = 32.768 kHz, Resonator connection **Note 5**	T_A = -40°C		0.21	2.04	μA
					T_A = +25°C		0.33	2.28	
					T_A = +50°C		0.49	4.98	
					T_A = +70°C		1.05	11.36	
					T_A = +85°C		1.76	20.04	
					T_A = +105°C		4.20	42.52	
	I_{DD3}	STOP mode	RAMSDS = 0**Note 6**		T_A = -40°C		0.15	1.45	μA
					T_A = +25°C		0.23	1.45	
					T_A = +50°C		0.45	4	
					T_A = +70°C		0.9	9	
					T_A = +85°C		1.6	17	
					T_A = +105°C		4	35	
			RAMSDS = 1**Note 7**		T_A = -40°C		0.14	1.45	μA
					T_A = +25°C		0.21	1.45	
					T_A = +50°C		0.4	3.5	
					T_A = +70°C		0.8	8.5	
					T_A = +85°C		1.4	15	
					T_A = +105°C		3.2	30	
			RAMSDS = 1, 128-Hz realtime clock operation**Note 8**		T_A = -40°C		0.22	1.53	μA
					T_A = +25°C		0.32	1.56	
					T_A = +50°C		0.53	3.62	
					T_A = +70°C		0.94	8.64	
					T_A = +85°C		1.55	15.15	
					T_A = +105°C		3.40	30.20	

(Notes and Remarks are listed on the next page.)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz **Note 2**	Basic operation	V_{DD} = 5.0 V		1.4	—	mA
						V_{DD} = 1.8 V		1.4	—	
					Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 1.8 V		3.0	5.0	
			LS (low-speed main) mode	f_{IH} = 24 MHz **Note 2**	Normal operation	V_{DD} = 5.0 V		2.3	3.8	mA
						V_{DD} = 1.8 V		2.3	3.8	
				f_{IH} = 16 MHz **Note 2**	Normal operation	V_{DD} = 5.0 V		1.7	2.8	mA
						V_{DD} = 1.8 V		1.7	2.7	
				f_{IM} = 4 MHz **Note 3**	Normal operation	V_{DD} = 5.0 V		0.4	0.7	mA
						V_{DD} = 1.6 V		0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz **Note 3**	Normal operation	V_{DD} = 5.0 V		203	329	μA
						V_{DD} = 1.6 V		202	328	
				f_{IM} = 1 MHz **Note 3**	Normal operation	V_{DD} = 5.0 V		115	181	μA
						V_{DD} = 1.6 V		114	180	
			HS (high-speed main) mode	f_{MX} = 20 MHz **Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	
			LS (low-speed main) mode	f_{MX} = 20 MHz **Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.8	3.0	mA
						V_{DD} = 1.8 V		1.7	3.0	
				f_{MX} = 20 MHz **Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.9	3.2	mA
						V_{DD} = 1.8 V		1.9	3.2	
				f_{MX} = 10 MHz **Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.6	mA
						V_{DD} = 1.8 V		0.9	1.6	
				f_{MX} = 10 MHz **Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.7	mA
						V_{DD} = 1.8 V		1.0	1.7	
				f_{MX} = 8 MHz **Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.8	1.3	mA
						V_{DD} = 1.8 V		0.7	1.3	
				f_{MX} = 8 MHz **Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		0.9	1.4	mA
						V_{DD} = 1.8 V		0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(Note and Remarks are listed on the next page.)

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz**Note 2**, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.3	6.1	μA
						T_A = +25°C		3.6	6.3	
						T_A = +50°C		3.9	9.6	
						T_A = +70°C		4.5	15.9	
						T_A = +85°C		5.4	25.3	
						T_A = +105°C		7.8	56.3	
				f_{SUB} = 32.768 kHz**Note 3**, Square wave input	Normal operation	T_A = -40°C		3.3	6.1	μA
						T_A = +25°C		3.5	6.4	
						T_A = +50°C		3.8	9.6	
						T_A = +70°C		4.4	16.1	
						T_A = +85°C		5.3	26.4	
						T_A = +105°C		7.8	57.0	
				f_{SUB} = 32.768 kHz**Note 3**, Resonator connection	Normal operation	T_A = -40°C		3.3	6.0	μA
						T_A = +25°C		3.5	6.0	
						T_A = +50°C		3.8	8.9	
						T_A = +70°C		4.4	15.3	
						T_A = +85°C		5.3	25.6	
						T_A = +105°C		7.9	55.3	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current**Note 1**	I_{DD2} **Note 2**	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 3**	V_{DD} = 5.0 V		0.57	1.97	mA
					V_{DD} = 1.8 V		0.56	1.96	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 3**	V_{DD} = 5.0 V		0.47	1.53	mA
					V_{DD} = 1.8 V		0.47	1.52	
				f_{IH} = 16 MHz**Note 3**	V_{DD} = 5.0 V		0.48	1.22	mA
					V_{DD} = 1.8 V		0.47	1.21	
				f_{IM} = 4 MHz**Note 4**	V_{DD} = 5.0 V		0.08	0.27	mA
					V_{DD} = 1.6 V		0.08	0.26	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 4**	V_{DD} = 5.0 V		38	126	µA
					V_{DD} = 1.6 V		37	125	
				f_{IM} = 1 MHz**Note 4**	V_{DD} = 5.0 V		32	79	µA
					V_{DD} = 1.6 V		32	79	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.23	1.07	mA
					V_{DD} = 1.8 V		0.19	1.03	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.23	1.07	mA
					V_{DD} = 1.8 V		0.19	1.03	
				f_{MX} = 20 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.41	1.30	mA
					V_{DD} = 1.8 V		0.40	1.28	
				f_{MX} = 10 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.14	0.57	mA
					V_{DD} = 1.8 V		0.12	0.54	
				f_{MX} = 10 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.24	0.69	mA
					V_{DD} = 1.8 V		0.23	0.68	
				f_{MX} = 8 MHz**Note 5**, Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz**Note 5**, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD2} **Note 2**	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz**Note 3**, Low-speed on-chip oscillator operation	T_A = -40°C		0.62	2.94	μA
					T_A = +25°C		0.74	3.00	
					T_A = +50°C		0.88	6.00	
					T_A = +70°C		1.22	12.01	
					T_A = +85°C		2.69	22.92	
					T_A = +105°C		5.08	54.47	
				f_{SUB} = 32.768 kHz, Square wave input **Note 4**	T_A = -40°C		0.25	2.54	μA
					T_A = +25°C		0.37	2.73	
					T_A = +50°C		0.74	7.35	
					T_A = +70°C		1.33	15.13	
					T_A = +85°C		2.35	27.33	
					T_A = +105°C		4.81	62.95	
				f_{SUB} = 32.768 kHz, Resonator connection **Note 5**	T_A = -40°C		0.27	2.68	μA
					T_A = +25°C		0.39	2.87	
					T_A = +50°C		0.78	7.63	
					T_A = +70°C		1.34	15.20	
					T_A = +85°C		2.35	27.33	
					T_A = +105°C		4.67	61.97	
	I_{DD3}	STOP mode	RAMSDS = 0**Note 6**		T_A = -40°C		0.19	2.00	μA
					T_A = +25°C		0.30	2.00	
					T_A = +50°C		0.65	5.00	
					T_A = +70°C		1.20	11.00	
					T_A = +85°C		2.20	20.00	
					T_A = +105°C		4.50	50.00	
			RAMSDS = 1**Note 7**		T_A = -40°C		0.18	2.00	μA
					T_A = +25°C		0.29	2.00	
					T_A = +50°C		0.60	4.50	
					T_A = +70°C		1.10	10.00	
					T_A = +85°C		2.00	19.00	
					T_A = +105°C		4.00	45.00	
			RAMSDS = 1, 128-Hz realtime clock operation**Note 8**		T_A = -40°C		0.23	2.05	μA
					T_A = +25°C		0.40	2.11	
					T_A = +50°C		0.72	4.62	
					T_A = +70°C		1.23	10.13	
					T_A = +85°C		2.14	19.14	
					T_A = +105°C		4.16	45.16	

(Notes and Remarks are listed on the next page.)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz**Note 2**	Basic operation	V_{DD} = 5.0 V		1.6	—	mA
						V_{DD} = 1.8 V		1.5	—	
					Normal operation	V_{DD} = 5.0 V		3.5	5.6	mA
						V_{DD} = 1.8 V		3.5	5.6	
			LS (low-speed main) mode	f_{IH} = 24 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		2.6	4.2	mA
						V_{DD} = 1.8 V		2.6	4.2	
				f_{IH} = 16 MHz**Note 2**	Normal operation	V_{DD} = 5.0 V		2.0	3.1	mA
						V_{DD} = 1.8 V		1.9	3.1	
				f_{IM} = 4 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		0.5	0.9	mA
						V_{DD} = 1.6 V		0.5	0.8	
			LP (low-power main) mode	f_{IM} = 2 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		229	361	μA
						V_{DD} = 1.6 V		227	358	
				f_{IM} = 1 MHz**Note 3**	Normal operation	V_{DD} = 5.0 V		128	197	μA
						V_{DD} = 1.6 V		125	193	
			HS (high-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		2.2	3.5	mA
						V_{DD} = 1.8 V		2.2	3.5	
			LS (low-speed main) mode	f_{MX} = 20 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		2.1	3.4	mA
						V_{DD} = 1.8 V		2.0	3.3	
				f_{MX} = 20 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		2.2	3.6	mA
						V_{DD} = 1.8 V		2.2	3.5	
				f_{MX} = 10 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		1.1	1.8	mA
						V_{DD} = 1.8 V		1.1	1.8	
				f_{MX} = 10 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.2	1.9	mA
						V_{DD} = 1.8 V		1.2	1.9	
				f_{MX} = 8 MHz**Note 4**, Square wave input	Normal operation	V_{DD} = 5.0 V		0.9	1.5	mA
						V_{DD} = 1.8 V		0.9	1.5	
				f_{MX} = 8 MHz**Note 4**, Resonator connection	Normal operation	V_{DD} = 5.0 V		1.0	1.6	mA
						V_{DD} = 1.8 V		1.0	1.6	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current **Note 1**	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz**Note 2**, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.8	7.7	μA
						T_A = +25°C		4.1	8.0	
						T_A = +50°C		4.6	13.5	
						T_A = +70°C		5.6	24.0	
						T_A = +85°C		7.1	40.8	
						T_A = +105°C		11.1	88.8	
				f_{SUB} = 32.768 kHz**Note 3**, Square wave input	Normal operation	T_A = -40°C		3.8	7.7	μA
						T_A = +25°C		4.0	8.0	
						T_A = +50°C		4.5	13.6	
						T_A = +70°C		5.3	24.1	
						T_A = +85°C		6.7	40.3	
						T_A = +105°C		10.7	88.1	
				f_{SUB} = 32.768 kHz**Note 3**, Resonator connection	Normal operation	T_A = -40°C		3.8	7.4	μA
						T_A = +25°C		4.1	7.8	
						T_A = +50°C		4.5	12.6	
						T_A = +70°C		5.4	24.2	
						T_A = +85°C		6.8	39.8	
						T_A = +105°C		10.8	87.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current[Note 1]	I_{DD2} [Note 2]	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz[Note 3]	V_{DD} = 5.0 V		0.60	2.00	mA
					V_{DD} = 1.8 V		0.59	1.99	
			LS (low-speed main) mode	f_{IH} = 24 MHz[Note 3]	V_{DD} = 5.0 V		0.49	1.56	mA
					V_{DD} = 1.8 V		0.48	1.55	
				f_{IH} = 16 MHz[Note 3]	V_{DD} = 5.0 V		0.49	1.24	mA
					V_{DD} = 1.8 V		0.48	1.23	
				f_{IM} = 4 MHz[Note 4]	V_{DD} = 5.0 V		0.09	0.28	mA
					V_{DD} = 1.6 V		0.09	0.27	
			LP (low-power main) mode	f_{IM} = 2 MHz[Note 4]	V_{DD} = 5.0 V		40	129	µA
					V_{DD} = 1.6 V		37	125	
				f_{IM} = 1 MHz[Note 4]	V_{DD} = 5.0 V		33	80	µA
					V_{DD} = 1.6 V		32	79	
			HS (high-speed main) mode	f_{MX} = 20 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.25	1.10	mA
					V_{DD} = 1.8 V		0.21	1.05	
			LS (low-speed main) mode	f_{MX} = 20 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.25	1.10	mA
					V_{DD} = 1.8 V		0.21	1.05	
				f_{MX} = 20 MHz[Note 5], Resonator connection	V_{DD} = 5.0 V		0.41	1.30	mA
					V_{DD} = 1.8 V		0.40	1.28	
				f_{MX} = 10 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.15	0.59	mA
					V_{DD} = 1.8 V		0.13	0.55	
				f_{MX} = 10 MHz[Note 5], Resonator connection	V_{DD} = 5.0 V		0.25	0.70	mA
					V_{DD} = 1.8 V		0.24	0.69	
				f_{MX} = 8 MHz[Note 5], Square wave input	V_{DD} = 5.0 V		0.13	0.48	mA
					V_{DD} = 1.8 V		0.11	0.45	
				f_{MX} = 8 MHz[Note 5], Resonator connection	V_{DD} = 5.0 V		0.22	0.59	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current [Note 1]	I_{DD2} [Note 2]	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz[Note 3], Low-speed on-chip oscillator operation	T_A = -40°C		0.62	3.95	μA
					T_A = +25°C		0.78	4.00	
					T_A = +50°C		1.03	9.16	
					T_A = +70°C		1.62	19.34	
					T_A = +85°C		3.50	37.35	
					T_A = +105°C		6.77	85.36	
				f_{SUB} = 32.768 kHz, Square wave input [Note 4]	T_A = -40°C		0.25	3.55	μA
					T_A = +25°C		0.41	3.73	
					T_A = +50°C		0.90	10.93	
					T_A = +70°C		1.76	23.42	
					T_A = +85°C		2.92	41.07	
					T_A = +105°C		6.27	94.30	
				f_{SUB} = 32.768 kHz, Resonator connection [Note 5]	T_A = -40°C		0.27	3.62	μA
					T_A = +25°C		0.43	3.87	
					T_A = +50°C		0.92	11.07	
					T_A = +70°C		1.79	23.63	
					T_A = +85°C		2.94	41.21	
					T_A = +105°C		6.28	94.37	
	I_{DD3}	STOP mode	RAMSDS = 0[Note 6]		T_A = -40°C		0.21	3.00	μA
					T_A = +25°C		0.35	3.00	
					T_A = +50°C		0.75	8.00	
					T_A = +70°C		1.60	18.00	
					T_A = +85°C		2.80	34.00	
					T_A = +105°C		6.00	80.00	
			RAMSDS = 1[Note 7]		T_A = -40°C		0.19	3.00	μA
					T_A = +25°C		0.32	3.00	
					T_A = +50°C		0.65	7.00	
					T_A = +70°C		1.25	17.00	
					T_A = +85°C		2.10	30.00	
					T_A = +105°C		4.50	70.00	
			RAMSDS = 1, 128-Hz realtime clock operation[Note 8]		T_A = -40°C		0.27	3.08	μA
					T_A = +25°C		0.42	3.10	
					T_A = +50°C		0.76	7.11	
					T_A = +70°C		1.38	17.13	
					T_A = +85°C		2.23	30.13	
					T_A = +105°C		4.64	70.14	

(Notes and Remarks are listed on the next page.)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM.

The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(4) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

	Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
<R>	High-speed on-chip oscillator operating current	I_{FIH} Note 1	HIPREC = 1			240	—	µA
<R>			HIPREC = 0			380	—	µA
	Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20	—	µA
	Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3	—	µA
	RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005	—	µA
			f_{RTCCLK} = 128 Hz			0.002	—	µA
	32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04	—	µA
	Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32	—	µA
	A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
				Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.75	mA
	AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			52	—	µA
	A/D converter internal reference voltage current	I_{ADREF} Note 1				114	—	µA
	Temperature sensor operating current	I_{TMPS} Note 1				110	—	µA
	D/A converter operating current	I_{DAC} Notes 1, 8	Per channel			150	—	µA
	Comparator operating current	I_{CMP} Notes 1, 9				6	—	µA
	LVD operating current	I_{LVD0} Notes 1, 10				0.02	—	µA
		I_{LVD1} Notes 1, 10				0.02	—	µA
	Self-programming operating current	I_{FSP} Notes 1, 11				2.5	12.2	mA
	Data flash rewrite operating current	I_{BGO} Notes 1, 12				2.5	12.2	mA

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

	Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
<R>	SNOOZE mode sequencer operating current	I_{SMS} **Notes 1, 13**	f_{IH} = 32 MHz		30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.1	—	mA
					30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.1	—	
					44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.4	—	
			f_{IL} = 32.768 kHz		30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.2	—	µA
					30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.2	—	
					44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.6	—	
<R>	SNOOZE operating current	I_{SNOZ} **Note 1**	f_{IH}=32 MHz	ADC to be in use	The ADC is shifting from the STOP mode to the SNOOZE mode. **Note 14**		0.6	0.81	mA
					The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		1.2	1.56	
				Simplified SPI (CSI)/UART to be in use			0.7	0.92	mA
				SMS **Note 19**	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.6	—	mA
					30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.7	—	
					44- to 80-pin package products with 384- to 768-Kbyte flash ROM, and 100- to 128-pin package products		2.0	—	
	Remote control signal receiver operating current	I_{REM} **Notes 1, 15**					0.03	—	µA
	Low-speed peripheral clock supply current	I_{SXP} **Notes 1, 16**	RTCLPC = 0				0.22	—	µA
	Output current control operating current	I_{CCDA} **Notes 1, 17**	The setting of the CCDE register is not 00H.				100	—	µA
		I_{CCDP} **Notes 1, 18**	Per single output current control port		Setting of the low-level output current: Hi-Z		30	—	µA
					Setting of the low-level output current: 2 to 15 mA		200	—	µA
<R>	Operating current of the true random number generator	I_{TRNG} **Note 1**					1.1	—	mA

(Notes and Remarks continue on the next page.)

Note 1. This current flows into V_{DD}.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{RTC}, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current. I_{DD2} in the subsystem clock operation mode includes the operating current of the realtime clock.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 5. This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is operating.

Note 6. This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter is operating or in the HALT mode.

Note 7. This current flows into AV_{REFP}.

Note 8. This current only flows to the D/A converter.
The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{DAC}, when the D/A converter is operating or in the HALT mode.

Note 9. This current only flows to the comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Note 10. This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

Note 11. This current only flows during self programming.

Note 12. This current only flows while the data flash memory is being rewritten.

<R> **Note 13.** This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{SMS}, when the SNOOZE mode sequencer is operating or in the HALT mode.

<R> **Note 14.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G23 User's Manual.

Note 15. This current flows into the remote control signal receiver. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the remote control signal receiver is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

<R> **Note 16.** This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the subsystem clock X (f_{SX}) selected as the CPU clock, while the subsystem clock X (fsx) is oscillating.

Note 17. This current is added to the supply current when the output voltage control port is set.

Note 18. This current does not include the current flowing into the I/O port pins.

<R> **Note 19.** The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to I_{DD1}. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SX}: Subsystem clock X frequency

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

2.4 AC Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.25		1	μs
			LP (low-power main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.5		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ V_{DD} ≤ 1.8 V	0.5		1	μs
External system clock frequency	f_{EX}	1.8 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		38.4	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	1.8 V ≤ V_{DD} ≤ 5.5 V			15			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}				$1/f_{MCK}$ + 10			ns**Note**
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	HS (high-speed main) mode LS (low-speed main) mode		4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ EV_{DD0} ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode LS (low-speed main) mode		4.0 V ≤ EV_{DD0} ≤ 5.5 V			16	MHz
				2.7 V ≤ EV_{DD0} < 4.0 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		LP (low-power main) mode		1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
		INTP1 to INTP11		1.6 V ≤ EV_{DD0} ≤ 5.5 V	1			μs
Key interrupt input low-level width	t_{KRH}, t_{KRL}	KR0 to KR7		1.8 V ≤ EV_{DD0} ≤ 5.5 V	250			ns
				1.6 V ≤ EV_{DD0} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

(Note and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$1.8 \text{ V} \leq EV_{DD0} < 2.7 \text{ V}$: 125 ns min.

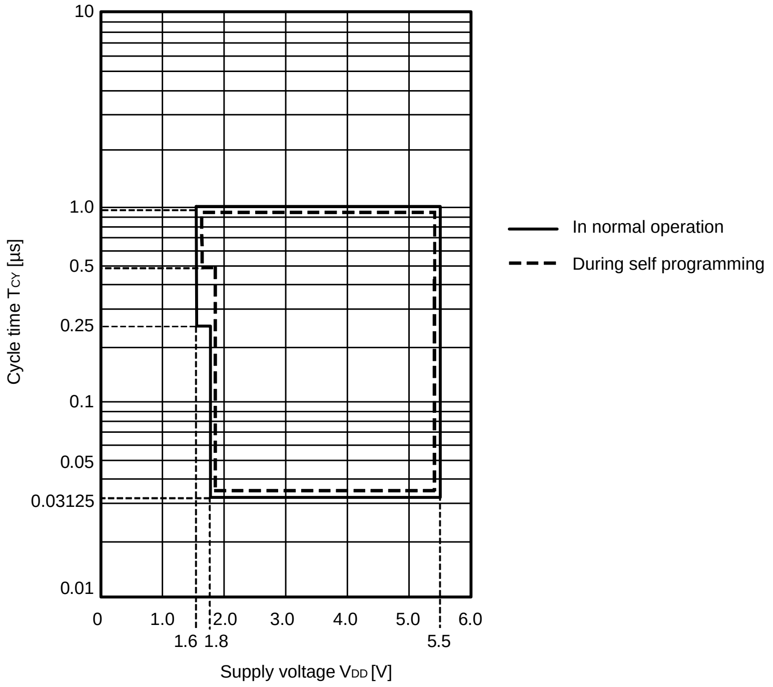
$1.6 \text{ V} \leq EV_{DD0} < 1.8 \text{ V}$: 250 ns min.

Remark f_{MCK}: Timer array unit operating clock frequency

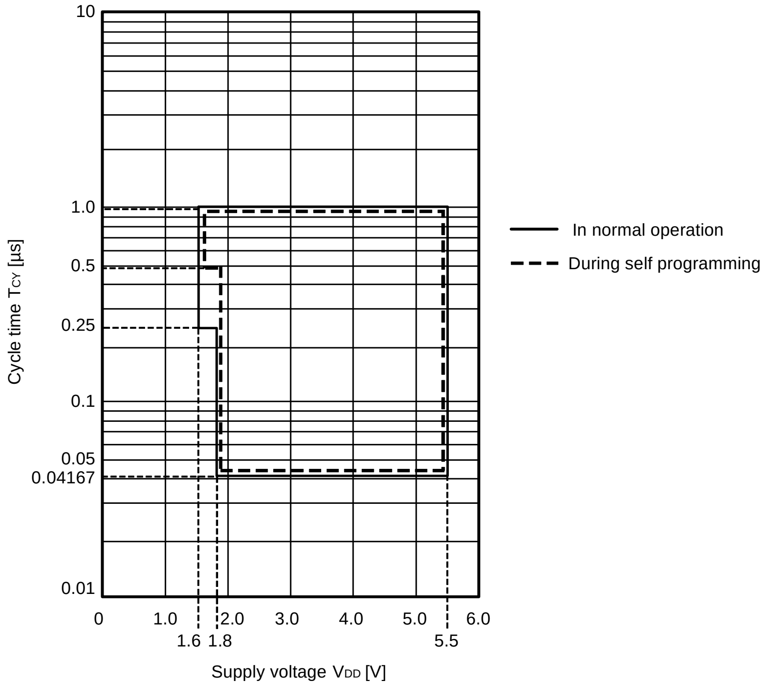
(To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn) (m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3).)

Minimum Instruction Execution Time during Main System Clock Operation

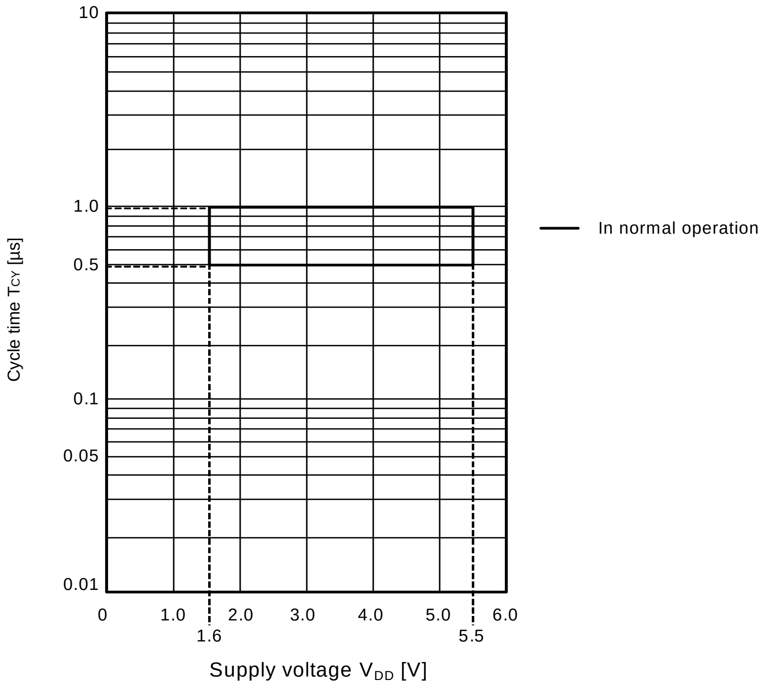
T_{CY} vs V_{DD} (HS (high-speed main) mode)



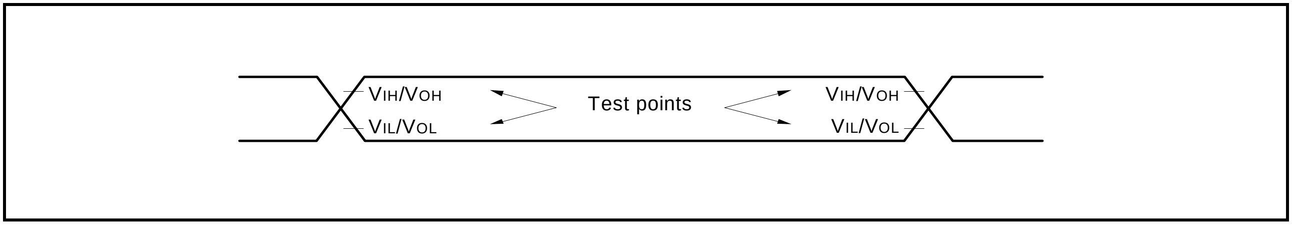
T_{CY} vs V_{DD} (LS (low-speed main) mode)



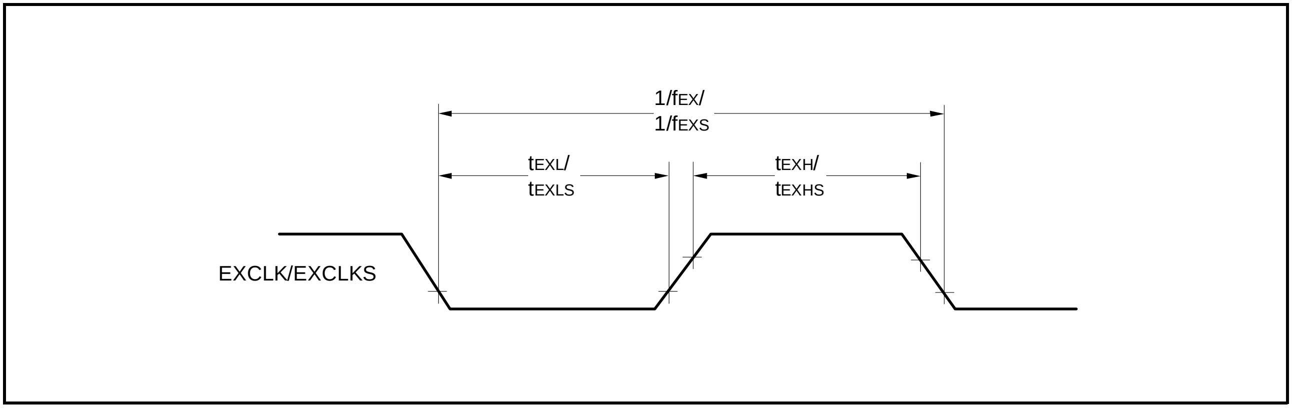
TCY vs VDD (LP (low-power main) mode)



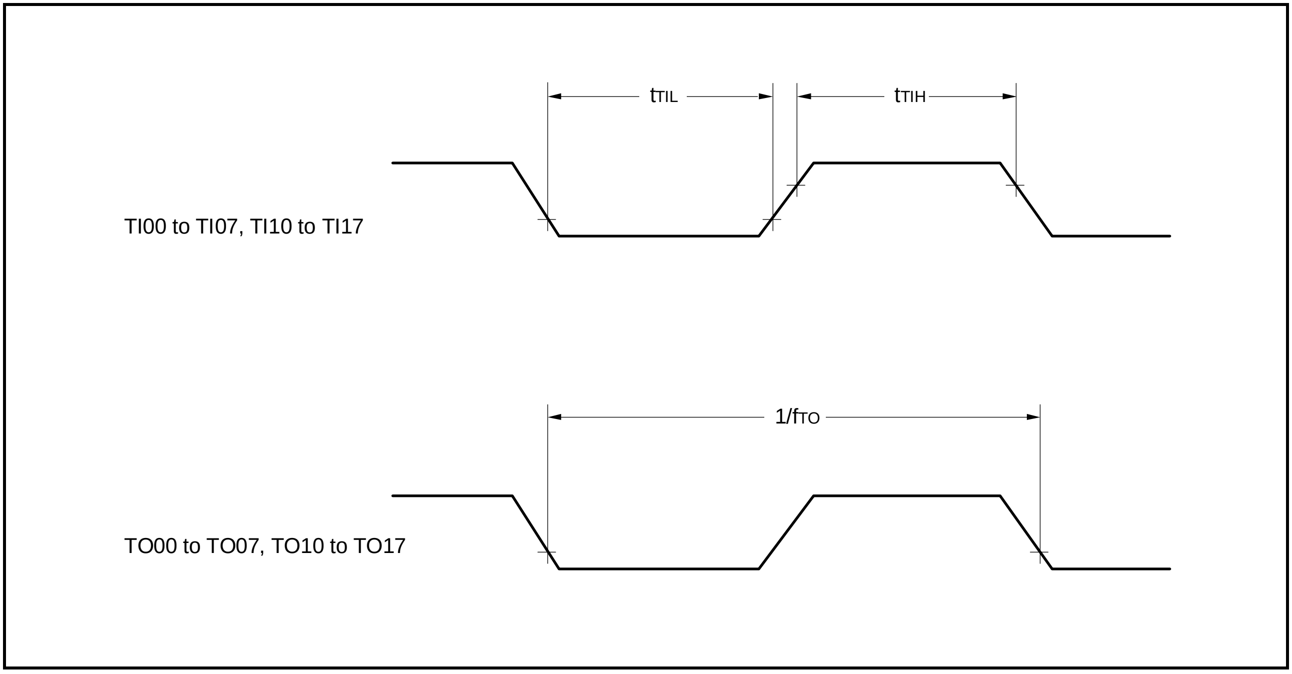
AC Timing Test Points


VIH/VOH
VIL/VOL
Test points
VIH/VOH
VIL/VOL

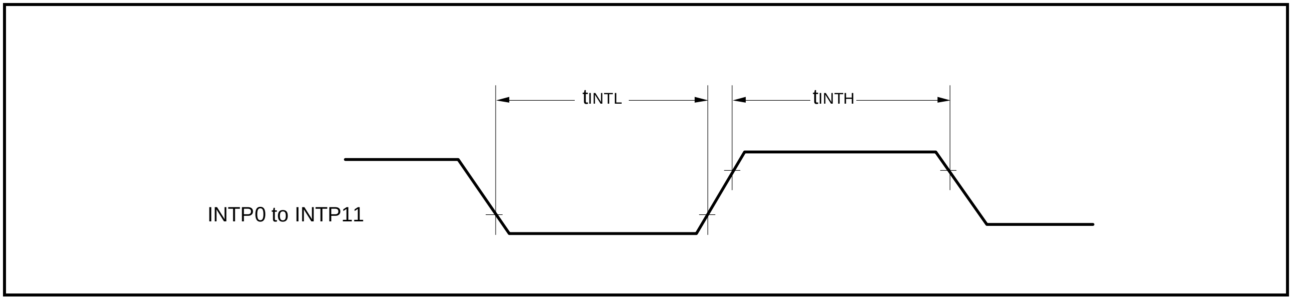
External System Clock Timing


1/fEX/
1/fEXS
tEXL/
tEXLS
tEXH/
tEXHS
EXCLK/EXCLKS

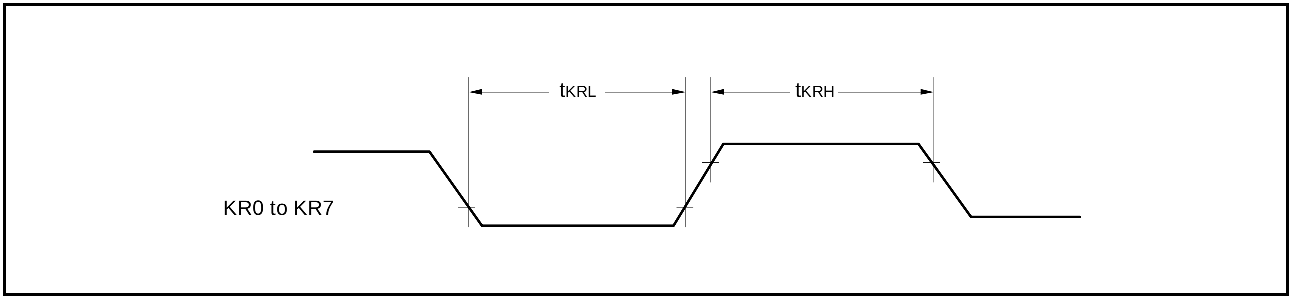
TI/TO Timing


tTIL
tTIH
TI00 to TI07, TI10 to TI17
1/fTO
TO00 to TO07, TO10 to TO17

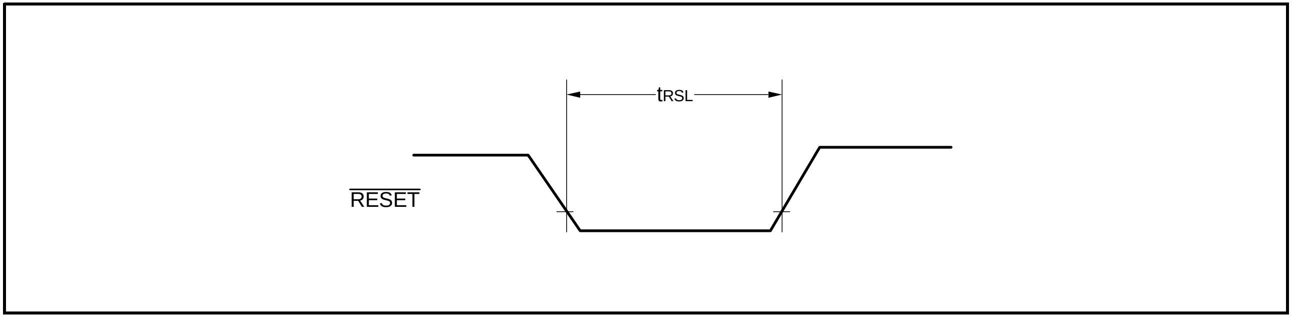
Interrupt Request Input Timing


t_{INTL}
t_{INTH}
INTP0 to INTP11

Key Interrupt Input Timing

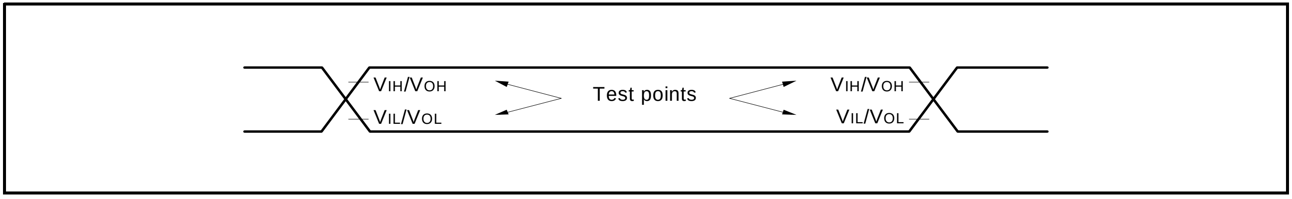

t_{KRL}
t_{KRH}
KR0 to KR7

$\overline{\text{RESET}}$ Input Timing


t_{RSL}
$\overline{\text{RESET}}$

2.5 Characteristics of the Peripheral Functions

AC Timing Test Points



2.5.1 Serial array unit

(1) In UART communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate **Note 1**		1.6 V ≤ EV_{DD0} ≤ 5.5 V		$f_{MCK}/6$ **Note 2**		$f_{MCK}/6$ **Note 2**		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 3**		5.3		4		0.33	Mbps

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

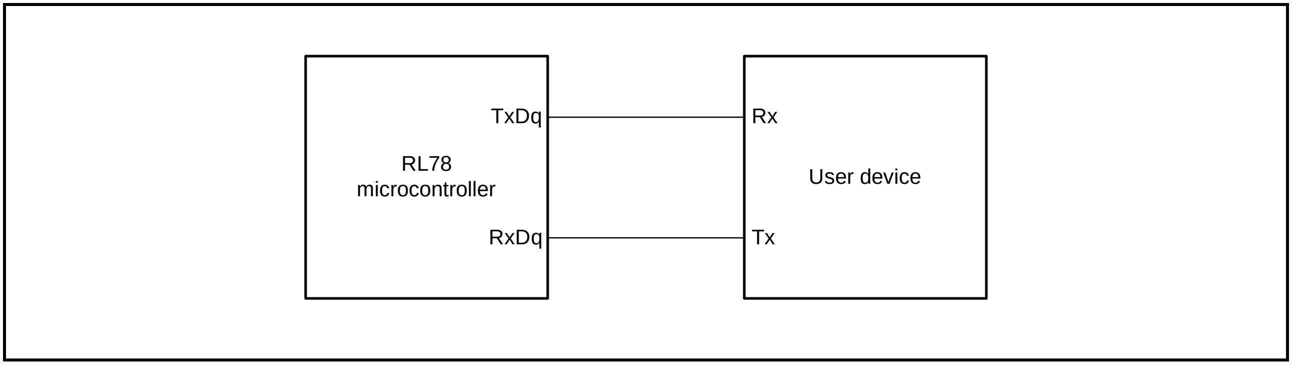
2.4 V ≤ EV_{DD0} < 2.7 V: 2.6 Mbps max.
1.8 V ≤ EV_{DD0} < 2.4 V: 1.3 Mbps max.
1.6 V ≤ EV_{DD0} < 1.8 V: 0.6 Mbps max.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are as follows.

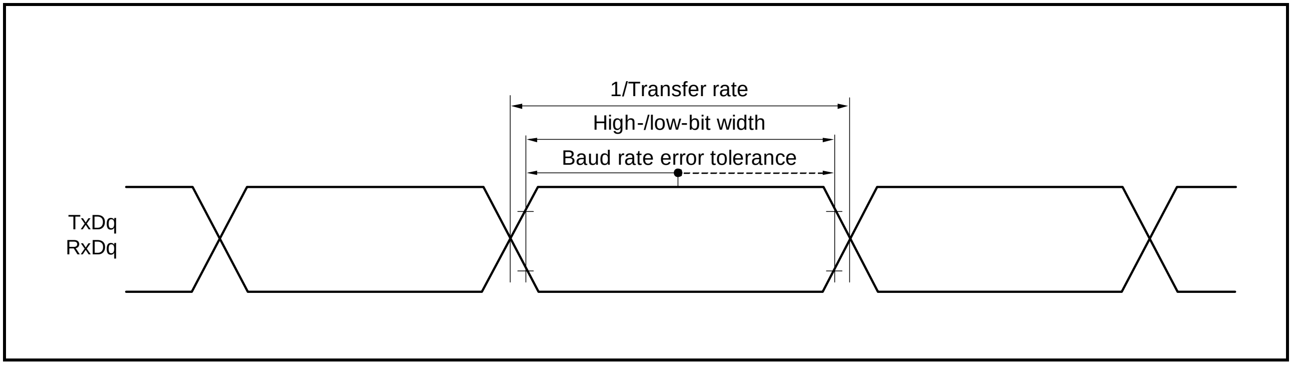
HS (high-speed main) mode: 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LS (low-speed main) mode: 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)
4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)
LP (low-power main) mode: 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Connection in the UART communications with devices operating at same voltage levels


RL78
microcontroller
TxDq
RxDq
Rx
Tx
User device

Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)


1/Transfer rate
High-/low-bit width
Baud rate error tolerance
TxDq
RxDq

Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

(To set this operating clock, set the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13).)

(2) In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 2/f_{CLK}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	62.5		83.3		1000		ns
			2.7 V ≤ EV_{DD0} ≤ 5.5 V	83.3		125		1000		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		$t_{KCY1}/2$ - 7		$t_{KCY1}/2$ - 10		$t_{KCY1}/2$ - 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		$t_{KCY1}/2$ - 10		$t_{KCY1}/2$ - 15		$t_{KCY1}/2$ - 50		ns
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		23		33		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		33		50		110		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp outputNote 2	t_{KSO1}	C = 20 pFNote 3			10		10		10	ns

Note 1. The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes "to SCKp↓" and that for the SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00).)

(3) In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	125		166		2000		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	250		250		2000		ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	500		500		2000		ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V	1000		1000		2000		ns
SCKp high-/ low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 12		t_{KCY1}/2 - 21		t_{KCY1}/2 - 50		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 18		t_{KCY1}/2 - 25		t_{KCY1}/2 - 50		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 38		t_{KCY1}/2 - 38		t_{KCY1}/2 - 50		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		t_{KCY1}/2 - 100		ns
SIp setup time (to SCKp↑)**Note 1**	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		44		54		110		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		44		54		110		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		75		75		110		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		110		110		110		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		220		220		220		ns
SIp hold time (from SCKp↑) **Note 1**	t_{KSI1}	1.6 V ≤ EV_{DD0} ≤ 5.5 V		19		19		19		ns
Delay time from SCKp↓ to SOp output**Note 2**	t_{KSO1}	1.6 V ≤ EV_{DD0} ≤ 5.5 V C = 30 pF**Note 3**			25		25		25	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes "to SCKp↓" and that for the SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

(4) In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time **Note 4**	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/ low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		t_{KCY2}/2 - 7		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		t_{KCY2}/2 - 8		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		t_{KCY2}/2 - 66		ns

(Notes, Caution, and Remarks are listed on the next page.)

(4) In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↑) **Note 1**	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 40		1/f_{MCK} + 40		1/f_{MCK} + 40		ns
SIp hold time (from SCKp↑) **Note 1**	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK} + 250		1/f_{MCK} + 250		1/f_{MCK} + 250		ns
Delay time from SCKp↓ to SOp output **Note 2**	t_{KSO2}	C = 30 pF **Note 3**	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 44		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 75		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 110		2/f_{MCK} + 110		2/f_{MCK} + 110	ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK} + 220		2/f_{MCK} + 220		2/f_{MCK} + 220	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the SIp setup time becomes “to SCKp↓” and that for the SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SOp output line.

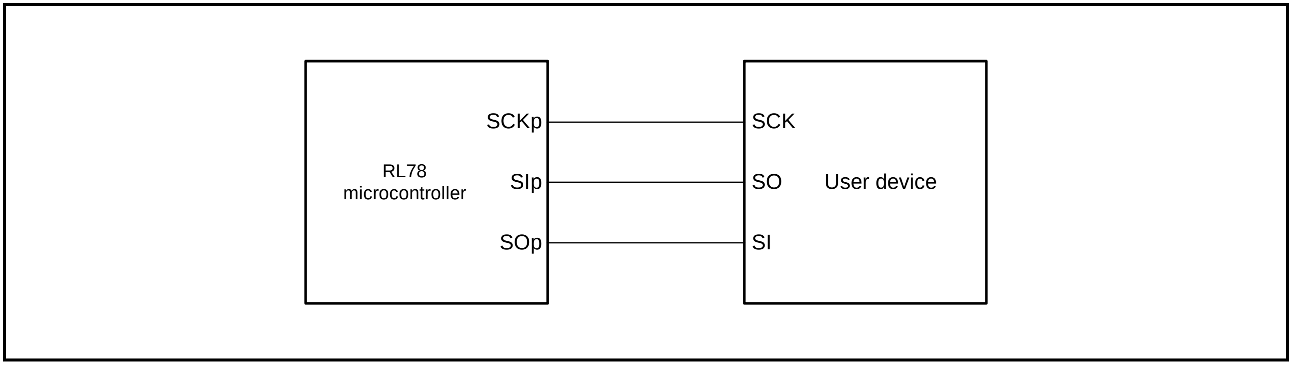
Note 4. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

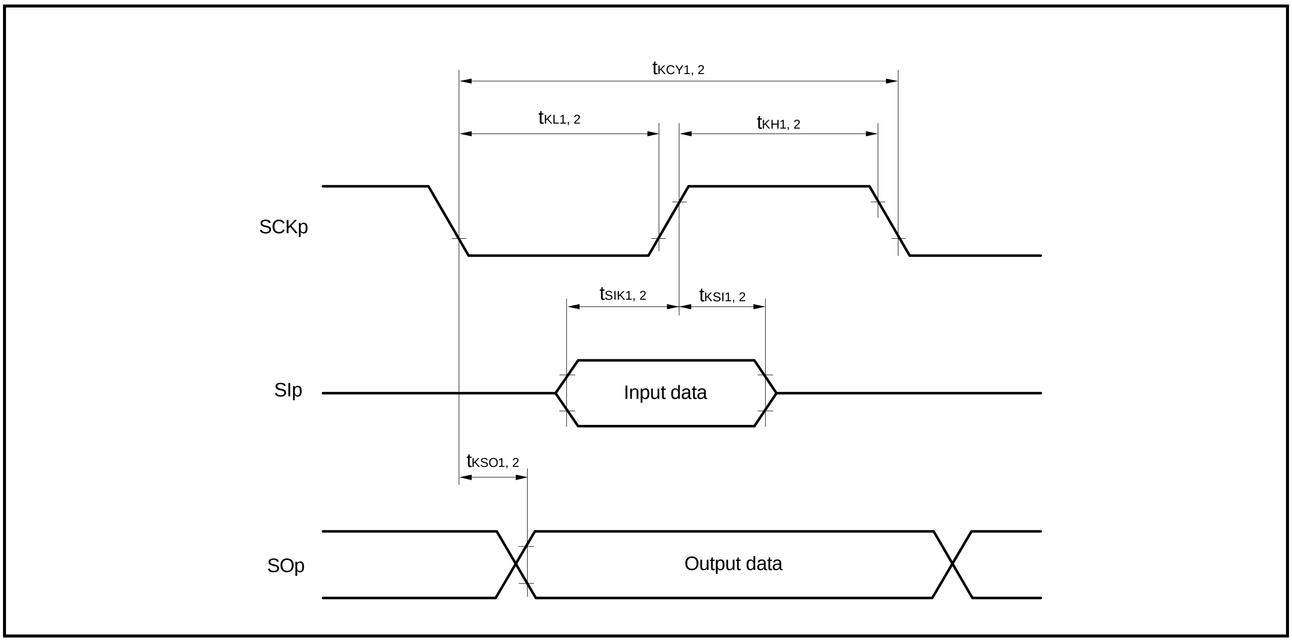
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

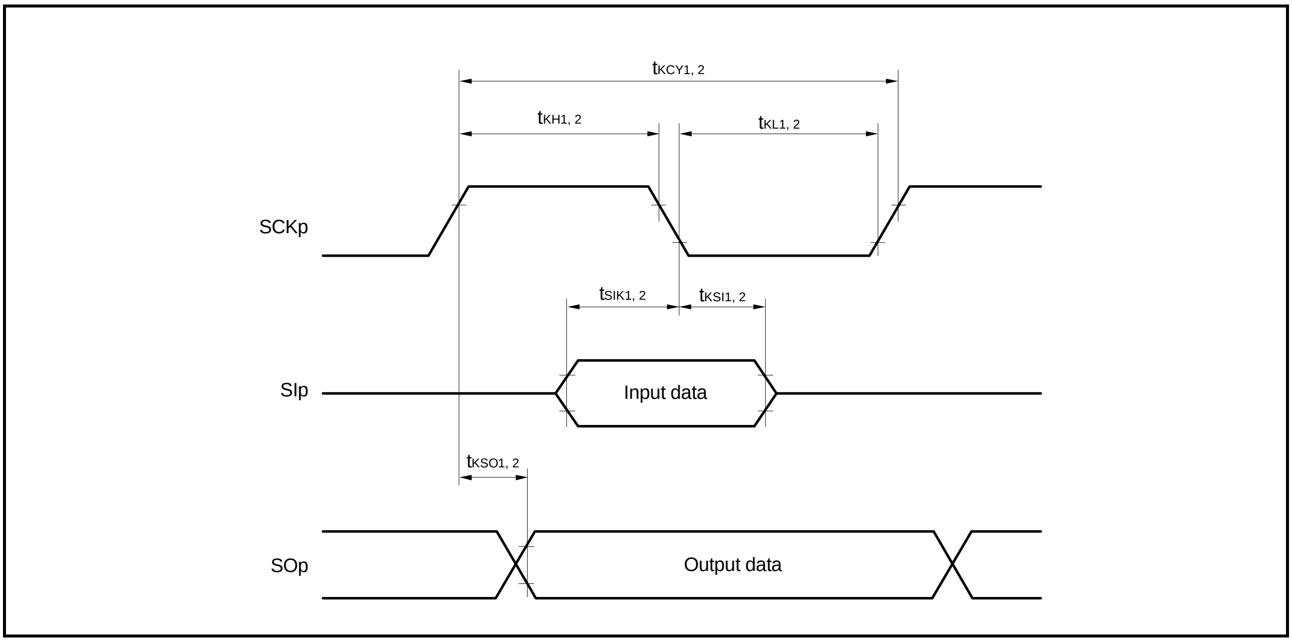
Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels


RL78
microcontroller
SCKp
SIp
SOp
SCK
SO
SI
User device

Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1


tKCY1, 2
tKL1, 2
tKH1, 2
SCKp
tSIK1, 2
tKSI1, 2
SIp
Input data
tKSO1, 2
SOp
Output data

Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0


tKCY1, 2
tKH1, 2
tKL1, 2
SCKp
tSIK1, 2
tKSI1, 2
SIp
Input data
tKSO1, 2
SOp
Output data

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) In simplified I^{2}C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 **Note 1**		1000 **Note 1**		400**Note 1**	kHz
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400**Note 1**		400**Note 1**		400**Note 1**	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300**Note 1**		300**Note 1**		300**Note 1**	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250**Note 1**		250**Note 1**		250**Note 1**	kHz
Hold time when SCLr is low	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(5) In simplified I^2C communications with devices operating at same voltage levels

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 85 **Note 2**		$1/f_{MCK}$ + 85 **Note 2**		$1/f_{MCK}$ + 145 **Note 2**		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 145 **Note 2**		$1/f_{MCK}$ + 145 **Note 2**		$1/f_{MCK}$ + 145 **Note 2**		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 230 **Note 2**		$1/f_{MCK}$ + 230 **Note 2**		$1/f_{MCK}$ + 230 **Note 2**		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	$1/f_{MCK}$ + 290 **Note 2**		$1/f_{MCK}$ + 290 **Note 2**		$1/f_{MCK}$ + 290 **Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	0	405	0	405	ns

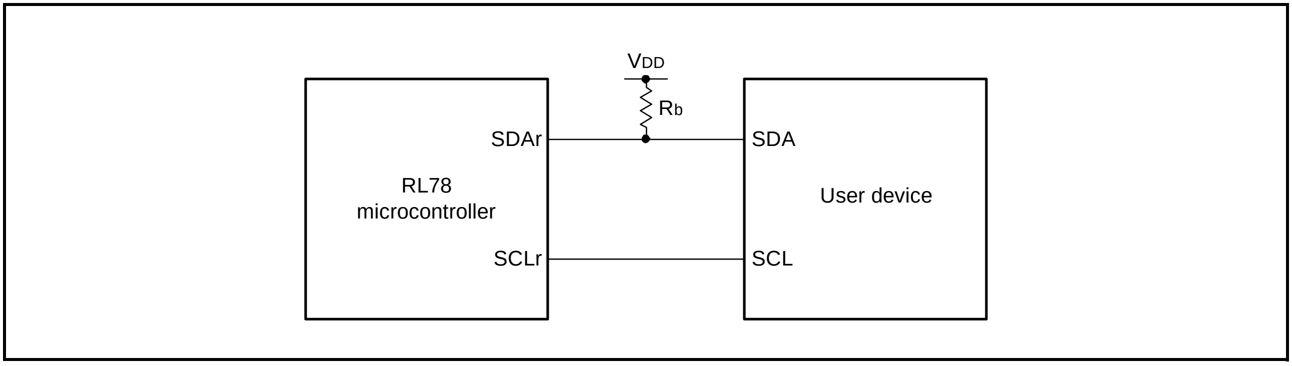
Note 1. The listed times must be no greater than $f_{MCK}/4$.

Note 2. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

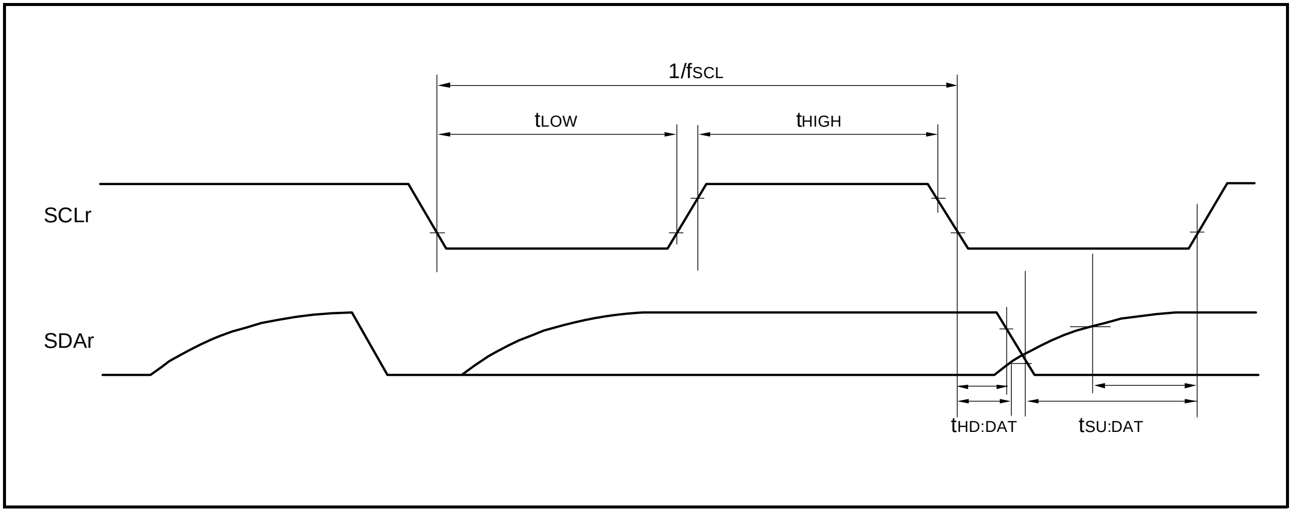
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Connection in the simplified I^2C communications with devices operating at same voltage levels


VDD
Rb
SDAr
SDA
RL78
microcontroller
User device
SCLr
SCL

Timing of serial transfer in the simplified I^2C communications with devices operating at same voltage levels


1/fSCL
tLOW
tHIGH
SCLr
SDAr
tHD:DAT
tSU:DAT

Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

(6) In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Reception	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		4		0.33	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		4		0.33	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		$f_{MCK}/6$ **Notes 1, 2, 3**		$f_{MCK}/6$ **Notes 1, 2**		$f_{MCK}/6$ **Notes 1, 2**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		4		0.33	Mbps

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. Use this rate with $EV_{DD0} \geq V_b$.

Note 3. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

2.4 V ≤ EV_{DD0} < 2.7 V: 2.6 Mbps (max.)

1.8 V ≤ EV_{DD0} < 2.4 V: 1.3 Mbps (max.)

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 24 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

(6) In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8**Note 2**		2.8**Note 2**		2.8**Note 2**	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2**Note 4**		1.2**Note 4**		1.2**Note 4**	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 7**		0.43 **Note 7**		0.43 **Note 7**	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 2. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes and Caution continue in the next page.)

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the "Conditions" column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with EV_{DD0} ≥ V_b.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

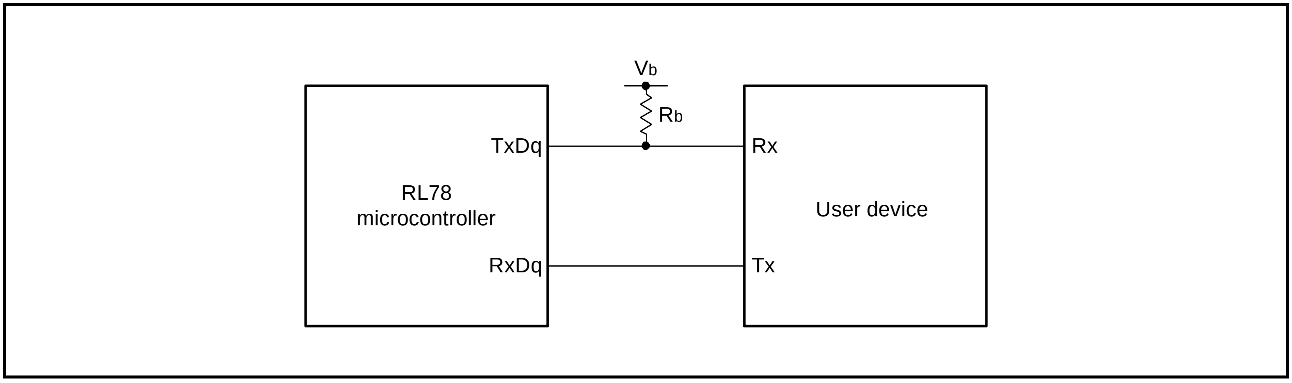
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

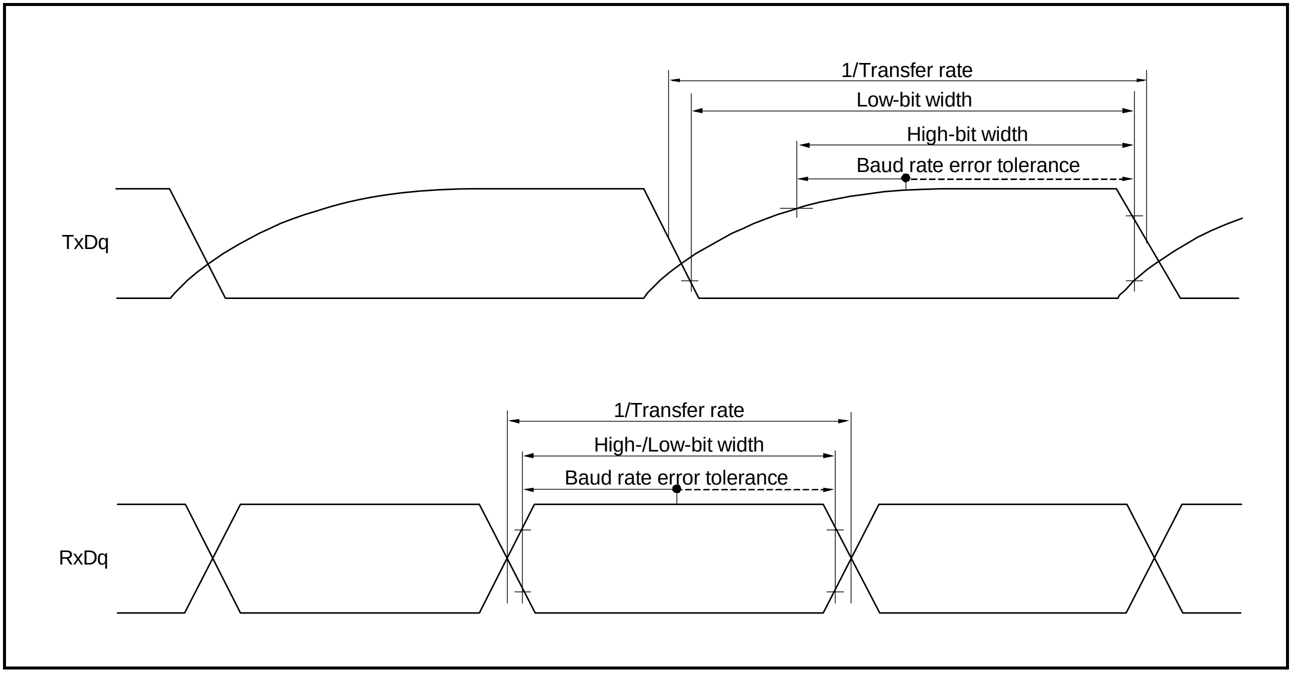
Note 7. This rate is calculated as an example when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

In UART communications with devices operating at different voltage levels


Vb
Rb
TxDq
Rx
RL78
microcontroller
User device
RxDq
Tx

Bit width in the UART communications with devices operating at different voltage levels (reference)


1/Transfer rate
Low-bit width
High-bit width
Baud rate error tolerance
TxDq
1/Transfer rate
High-/Low-bit width
Baud rate error tolerance
RxDq

Remark 1. R_b[Ω]: Communication line (TxDq) pull-up resistance, C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

(7) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		200		2300		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		300		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑)**Note 1**	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		58		479		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		121		479		ns
SIp hold time (from SCKp↑)**Note 1**	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output**Note 1**	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

(7) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(T_A = -40 to +105°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↓)Note 2	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	23		23		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33		33		110		ns
SIp hold time (from SCKp↓)Note 2	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp outputNote 2	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).)

Remark 4. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

(8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/3)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $4/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		300		2300		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		500		2300		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		$t_{KCY1}/2$ - 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		$t_{KCY1}/2$ - 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		$t_{KCY1}/2$ - 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ - 12		$t_{KCY1}/2$ - 12		$t_{KCY1}/2$ - 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ - 18		$t_{KCY1}/2$ - 18		$t_{KCY1}/2$ - 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V**Note**, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		$t_{KCY1}/2$ - 50		ns

Note Use this setting with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/3)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↑)Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		81		479		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		177		479		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑)Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp outputNote 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		483		483		483	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use this setting with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/3)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SIp setup time (to SCKp↓)[Note 1]	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		44		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		44		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓)[Note 1]	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output[Note 1]	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note 2], C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

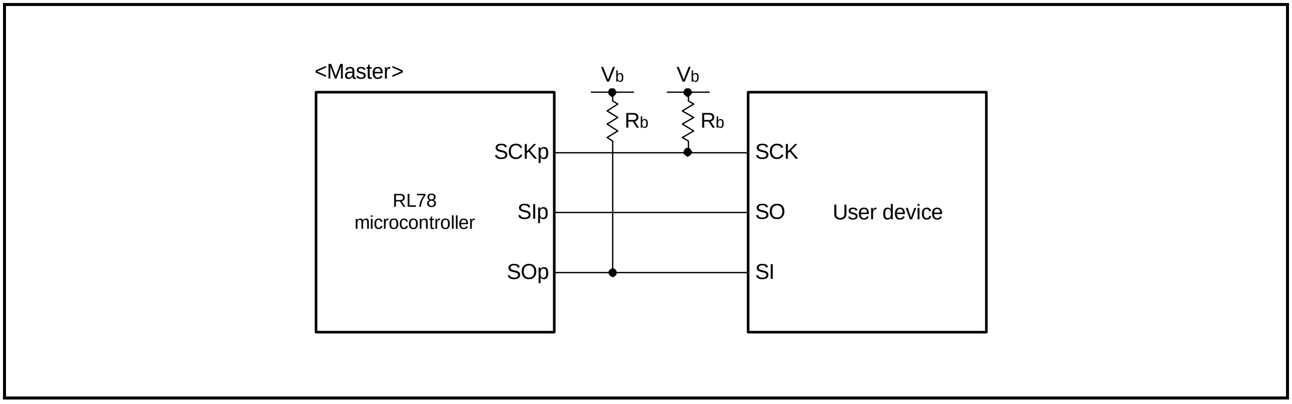
Note 1. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use this setting with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (when 30- to 52-pin products)/EV_{DD} tolerance (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels


<Master>
RL78 microcontroller
SCKp
SIp
SOp
Vb
Vb
Rb
Rb
SCK
SO
SI
User device

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

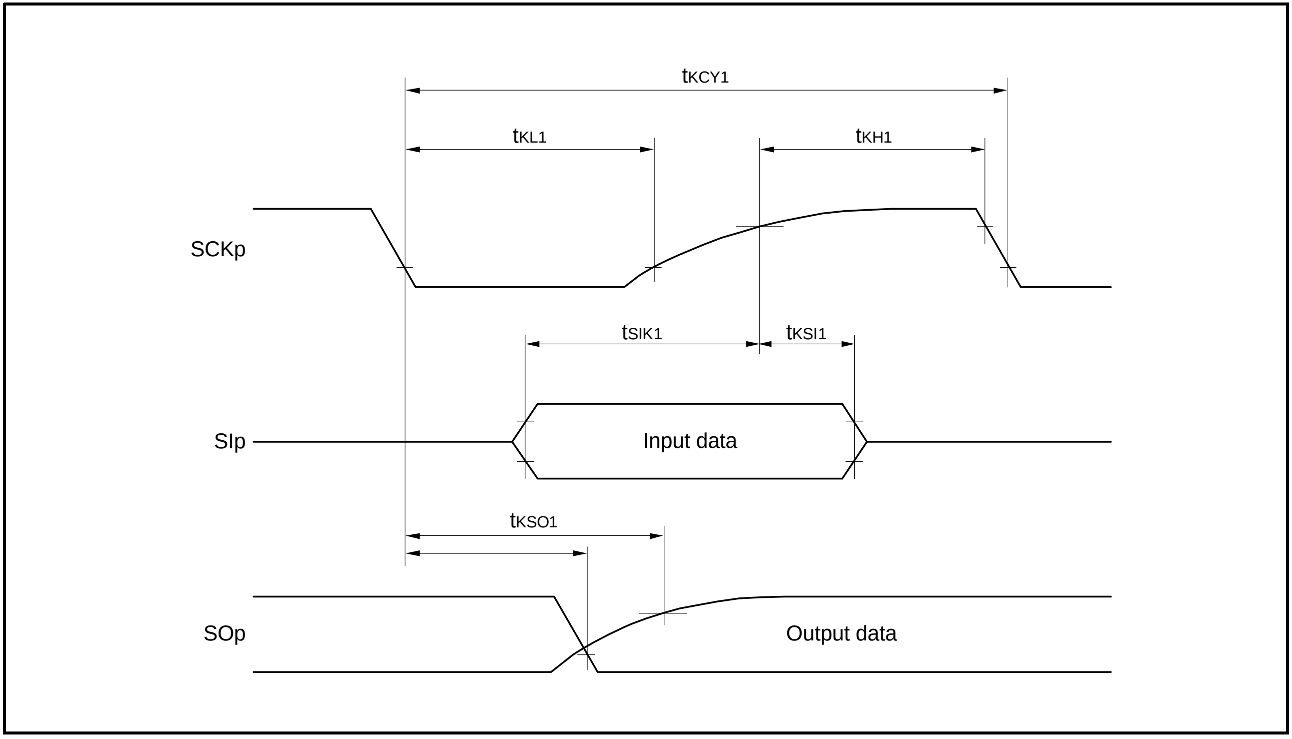
Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

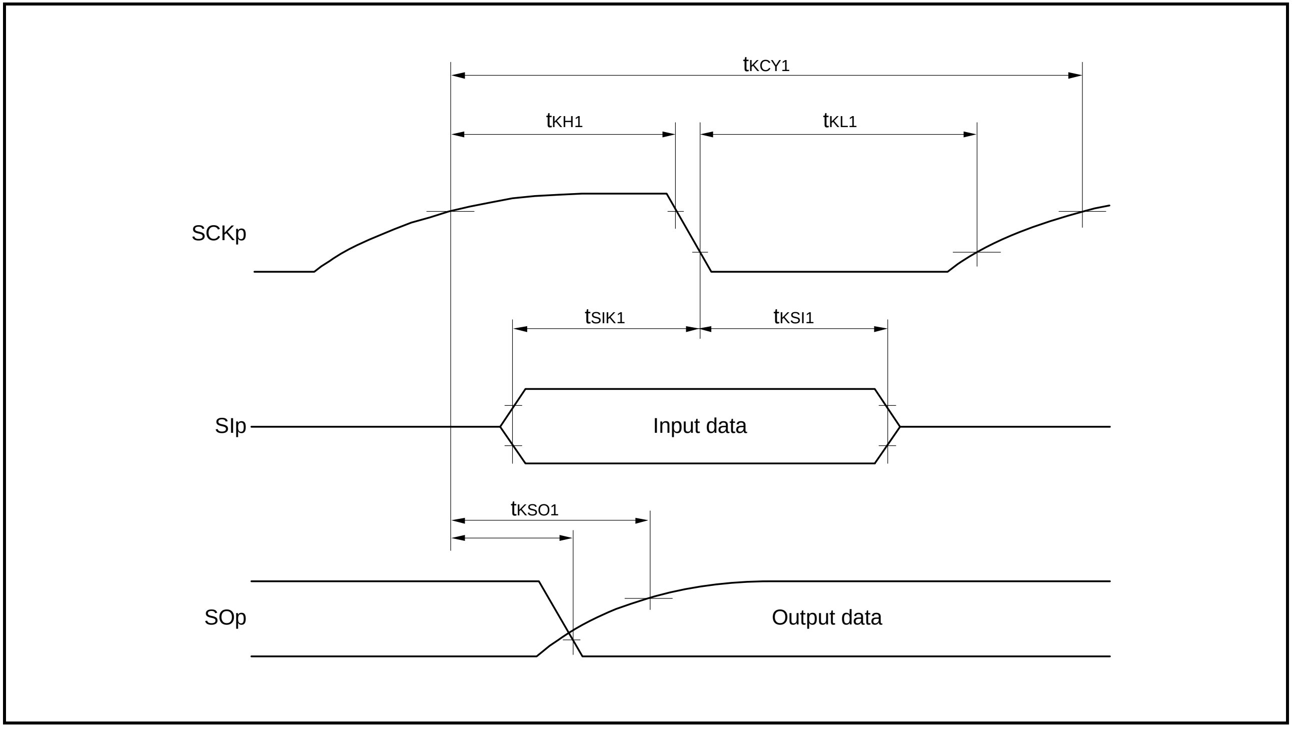
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).)

Remark 4. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1


tKCY1
tKL1
tKH1
SCKp
tSIK1
tKSI1
SIp
Input data
tKSO1
SOp
Output data

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0


tKCY1
tKH1
tKL1
SCKp
tSIK1
tKSI1
SIp
Input data
tKSO1
SOp
Output data

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 2. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(9) In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time **Note 1**	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		10/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V,	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		14/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		12/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		8/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		6/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		36/f_{MCK}		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		32/f_{MCK}		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		26/f_{MCK}		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(9) In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	t_{KCY2}/2 - 12		t_{KCY2}/2 - 12		t_{KCY2}/2 - 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 - 18		t_{KCY2}/2 - 18		t_{KCY2}/2 - 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**	t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		t_{KCY2}/2 - 50		ns
SIp setup time (to SCKp↑) **Note 3**	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 20		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) **Note 3**	t_{KSI2}		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output **Note 4**	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} + 120		2/f_{MCK} + 120		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 214		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Note 1. Transfer rate in the SNOOZE mode: 1 Mbps (max.)

Note 2. Use this setting with EV_{DD0} ≥ V_b.

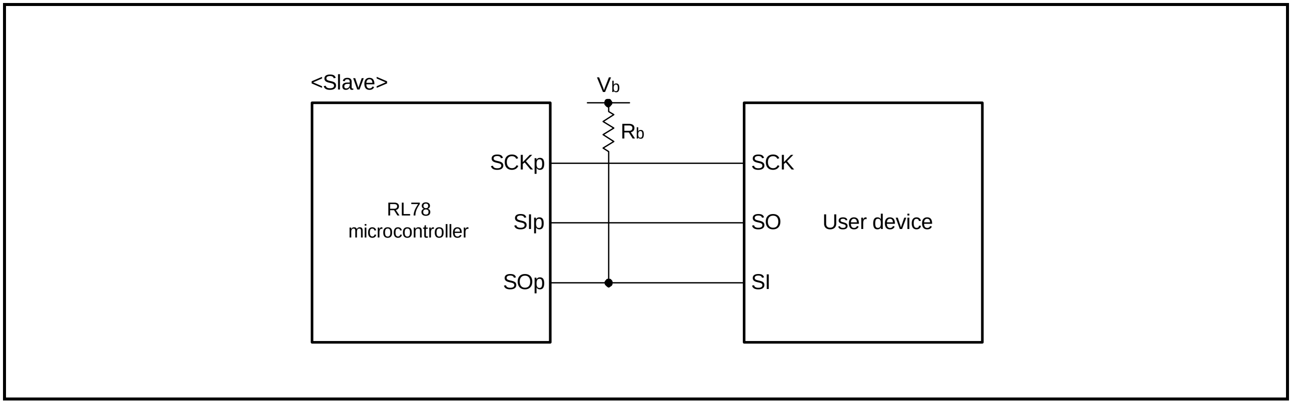
Note 3. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" and SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels


<Slave>
Vb
Rb
RL78 microcontroller
SCKp
SIp
SOp
SCK
SO
SI
User device

Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

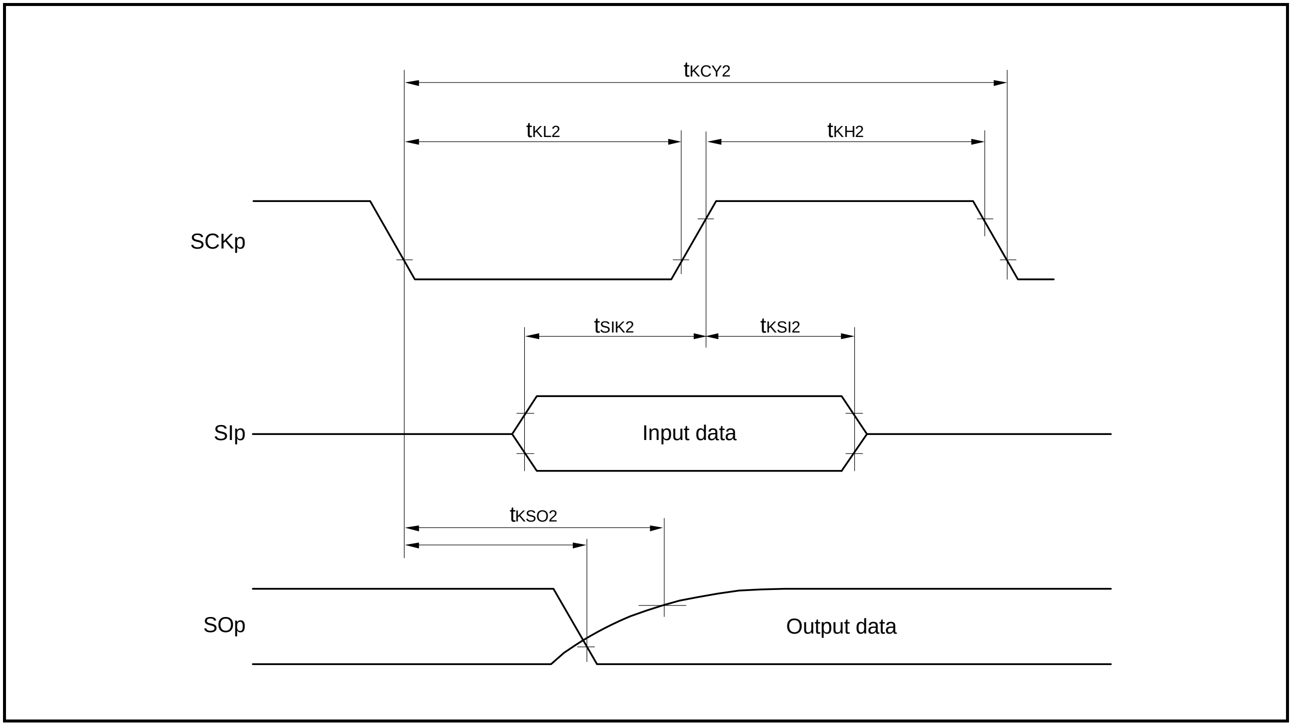
Remark 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

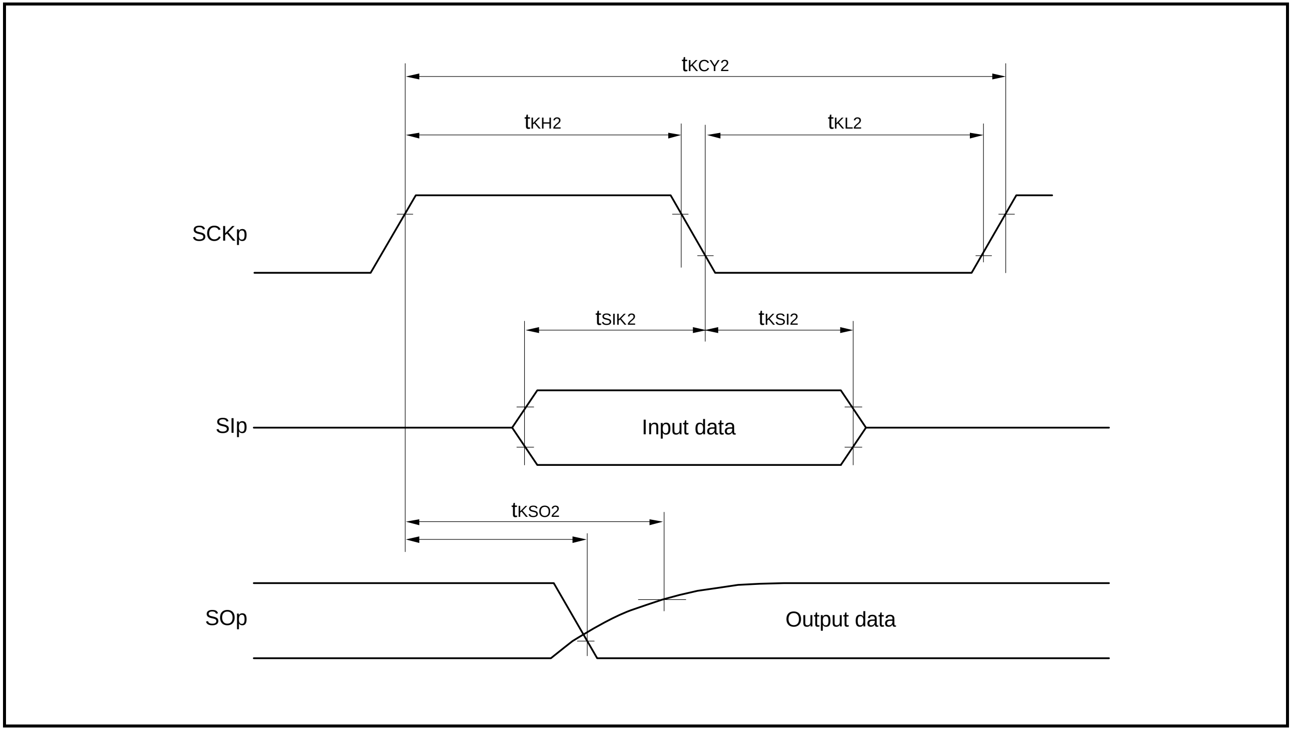
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 01, 02, 10, 12 and 13).)

Remark 4. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1


tKCY2
tKL2
tKH2
SCKp
tSIK2
tKSI2
SIp
Input data
tKSO2
SOp
Output data

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0


tKCY2
tKH2
tKL2
SCKp
tSIK2
tKSI2
SIp
Input data
tKSO2
SOp
Output data

Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 2. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(10) Simplified I^2C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 **Note 1**		1000 **Note 1**		300 **Note 1**	kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 **Note 1**		1000 **Note 1**		300 **Note 1**	kHz
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		400 **Note 1**		400 **Note 1**		300 **Note 1**	kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400 **Note 1**		400 **Note 1**		300 **Note 1**	kHz
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[**Note 2**], C_b = 100 pF, R_b = 5.5 kΩ		300 **Note 1**		300 **Note 1**		300 **Note 1**	kHz
Hold time when SCLr is low	t_{LOW}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[**Note 2**], C_b = 100 pF, R_b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	t_{HIGH}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[**Note 2**], C_b = 100 pF, R_b = 5.5 kΩ	610		610		610		ns

(10) Simplified I^2C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 **Note 3**		$1/f_{MCK}$ + 135 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 **Note 3**		$1/f_{MCK}$ + 135 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		$1/f_{MCK}$ + 190 **Note 3**		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note 2**, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than $f_{MCK}/4$.

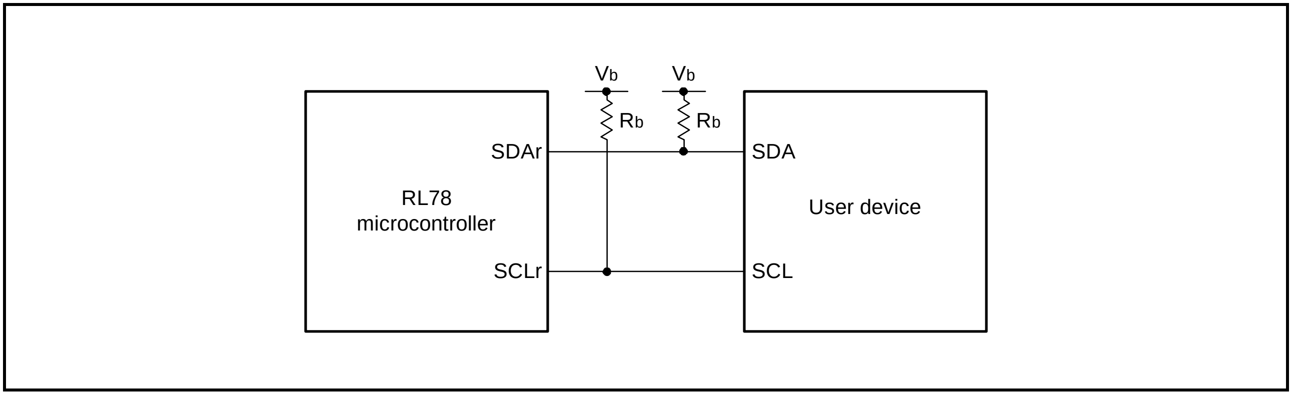
Note 2. Use this setting with EV_{DD0} ≥ V_b.

Note 3. Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

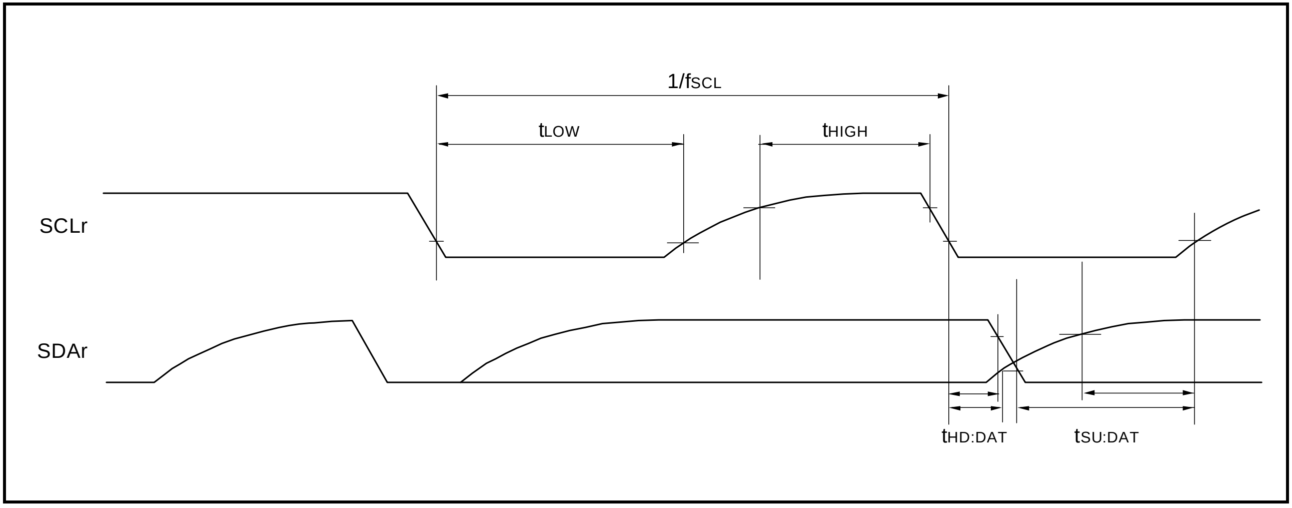
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Connection in the I^2C communications with devices operating at different voltage levels


Vb
Vb
Rb
Rb
SDAr
RL78
microcontroller
SCLr
SDA
User device
SCL

Timing of serial transfer in the simplified I^2C communications with devices operating at different voltage levels


1/fSCL
tLOW
tHIGH
SCLr
SDAr
tHD:DAT
tSU:DAT

Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 01, 02, 10, 12 and 13).)

2.5.2 Serial interface UARTA

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
<R> Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark g: PIM number (g = 3, 4, 7, 8), h: POM number (h = 3, 4, 7, 8, 12)

2.5.3 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0		100	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7			µs
Hold time**Note 1**	$t_{HD:STA}$		4.0			µs
Hold time when SCLA0 is low	t_{LOW}		4.7			µs
Hold time when SCLA0 is high	t_{HIGH}		4.0			µs
Data setup time (reception)	$t_{SU:DAT}$		250			ns
Data hold time (transmission)**Note 2**	$t_{HD:DAT}$		0		3.45	µs
Setup time of stop condition	$t_{SU:STO}$		4.0			µs
Bus-free time	t_{BUF}		4.7			µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The listed frequency and times apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz 1.8 V ≤ EV_{DD0} ≤ 5.5 V	0		400	kHz
Setup time of restart condition	$t_{SU:STA}$	1.8 V ≤ EV_{DD0} ≤ 5.5 V	0.6			µs
Hold time**Note 1**	$t_{HD:STA}$	1.8 V ≤ EV_{DD0} ≤ 5.5 V	0.6			µs
Hold time when SCLA0 is low	t_{LOW}	1.8 V ≤ EV_{DD0} ≤ 5.5 V	1.3			µs
Hold time when SCLA0 is high	t_{HIGH}	1.8 V ≤ EV_{DD0} ≤ 5.5 V	0.6			µs
Data setup time (reception)	$t_{SU:DAT}$	1.8 V ≤ EV_{DD0} ≤ 5.5 V	100			ns
Data hold time (transmission)**Note 2**	$t_{HD:DAT}$	1.8 V ≤ EV_{DD0} ≤ 5.5 V	0		0.9	µs
Setup time of stop condition	$t_{SU:STO}$	1.8 V ≤ EV_{DD0} ≤ 5.5 V	0.6			µs
Bus-free time	t_{BUF}	1.8 V ≤ EV_{DD0} ≤ 5.5 V	1.3			µs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
C_b = 320 pF, R_b = 1.1 kΩ

(3) I^{2}C fast mode plus

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz 2.7 V ≤ EV_{DD0} ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.26			µs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.26			µs
Hold time when SCLA0 is low	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.5			µs
Hold time when SCLA0 is high	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.26			µs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	50			ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0		0.45	µs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.26			µs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0.5			µs

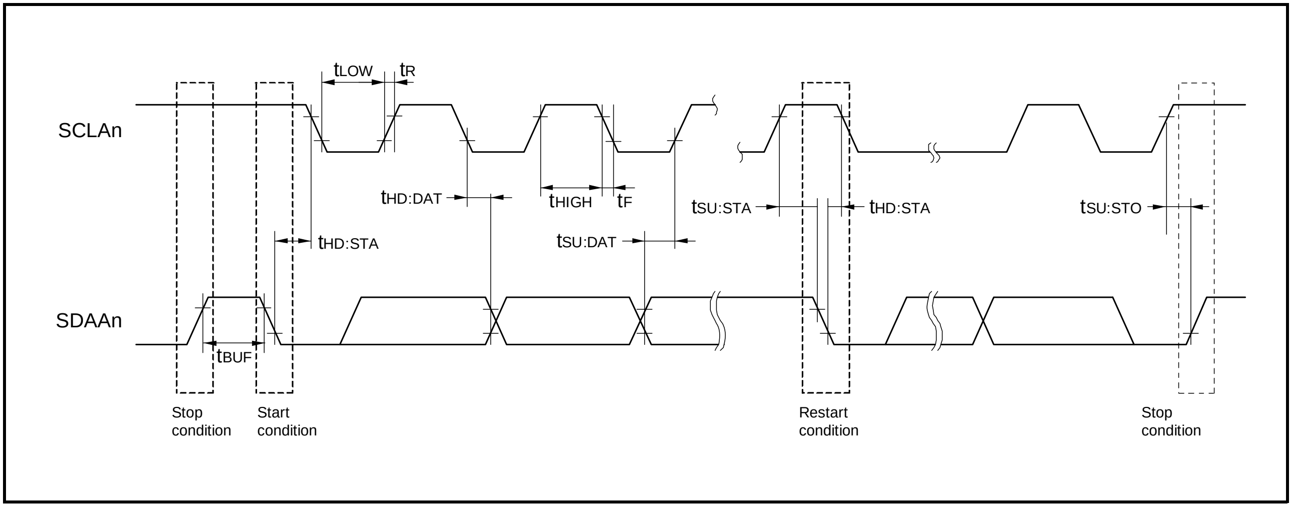
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of $t_{HD:DAT}$ applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
C_b = 120 pF, Rb = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

<R> (1) Normal modes 1 and 2

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES				12	bit
Conversion clock	f_{AD}		1		32	MHz
Overall error**Notes 1, 3, 4, 5, 7**	AINL	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.4	±4.5	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.9	±5.7	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±3.0	±5.8	LSB
Conversion time**Notes 6, 7**	t_{CONV}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error**Notes 1, 2, 3, 4, 5, 7**	E_{ZS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.01%	±0.08%	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.01%	±0.09%	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.03%	±0.13%	%FSR
Full-scale error**Notes 1, 2, 3, 4, 5, 7**	E_{FS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.03%	±0.09%	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.05%	±0.13%	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±0.05%	±0.13%	%FSR
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. We do not inspect the characteristics of the A/D converter before shipment. The listed values are only results of evaluation.

Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time.

Note 7. The listed values apply when the conversion resolution is set to 12 bits.

(T_A = -40 to +105°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,

reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),

target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error[Notes 1, 3, 4, 5]	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time[Note 6]	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			μs
Zero-scale error[Notes 1, 2, 3, 4, 5]	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error[Notes 1, 2, 3, 4, 5]	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error[Notes 1, 4, 5]	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time.

<R> (2) Low-voltage modes 1 and 2

(T_A = -40 to +105°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V,
reference voltage (+) = AV_{REFP} (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} (ADREFM = 1),
target pins ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		24	MHz
Overall error[Notes 1, 3, 4, 5]	AINL	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±12.0	LSB
Conversion time[Note 6]	t_{CONV}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	3.33			μs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	5.0			μs
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	10.0			μs
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	20.0			μs
Zero-scale error[Notes 1, 2, 3, 4, 5]	E_{ZS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Full-scale error[Notes 1, 2, 3, 4, 5]	E_{FS}	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.28	%FSR
Integral linearity error[Notes 1, 4, 5]	ILE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.0	LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±4.5	LSB
Differential linearity error[Note 1]	DLE	12-bit resolution	2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.5		LSB
			1.8 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
			1.6 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

(Notes continues in the next page.)

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.
Overall error: Add ±3 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS}, the maximum values are as follows.
Overall error: Add ±10 LSB to the maximum value.
Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.
Integral linearity error: Add ±4 LSB to the maximum value.

Note 5. When AV_{REFP} < V_{DD}, the maximum values are as follows.
Overall error/zero-scale error/full-scale error: Add (±0.75 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.
Integral linearity error: Add (±0.2 LSB × (V_{DD} voltage (V) - AV_{REFP} voltage (V)) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 µs. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (f_{AD}) of no more than 16 MHz.

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(3) When the internal reference voltage is selected as reference voltage (+)

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, low-voltage modes 1 and 2,
reference voltage (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0),
reference voltage (-) = AV_{REFM} (ADREFM = 1)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES			8		Bit
Conversion clock	f_{AD}	1.6 V ≤ V_{DD} ≤ 5.5 V	1		2	MHz
Zero-scale error[Notes 1, 2, 4]	E_{ZS}	1.6 V ≤ V_{DD} ≤ 5.5 V			±0.6	%FSR
Integral linearity error[Notes 1, 4]	ILE	1.6 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	1.6 V ≤ V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}		0		V_{BGR} **Note 3**	V

Note 1. This value does not include the quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. **Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics**.

Note 4. When reference voltage (-) is selected as V_{SS}, the maximum values are as follows.
Zero-scale error: Add ±0.35%FSR to the maximum value.
Integral linearity error: Add ±0.5 LSB to the maximum value.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to +105°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	F_{VTMPS}	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	t_{AMP}		5			µs

2.6.3 D/A converter characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES					8	Bit
Overall error	AINL	Rload = 8 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			± 2.5	LSB
		Rload = 4 MΩ	1.8 V ≤ V_{DD} ≤ 5.5 V			± 2.5	LSB
Settling time	t_{SET}	Cload = 20 pF	2.7 V ≤ V_{DD} ≤ 5.5 V			3	µs
			1.6 V ≤ V_{DD} ≤ 5.5 V			6	µs

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2.6.4 Comparator characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

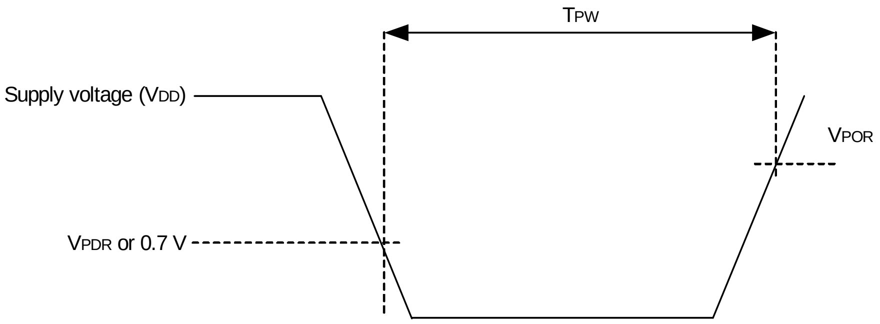
Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	I_{VREF}	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		V_{DD} - 1.4 and EV_{DD0}	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		EV_{DD0}	V
	I_{VCMP}	Input to the IVCMP0 and IVCMP1 pins		-0.3		EV_{DD0} + 0.3	V
Output delay	td	V_{DD} = 3.0 V, Input slew rate > 1 V/µs	High-speed mode			1.5	µs
			Low-speed mode		3.0		µs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	t_{CMP}			30			µs
Internal reference voltage	V_{BGR2}			1.4		1.6	V

2.6.5 POR circuit characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V_{POR}, V_{PDR}		1.43	1.50	1.57	V
Minimum pulse width^{Note}	T_{PW}		300			µs

Note This width is the minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This width is also the minimum time required for a POR reset from when V_{DD} falls below 0.7 V to when V_{DD} exceeds V_{POR} in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

(1) LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \le V_{DD} \le 5.5$ V, V_{SS} = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD00}	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		V_{LVD01}	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
		V_{LVD02}	The power supply voltage is rising.	2.59	2.67	2.75	V
			The power supply voltage is falling.	2.54	2.62	2.70	V
		V_{LVD03}	The power supply voltage is rising.	2.31	2.38	2.45	V
			The power supply voltage is falling.	2.26	2.33	2.40	V
		V_{LVD04}	The power supply voltage is rising.	1.84	1.90	1.95	V
			The power supply voltage is falling.	1.80	1.86	1.91	V
		V_{LVD05}	The power supply voltage is rising.	1.64	1.69	1.74	V
			The power supply voltage is falling.	1.60	1.65	1.70	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time						500	µs

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(2) LVD1 Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		V_{LVD11}	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		V_{LVD12}	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		V_{LVD13}	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.49	3.54	V
		V_{LVD14}	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		V_{LVD15}	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		V_{LVD16}	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		V_{LVD17}	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		V_{LVD18}	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		V_{LVD19}	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		V_{LVD110}	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		V_{LVD111}	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		V_{LVD112}	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		V_{LVD113}	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		V_{LVD114}	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		V_{LVD115} **Note**	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		V_{LVD116} **Note**	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
		V_{LVD117} **Note**	The power supply voltage is rising.	1.64	1.67	1.70	V
			The power supply voltage is falling.	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		500			µs
Detection delay time						500	µs

Note This setting can only be used when LVD0 is disabled.

2.6.7 Power supply voltage rising slope characteristics

(T_A = -40 to +105°C, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

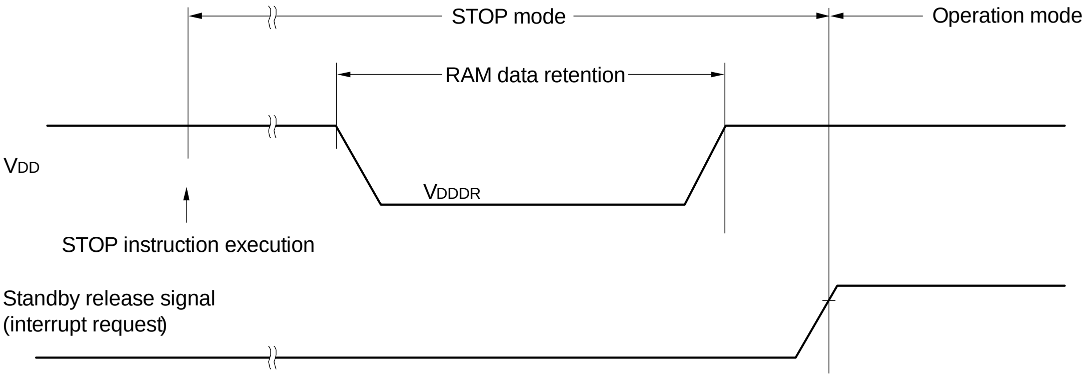
Caution Make sure to keep the internal reset state by the LVD0 circuit or an external reset until V_{DD} reaches the operating voltage range shown in AC characteristics.

2.7 RAM Data Retention Characteristics

(T_A = -40 to +105°C, V_{SS} = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDDR}		1.43**Note**		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}		1		32	MHz
Number of code flash rewrites**Notes 1, 2, 3**	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites**Notes 1, 2, 3**		Retained for 1 year T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using flash memory programmer and Renesas Electronics self programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

(1) Code flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	2 Kbytes	t_{E2K}	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	2 Kbytes	t_{BC2K}	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Security setting time		t_{AWSSAS}	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

(2) Data flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
<R> Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Dedicated Flash Memory Programmer Communication (UART)

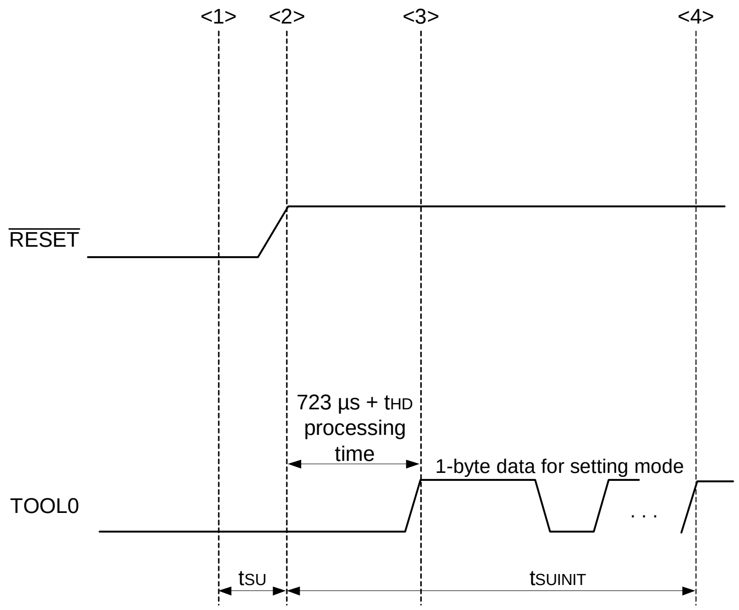
(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			µs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

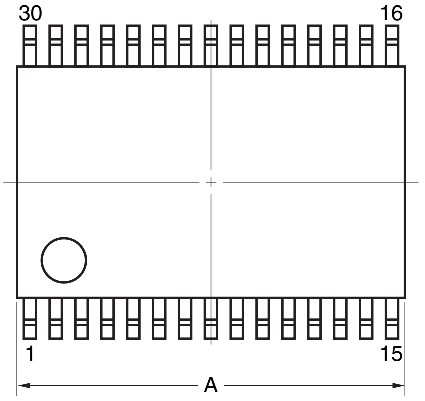
t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

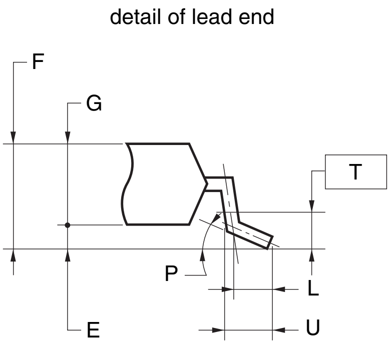
3. Package Drawings

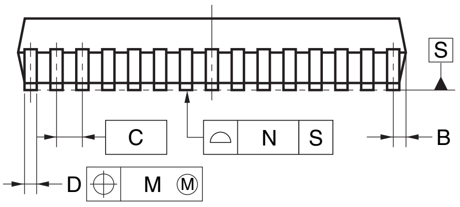
3.1 30-Pin Products

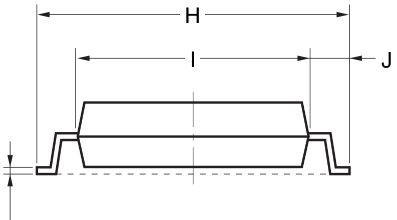
R7F100GAF3CSP, R7F100GAG3CSP, R7F100GAH3CSP, R7F100GAJ3CSP
R7F100GAF2DSP, R7F100GAG2DSP, R7F100GAH2DSP, R7F100GAJ2DSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18









NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15

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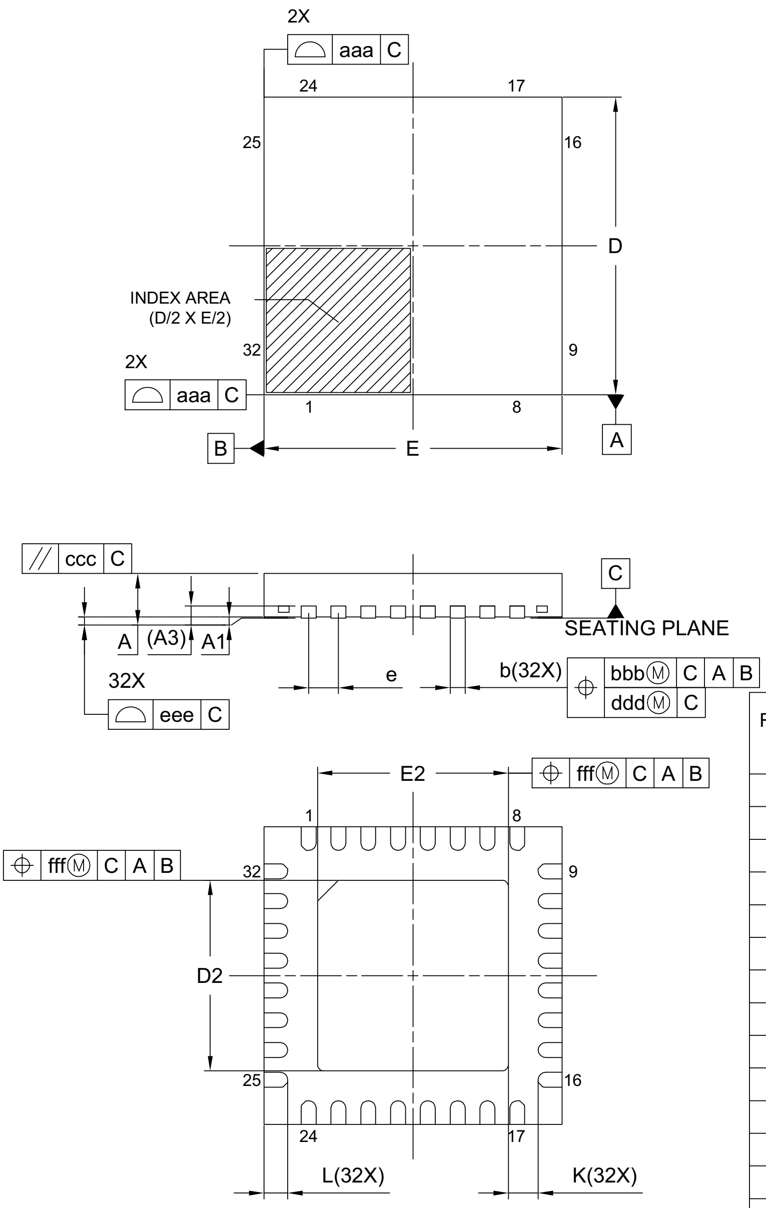
3.2 32-Pin Products

R7F100GBF3CNP, R7F100GBG3CNP, R7F100GBH3CNP, R7F100GBJ3CNP
R7F100GBF2DNP, R7F100GBG2DNP, R7F100GBH2DNP, R7F100GBJ2DNP

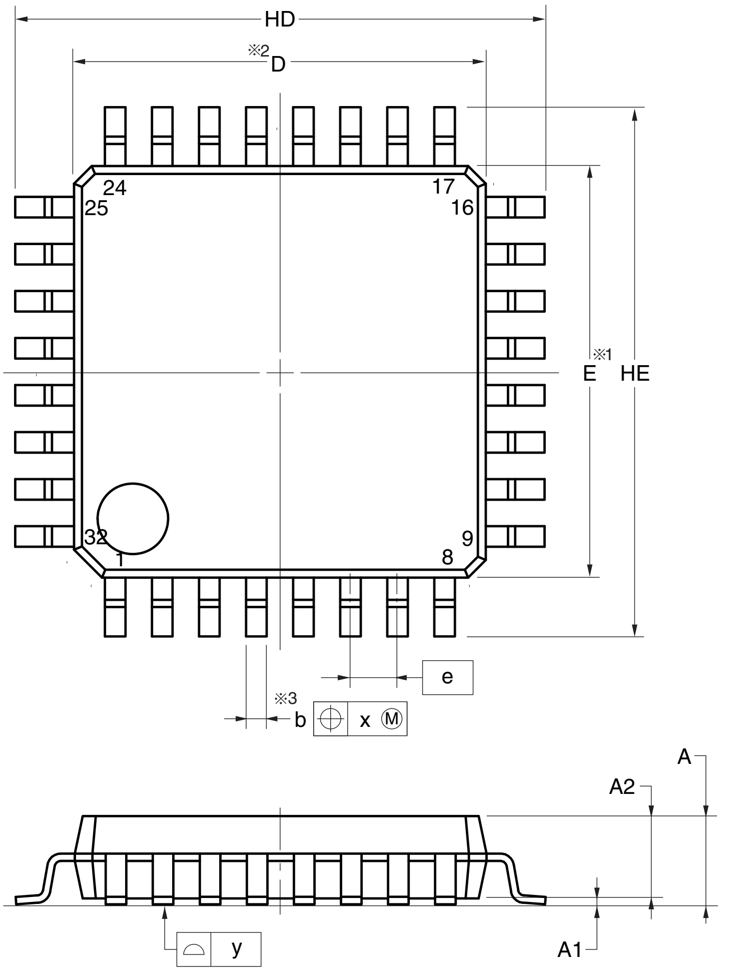
JEITA Package code	RENESAS code	MASS (TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06


2X
aaa C
24
17
25
16
D
INDEX AREA
(D/2 X E/2)
32
9
2X
aaa C
1
8
B
E
A
ccc C
C
A
(A3)
A1
SEATING PLANE
32X
eee C
e
b(32X)
bbbⓂ C A B
dddⓂ C
E2
fffⓂ C A B
1
8
fffⓂ C A B
32
9
D2
25
16
24
17
L(32X)
K(32X)

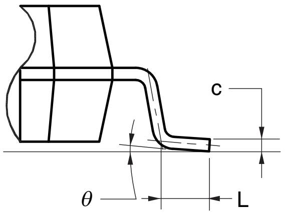
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D_2	3.15	3.20	3.25
E_2	3.15	3.20	3.25
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

R7F100GBF3CFP, R7F100GBG3CFP, R7F100GBH3CFP, R7F100GBJ3CFP
R7F100GBF2DFP, R7F100GBG2DFP, R7F100GBH2DFP, R7F100GBJ2DFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

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3.3 36-Pin Products

R7F100GCF3CLA, R7F100GCG3CLA, R7F100GCH3CLA, R7F100GCJ3CLA
R7F100GCF2DLA, R7F100GCG2DLA, R7F100GCH2DLA, R7F100GCJ2DLA

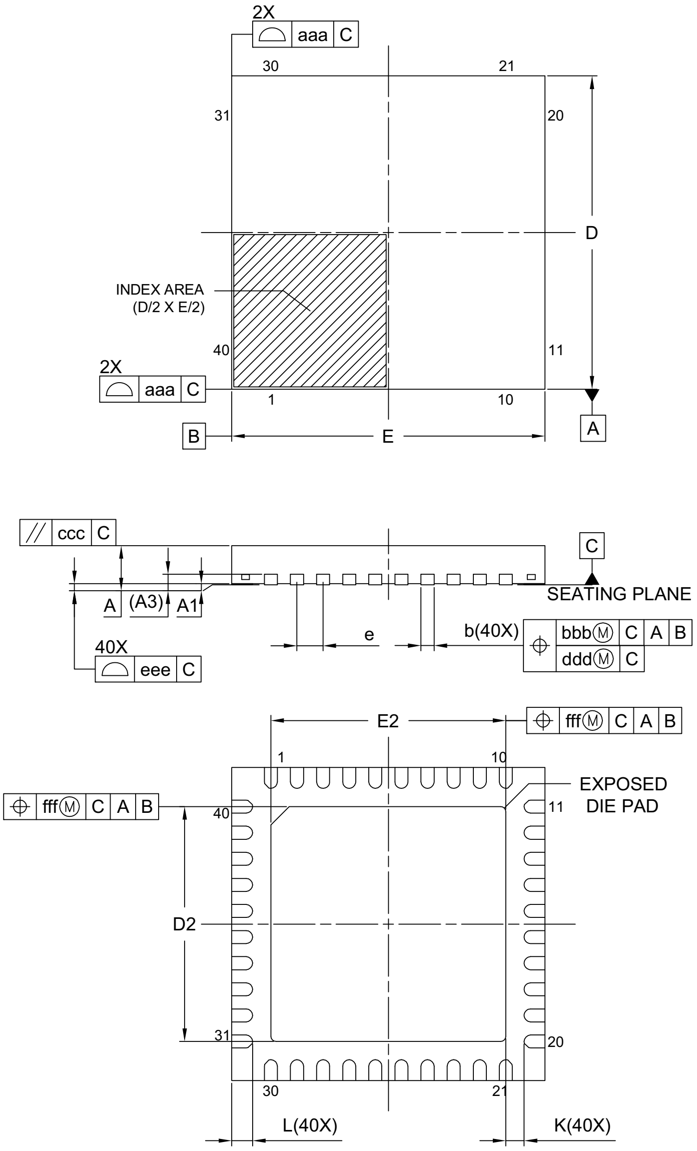
Contact a Renesas Electronics sales office for details.

3.4 40-Pin Products

R7F100GEF3CNP, R7F100GEG3CNP, R7F100GEH3CNP, R7F100GEJ3CNP
R7F100GEF2DNP, R7F100GEG2DNP, R7F100GEH2DNP, R7F100GEJ2DNP

<R>

JEITA Package code	RENESAS code	MASS (TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08

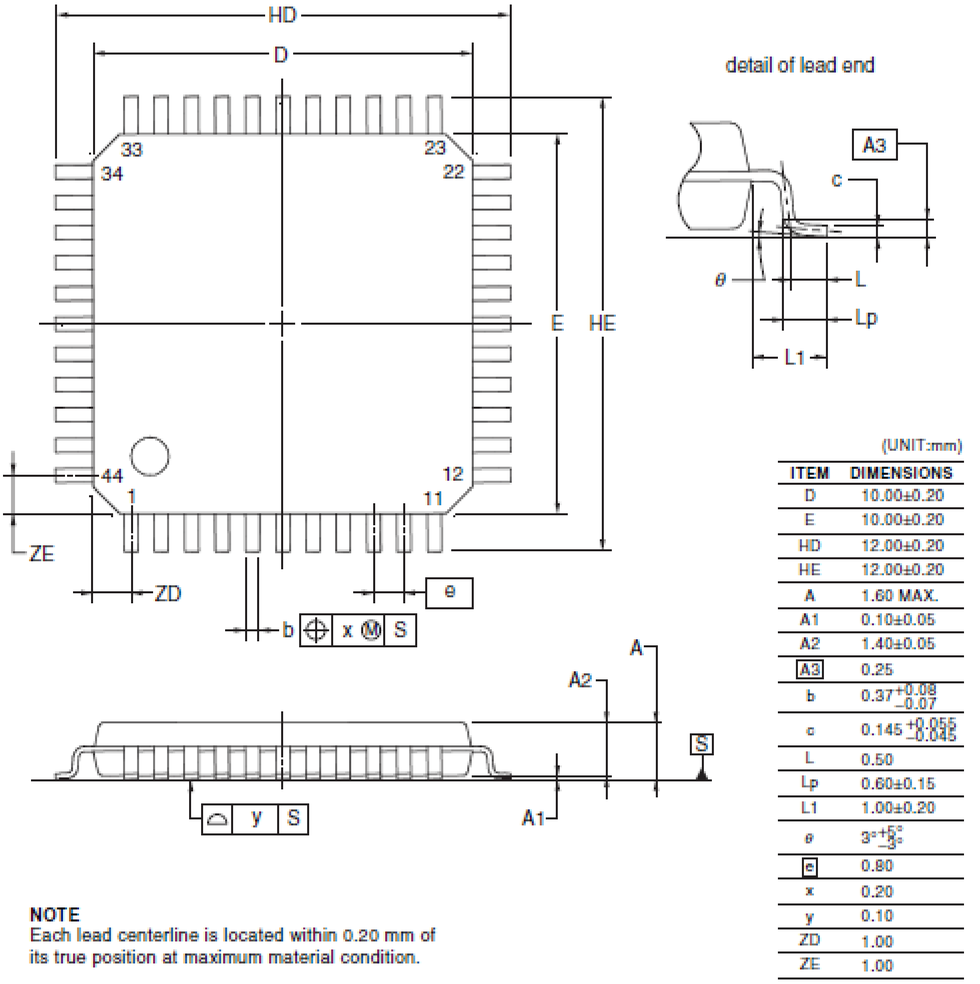

2X
aaa C
30
21
31
20
D
INDEX AREA
(D/2 X E/2)
40
11
2X
aaa C
1
10
B
E
A
ccc C
C
A
(A3)
A1
SEATING PLANE
e
b(40X)
bbbⓂ C A B
dddⓂ C
40X
eee C
E2
fffⓂ C A B
1
10
EXPOSED
DIE PAD
fffⓂ C A B
40
11
D2
31
20
30
21
L(40X)
K(40X)

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.18	0.25	0.30
D	6.00 BSC		
E	6.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

3.5 44-Pin Products

R7F100GFF3CFP, R7F100GFG3CFP, R7F100GFH3CFP, R7F100GFJ3CFP
R7F100GFK3CFP, R7F100GFL3CFP
R7F100GFN3CFP
R7F100GFF2DFP, R7F100GFG2DFP, R7F100GFH2DFP, R7F100GFJ2DFP
R7F100GFK2DFP, R7F100GFL2DFP
R7F100GFN2DFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

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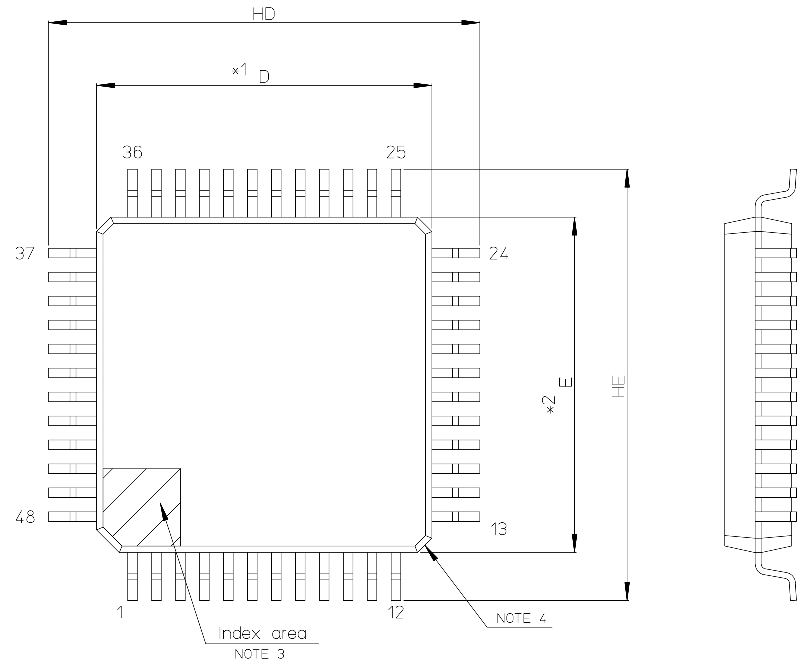
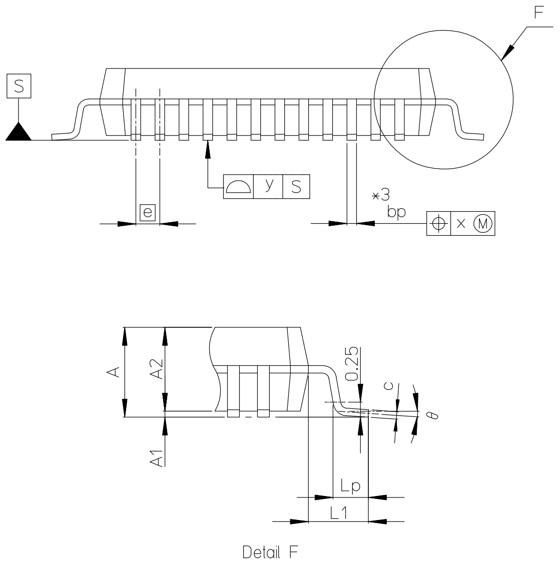
3.6 48-Pin Products

R7F100GGF3CFB, R7F100GGG3CFB, R7F100GGH3CFB, R7F100GGJ3CFB
R7F100GGK3CFB, R7F100GGL3CFB, R7F100GGN3CFB
R7F100GGF2DFB, R7F100GGG2DFB, R7F100GGH2DFB, R7F100GGJ2DFB
R7F100GGK2DFB, R7F100GGL2DFB, R7F100GGN2CFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2g


HD
*1 D
36
25
37
24
48
13
1
12
*2 E
HE
Index area
NOTE 3
NOTE 4


F
S
y S
e
*3
bp
x M
A
A2
A1
0.25
c
θ
Lp
L1
Detail F

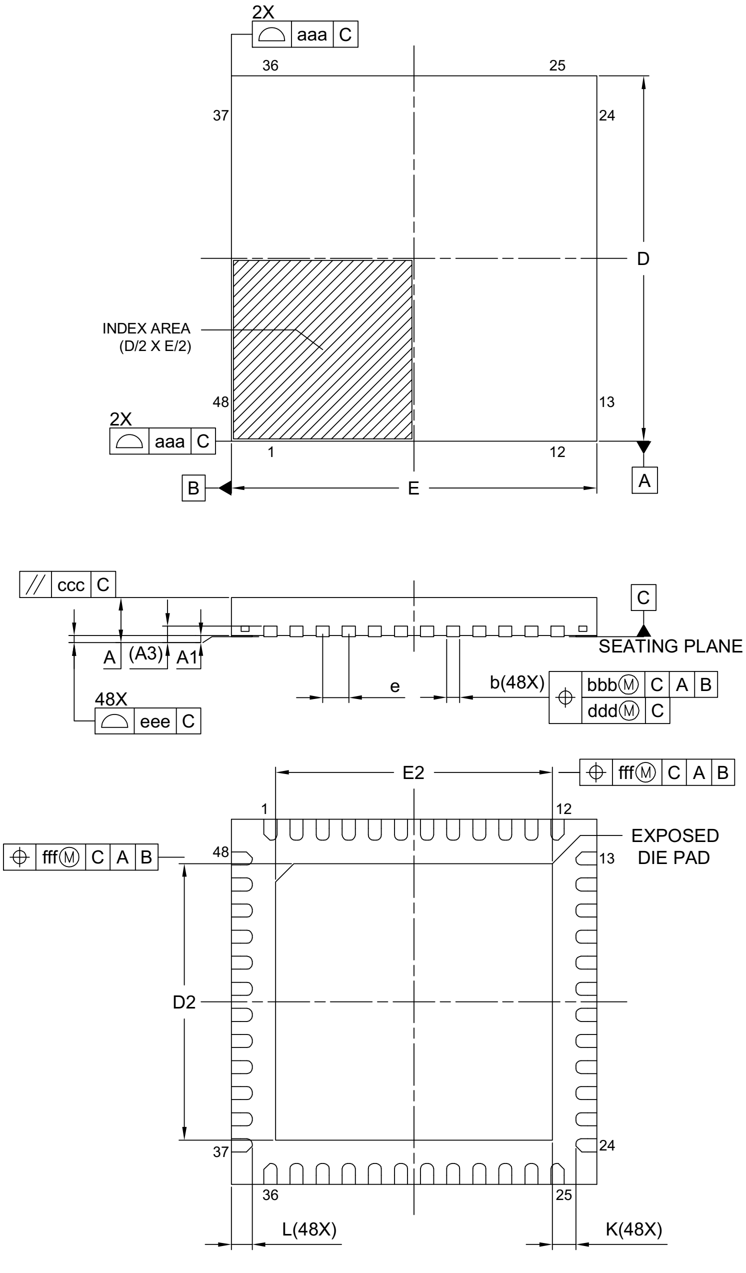
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	—	1.4	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

R7F100GGF3CNP, R7F100GGG3CNP, R7F100GGH3CNP, R7F100GGJ3CNP
R7F100GGK3CNP, R7F100GGL3CNP, R7F100GGN3CNP
R7F100GGF2DNP, R7F100GGG2DNP, R7F100GGH2DNP, R7F100GGJ2DNP
R7F100GGK2DNP, R7F100GGL2DNP, R7F100GGN2CNP

<R>

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

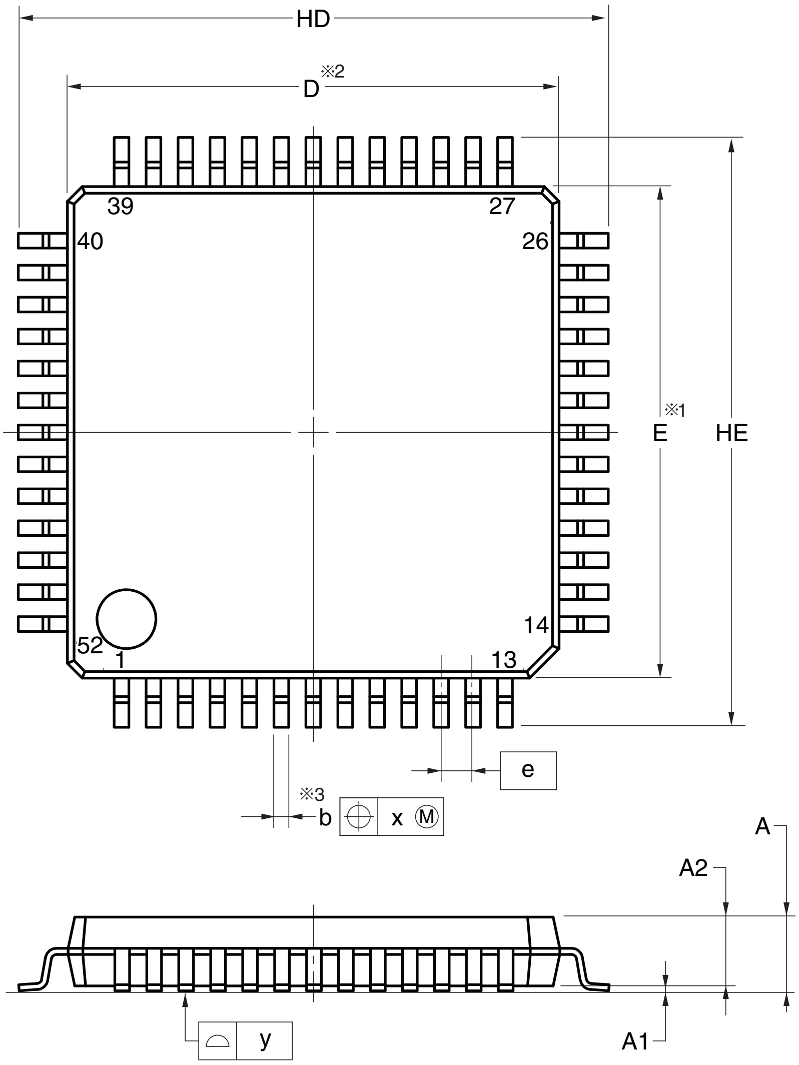

2X
aaa C
36
25
37
24
D
INDEX AREA
(D/2 X E/2)
48
13
2X
aaa C
1
12
B
E
A
ccc C
C
SEATING PLANE
A
(A3)
A1
e
b(48X)
bbbⓂ C A B
dddⓂ C
48X
eee C
E2
fffⓂ C A B
1
12
EXPOSED
DIE PAD
fffⓂ C A B
48
13
D2
37
24
36
25
L(48X)
K(48X)

Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	―	―	0.80
A_1	0.00	0.02	0.05
A_3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	―	―
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

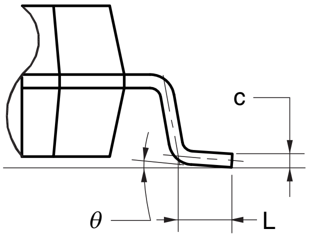
3.7 52-Pin Products

R7F100GJF3CFA, R7F100GJG3CFA, R7F100GJH3CFA, R7F100GJJ3CFA
R7F100GJK3CFA, R7F100GJL3CFA, R7F100GJN3CFA
R7F100GJF2DFA, R7F100GJG2DFA, R7F100GJH2DFA, R7F100GJJ2DFA
R7F100GJK2DFA, R7F100GJL2DFA, R7F100GJN2DFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

NOTE

1.Dimensions “※1” and “※2” do not include mold flash.

2.Dimension “※3” does not include trim offset.

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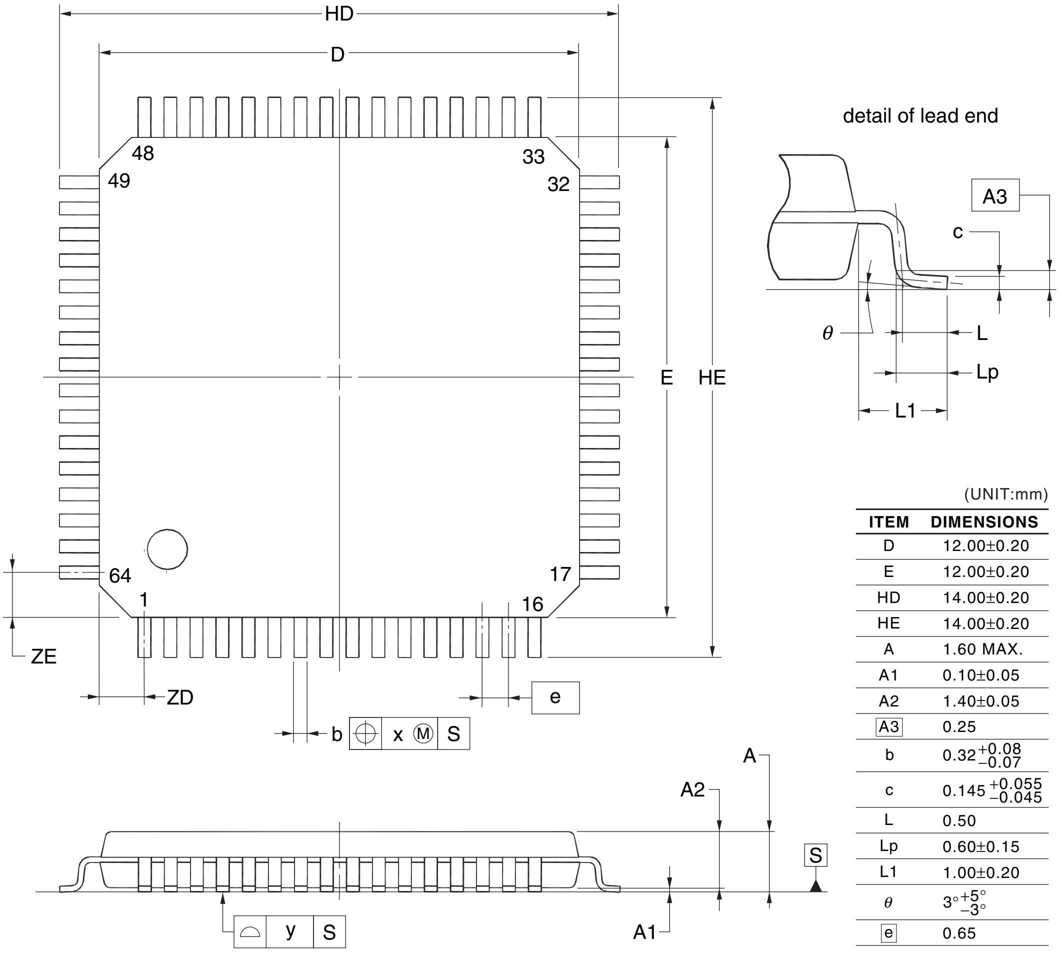
3.8 64-Pin Products

R7F100GLF3CFA, R7F100GLG3CFA, R7F100GLH3CFA, R7F100GLJ3CFA
R7F100GLK3CFA, R7F100GLL3CFA, R7F100GLN3CFA
R7F100GLF2DFA, R7F100GLG2DFA, R7F100GLH2DFA, R7F100GLJ2DFA
R7F100GLK2DFA, R7F100GLL2DFA, R7F100GLN2DFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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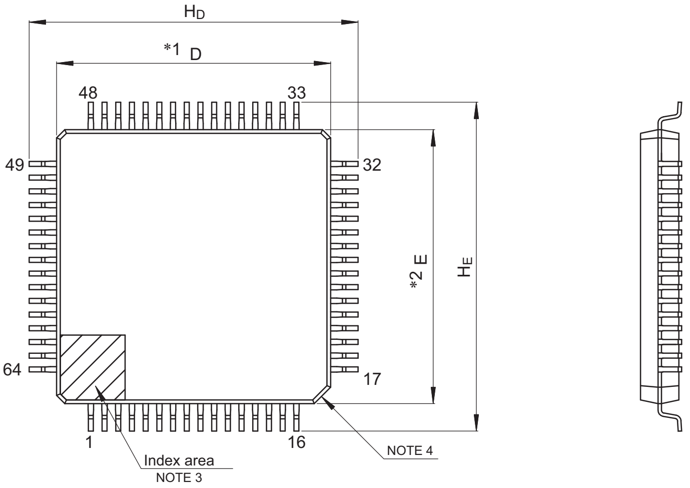
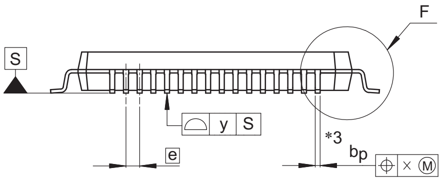
R7F100GLF3CFB, R7F100GLG3CFB, R7F100GLH3CFB, R7F100GLJ3CFB,
R7F100GLK3CFB, R7F100GLL3CFB, R7F100GLN3CFB
R7F100GLF2DFB, R7F100GLG2DFB, R7F100GLH2DFB, R7F100GLJ2DFB,
R7F100GLK2DFB, R7F100GLL2DFB, R7F100GLN2DFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

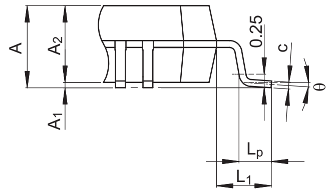
Unit: mm





NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—



Detail F

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R7F100GLF3CLA, R7F100GLG3CLA, R7F100GLH3CLA, R7F100GLJ3CLA,
R7F100GLK3CLA, R7F100GLL3CLA, R7F100GLN3CLA
R7F100GLF2DLA, R7F100GLG2DLA, R7F100GLH2DLA, R7F100GLJ2DLA,
R7F100GLK2DLA, R7F100GLL2DLA, R7F100GLN2DLA

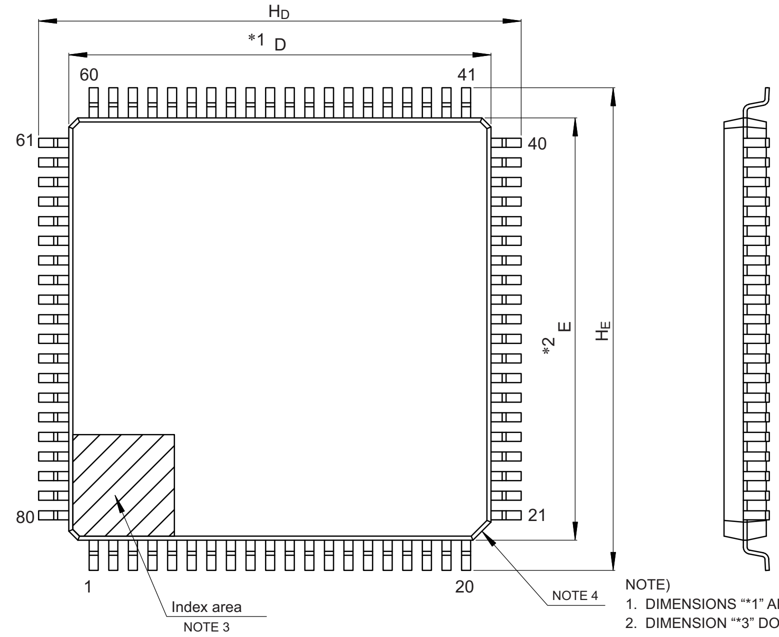
Contact a Renesas Electronics sales office for details.

3.9 80-Pin Products

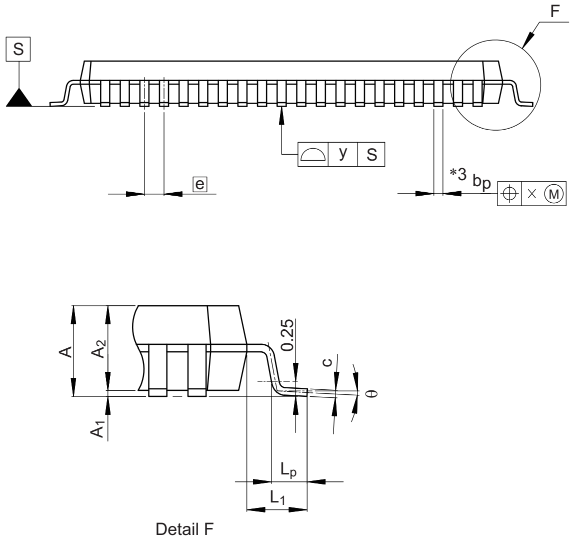
R7F100GMG3CFA, R7F100GMH3CFA, R7F100GMJ3CFA, R7F100GMK3CFA,
R7F100GML3CFA, R7F100GMN3CFA
R7F100GMG2DFA, R7F100GMH2DFA, R7F100GM2DFA, R7F100GMK2DFA,
R7F100GML2DFA, R7F100GMN2DFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LQFP80-14x14-0.65	PLQP0080JA-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.22	0.30	0.38
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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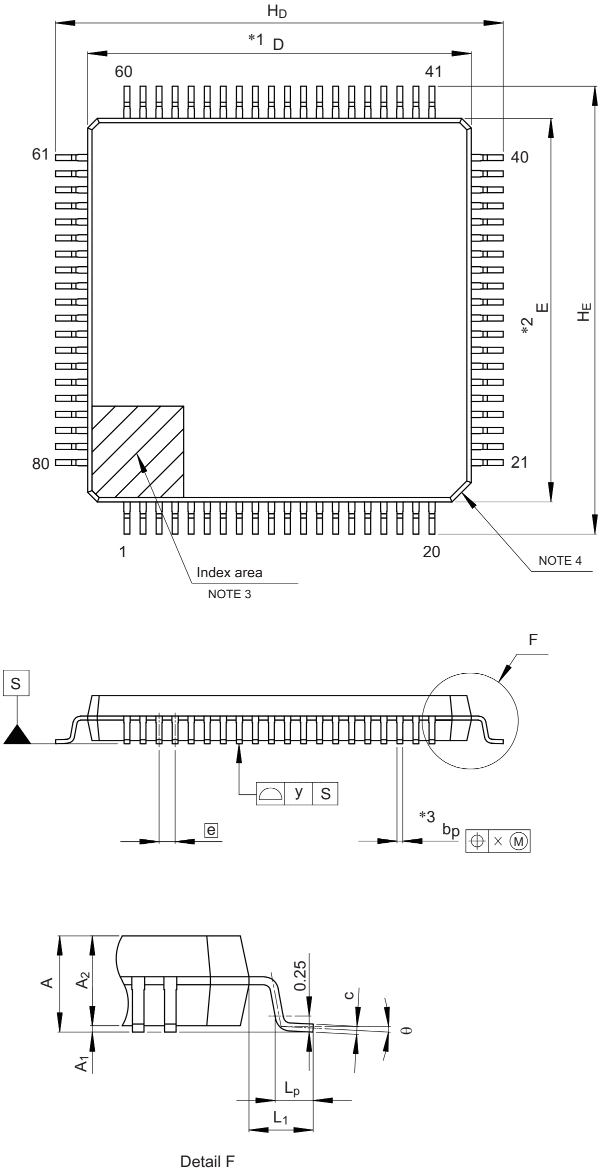
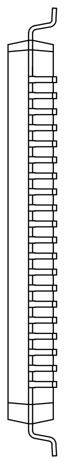
R7F100GMG3CFB, R7F100GMH3CFB, R7F100GMJ3CFB, R7F100GMK3CFB,
R7F100GML3CFB, R7F100GMN3CFB
R7F100GMG2DFB, R7F100GMH2DFB, R7F100GM2DFB, R7F100GMK2DFB,
R7F100GML2DFB, R7F100GMN2DFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5

Unit: mm



Detail F



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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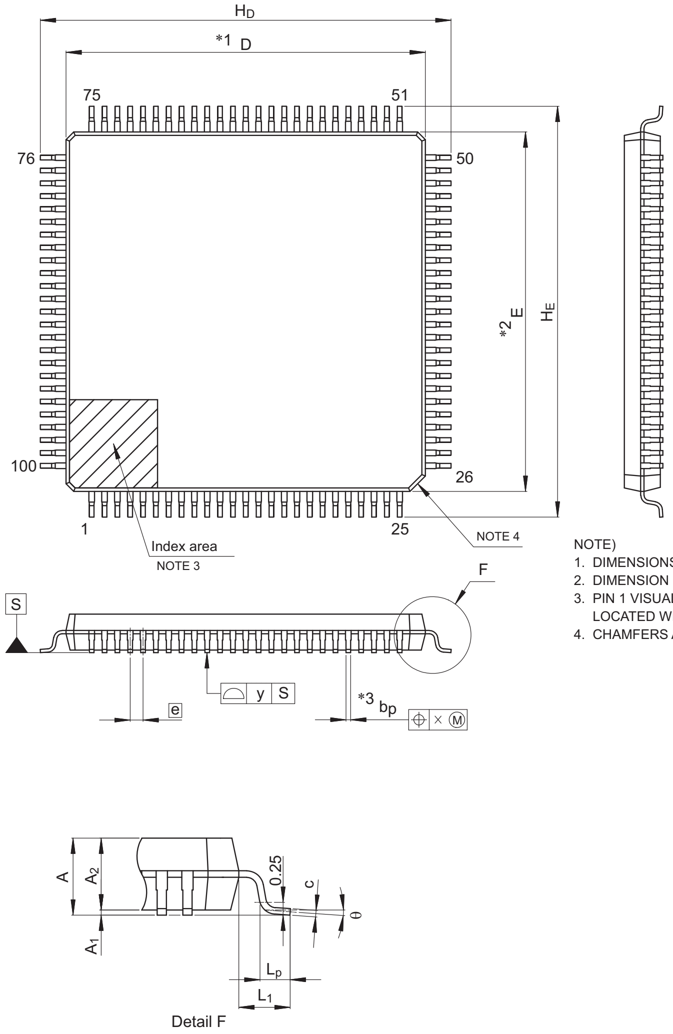
3.10 100-Pin Products

R7F100GPG3CFB, R7F100GPH3CFB, R7F100GPJ3CFB, R7F100GPK3CFB,
R7F100GPL3CFB, R7F100GPN3CFB
R7F100GPG2DFB, R7F100GPH2DFB, R7F100GPJ2DFB, R7F100GPK2DFB,
R7F100GPL2DFB, R7F100GPN2DFB

JEITA Package Code	**RENESAS Code**	**Previous Code**	**MASS (Typ) [g]**
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

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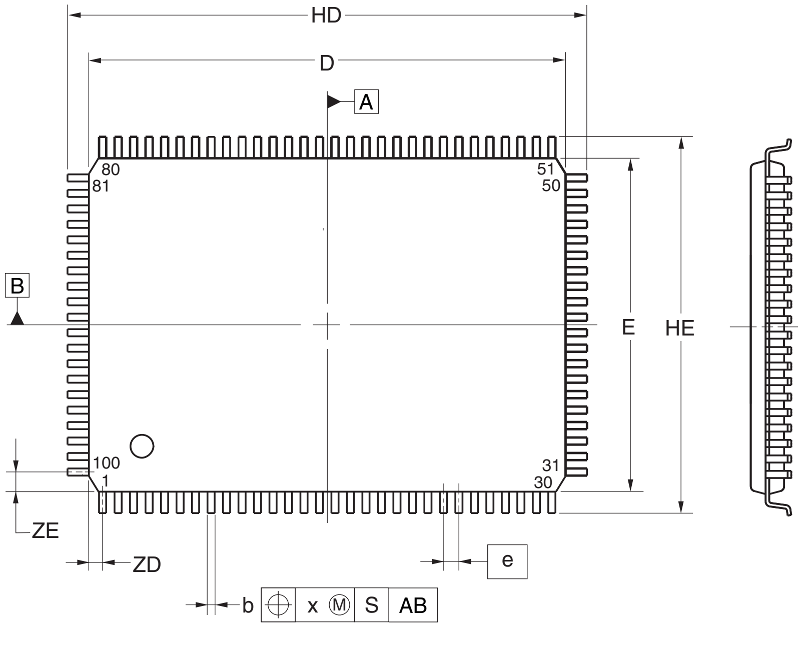
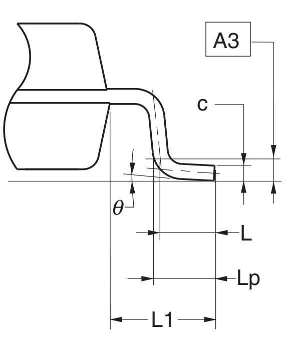
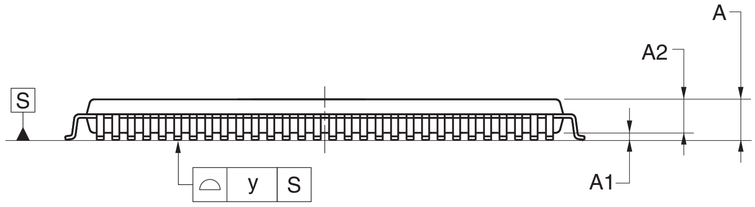
R7F100GPG3CFA, R7F100GPH3CFA, R7F100GPJ3CFA, R7F100GPK3CFA,
R7F100GPL3CFA, R7F100GPN3CFA
R7F100GPG2DFA, R7F100GPH2DFA, R7F100GPJ2DFA, R7F100GPK2DFA,
R7F100GPL2DFA, R7F100GPN2DFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



detail of lead end





(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825

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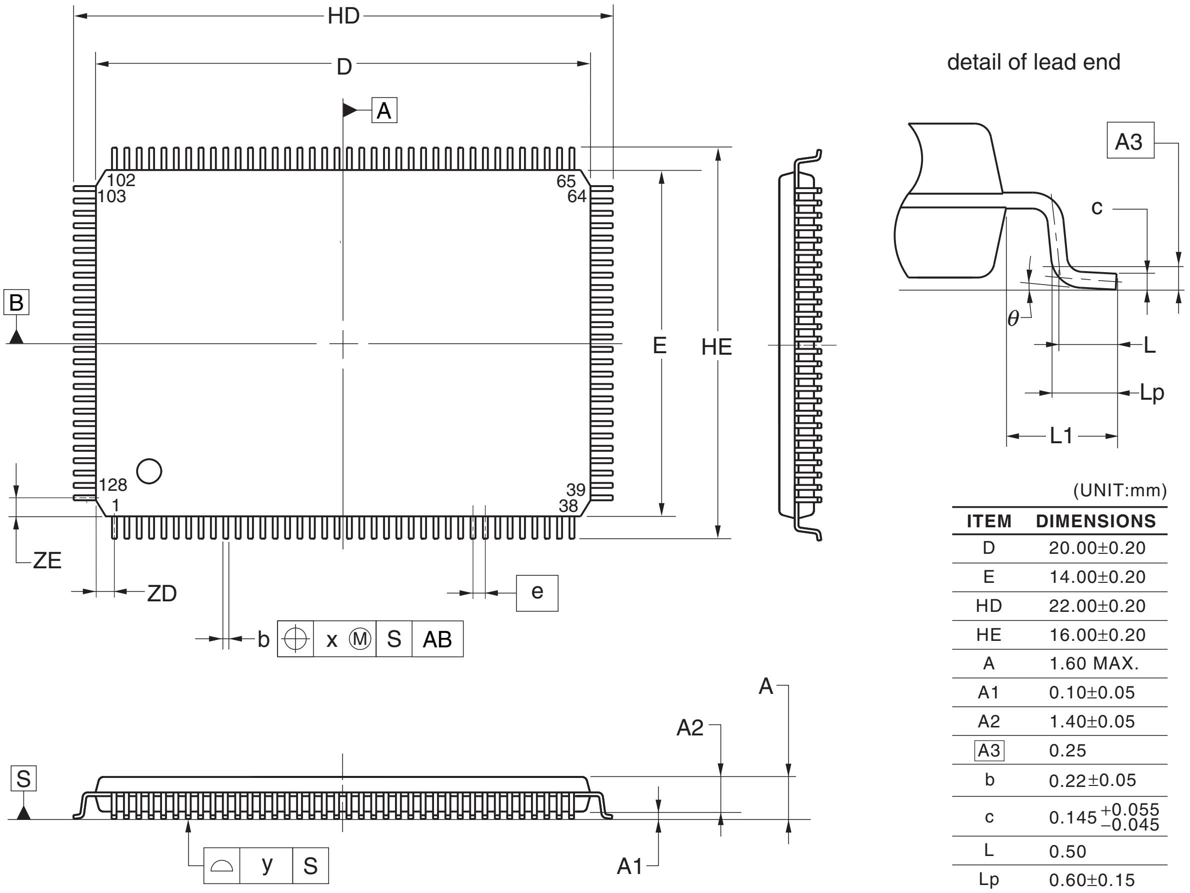
3.11 128-Pin Products

R7F100GSJ3CFB, R7F100GSK3CFB, R7F100GSL3CFB, R7F100GSN3CFB
R7F100GSJ2DFB, R7F100GSK2DFB, R7F100GSL2DFB, R7F100GSN2DFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92


HD
D
A
102
103
65
64
B
E
HE
128
1
39
38
ZE
ZD
e
b
x
M
S
AB
S
y
S
A
A2
A1
detail of lead end
A3
c
θ
L
Lp
L1

(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{\text{A3}}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
$\boxed{\text{e}}$	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

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REVISION HISTORY	RL78/G23 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 13, 2021	—	First edition issued
1.10	Nov 18, 2021	All	The module name for 3-wire SPI was changed to simplified SPI.
		All	The module name for SPI was changed to simplified SPI.
		p.1	The operating current in the title was modified.
		p.1	1.1 Features: The descriptions of Middle-speed on-chip oscillator were modified.
		p.2	1.1 Features: The descriptions of Timers were modified.
		p.4	Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23 was modified.
		p.11	1.3.4 40-pin products: Figure was modified.
		p.12	1.3.5 44-pin products: Figure was modified.
		p.13	1.3.6 48-pin products: Note 2 was modified.
		p.13	1.3.6 48-pin products: Remark 3 was added.
		p.23	1.5 Block Diagram was modified.
		p.24 to p.26	1.6 Outline of Functions [30-, 32-, 36-, 40-, 44-, and 48-pin products]: The descriptions were modified.
		p.27 to p.29	1.6 Outline of Functions [52-, 64-, 80-, 100-, and 128-pin products]: The descriptions were modified.
		p.31	2.1 Absolute Maximum Ratings: Note was modified.
		p.32	2.2.1 Characteristics of the X1 and XT1 oscillators: Condition was modified.
		p.35	2.3.1 Pin characteristics: Notes 4 to 6 were modified.
		p.36, p.37	2.3.1 Pin characteristics: Notes 3, 5, and 6 were modified.
		p.43 to p.49	2.3.2 Supply current characteristics, (1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM: The descriptions in the tables were modified.
		p.50 to p.56	2.3.2 Supply current characteristics, (2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM was added.
		p.57 to p.63	2.3.2 Supply current characteristics, (3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products was added.
		p.64 to p.66	2.3.2 Supply current characteristics, (4) Peripheral Functions (Common to all products): The descriptions in the tables were added. Notes 13, 14, and 16 were modified. Note 19 was modified.
		p.102	2.5.2 Serial interface UARTA: The table was modified.
		p.106	2.6.1 A/D converter characteristics, (1) Normal modes 1 and 2: The descriptions in the table were modified.
		p.108	2.6.1 A/D converter characteristics, (2) Low-voltage modes 1 and 2: The descriptions in the table were modified.
		P.110	2.6.1 A/D converter characteristics, (3) When the internal reference voltage is selected as reference voltage (+): The descriptions in the table were modified.
		p.111	2.6.4 Comparator characteristics: The descriptions in the table were modified.
		p.114	2.6.6 LVD circuit characteristics, (2) LVD1 Detection Voltage of Reset Mode and Interrupt Mode: The table was modified.

Rev.	Date	Description	
		Page	Summary
1.10	Nov 18, 2021	p.117	2.8 Flash Memory Programming Characteristics, (2) Data flash memory: The descriptions in the table were modified.
		p.123	3.4 40-Pin Products: The figure was added.
		p.126	3.6 48-Pin Products: The figure was added.

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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