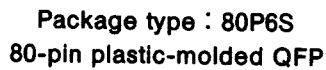
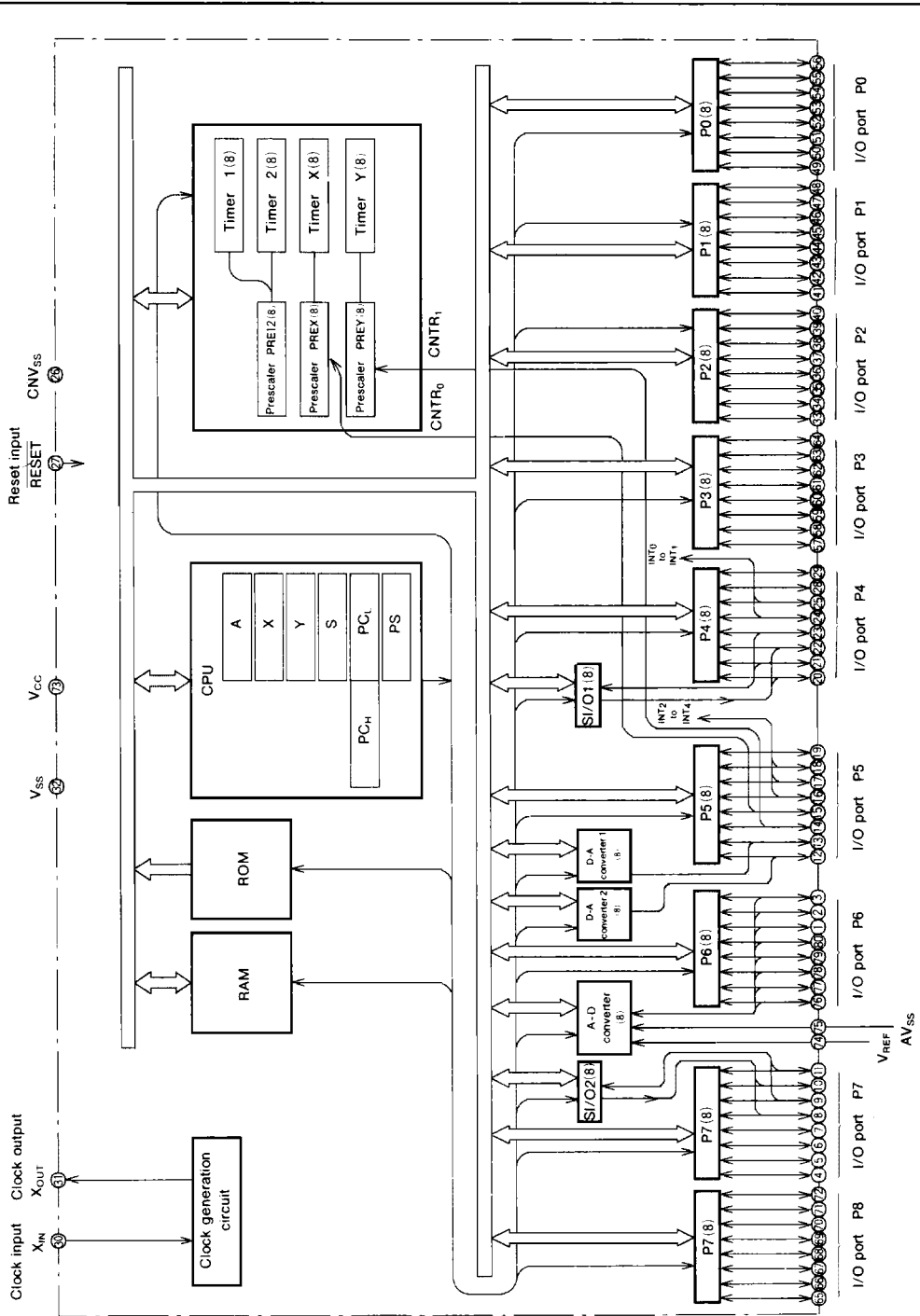


PIN CONFIGURATION (TOP VIEW)



SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N)



MITSUBISHI MICROCOMPUTERS
M3806x Group

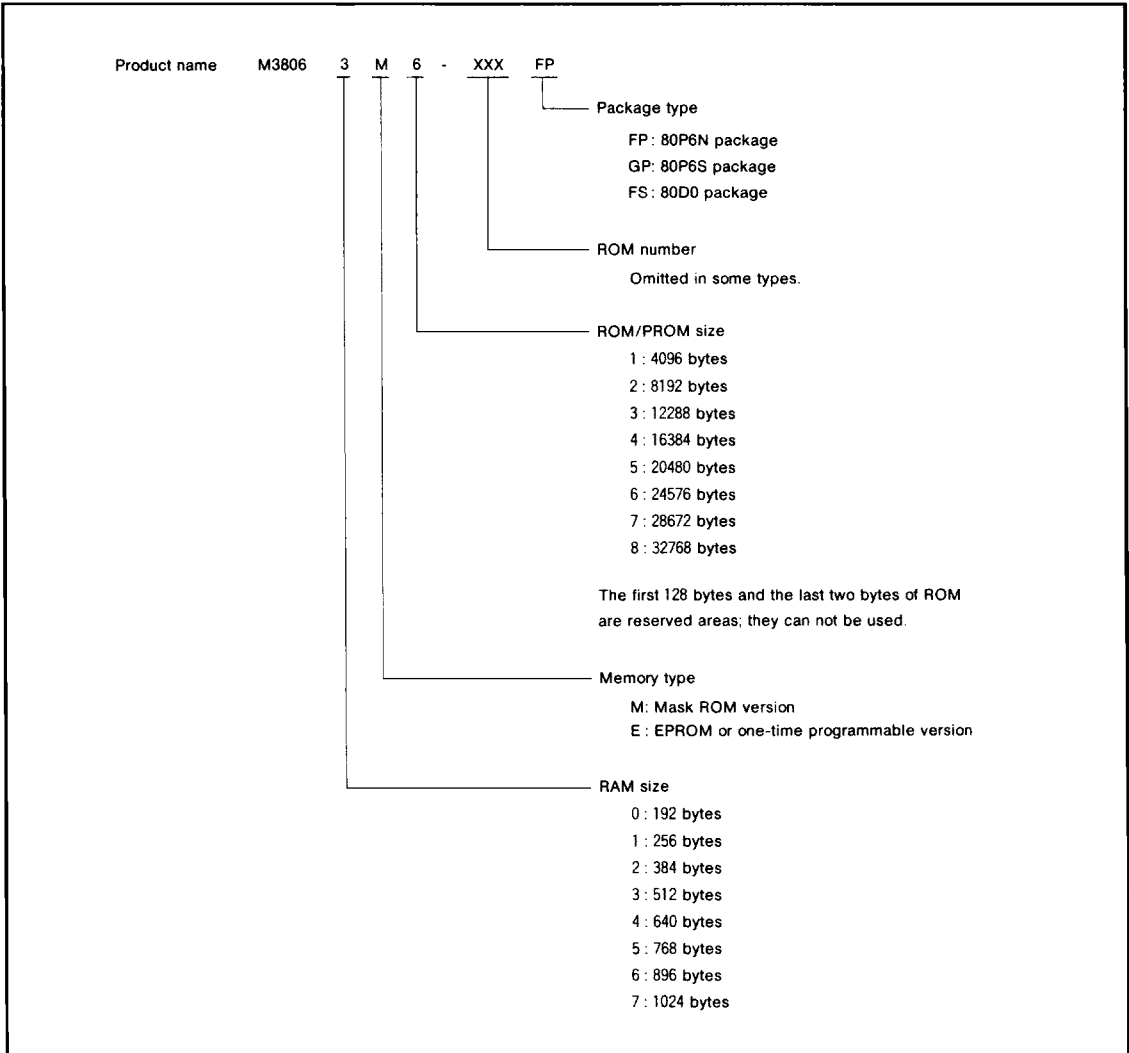
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Function	Alternate Function
V _{CC}	Power supply	Power supply inputs 4.0 to 5.5V to V _{CC} , and 0V to V _{SS} .	
V _{SS}			
CNV _{SS}	CNV _{SS}	This pin controls the operation mode of the chip. Normally connected to V _{SS} . If this pin is connected to V _{CC} , the internal ROM is inhibited and external memory is accessed.	
V _{REF}	Analog reference voltage	Reference voltage input pin for A-D and D-A converters.	
AV _{SS}	Analog power supply	GND input pin for A-D and D-A converter. Keep at the same potential as V _{SS} .	
RESET	Reset input	To reset the microcomputer, this pin should be kept at an "L" level for more than 2μs under normal operating conditions.	
X _{IN}	Clock input	Input and output signals for the internal clock generation circuit. Connect a ceramic resonator or quartz crystal between the X _{IN} and X _{OUT} pins to set the oscillation frequency. If an external clock is used, connect the clock source to the X _{IN} pin and leave the X _{OUT} pin open.	
X _{OUT}	Clock output		
P0 ₀ —P0 ₇	I/O port P0	An 8 bit CMOS I/O port. An I/O direction register allows each pin to be individually programmed as either input or output. At reset this port is set to input mode. In modes other than single-chip, these pins are used as address, data, and control bus I/O pins.	
P1 ₀ —P1 ₇	I/O port P1		
P2 ₀ —P2 ₇	I/O port P2		
P3 ₀ —P3 ₇	I/O port P3		
P4 ₀ , P4 ₁	I/O port P4	An 8-bit CMOS I/O port with the same function as port P0.	
P4 ₂ /INT ₀ , P4 ₃ /INT ₁			External interrupt input pin
P4 ₄ /R _X D, P4 ₅ /T _X D, P4 ₆ /S _{CLK1} , P4 ₇ /S _{RDY1}			Serial I/O1 I/O pins
P5 ₀			
P5 ₁ /INT ₂ — P5 ₃ /INT ₄	I/O port P5	An 8-bit CMOS I/O port with the same function as port P0.	External interrupt input pin
P5 ₄ /CNTR ₀ , P5 ₅ /CNTR ₁			Timer X and Timer Y I/O pins
P5 ₆ /DA ₁ , P5 ₇ /DA ₂			D-A converter output pins
P5 ₀			
P6 ₀ /AN ₀ — P6 ₇ /AN ₇	I/O port P6	An 8-bit CMOS I/O port with the same function as port P0.	A-D converter input pins
P7 ₀ /S _{IN2} , P7 ₁ /S _{OUT2} , P7 ₂ /S _{CLK2} , P7 ₃ /S _{RDY2}	I/O port P7	An 8-bit I/O port with the same function as port P0. The output structure of this port is N-channel open drain, and the input levels are CMOS compatible.	Serial I/O2 I/O pins
P7 ₄ —P7 ₇			
P8 ₀ —P8 ₇	I/O port P8	An 8-bit CMOS I/O port with the same function as port P0.	

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PART NUMBERING



MITSUBISHI MICROCOMPUTERS
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GROUP EXPANSION

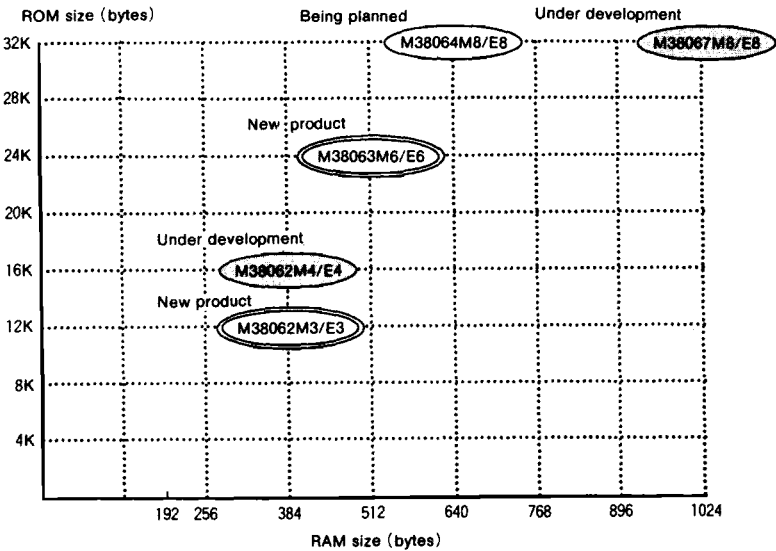
Mitsubishi plans to expand the M3806x group as follows:

- (1) Support for mask ROM, one-time programmable, and EPROM versions
ROM/PROM capacity 12K to 32K bytes
RAM capacity 384 to 1024 bytes

(2) Packages

- 80P6N 0.8mm-pitch plastic molded QFP
80P6S 0.65mm-pitch plastic molded QFP
80D0 0.8mm-pitch ceramic LCC

Memory expansion plan



The development schedule and other details of products under development may be revised without notice.
Currently supported products are listed below.

As of March 1992

Product name	(P) ROM size (bytes)	RAM size (bytes)	Package	Remarks
M38062M3-XXXFP	12K	384	80P6N	Mask ROM version
M38062E3-XXXFP				One-time programmable version
M38062E3FP				One-time programmable version (blank)
M38062M3-XXXGP			80P6S	Mask ROM version
M38062E3-XXXGP				One-time programmable version
M38062E3GP				One-time programmable version (blank)
M38062E3FS			80D0	EPROM version
M38062M6-XXXFP	24K	512	80P6N	Mask ROM version
M38062E6-XXXFP				One-time programmable version
M38063E6FP				One-time programmable version (blank)
M38063M6-XXXGP			80P6S	Mask ROM version
M38063E6-XXXGP				One-time programmable version
M38063E6GP				One-time programmable version (blank)
M38063E6FS			80D0	EPROM version

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

Microcomputers of the M3806x group use the standard MELPS 740 instruction set. Refer to the table of MELPS 740 addressing modes and machine instructions or the MELPS 740 Software Manual for details on the instruction set.

Machine-resident MELPS 740 instructions are as follows:

The FST and SLW instructions are not available for use.

The STP, WIT, MUL, and DIV instructions can be used.

CPU Mode Register

The CPU mode register (address 003B₁₆) contains processor mode bits that specify the operating mode of the chip. The CPU mode register also contains the stack page select bit.

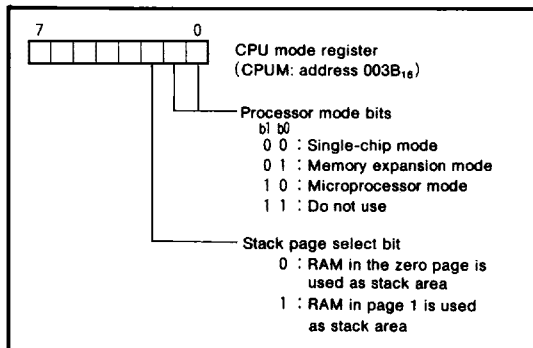


Fig. 1 Structure of CPU mode register

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

MEMORY

• Special Function Register (SFR) Area

The Special Function Register area contains registers which control functions such as I/O ports and timers, and is located in the zero page area.

• RAM

RAM is used for data storage as well for stack area.

• ROM

The first 128 bytes and the last two bytes of ROM are reserved for device testing and the rest is user area for storing programs.

• Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

• Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. This dedicated zero page addressing mode enables access to this area with only 2 bytes.

• Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. This dedicated special page addressing mode enables access to this area with only 2 bytes.

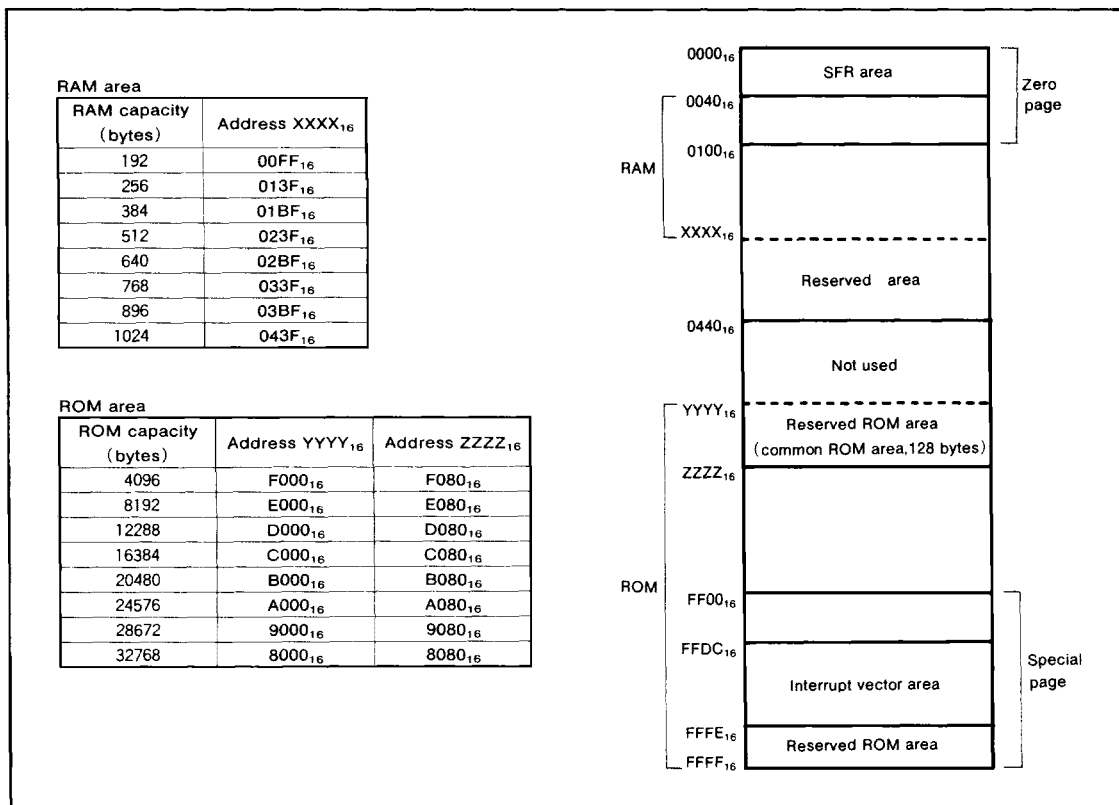


Fig. 2 Memory map diagram

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Prescaler 12 (PRE12)
0001 ₁₆	Port P0 direction register (P0D)	0021 ₁₆	Timer 1 (T1)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer 2 (T2)
0003 ₁₆	Port P1 direction register (P1D)	0023 ₁₆	Timer XY mode register (TM)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Prescaler X (PREX)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer X (TX)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Prescaler Y (PREY)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer Y (TY)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	
000A ₁₆	Port P5 (P5)	002A ₁₆	
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	
000C ₁₆	Port P6 (P6)	002C ₁₆	
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	
0012 ₁₆		0032 ₁₆	
0013 ₁₆		0033 ₁₆	
0014 ₁₆		0034 ₁₆	AD/DA control register (ADCON)
0015 ₁₆		0035 ₁₆	A-D conversion register (AD)
0016 ₁₆		0036 ₁₆	D-A1 conversion register (DA1)
0017 ₁₆		0037 ₁₆	D-A2 conversion register (DA2)
0018 ₁₆	Transmit/receive buffer 1 (TB1/RB1)	0038 ₁₆	
0019 ₁₆	Serial I/O1 status register (SIO1STS)	0039 ₁₆	
001A ₁₆	Serial I/O1 control register (SIO1CON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1 (IREQ1)
001D ₁₆	Serial I/O2 control register (SIO2CON)	003D ₁₆	Interrupt request register 2 (IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1 (ICON1)
001F ₁₆	Serial I/O2 register (SIO2)	003F ₁₆	Interrupt control register 2 (ICON2)

Fig. 3 Memory map of special function register (SFR)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

I/O PORTS

Direction Registers

The M3806x group microprocessors have 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input or output. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin, which is set for output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref. No.
P0 ₀ —P0 ₇	Port P0	Input/output, individual bits	CMOS 3-state output CMOS level input	Address lower-byte output	CPU mode register	(1)
P1 ₀ —P1 ₇	Port P1	Input/output, individual bits	CMOS 3-state output CMOS level input	Address upper-byte output	CPU mode register	
P2 ₀ —P2 ₇	Port P2	Input/output, individual bits	CMOS 3-state output CMOS level input	Data bus I/O	CPU mode register	
P3 ₀ —P3 ₇	Port P3	Input/output, individual bits	CMOS 3-state output CMOS level input	Control signal I/O	CPU mode register	
P4 ₀ , P4 ₁ P4 ₂ /INT ₀ , P4 ₃ /INT ₁	Port P4	Input/output, individual bits	CMOS 3-state output CMOS level input	External interrupt input	Interrupt edge selection register	(2)
P4 ₄ /R _X D, P4 ₅ /T _X D, P4 ₆ /SCLK ₁ , P4 ₇ /SRDY ₁				Serial I/O1 function I/O	Serial I/O control register	(3)
					UART control register	(4)
						(5)
P5 ₀	Port P5	Input/output, individual bits	CMOS 3-state output CMOS level input			(6)
P5 ₁ /INT ₂ , P5 ₂ /INT ₃ , P5 ₃ /INT ₄				External interrupt input	Interrupt edge selection register	(1)
P5 ₄ /CNTR ₀ , P5 ₅ /CNTR ₁				Timer XY function I/O		(2)
P5 ₆ /DA ₁ , P5 ₇ /DA ₂				D-A converter output	AD/DA control register	(7)
P6 ₀ /AN ₀ — P6 ₇ /AN ₇	Port P6	Input/output, individual bits	CMOS 3-state output CMOS level input	A-D converter input		(8)
P7 ₀ /SIN ₂ , P7 ₁ /SOUT ₂ , P7 ₂ /SCLK ₂ , P7 ₃ /SRDY ₂	Port P7	Input/output, individual bits	N-channel open-drain output CMOS level input	Serial I/O2 function I/O	Serial I/O2 control register	(9)
						(10)
						(11)
						(12)
P7 ₄ —P7 ₇	Port P8	Input/output, individual bits	CMOS 3-state output CMOS level input			(13)
						(14)
P8 ₀ —P8 ₇	Port P8	Input/output, individual bits	CMOS 3-state output CMOS level input			(1)

Note : For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, see the applicable sections.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

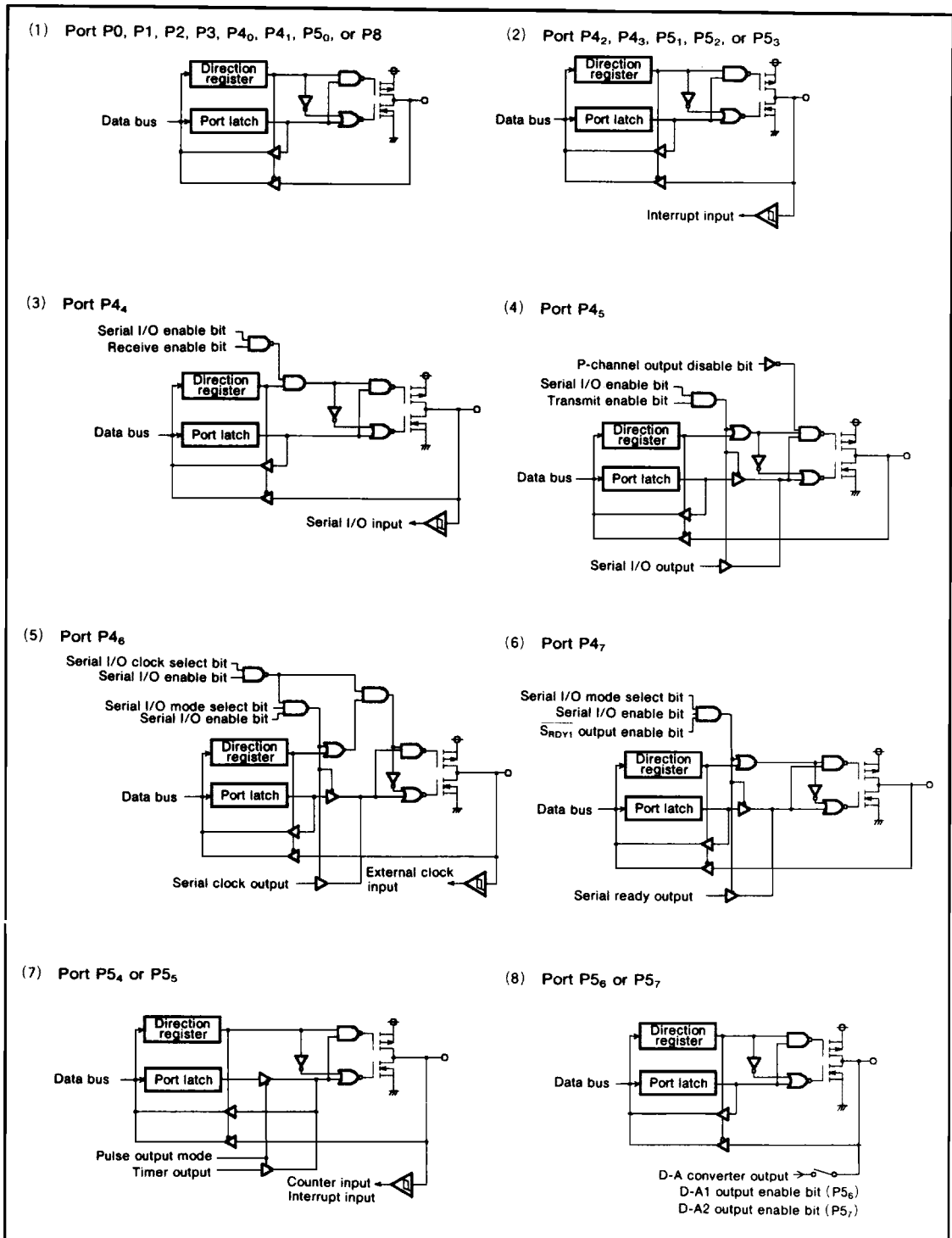


Fig. 4 Port block diagram (single-chip mode) (1)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

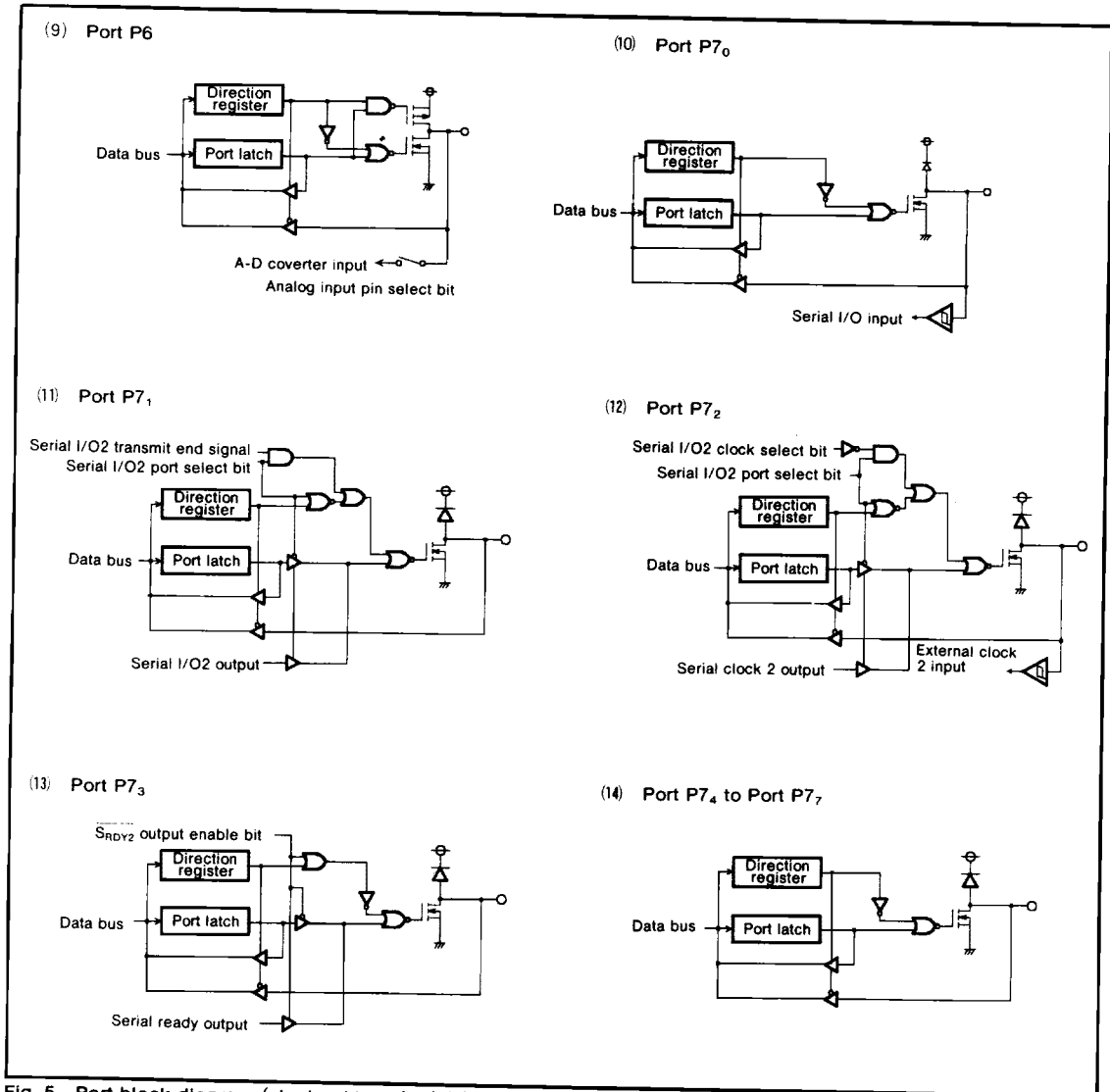


Fig. 5 Port block diagram (single-chip mode) (2)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

INTERRUPTS

A total of 16 sources can generate interrupts: 7 external, 8 internal, and 1 software.

● Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag—except for the software interrupt set by the BRK instruction. An interrupt is generated if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”. Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software.

The I flag disables all interrupts except for the BRK instruction interrupt.

● Interrupt Operation

When an interrupt is received, the program counter and processor status register are automatically pushed onto the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

● Notes on Use

When the active edge of an external interrupt (INT₀ to INT₄, CNTR₀, or CNTR₁) is changed, the corresponding interrupt request bit may also be set. To insure proper operation when selecting the active edge, disable interrupts before setting the interrupt edge selection.

Table 1 Interrupt vector addresses and priorities

Interrupt cause	Priority	Vector address (Note 1)		Interrupt request generation conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT ₀	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT ₀ input	External interrupt (active edge selectable)
INT ₁	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT ₁ input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF7 ₁₆	FFF6 ₁₆	At end of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF5 ₁₆	FFF4 ₁₆	At end of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF3 ₁₆	FFF2 ₁₆	At timer X overflow	
Timer Y	7	FFF1 ₁₆	FFF0 ₁₆	At timer Y overflow	
Timer 1	8	FFEF ₁₆	FFEE ₁₆	At timer 1 overflow	STP release timer overflow
Timer 2	9	FFED ₁₆	FFEC ₁₆	At timer 2 overflow	
CNTR ₀	10	FFEB ₁₆	FFEA ₁₆	At detection of either rising or falling edge of CNTR ₀ input	External interrupt (active edge selectable)
CNTR ₁	11	FFE9 ₁₆	FFE8 ₁₆	At detection of either rising or falling edge of CNTR ₁ input	External interrupt (active edge selectable)
Serial I/O2	12	FFE7 ₁₆	FFE6 ₁₆	At end of serial I/O2 data transfer	Valid when serial I/O2 is selected
INT ₂	13	FFE5 ₁₆	FFE4 ₁₆	At detection of either rising or falling edge of INT ₂ input	External interrupt (active edge selectable)
INT ₃	14	FFE3 ₁₆	FFE2 ₁₆	At detection of either rising or falling edge of INT ₃ input	External interrupt (active edge selectable)
INT ₄	15	FFE1 ₁₆	FFE0 ₁₆	At detection of either rising or falling edge of INT ₄ input	External interrupt (active edge selectable)
A-D converter	16	FFDF ₁₆	FFDE ₁₆	At end of A-D conversion	
BRK instruction	17	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Note 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

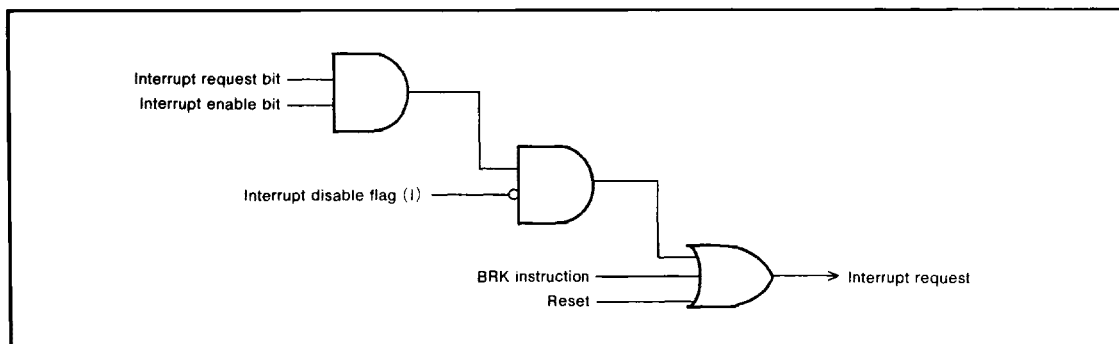


Fig. 6 Interrupt control

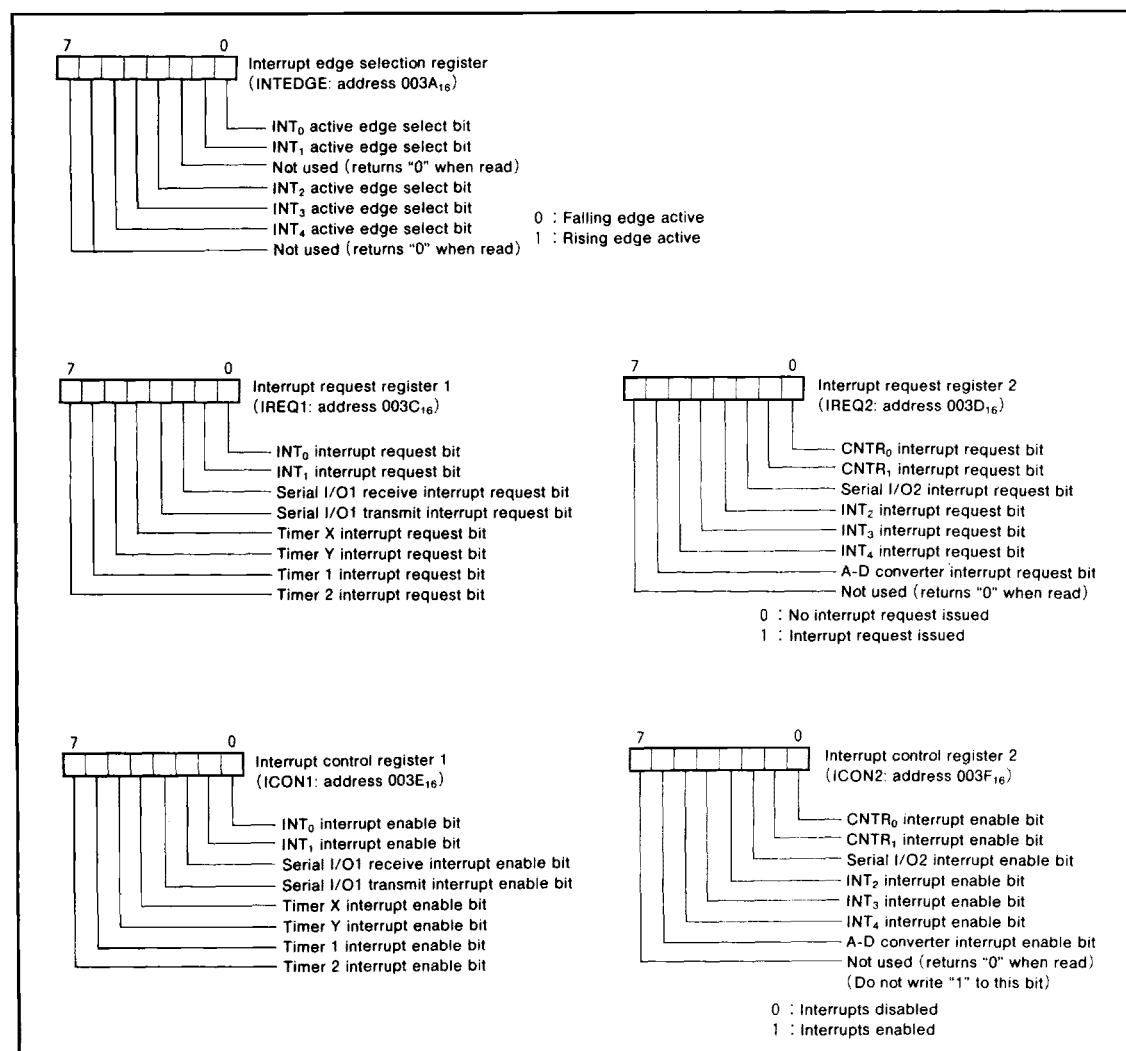


Fig. 7 Structure of interrupt-related registers

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

TIMERS

Microcomputers of the M3806x group have 4 timers: timer X, timer Y, timer 1, and timer 2.

The timers count down. Once a timer reaches 00_{16} , the next count pulse reloads the contents of the corresponding timer latch into the timer, and sets the corresponding interrupt request bit to 1.

The divide ratio of each timer or prescaler is given by $1/(n+1)$, where n is the value in the corresponding timer or prescaler latch.

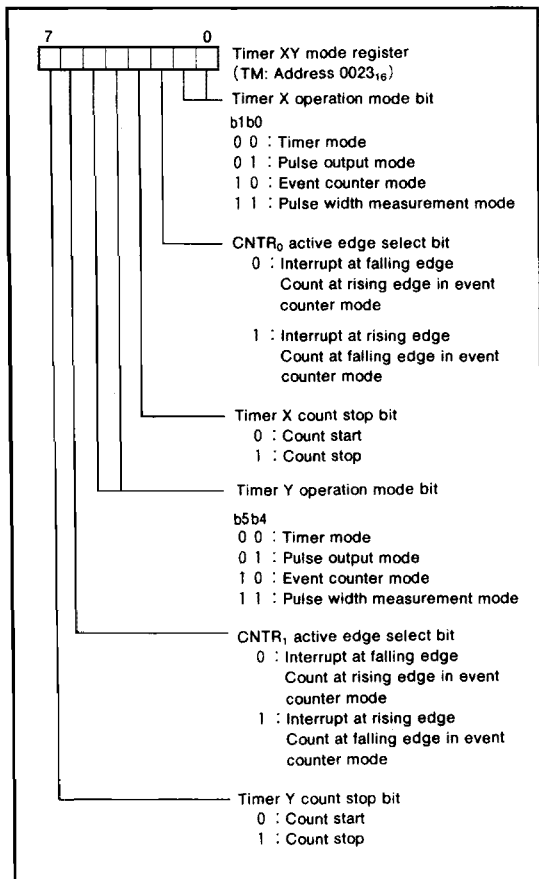


Fig. 8 Structure of timer XY register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer overflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each be set to operate in one of four operating modes by setting the timer XY mode register.

1. Timer Mode

In timer mode, the timer counts a signal that is the oscillation frequency divided by 16.

2. Pulse Output Mode

Timer X (or timer Y) counts a signal which is the oscillation frequency divided by 16. Whenever the contents of the timer reach "0", the signal output from the CNTR₀ (or CNTR₁) pin is inverted. If the CNTR₀ (or CNTR₁) active edge select bit is "0", output begins at "H". If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P5₄ (or port P5₅) direction register to output mode.

3. Event Counter Mode

Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the CNTR₀ or CNTR₁ pin.

4. Pulse Width Measurement Mode

If the CNTR₀ (or CNTR₁) active edge select bit is "0", the timer counts at the oscillation frequency divided by 16 while the CNTR₀ (or CNTR₁) pin is at "H". If the CNTR₀ (or CNTR₁) active edge select bit is "1", the count continues during the time that the CNTR₀ (or CNTR₁) pin is at "L".

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer overflows, the corresponding interrupt request bit is set.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

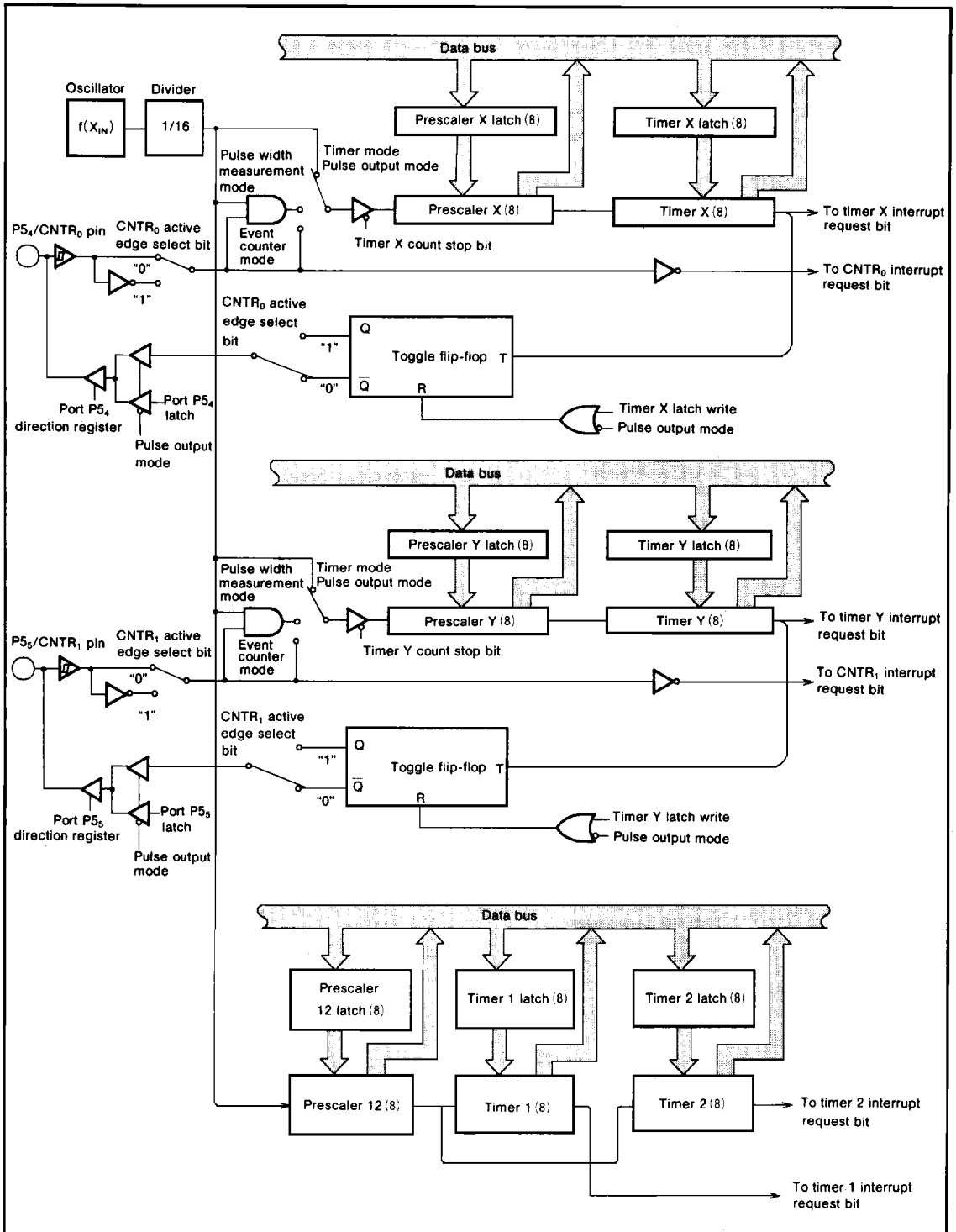


Fig. 9 Block diagram of timer X, timer Y, timer 1, and timer 2

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O1 mode can be selected by

setting the mode select bit of the serial I/O1 control register to "1".

For clock-synchronized serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit or receive buffer.

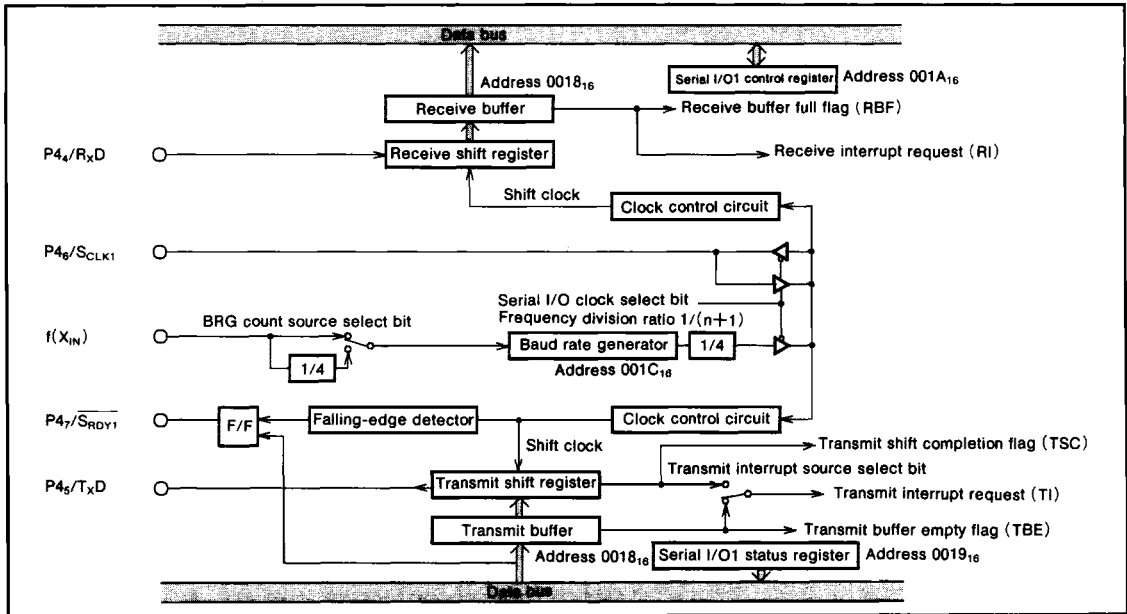


Fig. 10 Block diagram of clock-synchronized serial I/O1

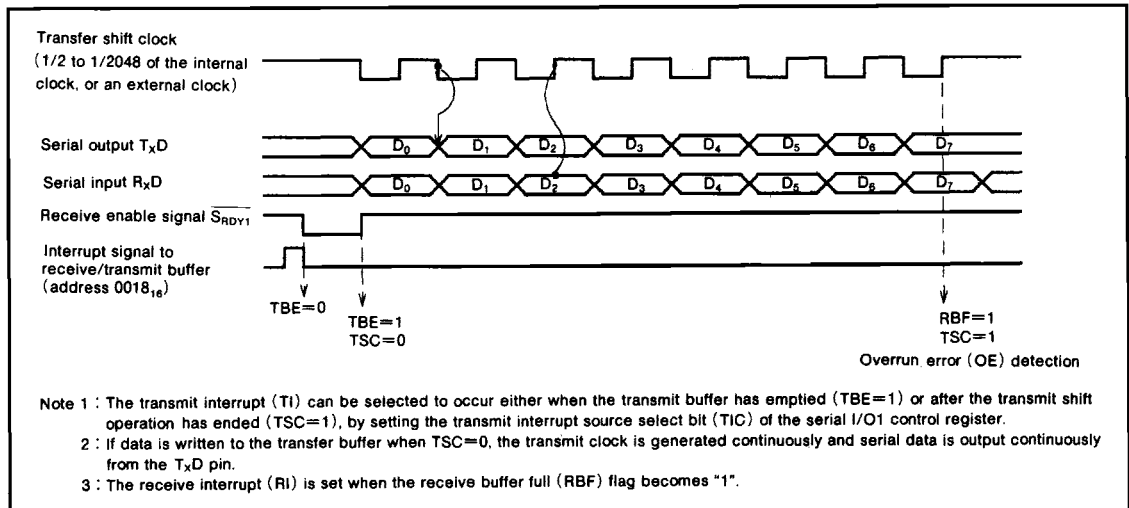


Fig. 11 Operation of clock-synchronized serial I/O1 function

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

(2) Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode select bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in mem-

ory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

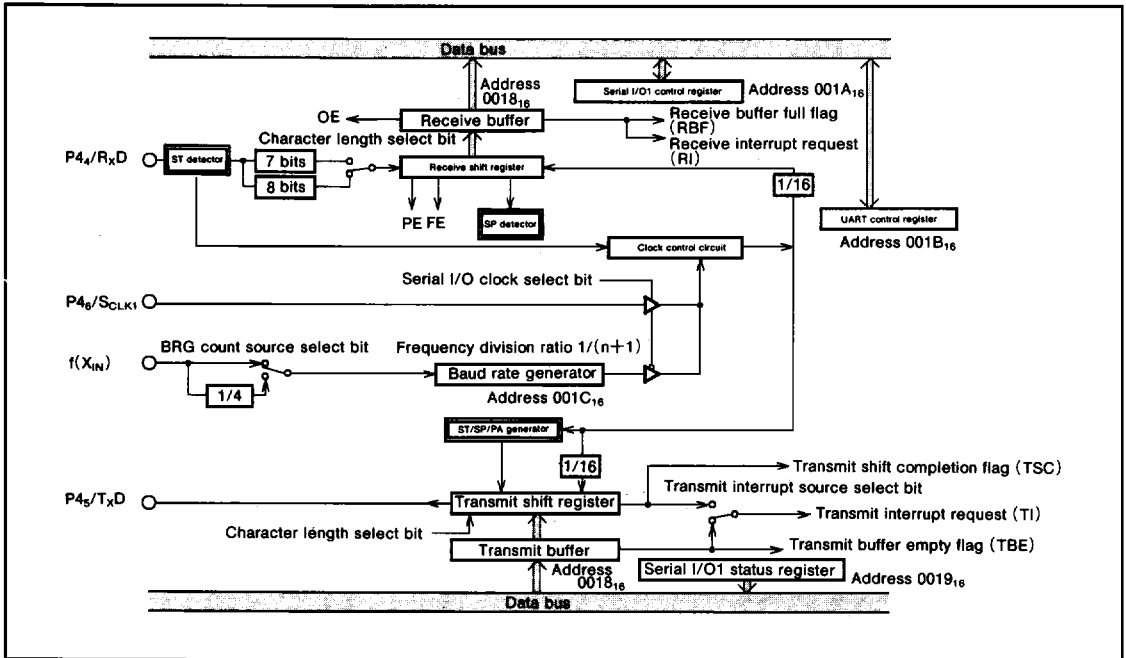


Fig. 12 Block diagram of UART serial I/O

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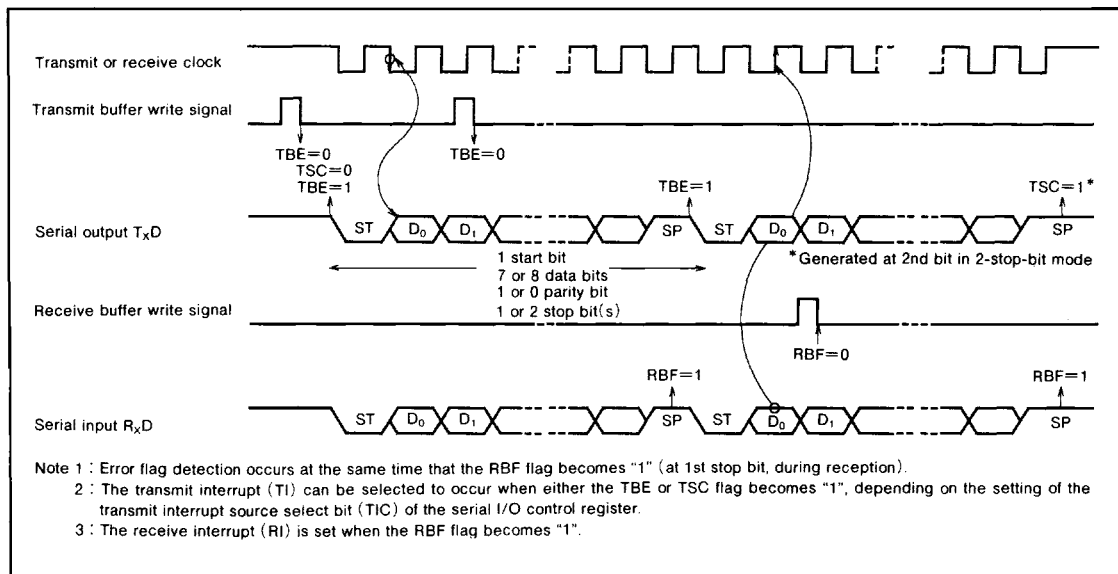


Fig. 13 Operation of UART serial I/O function

[Serial I/O Control Register (SIO1CON) 001A₁₆]

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON) 001B₁₆]

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4₅/T_xD pin.

[Serial I/O1 Status Register (SIO1STS) 0019₁₆]

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE,

FE, and SE (bit 3 to bit six, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmitter shift completion flag (bit 2) and the transmitter buffer empty flag (bit 0) become "1".

[Transmit Buffer/Receive Buffer (TB/RB) 0018₁₆]

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator (BRG) 001C₁₆]

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n+1)$, where n is the value written to the Baud Rate Generator.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

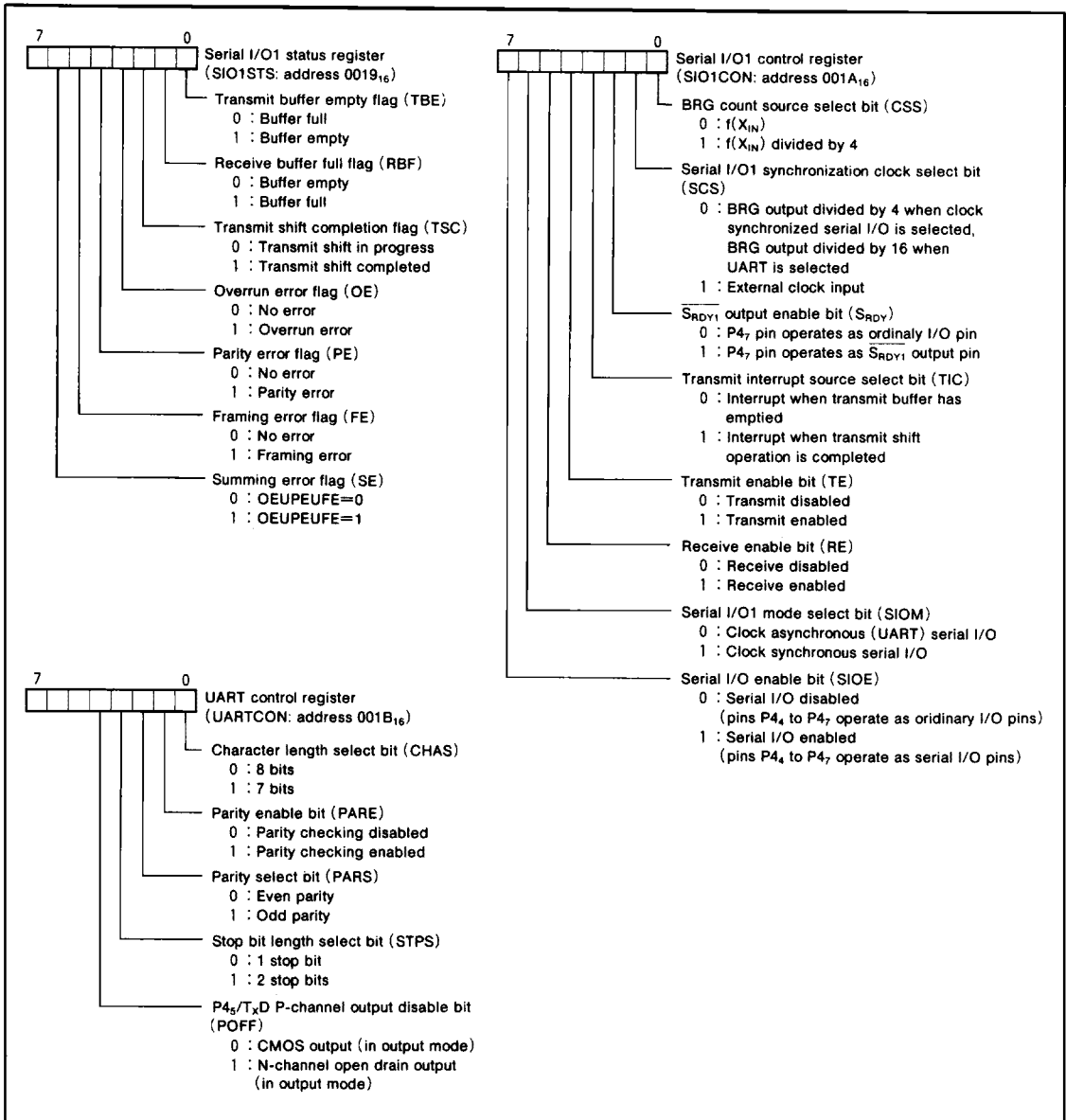


Fig. 14 Structure of serial I/O control registers

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SERIAL I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

Serial I/O2 Control Register (SIO2CON) 001D₁₆

The serial I/O2 control register contains seven bits which control various serial I/O functions.

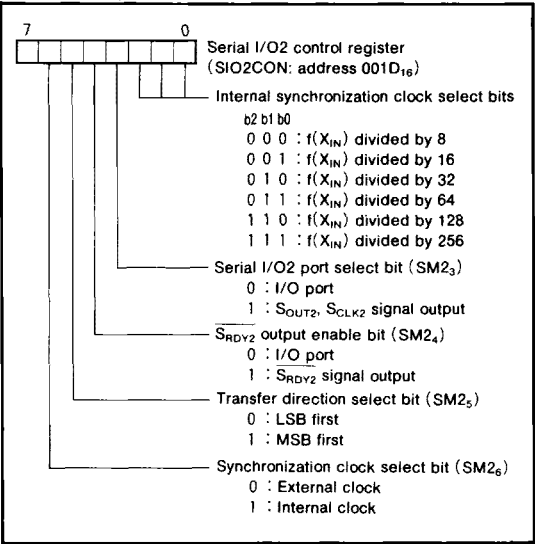


Fig. 15 Structure of serial I/O2 control register

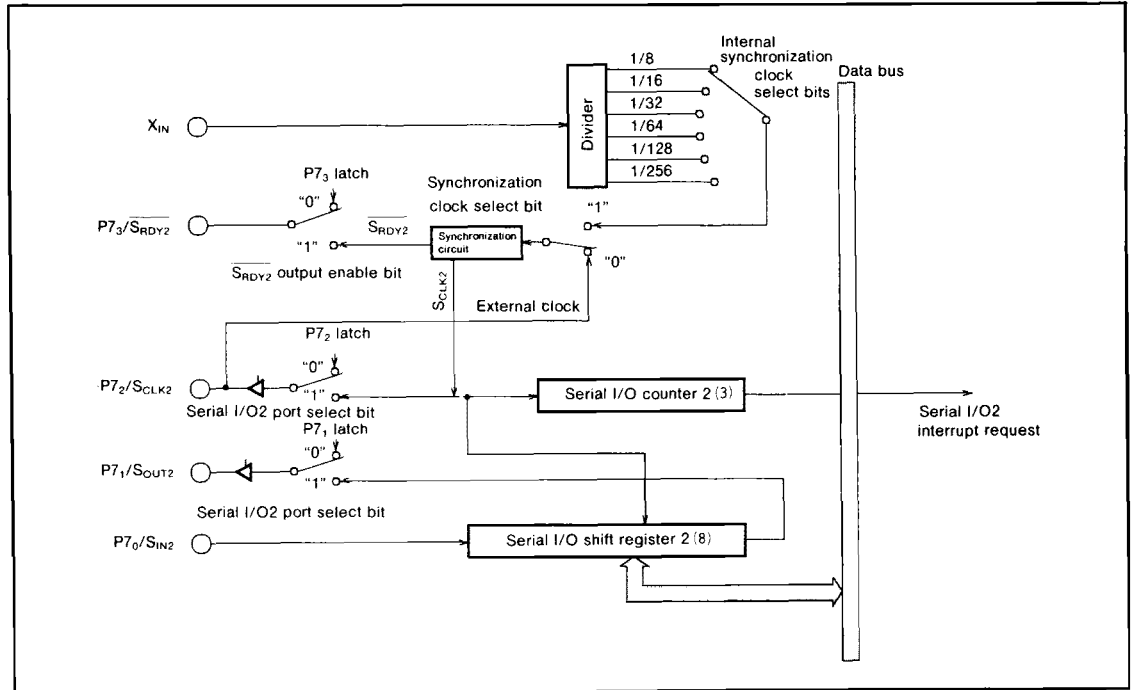


Fig. 16 Block diagram of serial I/O2 function

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

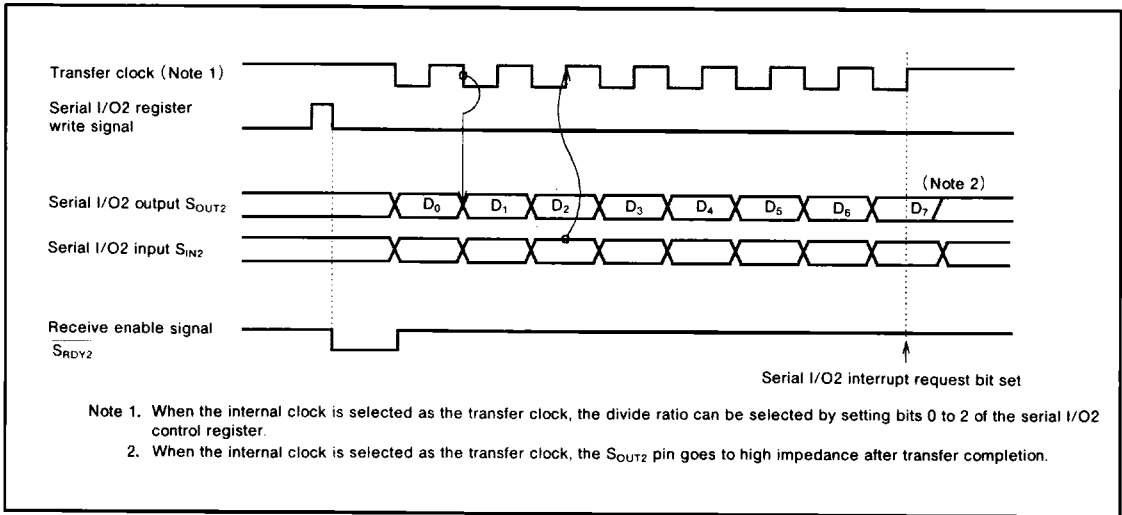


Fig. 17 Timing of serial I/O2 function

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register]

The A-D conversion register is a read-only register which contains the result of an A-D conversion. This register should not be read during an A-D conversion.

[AD/DA Control Register]

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bits 6 and 7 are used to control the output of the D-A converter.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV_{SS} and V_{REF} into 256 steps for comparison to the analog input.

[Channel Selector]

The channel selector selects one of the ports $P6_0/AN_0$ to $P6_7/AN_7$, and inputs the voltage to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

The comparator contains a capacitor, so $f(X_{IN})$ should be at least 500kHz during an A-D conversion.

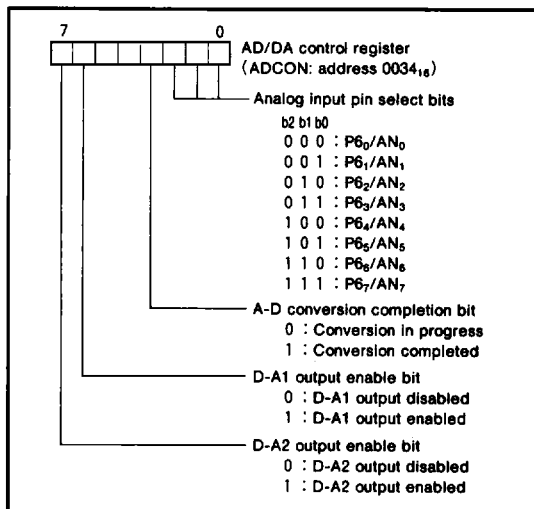


Fig. 18 Structure of AD/DA control register

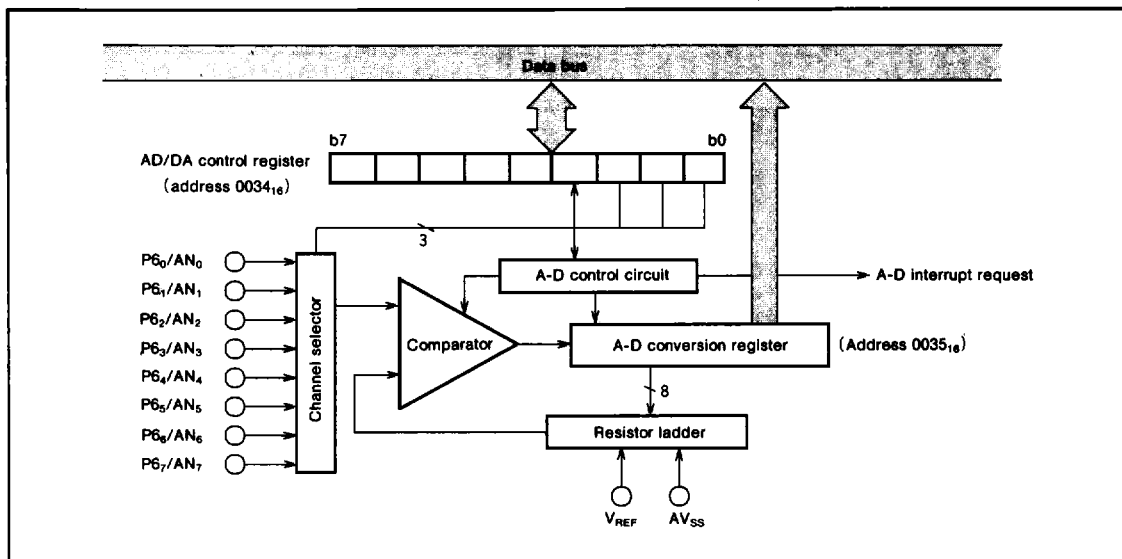


Fig. 19 Block diagram of A-D converter

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

D-A CONVERTER

Microcomputers of the M3806x group have two internal D-A converters (D-A1 and D-A2) with 8-bit resolutions.

The D-A converter outputs a voltage corresponding to the value in the D-A conversion register. The voltage is output from the DA₁ or DA₂ pin by setting the D-A output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit (DA₁/P5₆ or DA₂/P5₇) should be set to "0" (input status).

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n=0 \text{ to } 255)$$

Where V_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00", the D-A output enable bits are cleared to "0", and the P5₆/DA₁ and P5₇/DA₂ pins are set to input (high impedance). The D-A output is not buffered, so the user must supply an external buffer when driving a low-impedance load.

Set V_{CC} to at least 4.0V, when using the D-A converter.

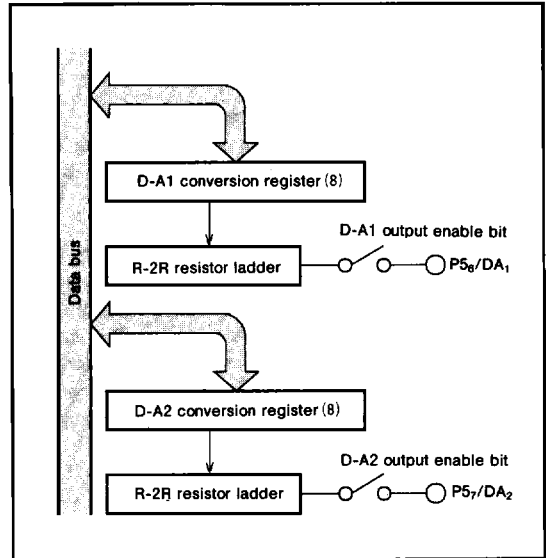


Fig. 20 Block diagram of D-A converter

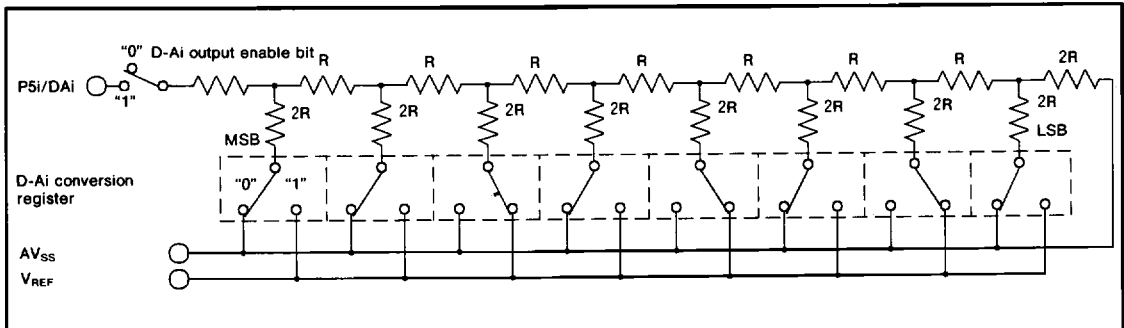


Fig. 21 Equivalent connection circuit of D-A converter

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

RESET CIRCUIT

A microcomputer in the M3806x group is reset if the $\overline{\text{RESET}}$ pin is held at a "L" level for at least $2\mu\text{s}$ then is returned to a "H" level (the power supply voltage should be between 4.0V and 5.5V). In order to give the X_{IN} clock time to stabilize, internal operation does not begin until after 8 to 12 X_{IN} clock cycles are complete. After the reset is completed, the program starts from the address contained in address FFFD_{16} (upper byte) and address FFFC_{16} (lower byte). Make sure that the reset input voltage is no more than 0.8V for a power supply voltage of 4.0V.

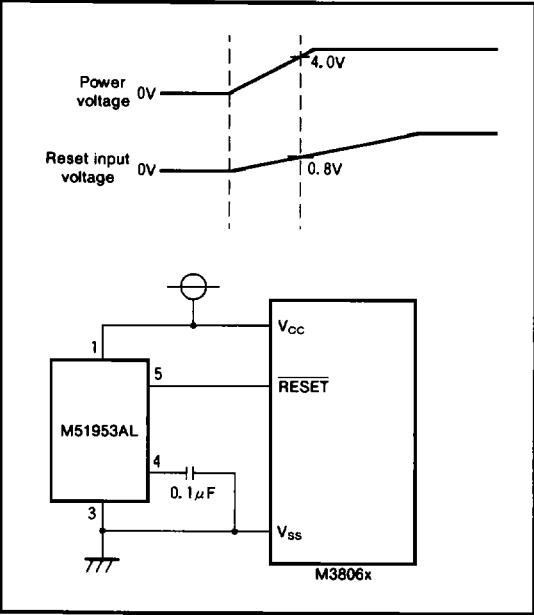


Fig. 22 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	(0 0 0 1 ₁₆)...	00 ₁₆
(2) Port P1 direction register	(0 0 0 3 ₁₆)...	00 ₁₆
(3) Port P2 direction register	(0 0 0 5 ₁₆)...	00 ₁₆
(4) Port P3 direction register	(0 0 0 7 ₁₆)...	00 ₁₆
(5) Port P4 direction register	(0 0 0 9 ₁₆)...	00 ₁₆
(6) Port P5 direction register	(0 0 0 B ₁₆)...	00 ₁₆
(7) Port P6 direction register	(0 0 0 D ₁₆)...	00 ₁₆
(8) Port P7 direction register	(0 0 0 F ₁₆)...	00 ₁₆
(9) Port P8 direction register	(0 0 1 1 ₁₆)...	00 ₁₆
(10) Serial I/O1 status register	(0 0 1 9 ₁₆)...	1 0 0 0 0 0 0 0
(11) Serial I/O1 control register	(0 0 1 A ₁₆)...	00 ₁₆
(12) UART control register	(0 0 1 B ₁₆)...	1 1 1 0 0 0 0 0
(13) Serial I/O2 control register	(0 0 1 D ₁₆)...	00 ₁₆
(14) Prescaler 12	(0 0 2 0 ₁₆)...	FF ₁₆
(15) Timer 1	(0 0 2 1 ₁₆)...	01 ₁₆
(16) Timer 2	(0 0 2 2 ₁₆)...	FF ₁₆
(17) Timer XY mode register	(0 0 2 3 ₁₆)...	00 ₁₆
(18) Prescaler X	(0 0 2 4 ₁₆)...	FF ₁₆
(19) Timer X	(0 0 2 5 ₁₆)...	FF ₁₆
(20) Prescaler Y	(0 0 2 6 ₁₆)...	FF ₁₆
(21) Timer Y	(0 0 2 7 ₁₆)...	FF ₁₆
(22) AD/DA control register	(0 0 3 4 ₁₆)...	0 0 0 0 1 0 0 0
(23) D-A1 conversion register	(0 0 3 6 ₁₆)...	00 ₁₆
(24) D-A2 conversion register	(0 0 3 7 ₁₆)...	00 ₁₆
(25) Interrupt edge selection register	(0 0 3 A ₁₆)...	00 ₁₆
(26) CPU mode register	(0 0 3 B ₁₆)...	0 0 0 0 0 0 0 ※ 0
(27) Interrupt control register 1	(0 0 3 E ₁₆)...	00 ₁₆
(28) Interrupt control register 2	(0 0 3 F ₁₆)...	00 ₁₆
(29) Processor status register	(P S)	× × × × × 1 × ×
(30) Program counter	(P C _H)	Contents of address FFFD_{16}
	(P C _L)	Contents of address FFFC_{16}

Note : × : Undefined
※ : The initial values of CM₁ are determined by the level at the CNV_{SS} pin.
The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software.

Fig. 23 Internal status of microcomputer after reset

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

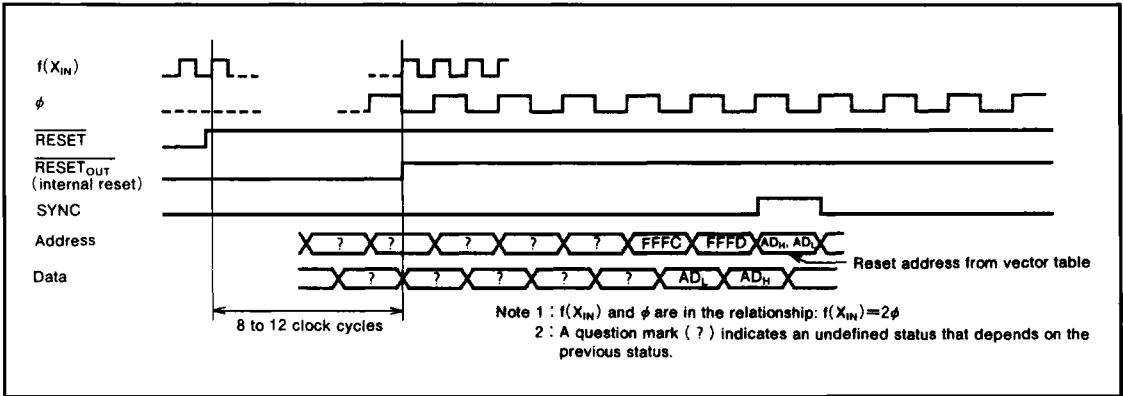


Fig. 24 Timing of reset

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

CLOCK GENERATION CIRCUIT

An oscillation circuit can be created by connecting a resonator between X_{IN} and X_{OUT} . When using an external clock signal, input the clock signal to the X_{IN} pin and leave the X_{OUT} pin open.

Oscillation Control

- (1) Stop Mode
If the STP instruction is executed, oscillation stops with the internal clock ϕ at "H". Timer 1 is set to "FF₁₆" and prescaler 12 is set to "01₁₆". Oscillation restarts when an external interrupt is received, but the internal clock ϕ remains at "H" until timer 1 overflows. This allows time for the clock circuit oscillation to stabilize. If oscillation is restarted by a reset, no wait time is generated, so keep the RESET pin at "L" level until oscillation has stabilized.
- (2) Wait Mode
If the WIT instruction is executed, the internal clock ϕ stops at a "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 overflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

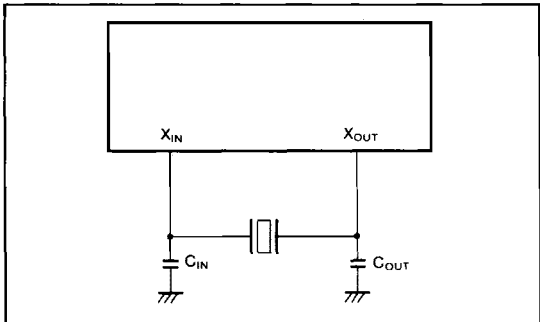


Fig. 25 Ceramic resonator circuit

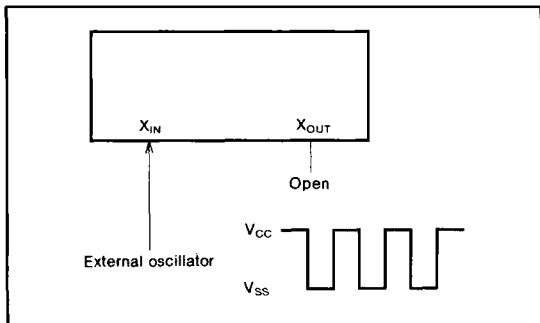


Fig. 26 External clock input circuit

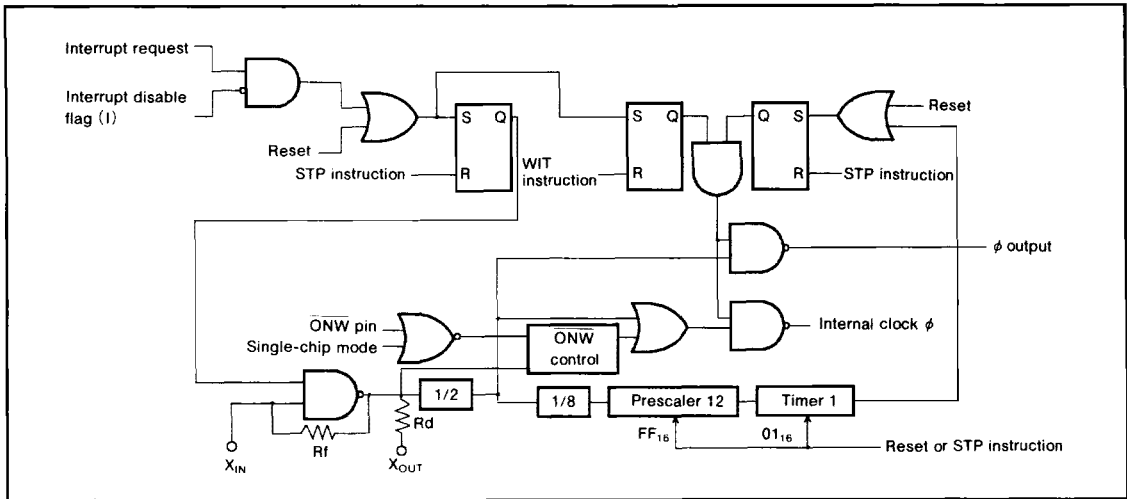


Fig. 27 Block diagram of clock generation circuit

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PROCESSOR MODES

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM_0 and CM_1 (bits 0 and 1 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table 2 Functions of ports in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs lower byte of address.
Port P1	Outputs upper byte of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction codes).
Port P3	P_3_0 and P_3_1 function only as output pins (except that the port latch cannot be read). P_3_2 is the $\overline{ONW}$ input pin. P_3_3 is the $\overline{RESET}_{OUT}$ output pin. (Note) P_3_4 is the ϕ output pin. P_3_5 is the $\overline{SYNC}$ output pin. P_3_6 is the $\overline{WR}$ output pin, and P_3_7 is the $\overline{RD}$ output pin.

Note : If CNV_{SS} is connected to V_{SS} , the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $\overline{RESET}_{OUT}$ output pin.

● Single-Chip Mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS} .

● Memory Expansion Mode

Select this mode by setting the processor mode bits to "01" in software with CNV_{SS} connected to V_{SS} . This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.

● Microprocessor Mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC} , or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS} . In microprocessor mode, the internal ROM is no longer valid and external memory must be used.

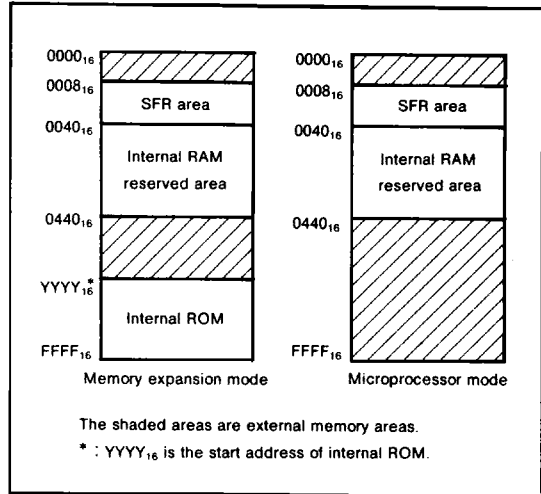


Fig. 28 Memory maps in various processor modes

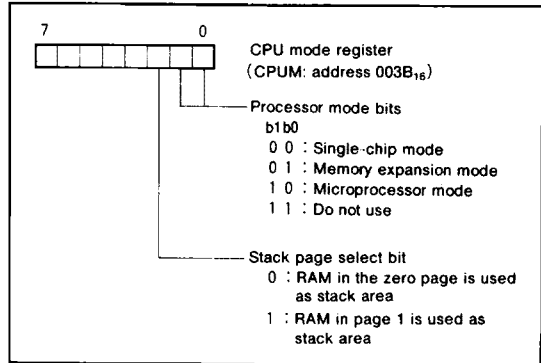


Fig. 29 Structure of CPU mode register

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Bus Control with Memory Expansion

Microcomputers of the M3806x group have a built-in ONW function to facilitate access to extra memory and I/O functions in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the $\overline{\text{ONW}}$ pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ . During this extended period, the RD or WR signal remains at "L". This extension period is valid only for writing to and reading from addresses 0000₁₆ to 0007₁₆ and 0440₁₆ to FFFF₁₆, and only read and write cycles are extended.

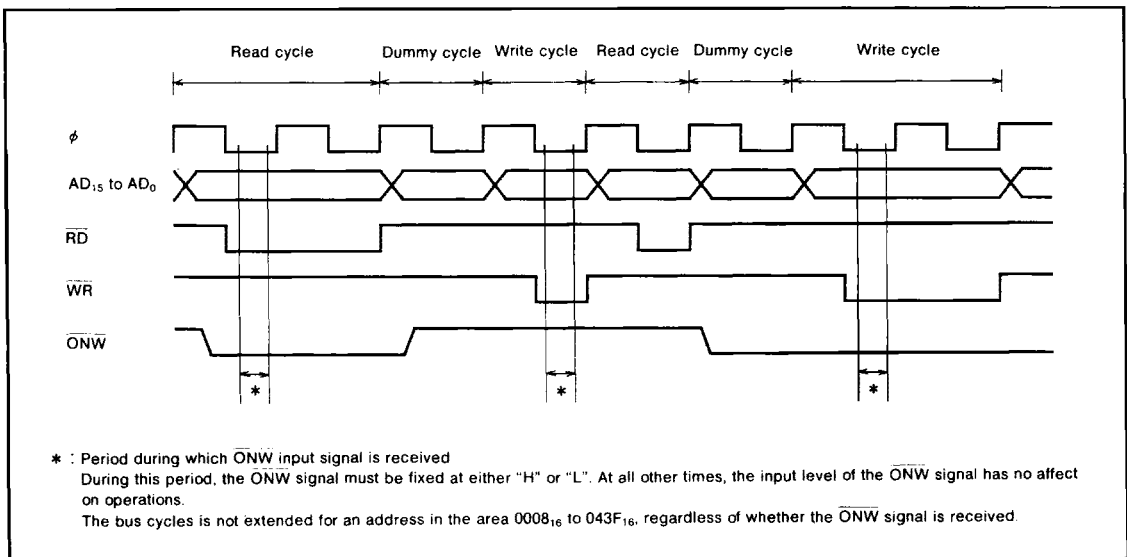


Fig. 30 ONW function timing

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**NOTES ON PROGRAMMING
Processor Status Register**

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". Therefore, flags that affect program execution must be initialized after a reset.

In particular, it is essential to initialize the T and D flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute a ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred, but must be initialized before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

The MUL and DIV instructions do not affect the T and D flags.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. Programs can not use the value of a direction register as an index, or bit-test a direction register (BBC or BBS), or perform a read-modify-write instruction such as ROR, CLB, or SEB. Use instructions such as LDM and STA to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{S_{RDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{S_{RDY1}}$ output enable bit to "1".

Serial I/O1 continues to output the final bit from the T_{xD} pin after transmission is completed. The S_{OUT2} pin from serial I/O2 goes to high impedance after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(X_{IN})$ is at least 500kHz during an A-D conversion. (If the ONW pin has been set to "L", the A-D conversion will take twice as long to match the longer bus cycle, and so $f(X_{IN})$ must be at least 1MHz.)

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes poor rapidly under the $V_{CC} = 4.0V$ or less condition. So set V_{CC} to at least 4.0V, when using the D-A converter.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency.

When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth the X_{IN} frequency.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mask Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

ROM Writing Method

The built-in PROM of the blank one-time programmable version and built-in EPROM version can be read from and written to with an normal EPROM writer using a special write adapter.

Package	Name of Write Adapter
80P6N	PCA4738F-80
80P6S	PCA4738G-80
80D0	PCA4738L-80

The PROM of the blank one-time programmable version is not tested or screened after assembly. To ensure proper operation after writing, the procedure shown in Figure 31 is recommended to verify programming.

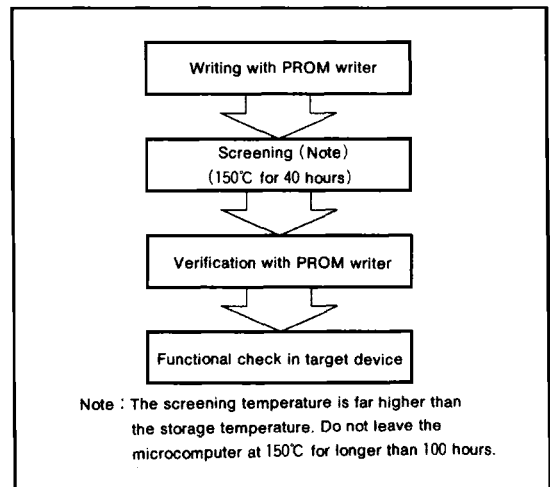


Fig. 31 Writing and testing of one-time programmable version

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	All voltages measured with reference to the V_{SS} pin, output transistors isolated.	-0.3 to 7.0	V
V_I	Input voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$, V_{REF}		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage RESET, X_{IN}		-0.3 to $V_{CC}+0.3$	V
V_I	Input voltage CNV_{SS}		-0.3 to 13	V
V_O	Output voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$, X_{OUT}		-0.3 to $V_{CC}+0.3$	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	500	mW
T_{opr}	Operating temperature		-20 to 85	$^\circ\text{C}$
T_{stg}	Storage temperature		-40 to 125	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = 3.0$ to 5.5V , $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage ($f(X_{IN}) \leq 2\text{MHz}$)	3.0	5.0	5.5	V
	Supply voltage ($f(X_{IN}) > 2\text{MHz}$)	4.0	5.0	5.5	
	Supply voltage (when D-A converter is used)	4.0	5.0	5.5	
V_{SS}	Supply voltage		0		V
V_{REF}	Analog reference voltage (when A-D converter is used)	2.0		V_{CC}	V
	Analog reference voltage (when D-A converter is used)	4.0		V_{CC}	
AV_{SS}	Analog power voltage		0		V
V_{IA}	Analog input voltage AN_0 - AN_7	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$	$0.8V_{CC}$		V_{CC}	V
V_{IH}	"H" input voltage RESET, X_{IN} , CNV_{SS}	$0.8V_{CC}$		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage RESET	0		$0.2V_{CC}$	V
V_{IL}	"L" input voltage X_{IN}	0		$0.16V_{CC}$	V
V_{IL}	"L" input voltage CNV_{SS}	0		$0.2V_{CC}$	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P8_0$ - $P8_7$ (Note 1)			-80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$ (Note 1)			-80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P8_0$ - $P8_7$ (Note 1)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$ (Note 1)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P8_0$ - $P8_7$ (Note 1)			-40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$ (Note 1)			-40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P8_0$ - $P8_7$ (Note 1)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$ (Note 1)			40	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P8_0$ - $P8_7$ (Note 2)			-10	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$ (Note 2)			10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P8_0$ - $P8_7$ (Note 3)			-5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$ (Note 3)			5	mA
$f(X_{IN})$	Internal clock oscillation frequency ($V_{CC}=4.0$ - 5.5V)			8	MHz
	Internal clock oscillation frequency ($V_{CC}=3.0$ - 5.5V)			2	

Note 1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.

2. The peak output current is the peak current flowing in each port.

3. The average output current $I_{OL}(avg)$, $I_{OH}(avg)$ in an average value measured over 100ms.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 3.0$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$ (Note 1)	$I_{OH} = -10mA$ $V_{CC} = 4.0 \sim 5.5V$	$V_{CC} - 2.0$			V
		$I_{OH} = -1.0mA$ $V_{CC} = 3.0 \sim 5.5V$	$V_{CC} - 1.0$			
V_{OL}	"L" output voltage $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$	$I_{OL} = 10mA$ $V_{CC} = 4.0 \sim 5.5V$			2.0	V
		$I_{OL} = 1.0mA$ $V_{CC} = 3.0 \sim 5.5V$			1.0	
$V_{T+} - V_{T-}$	Hysteresis $CNTR_0$, $CNTR_1$, INT_0 - INT_4			0.4		V
$V_{T+} - V_{T-}$	Hysteresis RxD , $SCLK1$, $SIN2$, $SCLK2$			0.5		V
$V_{T+} - V_{T-}$	Hysteresis $RESET$			0.5		V
I_{IH}	"H" input current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current $RESET$, CNV_{SS}	$V_i = V_{CC}$			5.0	μA
I_{IH}	"H" input current X_{IN}	$V_i = V_{CC}$		4		μA
I_{IL}	"L" input current $P0_0$ - $P0_7$, $P1_0$ - $P1_7$, $P2_0$ - $P2_7$, $P3_0$ - $P3_7$, $P4_0$ - $P4_7$, $P5_0$ - $P5_7$, $P6_0$ - $P6_7$, $P7_0$ - $P7_7$, $P8_0$ - $P8_7$, $RESET$, CNV_{SS}	$V_i = V_{SS}$			-5.0	μA
		$V_i = V_{SS}$		-4		
V_{RAM}	RAM hold voltage	With clock stopped	2.0		5.5	V
I_{CC}	Supply current	$f(X_{IN}) = 8MHz$, $V_{CC} = 5V$		6.4	13	mA
		$f(X_{IN}) = 5MHz$, $V_{CC} = 5V$		4	8	
		$f(X_{IN}) = 2MHz$, $V_{CC} = 3V$		0.8	2.0	
		When WIT instruction is executed with $f(X_{IN}) = 8MHz$, $V_{CC} = 5V$		1.5		
		When WIT instruction is executed with $f(X_{IN}) = 5MHz$, $V_{CC} = 5V$		1		
		When WIT instruction is executed with $f(X_{IN}) = 2MHz$, $V_{CC} = 3V$		0.2		
		When STP instruction is executed with clock stopped, output transistors isolated.	$T_a = 25^\circ C$ (Note 2)	0.1	1	μA
			$T_a = 85^\circ C$ (Note 2)		10	

Note 1 : $P4_5$ is measured when the $P4_5/TxD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".

2 : With output transistors isolated and A-D converter having completed conversion, and not including current flowing through V_{REF} pin.

A-D CONVERTER CHARACTERISTICS

($V_{CC} = 3.0$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $V_{REF} = 2.0V$ to V_{CC} , $T_a = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			± 1	± 2.5	LSB
t_{CONV}	Conversion time				50	$t_C (\phi)$
R_{LADDER}	Ladder resistor			35		k Ω
I_{VREF}	Reference power source input current (Note)	$V_{REF} = 5.0V$	50	150	200	μA
$I_1 (AD)$	A-D port input current			0.5		μA

Note : When D-A conversion registers (addresses 0036_{16} and 0037_{16}) contain "00₁₆".

D-A CONVERTER CHARACTERISTICS

($V_{CC} = 4.0$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $V_{REF} = 4.0V$ to V_{CC} , $T_a = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
t_{SU}	Setting time				3	μs
R_O	Output resistor		1	2.5	4	k Ω
I_{VREF}	Reference power source input current (Note)				3.2	mA

Note : Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00₁₆", and excluding currents flowing through the A-D resistance ladder.

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TIMING REQUIREMENTS 1 ($V_{CC}=4.0$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\text{RESET})$	Reset input "L" pulse width	2			μs
$t_C(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	50			ns
$t_C(\text{CNTR})$	CNTR ₀ , CNTR ₁ input cycle time	200			ns
$t_{WH}(\text{CNTR})$	CNTR ₀ , CNTR ₁ input "H" pulse width	80			ns
$t_{WH}(\text{INT})$	INT ₀ to INT ₄ input "H" pulse width	80			ns
$t_{WL}(\text{CNTR})$	CNTR ₀ , CNTR ₁ input "L" pulse width	80			ns
$t_{WL}(\text{INT})$	INT ₀ to INT ₄ input "L" pulse width	80			ns
$t_C(\text{SCLK}_1)$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_C(\text{SCLK}_2)$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(\text{SCLK}_1)$	Serial I/O1 clock input "H" pulse width (Note)	370			ns
$t_{WH}(\text{SCLK}_2)$	Serial I/O2 clock input "H" pulse width	400			ns
$t_{WL}(\text{SCLK}_1)$	Serial I/O1 clock input "L" pulse width (Note)	370			ns
$t_{WL}(\text{SCLK}_2)$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{SU}(R_{XD}-\text{SCLK}_1)$	Serial I/O1 input set up time	220			ns
$t_{SU}(S_{IN2}-\text{SCLK}_2)$	Serial I/O2 input set up time	200			ns
$t_H(\text{SCLK}_1-R_{XD})$	Serial I/O1 input hold time	100			ns
$t_H(\text{SCLK}_2-S_{IN2})$	Serial I/O2 input hold time	200			ns

Note : When $f(X_{IN})=8\text{MHz}$ and bit 6 of address 001A₁₆ is "1". Divide this value by four when $f(X_{IN})=8\text{MHz}$ and bit 6 of address 001A₁₆ is "0".

TIMING REQUIREMENTS 2 ($V_{CC}=3.0$ to $5.5V$, $V_{SS}=0V$, $T_a=-20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_W(\text{RESET})$	Reset input "L" pulse width	2			μs
$t_C(X_{IN})$	External clock input cycle time	500			ns
$t_{WH}(X_{IN})$	External clock input "H" pulse width	200			ns
$t_{WL}(X_{IN})$	External clock input "L" pulse width	200			ns
$t_C(\text{CNTR})$	CNTR ₀ , CNTR ₁ input cycle time	500			ns
$t_{WH}(\text{CNTR})$	CNTR ₀ , CNTR ₁ input "H" pulse width	230			ns
$t_{WH}(\text{INT})$	INT ₀ to INT ₄ input "H" pulse width	230			ns
$t_{WL}(\text{CNTR})$	CNTR ₀ , CNTR ₁ input "L" pulse width	230			ns
$t_{WL}(\text{INT})$	INT ₀ to INT ₄ input "L" pulse width	230			ns
$t_C(\text{SCLK}_1)$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_C(\text{SCLK}_2)$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(\text{SCLK}_1)$	Serial I/O1 clock input "H" pulse width (Note)	950			ns
$t_{WH}(\text{SCLK}_2)$	Serial I/O2 clock input "H" pulse width	950			ns
$t_{WL}(\text{SCLK}_1)$	Serial I/O1 clock input "L" pulse width (Note)	950			ns
$t_{WL}(\text{SCLK}_2)$	Serial I/O2 clock input "L" pulse width	950			ns
$t_{SU}(R_{XD}-\text{SCLK}_1)$	Serial I/O1 input set up time	400			ns
$t_{SU}(S_{IN2}-\text{SCLK}_2)$	Serial I/O2 input set up time	400			ns
$t_H(\text{SCLK}_1-R_{XD})$	Serial I/O1 input hold time	200			ns
$t_H(\text{SCLK}_2-S_{IN2})$	Serial I/O2 input hold time	300			ns

Note : When $f(X_{IN})=2\text{MHz}$ and bit 6 of address 001A₁₆ is "1". Divide this value by four when $f(X_{IN})=2\text{MHz}$ and bit 6 of address 001A₁₆ is "0".

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SWITCHING CHARACTERISTICS 1 ($V_{CC} = 4.0$ to $5.5V$, $V_{SS} = 0V$, $T_A = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK_1)$	Serial I/O1 clock output "H" pulse width	$t_c(SCLK_1)/2-30$			ns
$t_{WH}(SCLK_2)$	Serial I/O2 clock output "H" pulse width	$t_c(SCLK_2)/2-160$			ns
$t_{WL}(SCLK_1)$	Serial I/O1 clock output "L" pulse width	$t_c(SCLK_1)/2-30$			ns
$t_{WL}(SCLK_2)$	Serial I/O2 clock output "L" pulse width	$t_c(SCLK_2)/2-160$			ns
$t_d(SCLK_1-TxD)$	Serial I/O1 output delay time (Note 1)			140	ns
$t_d(SCLK_2-SOUT_2)$	Serial I/O2 output delay time			$0.2 \times t_c(SCLK_2)$	ns
$t_v(SCLK_1-TxD)$	Serial I/O1 output valid time (Note 1)	-30			ns
$t_v(SCLK_2-SOUT_2)$	Serial I/O2 output valid time	0			ns
$t_r(SCLK_1)$	Serial I/O1 clock output rise time			30	ns
$t_f(SCLK_1)$	Serial I/O1 clock output fall time			30	ns
$t_f(SCLK_2)$	Serial I/O2 clock output fall time			40	ns
$t_r(CMOS)$	CMOS output rise time (Note 2)		10	30	ns
$t_f(CMOS)$	CMOS output fall time (Note 2)		10	30	ns

Note 1 : When the P4₅/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".

2 : X_{OUT} pin excluded.

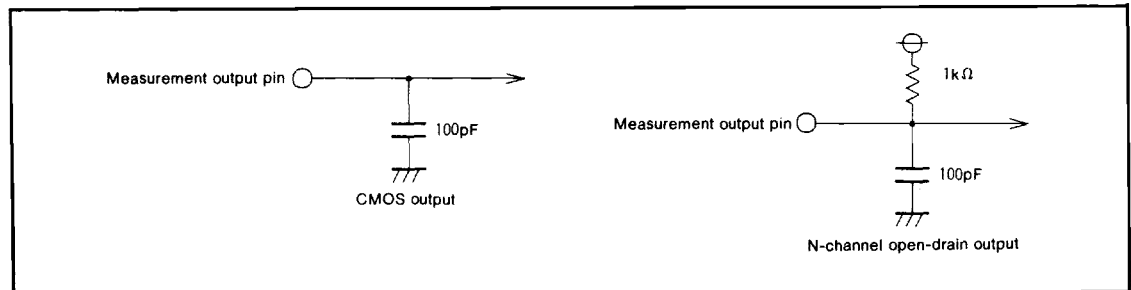


Fig. 32 Circuit for measuring output switching characteristics (1)

SWITCHING CHARACTERISTICS 2 ($V_{CC} = 3.0$ to $5.5V$, $V_{SS} = 0V$, $T_A = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(SCLK_1)$	Serial I/O1 clock output "H" pulse width	$t_c(SCLK_1)/2-50$			ns
$t_{WH}(SCLK_2)$	Serial I/O2 clock output "H" pulse width	$t_c(SCLK_2)/2-240$			ns
$t_{WL}(SCLK_1)$	Serial I/O1 clock output "L" pulse width	$t_c(SCLK_1)/2-50$			ns
$t_{WL}(SCLK_2)$	Serial I/O2 clock output "L" pulse width	$t_c(SCLK_2)/2-240$			ns
$t_d(SCLK_1-TxD)$	Serial I/O1 output delay time (Note 1)			350	ns
$t_d(SCLK_2-SOUT_2)$	Serial I/O2 output delay time			$0.2 \times t_c(SCLK_2)$	ns
$t_v(SCLK_1-TxD)$	Serial I/O1 output valid time (Note 1)	-30			ns
$t_v(SCLK_2-SOUT_2)$	Serial I/O2 output valid time	0			ns
$t_r(SCLK_1)$	Serial I/O1 clock output rise time			50	ns
$t_f(SCLK_1)$	Serial I/O1 clock output fall time			50	ns
$t_f(SCLK_2)$	Serial I/O2 clock output fall time			50	ns
$t_r(CMOS)$	CMOS output rise time (Note 2)		20	50	ns
$t_f(CMOS)$	CMOS output fall time (Note 2)		20	50	ns

Note 1 : When the P4₅/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".

2 : X_{OUT} pin excluded.

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TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

($V_{CC} = 4.0$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{SU}(\overline{ONW}-\phi)$	ONW input set up time	-20			ns
$t_{H}(\phi-\overline{ONW})$	ONW input hold time	-20			ns
$t_{SU}(\overline{DB}-\phi)$	Data bus set up time	60			ns
$t_{H}(\phi-\overline{DB})$	Data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

($V_{CC} = 4.0$ to $5.5V$, $V_{SS} = 0V$, $T_a = -20$ to $85^\circ C$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_C(\phi)$	ϕ clock cycle time		$2 \times t_{C(X_{IN})}$		ns
$t_{WH}(\phi)$	ϕ clock "H" pulse width	$t_{C(X_{IN})} - 10$			ns
$t_{WL}(\phi)$	ϕ clock "L" pulse width	$t_{C(X_{IN})} - 10$			ns
$t_d(\phi-AH)$	AD_{15} to AD_8 delay time		20	40	ns
$t_v(\phi-AH)$	AD_{15} to AD_8 valid time	6	10		ns
$t_d(\phi-AL)$	AD_7 to AD_0 delay time		25	45	ns
$t_v(\phi-AL)$	AD_7 to AD_0 valid time	6	10		ns
$t_d(\phi-SYNC)$	SYNC delay time		20		ns
$t_v(\phi-SYNC)$	SYNC valid time		10		ns
$t_d(\phi-WR)$	RD and WR delay time		10	20	ns
$t_v(\phi-WR)$	RD and WR valid time	3	5	10	ns
$t_d(\phi-DB)$	Data bus delay time		20	70	ns
$t_v(\phi-DB)$	Data bus valid time	15			ns
$t_d(\overline{RESET}-\overline{RESET_{OUT}})$	$\overline{RESET_{OUT}}$ output delay time (Note 1)			200	ns
$t_v(\phi-\overline{RESET})$	$\overline{RESET_{OUT}}$ output valid time (Note 1)	0		200	ns

Note 1 : The $\overline{RESET_{OUT}}$ output goes "H" in sync with the rise of the ϕ clock that is anywhere between about 1 cycle and 19 cycles after the RESET input goes "H"

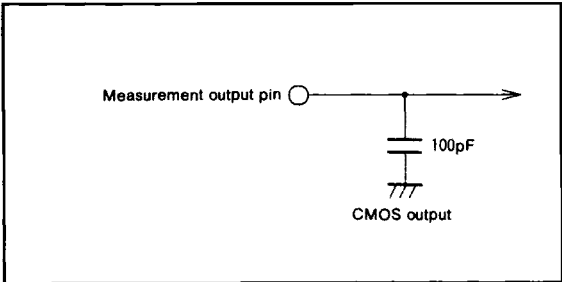
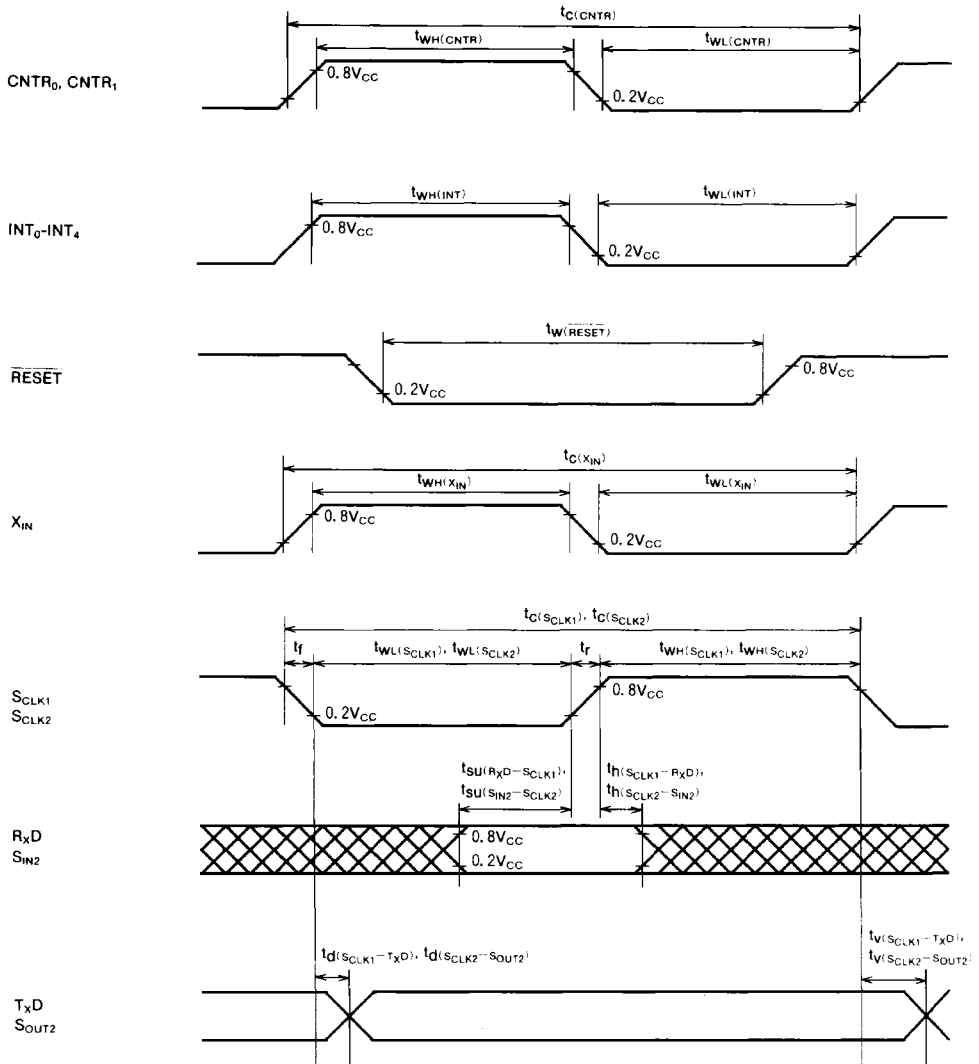


Fig. 33 Circuit for measuring output switching characteristics (2)

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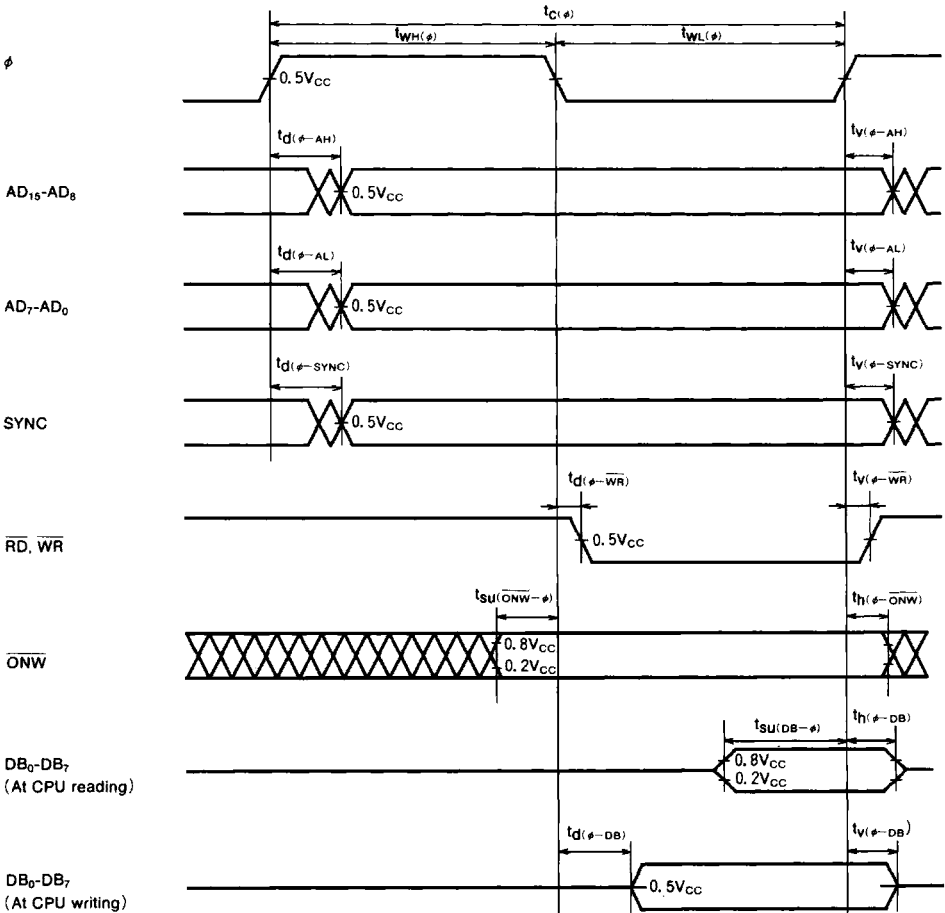
TIMING DIAGRAM

(1) Timing diagram



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(2) Timing diagram in memory expansion mode and microprocessor mode



(3) Timing diagram in microprocessor mode

