

GENERAL DESCRIPTION

This document describes the specifications for the IDTF1178 Zero-Distortion™ RF to IF Downconverting Dual Mixer. This device is part of a series of mixers offered with high side and/or low side injection options for all UTRA bands. See the Part# Matrix for pin compatible & feature compatible devices in this series.

The F1178 dual channel device is designed to operate with a single 5V supply. It is optimized for operation in a Multi-mode, Multi-carrier BaseStation Receiver for RF bands from 3400MHz - 3800MHz with Low Side LO injection. IF frequencies from 30MHz to 550MHz are supported. Nominally, the device offers +37.5dBm Output IP3 with 297mA of I_{CC} .

COMPETITIVE ADVANTAGE

In typical basestation receivers, the RF to IF mixer dominates the linearity performance for the entire receive system. The Zero-Distortion™ family of mixers dramatically improves the maximum signal levels (IM_3 tones) that the BTS can withstand at a desired Signal to Noise Ratio (SNR). Zero-Distortion™ technology allows realization of either benefit.

- ✓ $IP3_0$: ↑ **9dB**
- ✓ Dissipation: ↓ **23%**
- ✓ Noise Figure: 8.5dB



PART# MATRIX

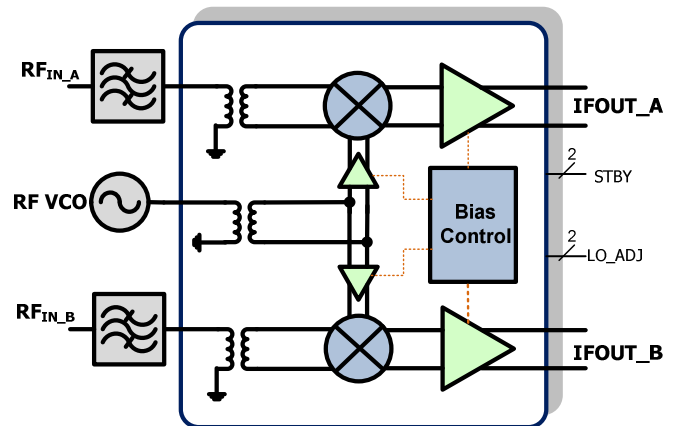
| Part# | RF freq range (MHz) | UTRA bands | IF freq range (MHz) | Typ. Gain (dB) | Injection |
|--------------|---------------------|---|---------------------|----------------|-----------------|
| F1100 | 698 - 915 | 5,6,8,12,13,14,17,19,20 | 150 - 450 | 9.0 | High Side |
| F1102 | 400 - 1000 | 5,6,8,12,13,14,17,19,20 | 50 - 300 | 9.0 | Both |
| F1150 | 1700 - 2200 | 1,2,3,4,9,10,33,34,35,36,37,39 | 50 - 450 | 8.5 | High Side |
| F1152 | 1400 - 2200 | 1,2,3,4,9,10,11 ¹ ,21 ¹ ,24 ¹ ,33,34,35,36,37,39 | 50 - 350 | 8.5 | Low Side |
| F1162 | 2300 - 2700 | 7,38,40,41 | 50 - 500 | 8.9 | Both |
| F1178 | 3400 - 3800 | 22, 42, 43 | 30 - 550 | 9.0 | Low Side |

1 – with High Side injection

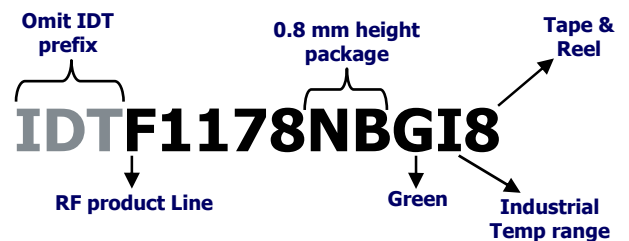
FEATURES

- Dual Path for Diversity Systems
- Ideal for Multi-Carrier Systems
- 9dB Gain
- Ultra linear **+37.5dBm $IP3_0$**
- 8.5dB NF
- 200 Ω output impedance
- High +11dBm $P1dB_I$
- **Pin & Feature Compatible**
- 6mm x 6mm, 36-pin package
- **Individual Path Standby Mode**
- <400 nsec settling from Power Up
- $I_{CC} = 297mA$

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

| Parameter / Condition | Symbol | Min | Max | Unit |
|--|--|------|---------------------|------|
| VCC to GND | VCC | -0.3 | +5.5 | V |
| STBY1, STBY2 | V_{STBY1}, V_{STBY2} | -0.3 | VCC + 0.3 | V |
| IF_A+, IF_B+, IF_A-, IF_B- | $V_{IF_A+}, V_{IF_B+}, V_{IF_A-}, V_{IF_B-}$ | +1.0 | VCC+ 0.3 | V |
| LO1_ADJ | V_{LO1_ADJ} | +1.0 | 3.0 | V |
| LO2_ADJ | V_{LO2_ADJ} | +2.1 | 4.0 | V |
| LO_IN, RF_A, RF_B | $V_{LO_IN}, V_{RF_A}, V_{RF_B}$ | -0.3 | +0.3 | V |
| IF_BiasA, IF_BiasB to GND | $V_{IF_BiasA}, V_{IF_BiasB}$ | -0.3 | +0.3 | V |
| RF Input Power | $P_{LO_IN}, P_{RF_A}, P_{RF_B}$ | | +20 | dBm |
| Continuous Power Dissipation | | | 2.2 | W |
| Operating Temperature Range (Case Temperature) | T_C | -40 | +105 | °C |
| Maximum Junction Temperature | T_{Jmax} | | 150 | °C |
| Storage Temperature Range | T_{ST} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T_{LEAD} | | +260° | °C |
| ESD Voltage– HBM (Per JESD22-A114) | V_{ESDHBM} | | Class 2 (2500V) | |
| ESD Voltage – CDM (Per JESD22-C101) | V_{ESDCDM} | | Class C3 (1000V) | |

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|---------|
| θ_{JA} (Junction – Ambient) | 35°C/W |
| θ_{JC} (Junction – Case) The Case is defined as the exposed paddle | 2.5°C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL 1 |

IDTF1178 RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Comment | min | typ | max | Units |
|-----------------------------|------------|-------------------|------|-----|------|-------|
| Supply Voltage(s) | V_{CC} | All V_{CC} pins | 4.75 | | 5.25 | V |
| LO Power | P_{LO} | | -3 | | +3 | dBm |
| Operating Temperature Range | T_{CASE} | Case Temperature | -40 | | +105 | deg°C |
| RF Freq Range | F_{RF} | | 3400 | | 3800 | MHz |
| LO Freq Range | F_{LO} | | 2900 | | 3620 | |
| IF Freq Range | F_{IF} | | 30 | | 550 | |

The F1178 is well suited for DPD applications with a broad IF frequency range from 30 MHz to 550 MHz using the standard BOM specified in this datasheet

IDTF1178 SPECIFICATION

Typical Application Circuit specifications apply at $V_{CC} = +5.00V$, $T_C = +25^\circ C$ using LS LO. $F_{RF} = 3550$ MHz, $F_{LO} = 3250$ MHz, $F_{IF} = 300$ MHz, $P_{in} = -10$ dBm/tone unless otherwise stated, $P_{LO} = 0$ dBm, STBY = GND, Transformer Loss not included (de-embedded), RF trace de-embedded unless otherwise noted.

| Parameter | Symbol | Comment | min | typ | max | units |
|---------------------------------|------------------|--|-------------|------------|------------------------|----------------|
| Logic Input High ³ | V_{IH} | For Standby Pins | 1.1 | | | V |
| Logic Input Low ³ | V_{IL} | For Standby Pins | | | 0.60 | V |
| Logic Current | I_{IH}, I_{IL} | For Standby Pins | -110 | | +5 | μA |
| Supply Current | I_{2CHAN} | Total Both Channels | | 297 | 345¹ | mA |
| | I_{1CHAN} | Single Channel | | 155 | 180 | |
| | I_{STBY} | <ul style="list-style-type: none"> ▪ STBY = V_{IH} ▪ Total Both Channels | | 14 | 24 | |
| Power Up Time | T_{ON} | <ul style="list-style-type: none"> • Pin = -13 dBm • Gate STBY from V_{IH} to V_{IL} • Time for IF Signal to settle to within 0.1 dB of final value | | 0.38 | | μsec |
| Power Down Time | T_{OFF} | <ul style="list-style-type: none"> • Pin = -13 dBm • Gate STBY from V_{IL} to V_{IH} Time for IF Signal to settle to within 0.1 dB of final value | | 0.155 | | μsec |
| Conversion Gain | G | | 7.8 | 9 | 10 | dB |
| Gain, Temperature drift | G_{DRIFT} | Tcase: $-40^\circ C$ to $+105^\circ C$ | | 0.015 | | dB/ $^\circ C$ |
| Noise Figure | NF | | | 8.5 | | dB |
| Noise Figure - HOT | NF_{HOT} | Tcase = $105^\circ C$ | | 10.3 | | dB |
| Noise Figure, Temperature drift | NF_{DRIFT} | Tcase: $-40^\circ C$ to $+105^\circ C$ | | 0.022 | | dB/ $^\circ C$ |
| Noise Figure w/Blocker | NF_{BLK} | <ul style="list-style-type: none"> ▪ +100MHz offset blocker ▪ $P_{IN} = +8$ dBm | | 18.5 | | dB |
| Output IP3 | $IP3_O$ | 5MHz Tone Separation | 33 | 37.5 | | dBm |
| 2RF – 2LO rejection | 2x2 | <ul style="list-style-type: none"> ▪ $P_{RF} = -10$ dBm ▪ Frequency = $F_{RF} - \frac{1}{2} F_{IF}$ | | -64 | -54 | dBc |
| 3RF – 3LO rejection | 3x3 | <ul style="list-style-type: none"> ▪ $P_{RF} = -10$ dBm ▪ Frequency = $F_{RF} - 1/3 F_{IF}$ | | -75 | -65 | dBc |
| 1 dB Compression | $P1dB_I$ | Input referred | 9 | 11 | | dBm |

IDTF1178 SPECIFICATION (CONTINUED)

Typical Application Circuit specifications apply at $V_{CC} = +5.00V$, $T_C = +25^\circ C$ using LS LO. $F_{RF} = 3550$ MHz, $F_{LO} = 3250$ MHz, $F_{IF} = 300$ MHz, $P_{in} = -10$ dBm/tone unless otherwise stated, $P_{LO} = 0$ dBm, STBY = GND, Transformer Loss not included (de-embedded), RF trace de-embedded unless otherwise noted.

| Parameter | Symbol | Comment | min | typ | max | units |
|-----------------------|------------|-------------------------------------|-----|-----|-----|----------|
| RF Input Impedance | Z_{RF} | Single Ended | | 50 | | Ω |
| RF Input Return Loss | RL_{RF} | No external matching | | 18 | | dB |
| IF Output Impedance | Z_{IF} | Differential | | 200 | | Ω |
| IF Output Return Loss | RL_{IF} | No external matching | | 13 | | dB |
| LO Port Impedance | Z_{LO} | Single Ended | | 50 | | Ω |
| LO Port Return Loss | LO_{RF} | No external matching | | 14 | | dB |
| Channel Isolation | ISO_C | IF_B Pout vs. IF_A w/ RF_A input | 40 | 44 | | dB |
| LO to IF leakage | ISO_{LI} | | | -30 | -25 | dBm |
| RF to IF leakage | ISO_{RI} | Relative to IF Pout | | -50 | -40 | dBc |
| LO to RF leakage | ISO_{LR} | | | -30 | | dBm |

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test

2 – All other Items in min/max columns are Guaranteed by Design Characterization

3 – JEDEC 1.8V logic

STANDBY LOGIC TABLE

| Main Channel | Diversity Channel | STBY1 (pin 22) | STBY2 (pin 24) |
|---------------------|--------------------------|-----------------------|-----------------------|
| ON | ON | 0 | 0 |
| OFF | OFF | 1 | 0 |
| ON | OFF | 0 | 1 |
| OFF | ON | 1 | 1 |

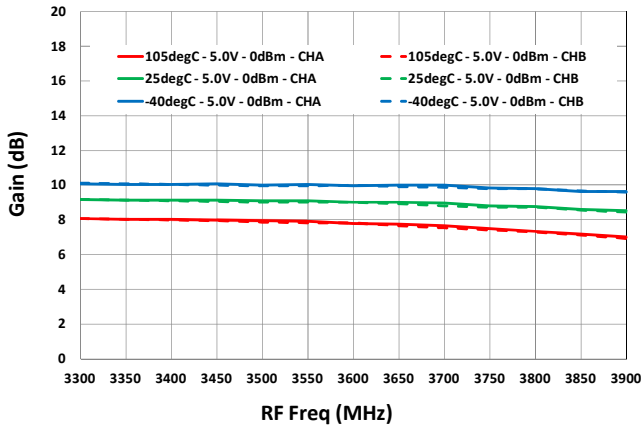
TYPICAL OPERATING CONDITIONS

Unless otherwise noted, the following conditions apply to the Typ Ops Graphs:

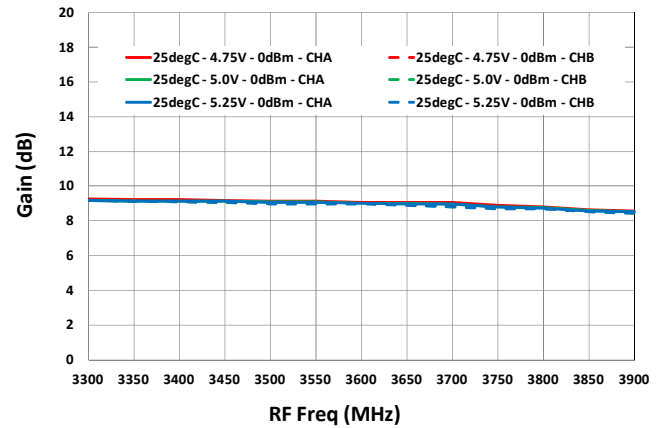
- 5MHz Tone Spacing
- Low Side LO injection graphs with 300MHz & 400MHz & 500MHz IF
- Pin = - 10 dBm per Tone
- LO port = Pin 19 (Main Port)
- Listed Temperatures are Case Temperature (TC = Case Temperature)
- Where noted, TA or TAMB = Ambient Temperature

TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-1-)

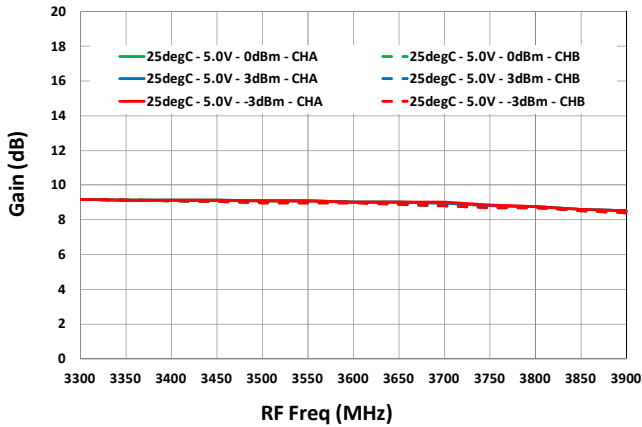
Gain vs. T_{CASE}



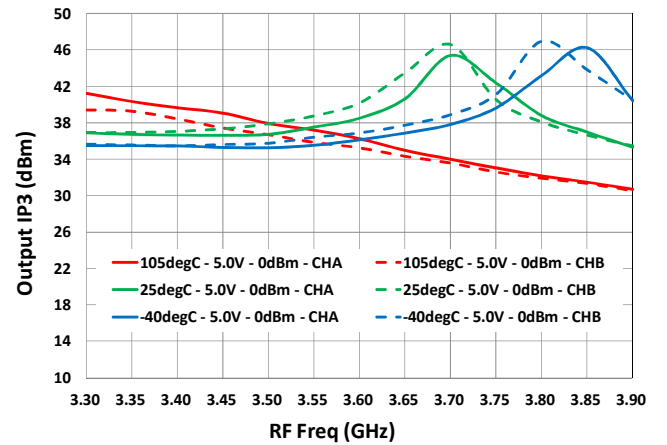
Gain vs. V_{cc}



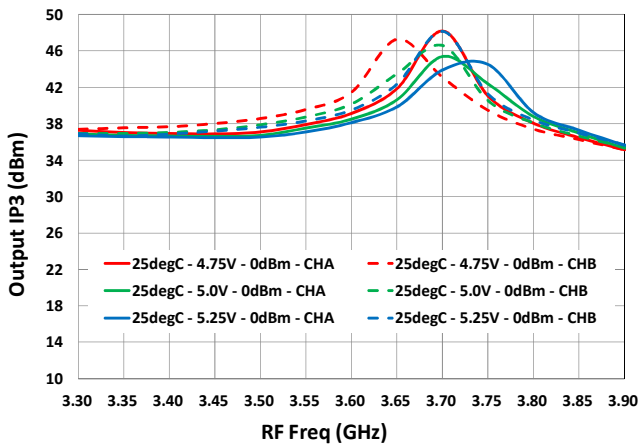
Gain vs. Lo Level



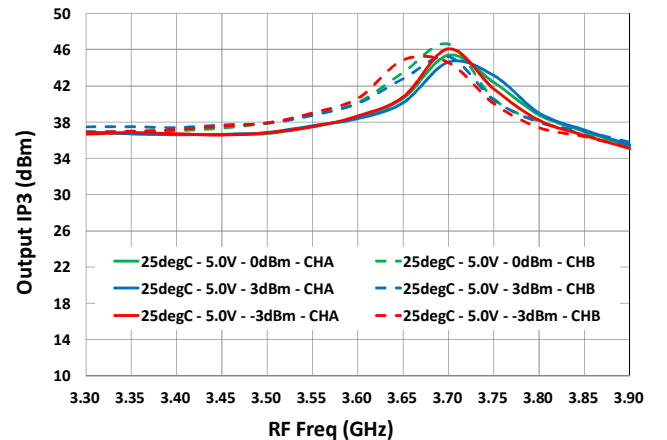
Output IP3 vs. T_{CASE}



Output IP3 vs. V_{cc}

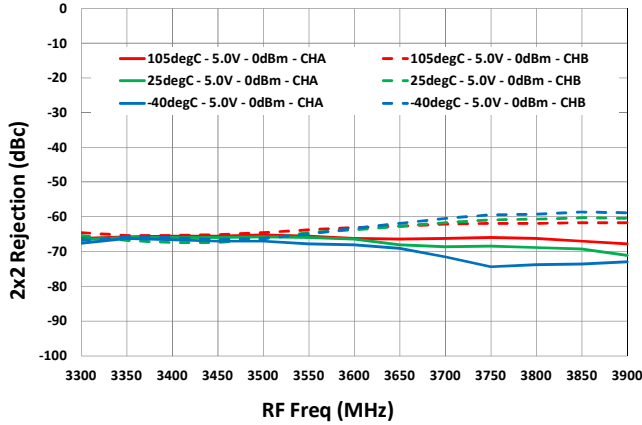


Output IP3 vs. LO Level

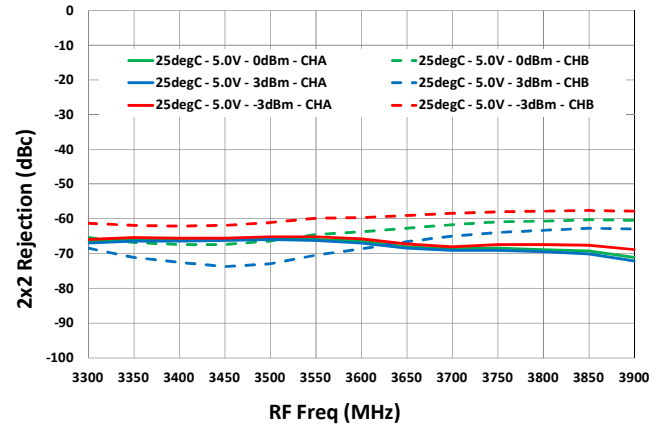


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-2-)

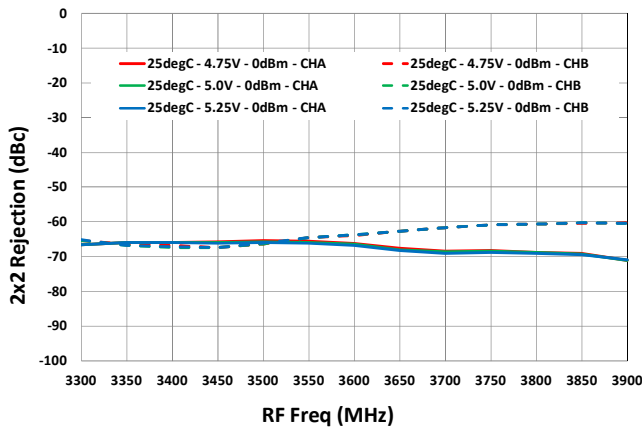
2RF x 2LO rejection vs. T_{CASE}



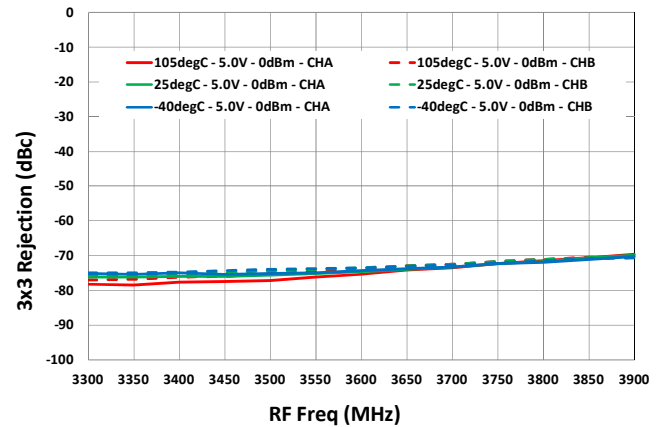
2RF x 2LO Rejection vs. LO Level



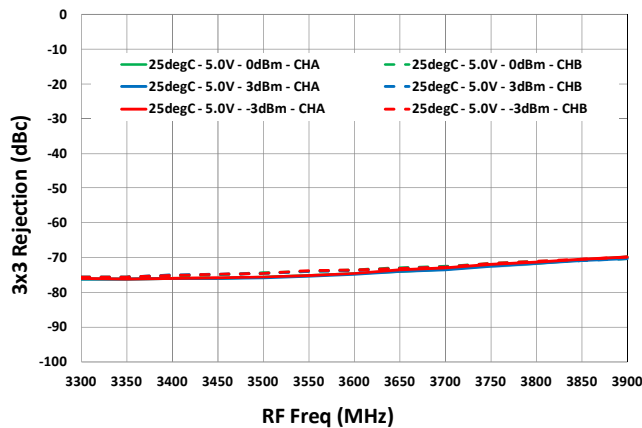
2RF x 2LO Rejection vs. V_{CC}



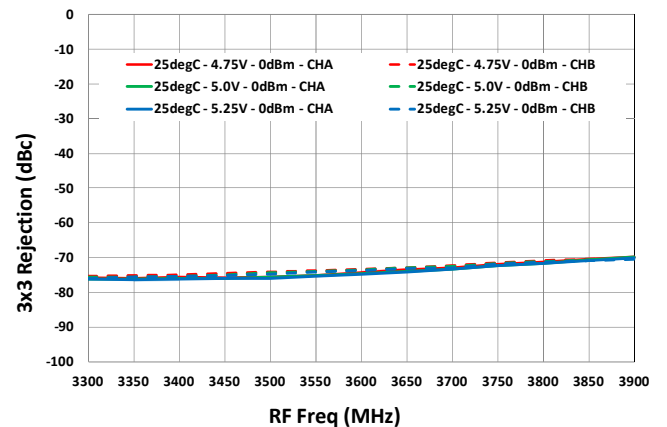
3RF x 3LO rejection vs. T_{CASE}



3RF x 3LO Rejection vs. LO Level

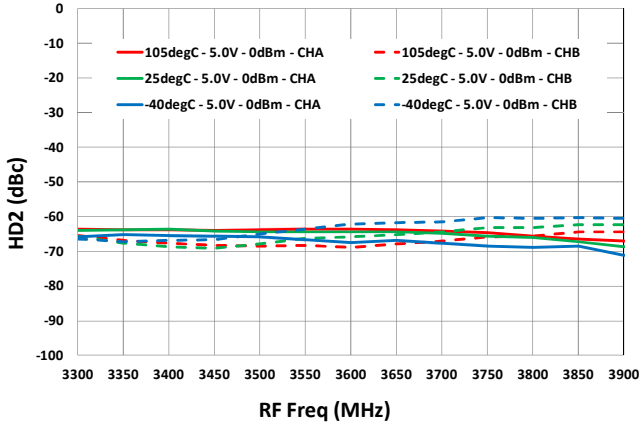


3RF x 3LO Rejection vs. V_{CC}

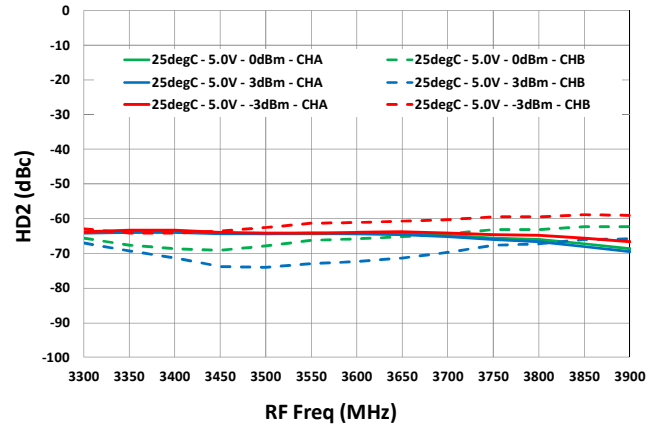


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-3-)

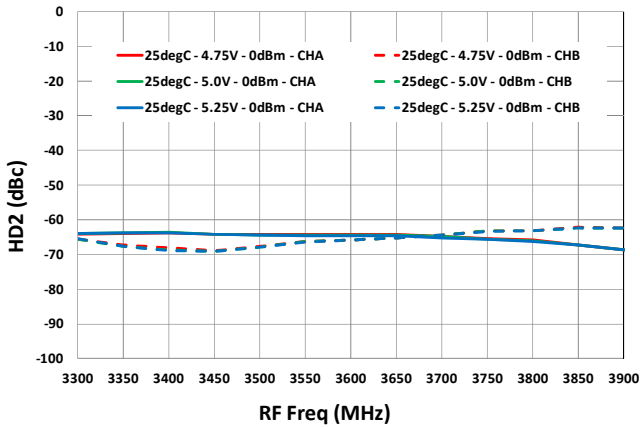
2nd Harmonic vs. T_{CASE}



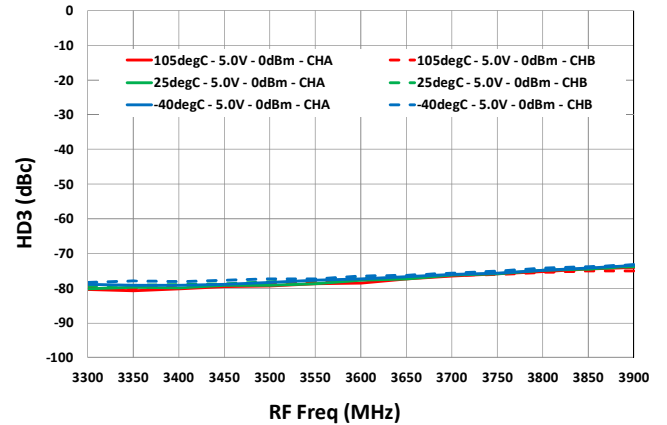
2nd Harmonic vs. LO Level



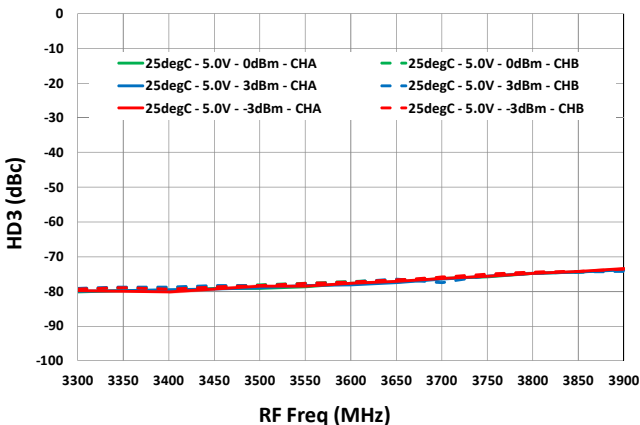
2nd Harmonic vs. V_{CC}



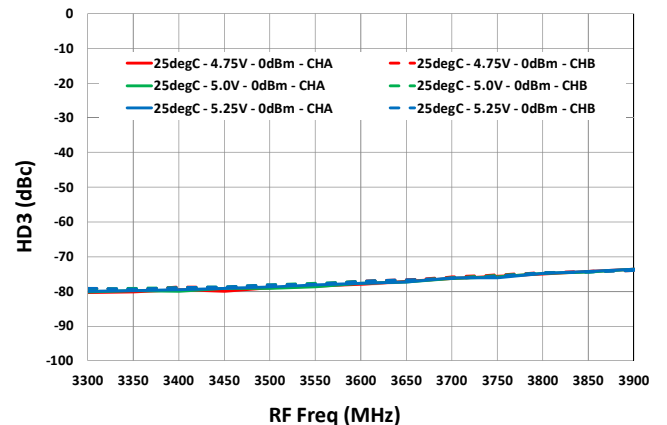
3rd Harmonic vs. T_{CASE}



3rd Harmonic vs. Lo Level

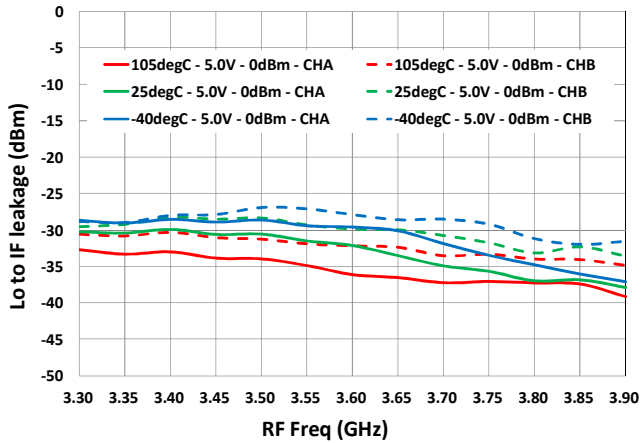


3rd Harmonic vs. V_{CC}

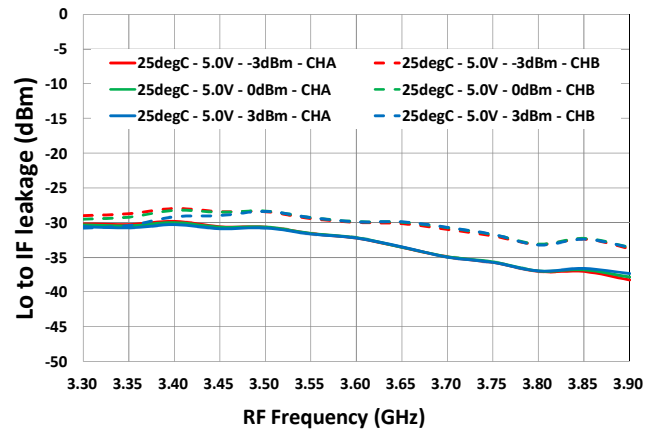


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-4-)

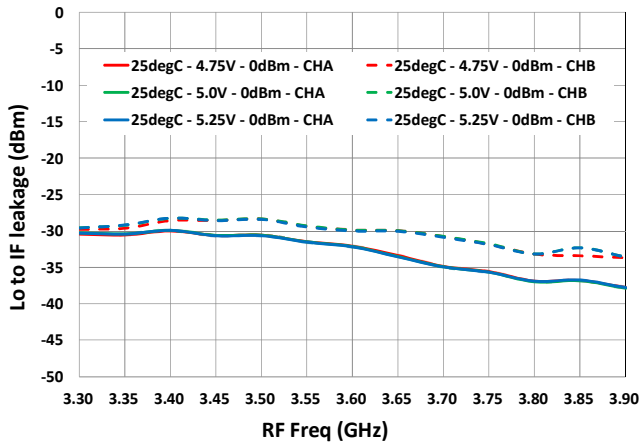
LO-IF Leakage vs. T_{CASE}



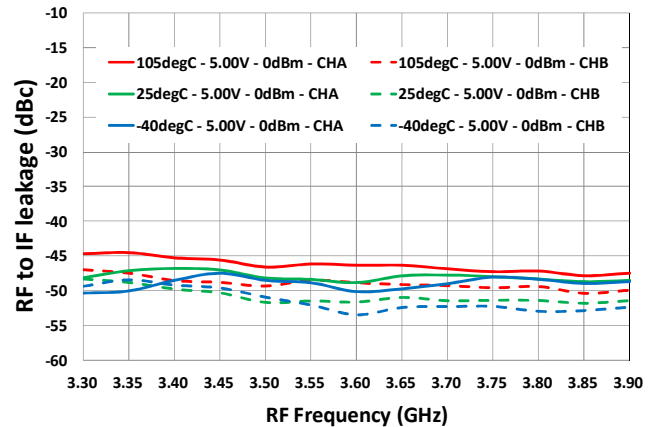
LO-IF Leakage vs. LO Level



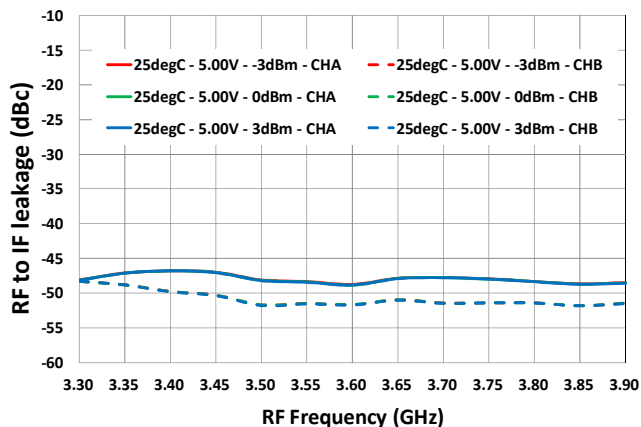
LO-IF Leakage vs. V_{CC}



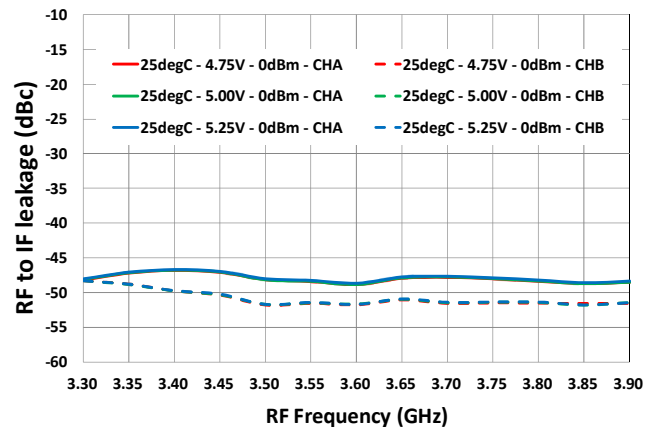
RF-IF Leakage vs. T_{CASE}



RF-IF Leakage vs. LO Level

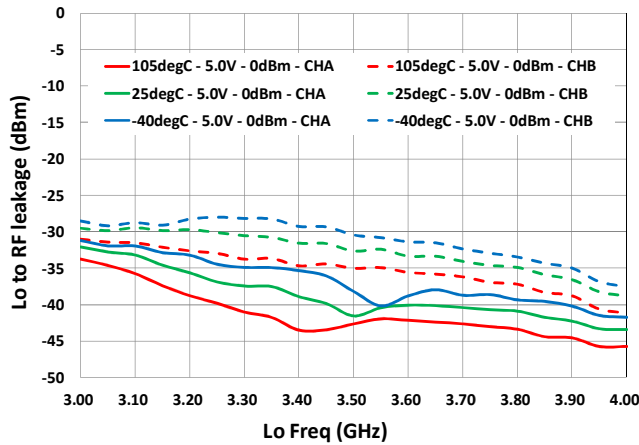


RF-IF Leakage vs. V_{CC}

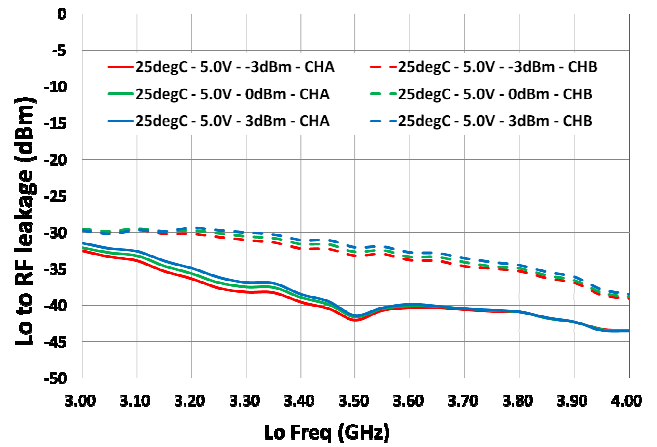


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-5-)

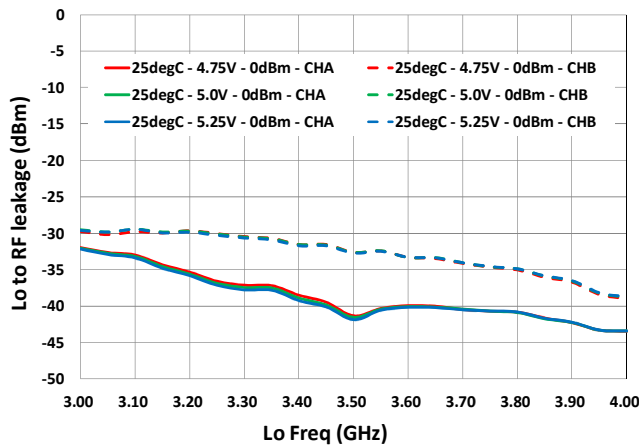
Lo-RF Leakage vs. T_{CASE}



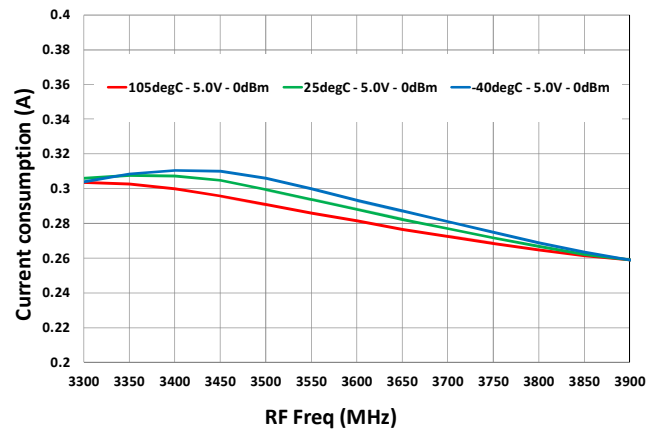
Lo-RF Leakage vs. LO Level



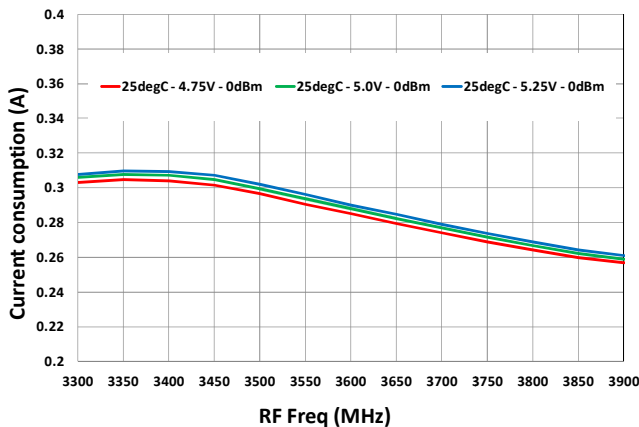
Lo-RF Leakage vs. V_{CC}



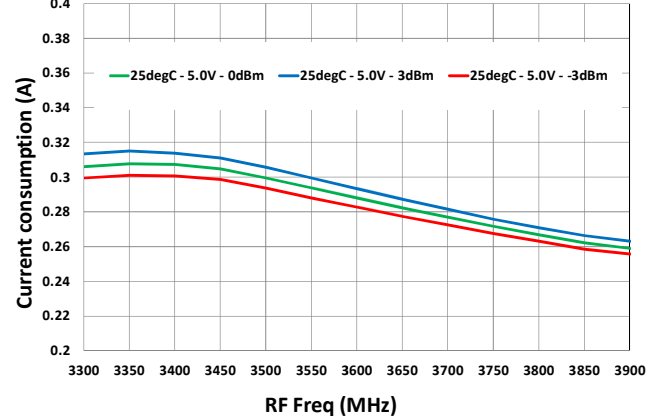
I_{CC} vs. T_{CASE}



I_{CC} vs. V_{CC}

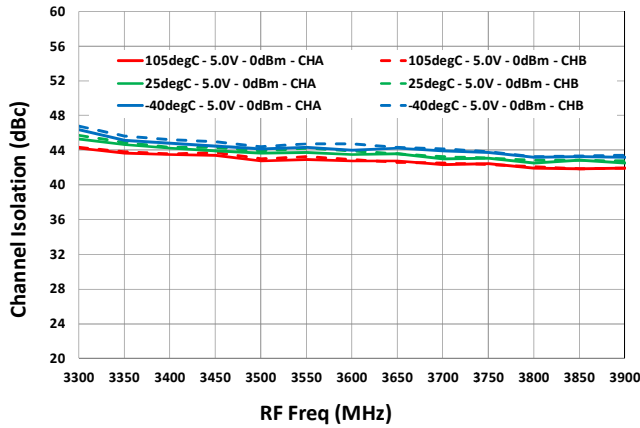


I_{CC} vs. LO Level

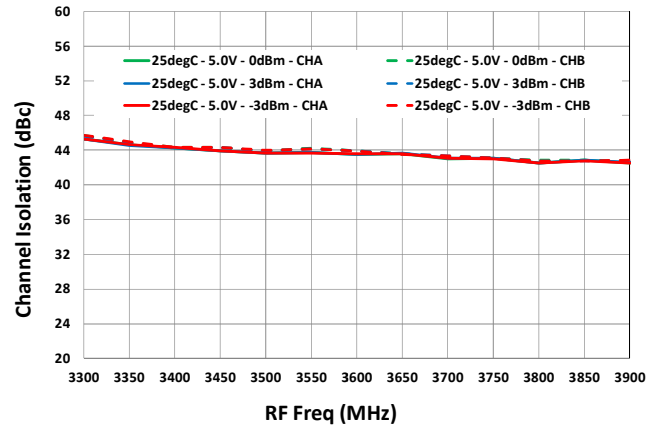


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-6-)

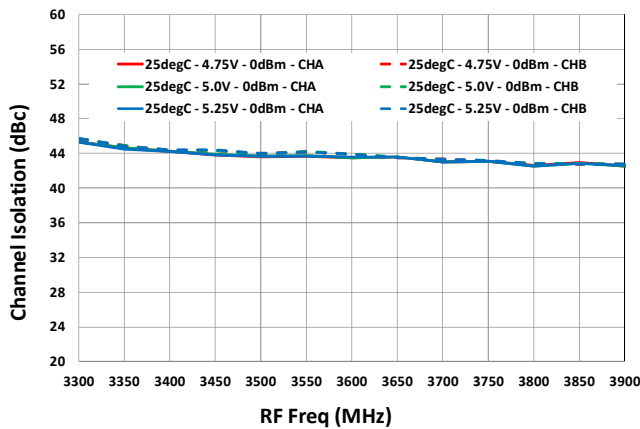
Channel Isolation vs. T_{CASE}



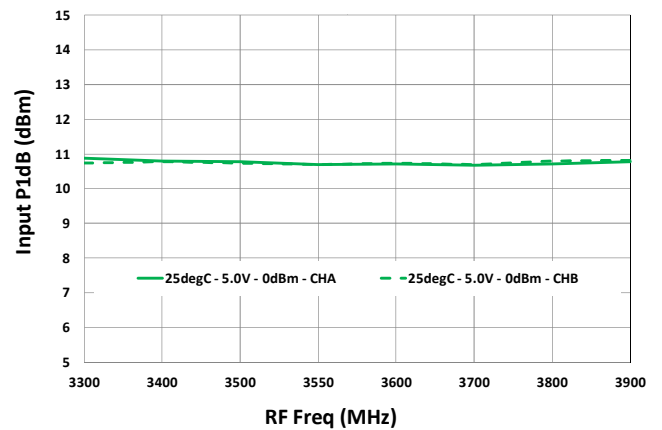
Channel Isolation vs. LO Level



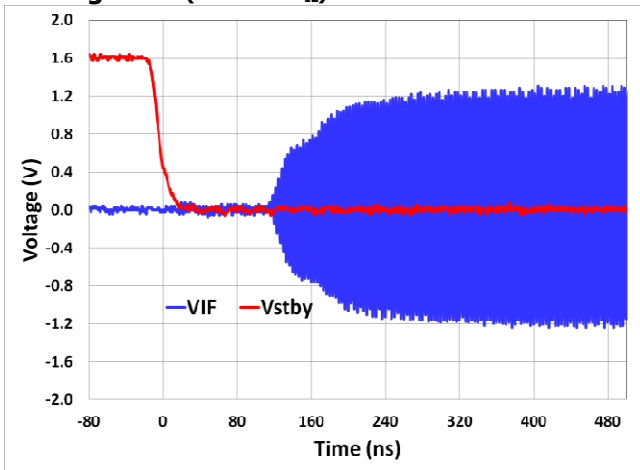
Channel Isolation vs. V_{CC}



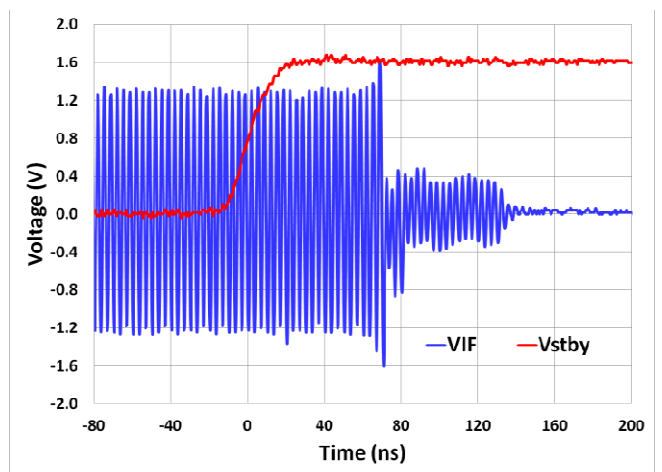
INPUT P1dB



Settling Time (STBY -> V_{IL})

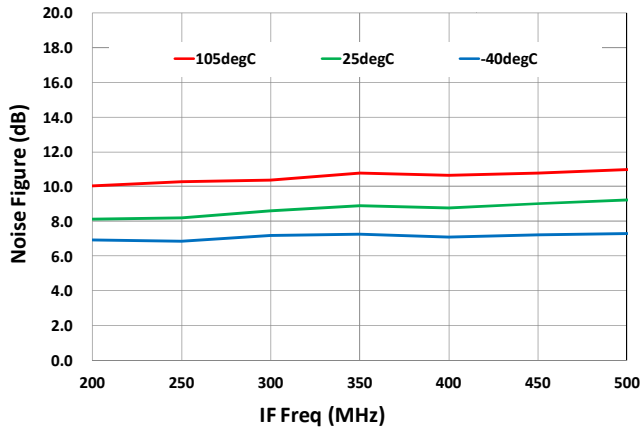


Settling Time (STBY -> V_{IH})

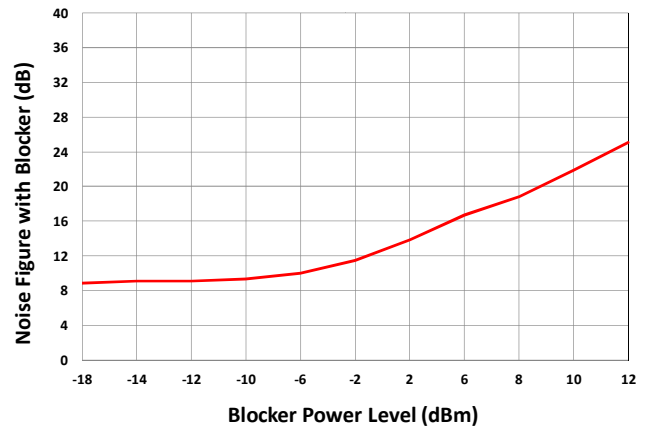


TYPICAL OPERATION CONDITIONS [IF = 300MHz, LOW SIDE INJECTION] (-7-)

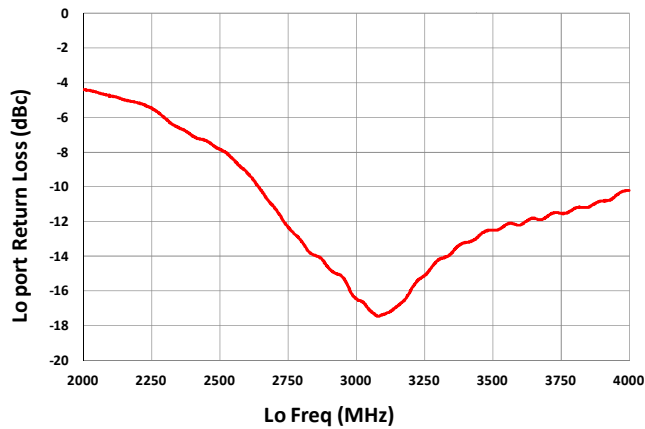
NOISE FIGURE [RF: 3550MHz]



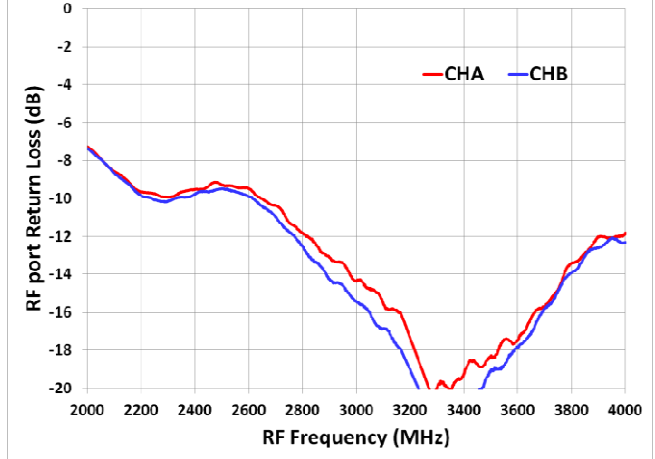
NOISE FIGURE w/ BLOCKER 100MHz OFFSET [RF: 3550MHz]



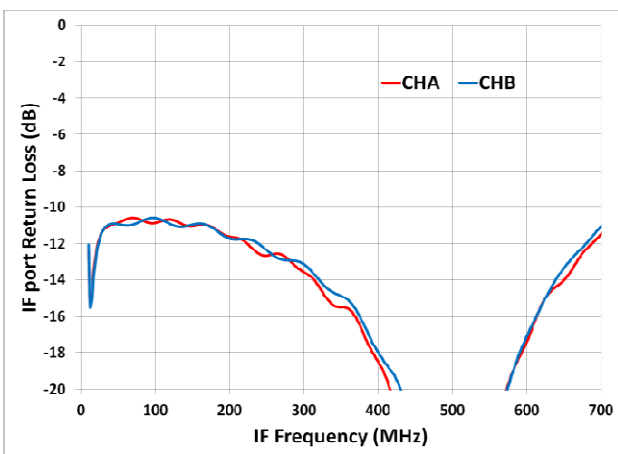
LO PORT RETURN LOSS



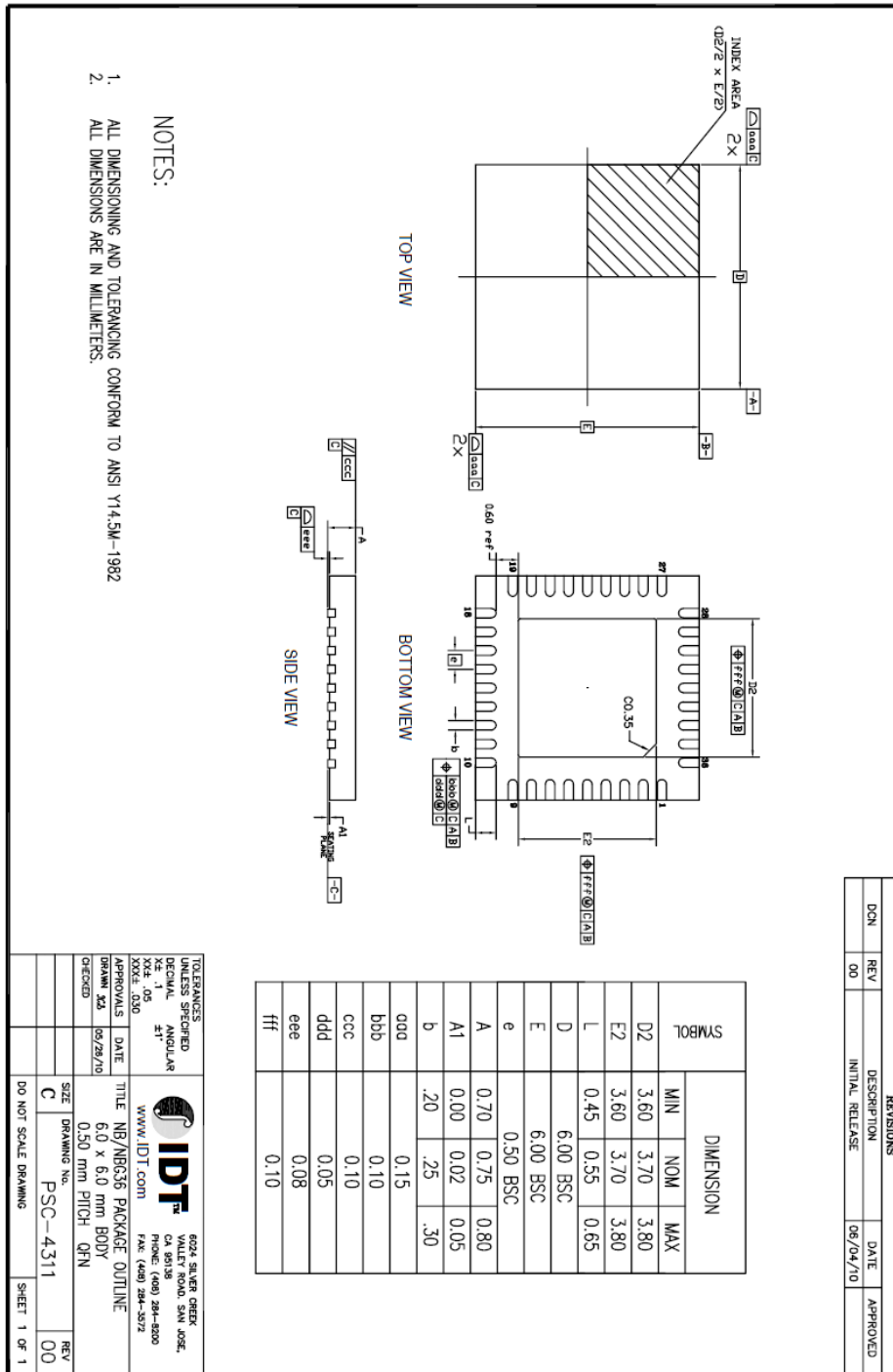
RF PORT RETURN LOSS



IF PORT RETURN LOSS



PACKAGE DRAWING (6X6 QFN)



| REVISIONS | | | |
|-----------|-----|-----------------|----------|
| DEN | REV | DESCRIPTION | DATE |
| | 00 | INITIAL RELEASE | 06/04/10 |
| | | | APPROVED |

TOLERANCES UNLESS SPECIFIED

DECIMAL ANGULAR
 X.X .05 1°
 X.XX .030

APPROVALS

| APPROVALS | DATE | TITLE |
|-----------|----------|---------------------------|
| DESIGNED | 05/29/10 | NB/NB6356 PACKAGE OUTLINE |
| DRAWN | | 6.0 x 6.0 mm BODY |
| CHECKED | | 0.50 mm PITCH QFN |

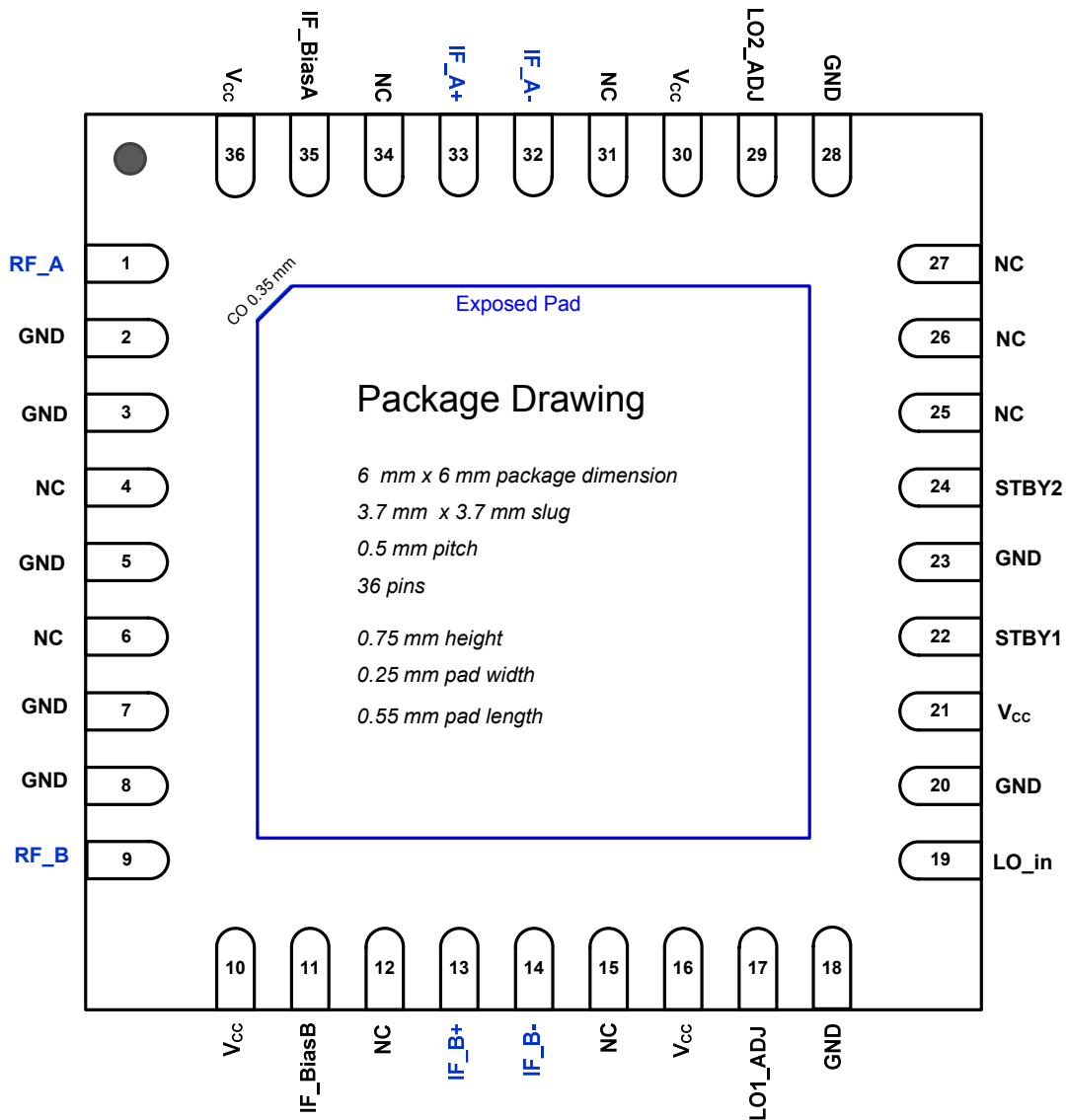
SIZE: C DRAWING No.: PSC-4311 REV: 00

DO NOT SCALE DRAWING SHEET 1 OF 1

IDT 6201 SILVER CREEK VALLEY ROAD, SUITE 400E, CA 94538
 PHONE: (415) 284-8500 FAX: (415) 284-3572
 WWW.IDT.COM

F1178 PINOUT

Signal Path Inputs & Outputs in **BLUE**



PIN DESCRIPTION TABLE

| Pin | Name | Function |
|----------------------------------|------------|--|
| 1 | RF_A | Main Channel RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin. Place the coupling capacitor close as close to the pin as possible. |
| 2, 3, 5, 7, 8, 18, 20, 23, 28 | GND | Ground these pins. |
| 4, 6, 12, 15, 25, 26, 27, 31, 34 | N.C. | No Connection. Not internally connected. OK to connect to Vcc. OK to connect to GND. |
| 10, 16, 21, 30, 36 | VCC | Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin. |
| 9 | RF_B | Diversity Channel RF Input. Internally matched to 50Ω. DO NOT apply DC to this pin. Place the coupling capacitor close as close to the pin as possible. |
| 11 | IF_BiasB | Connect the specified resistor from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor. |
| 13, 14 | IFB+, IFB- | Diversity Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit). |
| 17 | LO1_ADJ | Connect the specified resistor from this pin to ground to set the first stage LO common buffer Icc. |
| 19 | LO_in | Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor. DO NOT apply DC to this pin. |
| 22 | STBY1 | STBY control pin 1. See STBY Logic Table for desired setting |
| 24 | STBY2 | STBY control pin 2. See STBY Logic Table for desired setting |
| 29 | LO2_ADJ | Connect the specified resistor from this pin to ground to set the first stage LO common buffer Icc. |
| 32, 33 | IFA-, IFA+ | Main Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit). |
| 35 | IF_BiasA | Connect the specified resistor from this pin to ground to set the bias for the Main IF amplifier. This is NOT a current set resistor. |
| | — EP | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance. |

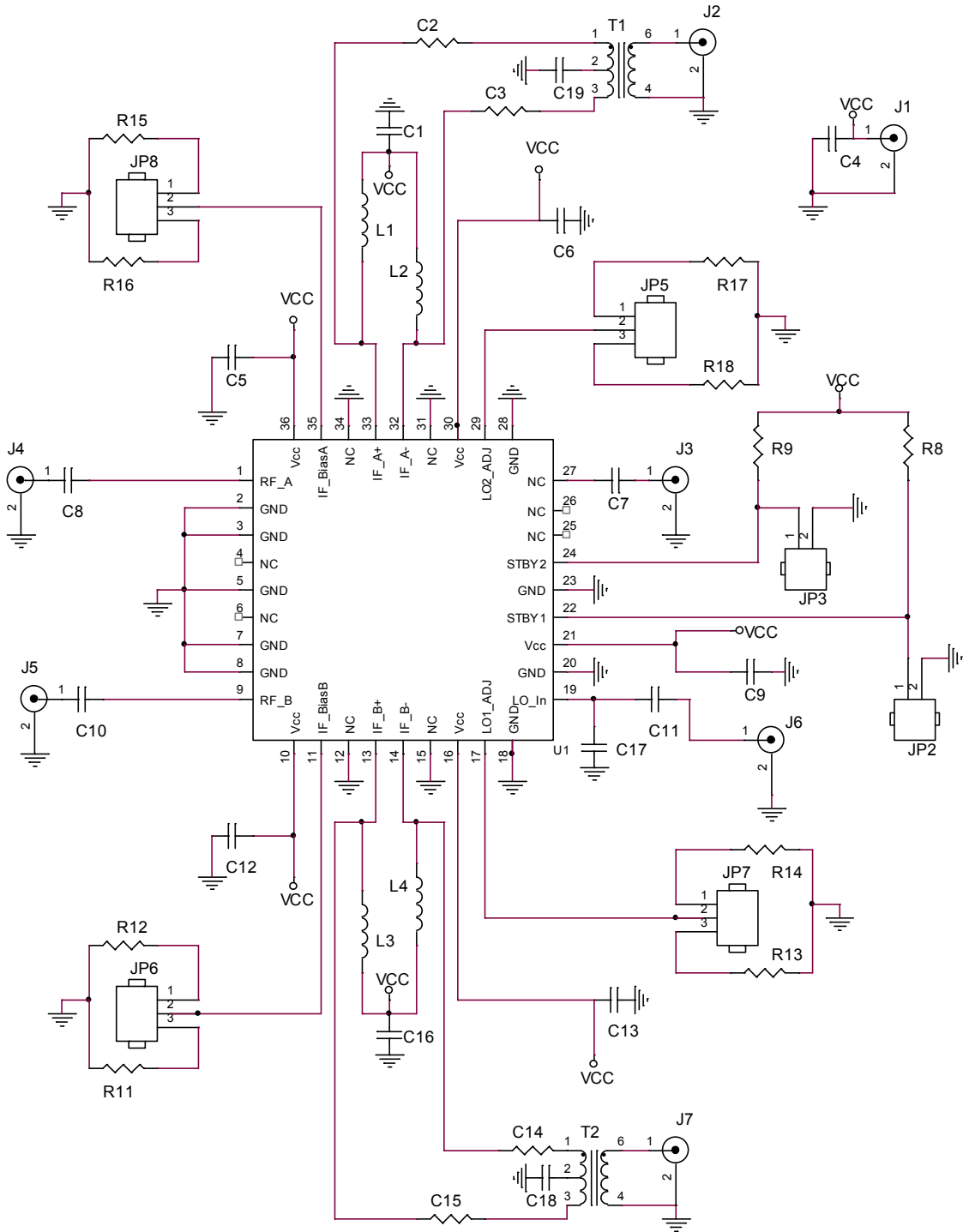
DIGITAL PIN VOLTAGE & RESISTANCE VALUES

| Pin | Name | DC voltage (volts) | Resistance (ohms) |
|-----|-------|--------------------|-------------------|
| 22 | STBY1 | 5 | 50K |
| 24 | STBY2 | Floating voltage | Open Circuit |

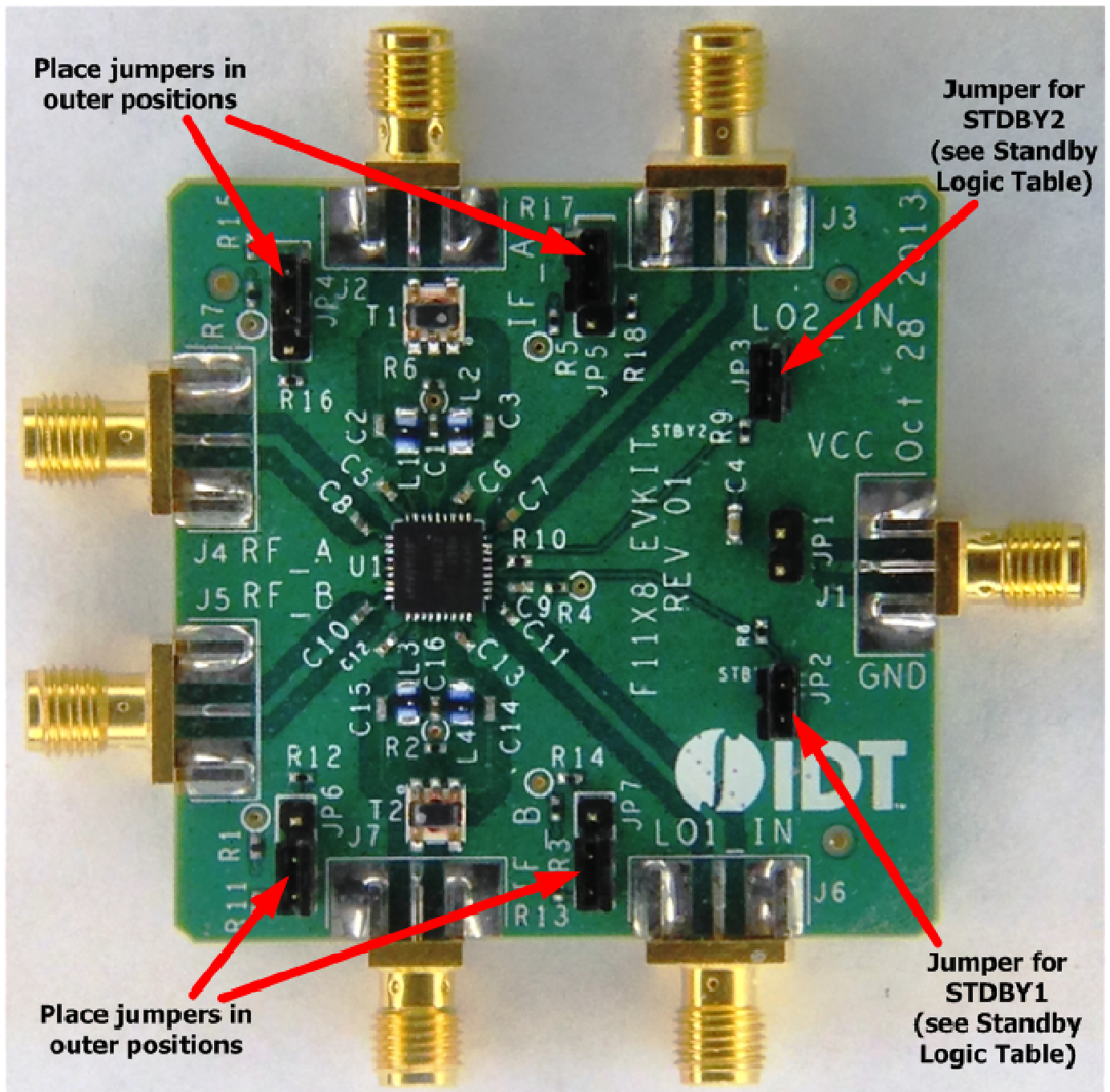
POWER SUPPLIES

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

EVKIT & TYPICAL APPLICATION SCHEMATIC



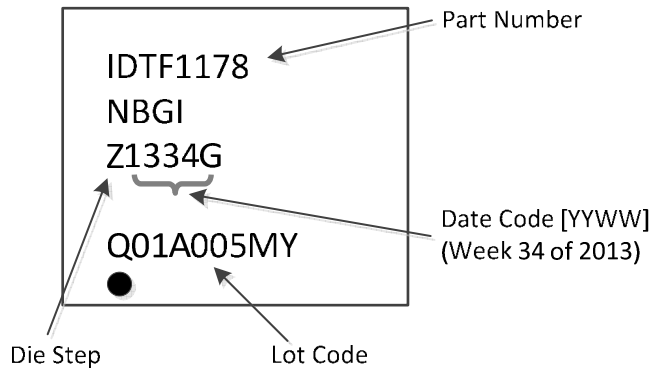
EVKIT PICTURE



EVKIT BOM

| Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|-------------------------------|-----|--|----------------|-----------------|
| C1, C5, C6, C9, C12, C13, C16 | 7 | 10000pF ±10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71C103K | Murata |
| C8, C10, C11 | 3 | 39pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H390J | Murata |
| C17 | 1 | 0.3pF ±0.05pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1HR30W | Murata |
| C18, C19 | 2 | 1000pF ±5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| C4 | 1 | 10uF ±20%, 6.3V, X5R Ceramic Capacitor (0603) | GRM188R60J106M | Murata |
| R1-R7, R10 | 8 | 0Ω 1/10W Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| C2, C3, C14, C15 | 4 | 10Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF10R0X | Panasonic |
| R13 | 1 | 240Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF2400X | Panasonic |
| R14 | 1 | 270Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF2700X | Panasonic |
| R11, R12, R15, R16 | 4 | 330Ω ±1%, 1/10W, Resistor (0402) | ERJ-2RKF3300X | Panasonic |
| R17 | 1 | 2.4kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF2401X | Panasonic |
| R18 | 1 | 2.67kΩ ±1%, 1/10W, Resistor (0402) | ERJ-2RKF2671X | Panasonic |
| R8, R9 | 2 | 47kΩ ±1%, 1/10W, Resistor (0402) | RC0402FR-0747K | Yageo |
| L1-L4 | 4 | 1.8uH ±5%, .410A, Ferrite Chip Inductor (0805) | 0805LS-182XJLB | Coil Craft |
| T1, T2 | 2 | 3-800Mhz 50Ω, RF Transformer (4:1) | TC4-1WG2+ | Mini Circuits |
| JP1, JP2, JP3 | 3 | CONN HEADER VERT SGL 2 X 1 POS GOLD | 961102-6404-AR | 3M |
| JP4, JP5, JP6, JP7 | 4 | CONN HEADER VERT SGL 3 X 1 POS GOLD | 961103-6404-AR | 3M |
| J1, J2, J7 | 3 | Edge Launch SMA (0.250 inch pitch ground round) | 142-0711-821 | Emerson Johnson |
| J3, J4, J5, J6 | 4 | Edge Launch SMA (0.375 inch pitch ground tabs) | 142-0701-851 | Emerson Johnson |
| U1 | 1 | RF to IF Dual Downconverting MIXER 6 X 6 QFN36 | F1178NBGI | IDT |
| | 1 | Printed Circuit Board | F1178 REV (01) | IDT |
| C7 | | No Installed Ceramic Capacitor (0402) | N/A | N/A |

TOP MARKINGS



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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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