Description

The F1129MB is a single-ended input / differential output 3GHz to 4.2GMHz high gain RF amplifier. The combination of impedance translation, high gain, high linearity, and low noise performance makes this device an ideal amplifier for a variety of receiver applications.

The F1129MB has been optimized to operate with a single 5V power supply and a nominal 60mA of I_{CC}. When operated at 3.55GHz, the F1129MB provides 19dB typical gain with 1.8dB noise figure and +32dBm OIP3.

The F1129MB is pin-compatible with Renesas' F1129xx family of RF amplifiers, offering additional frequency and output impedance options. Each F1129 variant is packaged in a 2 × 2 mm, 12-pin DFN, with a 50Ω single-ended RF input and 100Ω differential RF output impedances for ease of integration into the signal-path.

F1129xx Base Part Number	Differential Output Impedance	Frequency Band	Frequency Coverage
F1129LB	100Ω	Low	1.4GHz to 3.2GHz
F1129MB	100Ω	Mid	3.0GHz to 4.2GHz
F1129HB	100Ω	High	4.0GHz to 6.0GHz

Competitive Advantage

- High gain
- Excellent gain flatness over frequency
- Outstanding gain variance over temperature
- STBY feature
- Differential output to directly drive transceiver inputs

Typical Applications

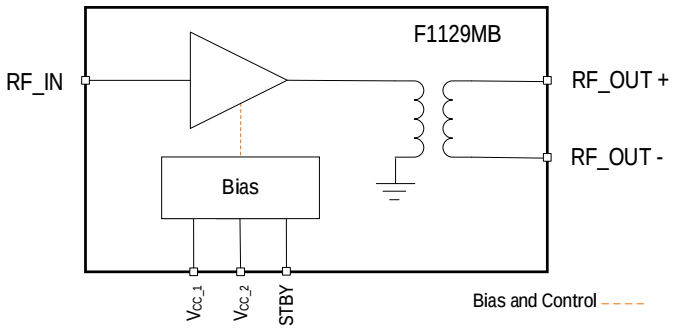
- 5G / Massive MIMO Base Stations
- 4G TDD and FDD Base Stations
- 2G/3G Base Stations
- Repeaters and DAS
- Point to Point Infrastructure
- Public Safety Infrastructure
- Military Handhelds

Features

- RF range: 3.0GHz to 4.2GHz
- Gain = 19dB at 3.55GHz
- Noise figure = 1.8dB at 3.55GHz
- OIP3 = +32dBm at 3.55GHz
- Output P1dB = +18dBm at 3.55GHz
- Gain variation over temperature = ±0.15dB typical
- 50Ω single-ended input impedances
- 100Ω differential output impedances
- 3.3V or 5V power supply
- I_{CC} = 60mA at 5V
- 1.3mA standby current
- 1.8V and 3.3V logic support for STBY control
- Operating temperature (T_{EP}) range: -40°C to +115°C
- 2 × 2 mm, 12-DFN package

Block Diagram

Figure 1. F1129MB Block Diagram



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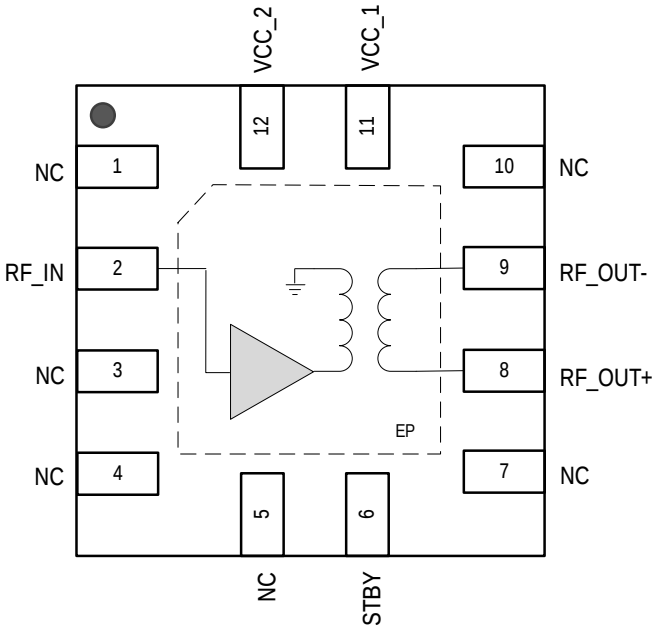
Pin Assignments

Figure 2. F1129MB Pin Assignments for 2 × 2 × 0.75 mm 12-DFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 3, 4, 5, 7, 10	NC	No internal connection. It is highly recommended that these pins be connected to a ground via which is located as close to each pin as possible.
2	RF_IN	Single ended RF Input. Must use external DC block.
6	STBY	Standby. If the pin is not connected or is logic LOW, the device will operate under its normal operating condition. Apply a logic HIGH for STBY.
8	RF_OUT+	Differential RF Output +. Internally tied to ground. Recommended to use an external DC block to prevent shorting of any DC voltage that may be present on the following RF stage.
9	RF_OUT-	Differential RF Output -. Internally tied to ground. Recommended to use an external DC block to prevent shorting of any DC voltage that may be present on the following RF stage.
11	VCC_1	Connect to supply voltage via choke. An external bypass capacitor must be placed as close to the pin as possible.
12	VCC_2	Connect to V_{CC}. An external bypass capacitor must be placed as close to the pin as possible.
	EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1129MB at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VCC_1, VCC_2 to GND	V_{CC}	-0.3	+5.5	V
STBY	V_{STBY}	-0.3	Lower of (5V, V_{CC} + 0.25V)	V
RF Input Power Applied for 24 Hours Maximum (VCC applied, f = 3.6GHz, T_{EP} = +115°C, and input / output VSWR = 1:1 based on a 100Ω system.) [b]	P_{MAX24}		+20	dBm
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM	V_{ESDHBM}		500	V
Electrostatic Discharge – CDM	V_{ESDCDM}		1500	V

[a] Exposure to these maximum RF levels can result in significant V_{CC} current draw due to overdriving the amplifier stages.

[b] Tested using an external 2:1 transformer at the RF output.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage [a]	V_{CC}	V_{CC} pins	4.75		5.25	V
Operating Temperature Range	T_{EP}	Exposed paddle temperature	-40		+115	°C
Junction Temperature	T_{JMAX}				150	°C
RF Frequency Range [b]	f_{RF}		3.0		4.2	GHz
RF_IN Source Impedance	Z_{RF_IN}	Single-ended		50		Ω
RF_OUT Load Impedance	Z_{RF_OUT}	Differential		100		Ω

[a] Although the device will operate with a minimum supply voltage of 3.15V, the performance of the device has been optimized to operate within a supply voltage range of 4.75V to 5.25V.

[b] To optimize RF performance, different matching components might be used as described in the BOM.

Electrical Characteristics - 5V Supply

See the F1129MB application circuit. Specifications apply when operated at V_{CC} = +5.0V, f_{RF} = 3.55GHz, T_{EP} = +25°C, STBY = logic LOW, Z_S = 50Ω single ended, Z_L = 100Ω differential, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics with a 5V Supply

Note: See important table notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		*1.17*[a]			V
Logic Input Low Threshold	V_{IL}				*0.63*	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	*-5*		*+80*	µA
Supply Current	I_{CC}			60	*76*	mA
Standby Current	I_{CC_STBY}			1.3		mA
Settling Time	t_{SETTLE}	From 50% STBY control to within ±0.5dB of final gain.		300		ns
RF Input Return Loss	RL_{IN}	f_{RF} = 3.0GHz		16		dB
		f_{RF} = 3.3GHz		16		
		f_{RF} = 3.55GHz		17		
		f_{RF} = 3.8GHz		16		
		f_{RF} = 4.2GHz		12		
RF Output Return Loss	RL_{OUT}	f_{RF} = 3.0GHz		16		dB
		f_{RF} = 3.3GHz		12		
		f_{RF} = 3.55GHz		13		
		f_{RF} = 3.8GHz		17		
		f_{RF} = 4.2GHz		13		
Gain	G	f_{RF} = 3.0GHz		19.5		dB
		f_{RF} = 3.3GHz		19.5		
		f_{RF} = 3.55GHz	*17*	19		
		f_{RF} = 3.8GHz		19		
		f_{RF} = 4.2GHz		18		
Gain Flatness (amplitude)	G_{VAR}	f_{RF} = 3.1GHz, ±100MHz		0.1		dB
		f_{RF} = 3.3GHz, ±100MHz		0.1		
		f_{RF} = 3.55GHz, ±100MHz		0.1		
		f_{RF} = 3.8GHz, ±100MHz		0.2		
		f_{RF} = 4.1GHz, ±100MHz		0.8		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain Variation over Temperature	G_{TEMP}	T_{EP} = -40°C to +115°C		±0.15		dB
Reverse Isolation	REV_{ISO}			31		dB
Amplitude Imbalance[b]	$IMBAL_{AMP}$	f_{RF} = 3.0GHz		0.2		dB
		f_{RF} = 3.3GHz		0.3		
		f_{RF} = 3.55GHz		0.5		
		f_{RF} = 3.8GHz		0.6		
		f_{RF} = 4.2GHz		0.8		
Phase Imbalance[c]	$IMBAL_{PH}$	f_{RF} = 3.0GHz		3.3		deg
		f_{RF} = 3.3GHz		2.6		
		f_{RF} = 3.55GHz		1.8		
		f_{RF} = 3.8GHz		1.2		
		f_{RF} = 4.2GHz		1.6		
Common Mode Rejection[d]	CMR	f_{RF} = 3.0GHz		29		dB
		f_{RF} = 3.3GHz		29.5		
		f_{RF} = 3.55GHz		29.5		
		f_{RF} = 3.8GHz		28		
		f_{RF} = 4.2GHz		26		
Noise Figure	NF	f_{RF} = 3.0GHz		1.7		dB
		f_{RF} = 3.3GHz		1.7		
		f_{RF} = 3.55GHz		1.8	2	
		f_{RF} = 3.8GHz		1.9		
		f_{RF} = 4.2GHz		2.1		
Noise Figure Variation over Temp	NF_{TEMP}	T_{EP} = -40°C to +115°C		± 0.5		dB
Output Third Order Intercept Point[e]	OIP3	f_{RF} = 3.0GHz		34		dBm
		f_{RF} = 3.3GHz		33		
		f_{RF} = 3.55GHz	30	32		
		f_{RF} = 3.8GHz		32		
		f_{RF} = 4.2GHz		29		
Output P1dB	OP1dB	f_{RF} = 3.0GHz		20		dBm
		f_{RF} = 3.3GHz		19		
		f_{RF} = 3.55GHz	16	18		
		f_{RF} = 3.8GHz		18		
		f_{RF} = 4.2GHz		16.5		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ amplitude.

[c] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ phase. Deviation is from ideal 180 degrees.

[d] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+.

[e] OIP3 test conditions: Tone spacing = 5MHz, P_{OUT} = +0dBm/tone.

Electrical Characteristics - 3.3V Supply

See the F1129MB application circuit. Specifications apply when operated at VCC = +3.3V, f_{RF} = 3.55GHz, T_{EP} = +25°C, STBY = logic LOW, ZS = 50Ω single ended, ZL = 100Ω differential, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 5. Electrical Characteristics with a 3.3V Supply

Note: See important table notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		1.17[a]			V
Logic Input Low Threshold	V_{IL}				0.63	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	-10		+100	µA
Supply Current	I_{CC}			30		mA
Settling Time	t_{SETTLE}	From 50% STBY control to within ±0.5dB of final gain.		500		ns
RF Input Return Loss	RL_{IN}	f_{RF} = 3.0GHz		13		dB
		f_{RF} = 3.3GHz		13		
		f_{RF} = 3.55GHz		13		
		f_{RF} = 3.8GHz		13		
		f_{RF} = 4.2GHz		12		
RF Output Return Loss	RL_{OUT}	f_{RF} = 3.0GHz		15		dB
		f_{RF} = 3.3GHz		12		
		f_{RF} = 3.55GHz		13		
		f_{RF} = 3.8GHz		16		
		f_{RF} = 4.2GHz		11		
Gain	G	f_{RF} = 3.0GHz		18		dB
		f_{RF} = 3.3GHz		18		
		f_{RF} = 3.55GHz		18		
		f_{RF} = 3.8GHz		18		
		f_{RF} = 4.2GHz		16.5		
Gain Flatness (amplitude)	G_{VAR}	f_{RF} = 3.1GHz, ±100MHz		0.2		dB
		f_{RF} = 3.3GHz, ±100MHz		0.1		
		f_{RF} = 3.55GHz, ±100MHz		0.1		
		f_{RF} = 3.8GHz, ±100MHz		0.3		
		f_{RF} = 4.1GHz, ±100MHz		0.9		
Gain Variation over Temperature	G_{TEMP}	T_{EP} = -40°C to +115°C		±0.2		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Reverse Isolation	REV_{ISO}			31		dB
Amplitude Imbalance[b]	$IMBAL_{AMP}$	f_{RF} = 3.0GHz		0.2		dB
		f_{RF} = 3.3GHz		0.3		
		f_{RF} = 3.55GHz		0.5		
		f_{RF} = 3.8GHz		0.6		
		f_{RF} = 4.2GHz		0.8		
Phase Imbalance[c]	$IMBAL_{PH}$	f_{RF} = 3.0GHz		3.3		deg
		f_{RF} = 3.3GHz		2.5		
		f_{RF} = 3.55GHz		1.8		
		f_{RF} = 3.8GHz		1.1		
		f_{RF} = 4.2GHz		1.6		
Common Mode Rejection[d]	CMR	f_{RF} = 3.0GHz		29		dB
		f_{RF} = 3.3GHz		29.5		
		f_{RF} = 3.55GHz		29.5		
		f_{RF} = 3.8GHz		28		
		f_{RF} = 4.2GHz		26		
Noise Figure	NF	f_{RF} = 3.0GHz		1.8		dB
		f_{RF} = 3.3GHz		1.8		
		f_{RF} = 3.55GHz		1.9		
		f_{RF} = 3.8GHz		2		
		f_{RF} = 4.2GHz		2.2		
Noise Figure Variation over Temp	NF_{TEMP}	T_{EP} = -40°C to +115°C		±0.5		dB
Output Third Order Intercept Point[e]	OIP3	f_{RF} = 3.0GHz		27		dBm
		f_{RF} = 3.3GHz		27		
		f_{RF} = 3.55GHz		26		
		f_{RF} = 3.8GHz		25		
		f_{RF} = 4.2GHz		21		
Output P1dB	OP1dB	f_{RF} = 3.0GHz		15		dBm
		f_{RF} = 3.3GHz		14.5		
		f_{RF} = 3.55GHz		13		
		f_{RF} = 3.8GHz		13		
		f_{RF} = 4.2GHz		12		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ amplitude.

[c] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ phase. Deviation is from ideal 180 degrees.

[d] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+.

[e] OIP3 test conditions: Tone spacing = 5MHz, P_{OUT} = +0dBm/tone.

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	112.57	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	27.6	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Evaluation kit connector and trace losses de-embedded
- V_{CC} = 5.0V (plots also taken with V_{CC} = 3.3V)
- T_{EP} = 25°C
- STBY = not connected (internally pulled logic LOW)
- Small signal parameters measured with P_{OUT} = 0dBm
- Two tone tests P_{OUT} = 0dBm/tone with 5MHz tone spacing
- All unused ports properly terminated
- S-parameters (S11, S21, S12, and S22) measured using a de-embedded Differential Board EVKit with Z_S = single-ended 50Ω and Z_L = differential 100Ω. The inputs are mathematically combined using an ideal 1:2 (50Ω:100Ω) transformer to produce the 2 port S-parameters.
- OIP3, Output P1dB and Noise Figure measured using a Transformer Board EVKit with Z_S = Z_L = single-ended 50Ω
- Amplitude and phase imbalances measures RF_IN to RF_OUT+ and compares to RF_IN to RF_OUT-
- Phase imbalance is the deviation from an ideal 180 degrees

Note: The use of the external transformer T1 is included for simple 2 port evaluation purposes. At some frequencies the external transformer interacts with the on-chip balun affecting the gain and noise figure flatness responses. These interactions have been removed from the noise figure TOCs.

Typical 5V Performance Characteristics

Figure 3. Gain

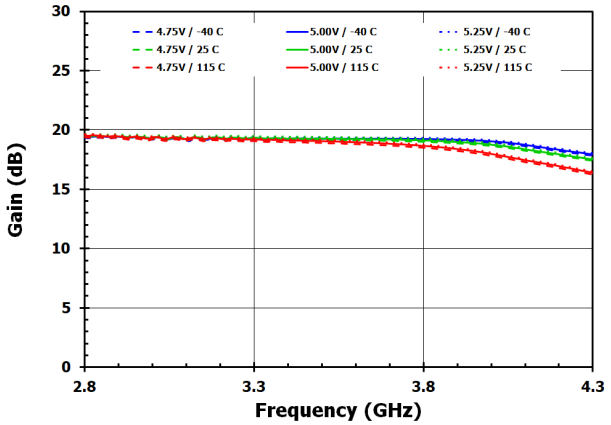


Figure 4. Reverse Isolation

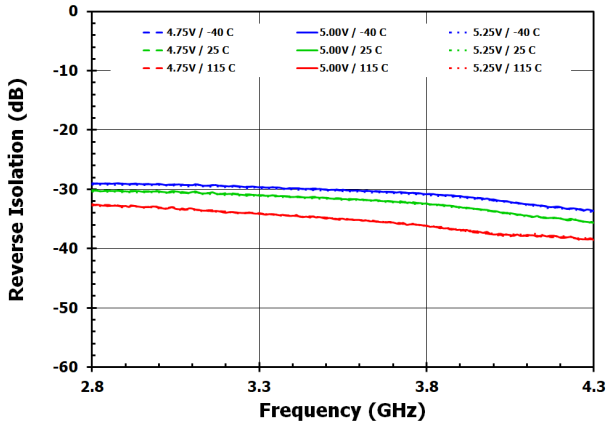


Figure 5. Input Return Loss

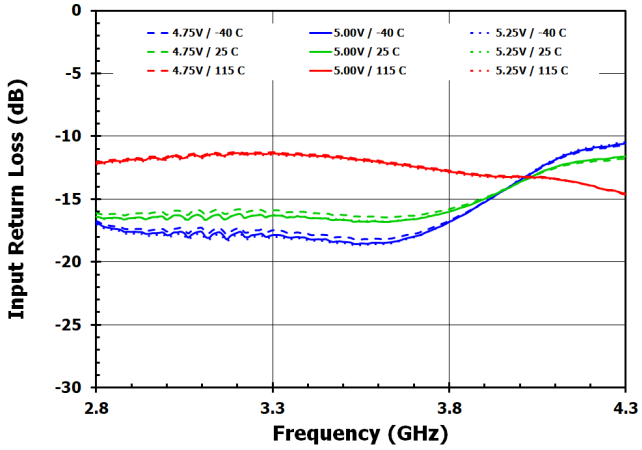


Figure 6. Output Return Loss

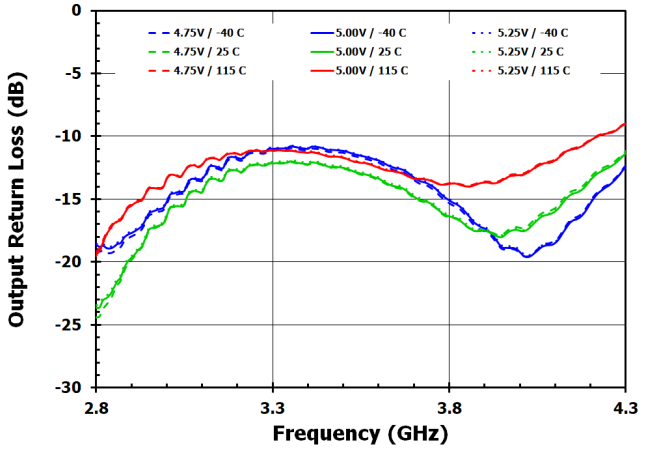


Figure 7. Output IP3

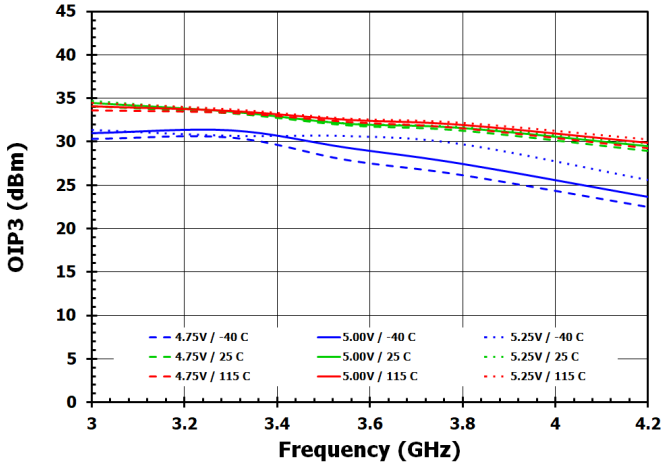


Figure 8. Output P1dB

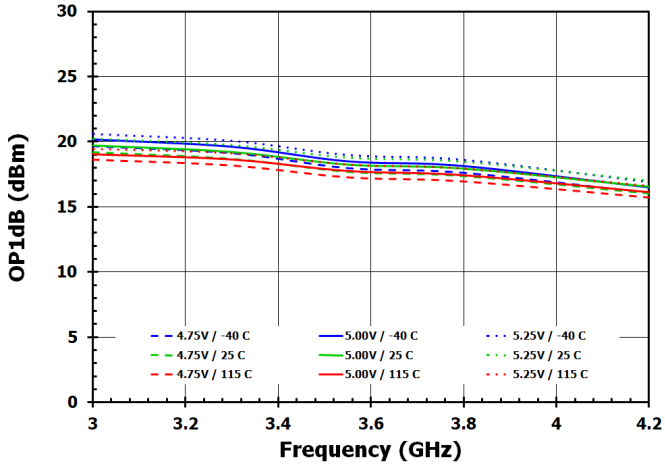


Figure 9. Noise Figure

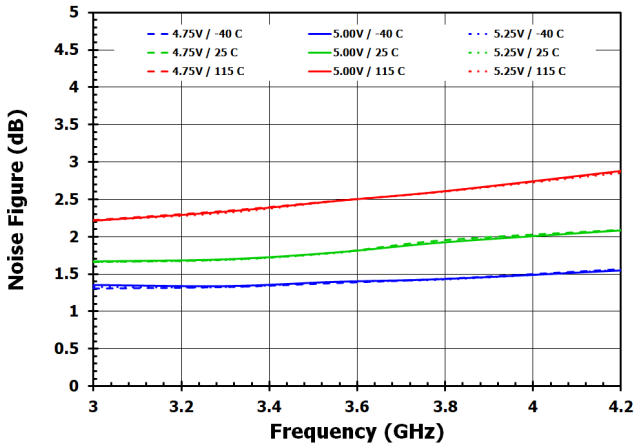


Figure 10. Amplitude Imbalance

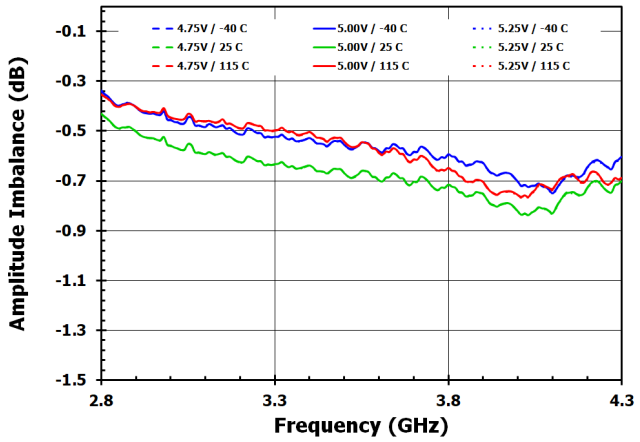


Figure 11. Phase Imbalance

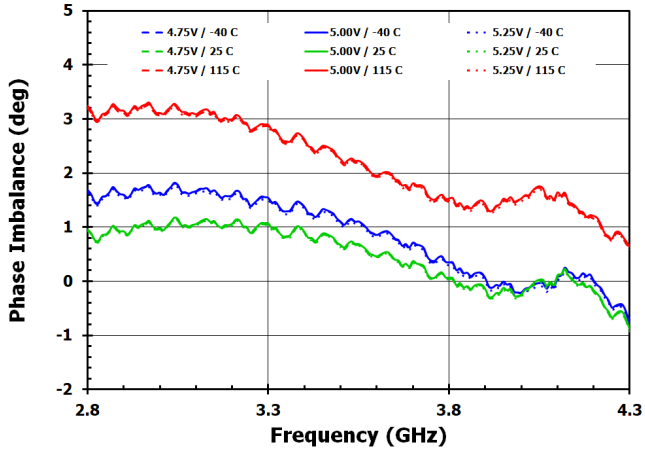
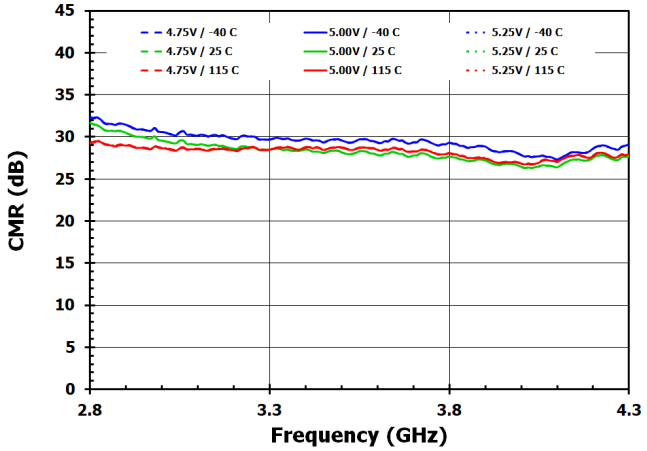


Figure 12. CMR



Typical 3.3V Performance Characteristics

Figure 13. Gain

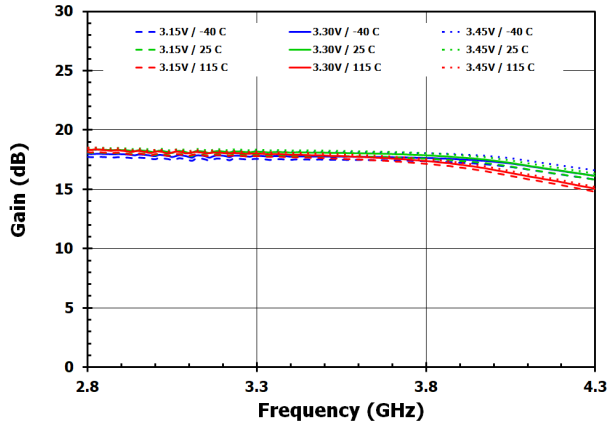


Figure 14. Reverse Isolation

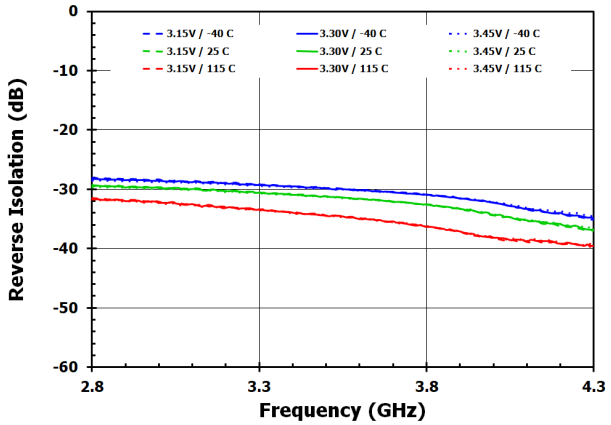


Figure 15. Input Return Loss

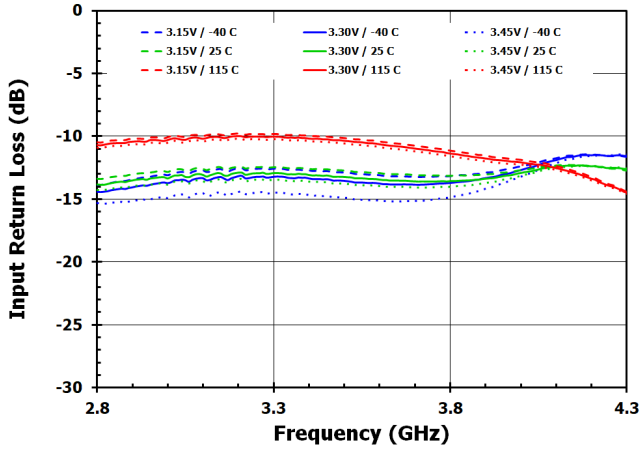


Figure 16. Output Return Loss

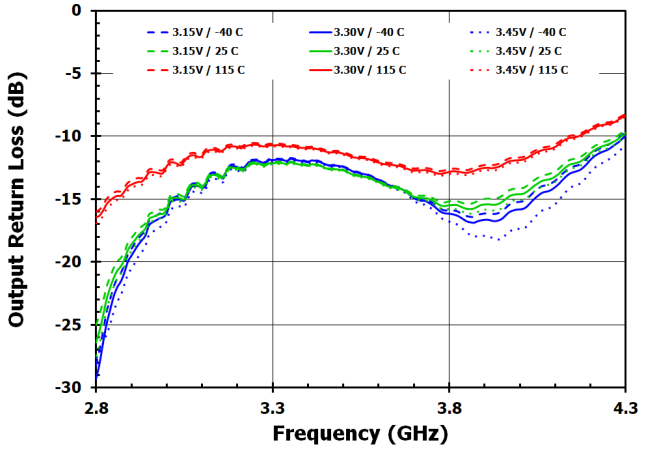


Figure 17. Output IP3

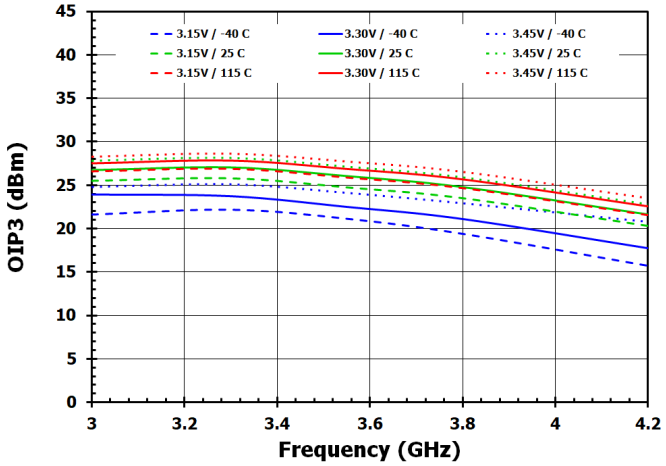


Figure 18. Output P1dB

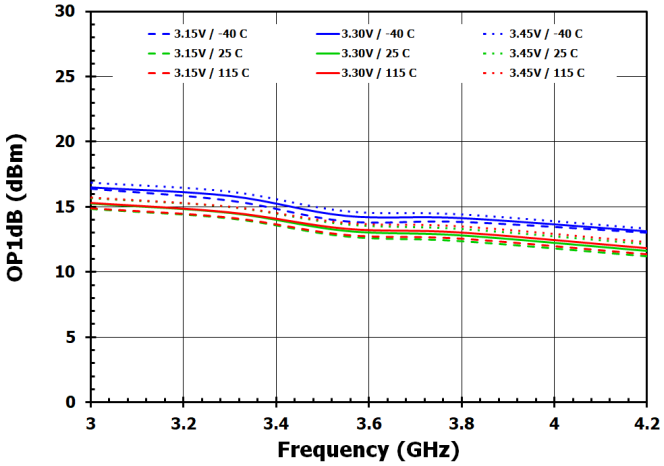


Figure 19. Noise Figure

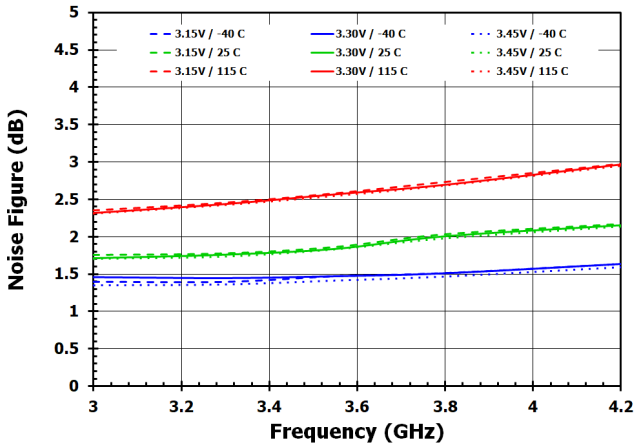


Figure 20. Amplitude Imbalance

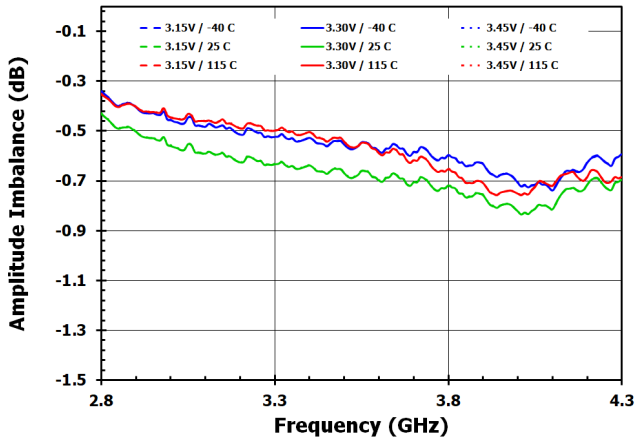


Figure 21. Phase Imbalance

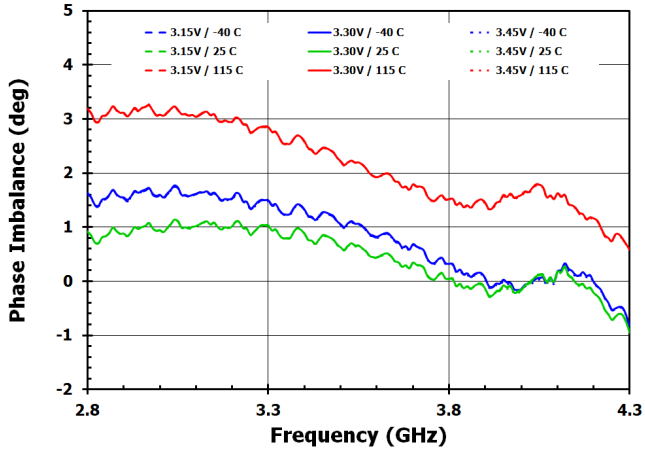
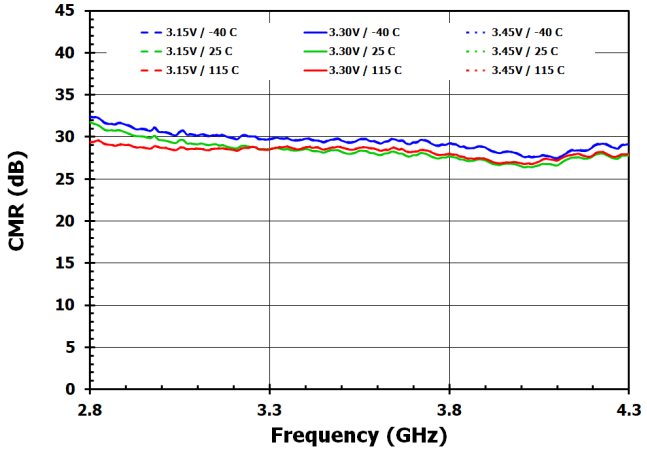


Figure 22. CMR



Evaluation Kit Picture

Figure 23. Top View

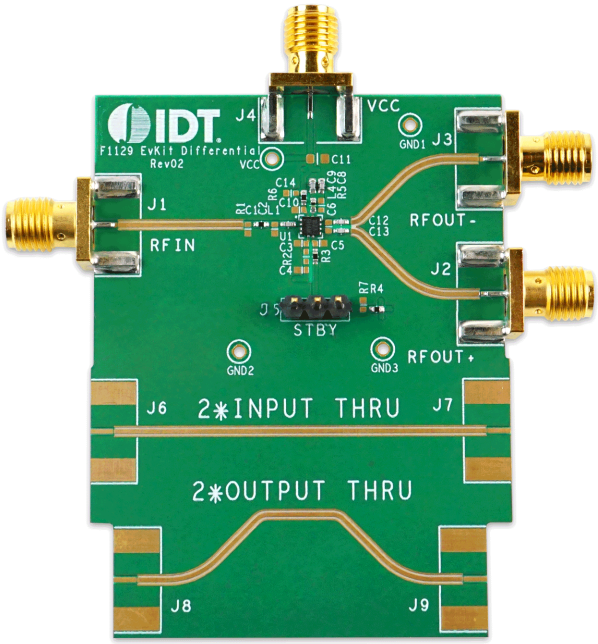
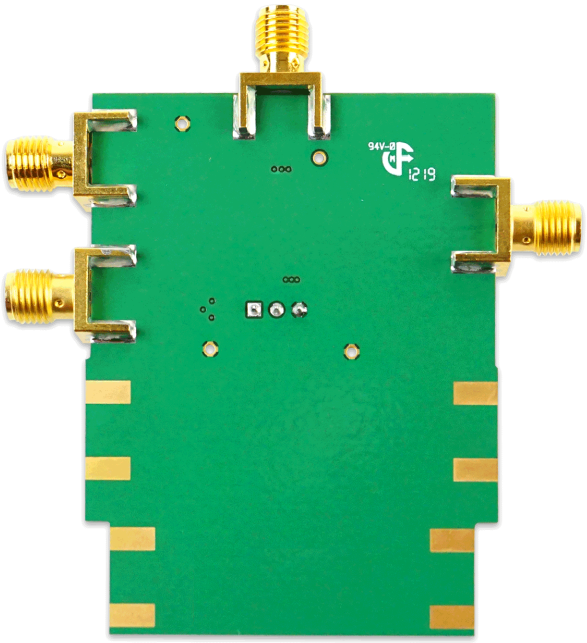


Figure 24. Bottom View



Evaluation Kit Circuit

Figure 25. Evaluation Kit Electrical Schematic

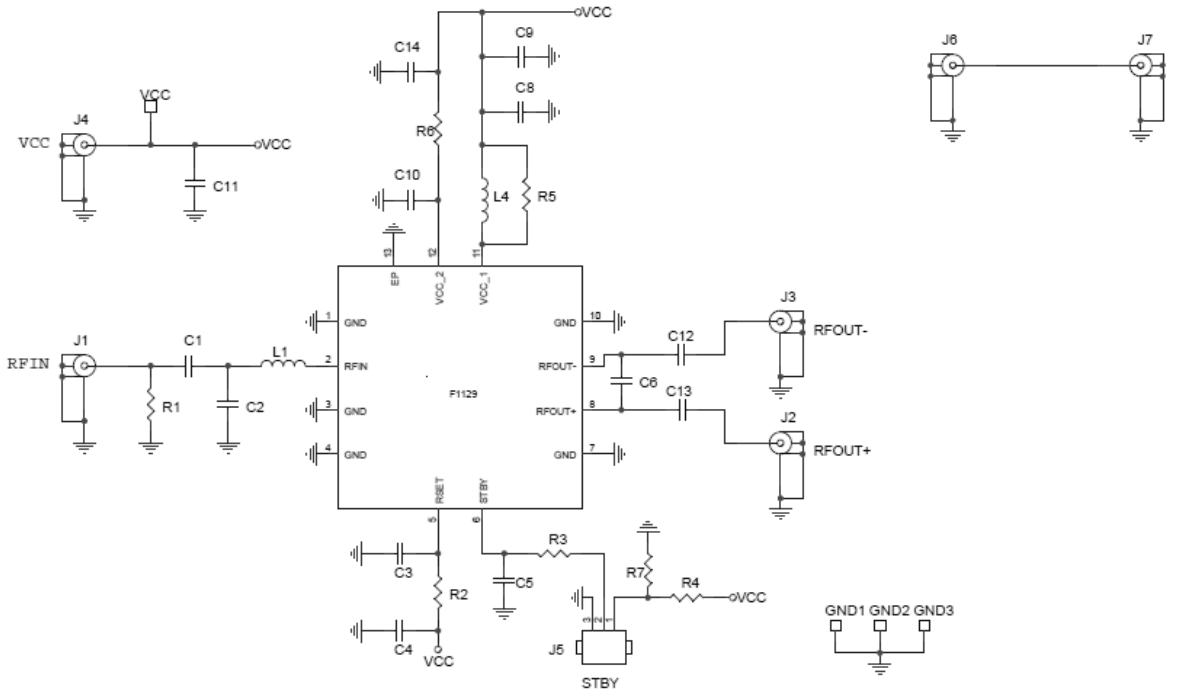


Table 7. Evaluation Kit Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1,R6,R3,R4	4	0 ohm Jumper 1/10W (0402)	ERJ2GE0R00X	Panasonic
C9	1	1000pF C0G 50v (0402)	GRM1555C1H102J	Murata
C8	1	100pF C0G 50v (0402)	GRM1555C1H101J	Murata
L1	1	10pF C0G 50v (0402)	GRM1555C1H100J	Murata
L4	1	1.0nH ±0.3 (0402)	LQG15HS1N0S02	Murata
C12,C13	2	5pF NP0 50V (0402)	GRM1555C1H50BA01D	Murata
J5	1	CONN HEADER VERT 1x3 POS 2.54MM	61300311121	Würth Elektronik
J1,J2, J3, J4, J6, J7, J8, J9	8	SMA Edge Mount	142-0701-851	Cinch Connectivity
C10,C11,C14,C2,,C3,C4,C5,C6,R1,R2,R5,R7	0	Do not install		
U1	1	F1129MB 50Ω SE-In – 100Ω DIFF-Out Amplifier	F1129MBNELI	IDT Renesas
	1	Printed Circuit Board	F1129 EVKIT DIFF Rev.02	Vector Fab

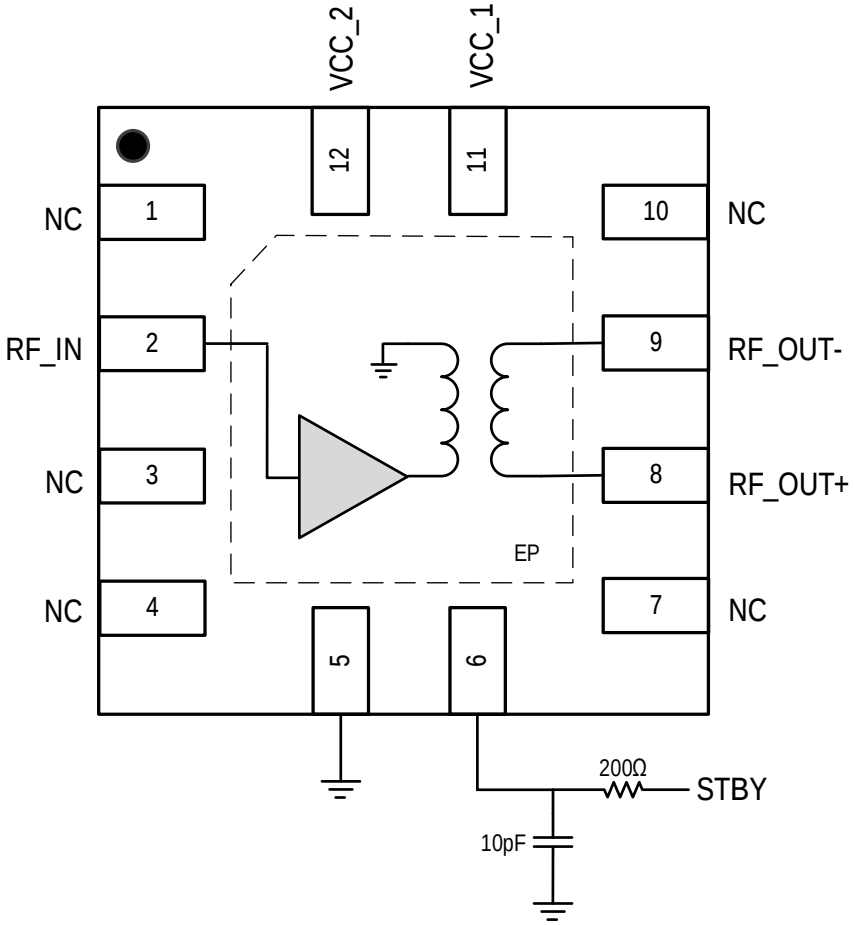
Application Information

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of the STBY control pin is recommended. This applies to the STBY pin as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

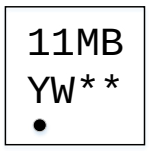
Figure 26. Control Pin Interface Schematic



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



Line 1: 11MB = abbreviated the part number (F1129MB).
Line 2: Y = Year code, last digit of production year ("8" would correspond to 2018).
W = Work week code ("W" corresponds to week 30).
** = Sequential alpha characters for lot traceability.

Ordering Information

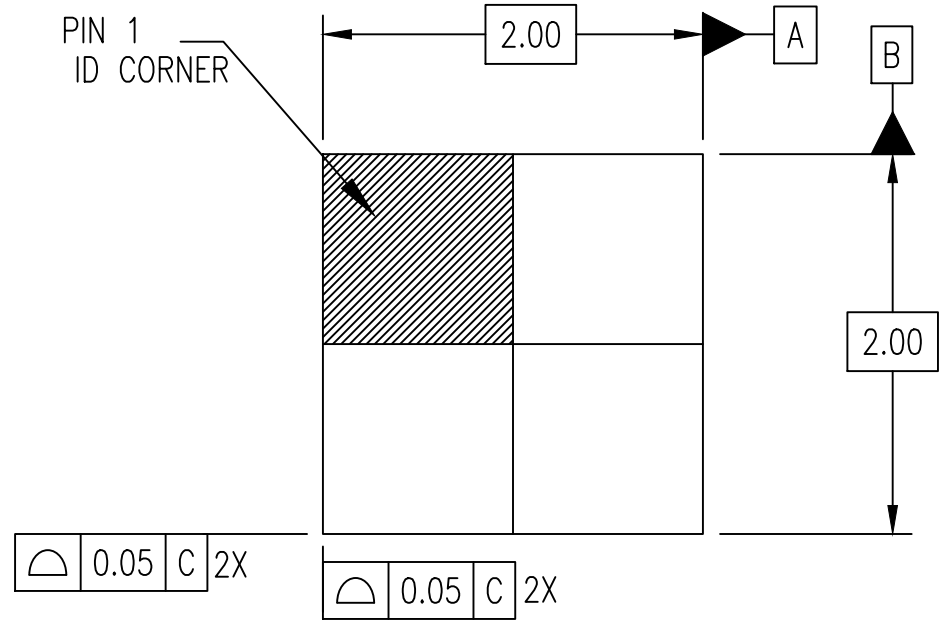
Orderable Part Number	Package	MSL Rating	Carrier Type	Temperature
F1129MBNELI	2 × 2 × 0.75 mm 12-DFN	1	Cut Reel	-40° to +115°C
F1129MBNELI8	2 × 2 × 0.75 mm 12-DFN	1	Reel	-40° to +115°C
F1129MBEVB	Evaluation Board			

Revision History

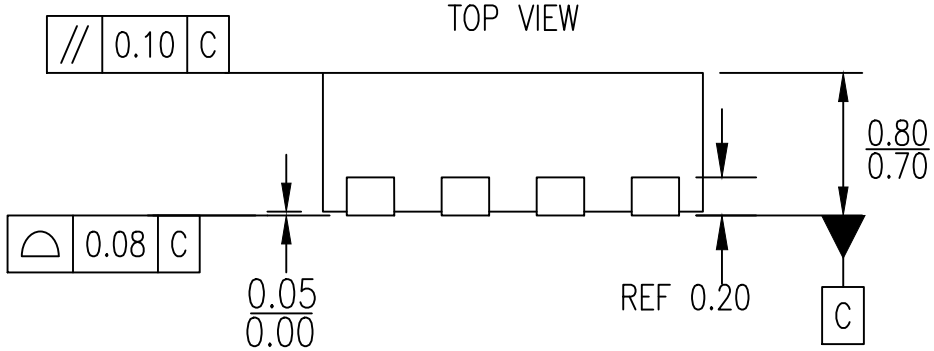
Revision Date	Description of Change
January 31, 2021	▪ Updated the Package Outline Drawings website link ▪ Updated the Carrier Type information in Ordering Information
May 21, 2020	Updated base part number table in Description.
April 29, 2020	Added Application Information for Power Supplies.
January 21, 2020	Updated Evaluation Kit pictures.
December 5, 2019	Initial release.

VFQFPN-12, Package Outline Drawing

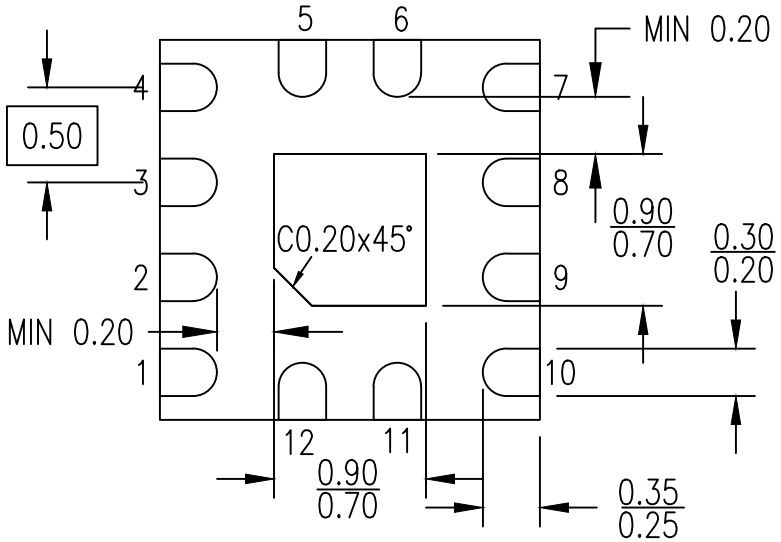
2.0 x 2.0 x 0.75 mm Body, 0.5mm Pitch Epad 0.80 x 0.80 mm



TOP VIEW



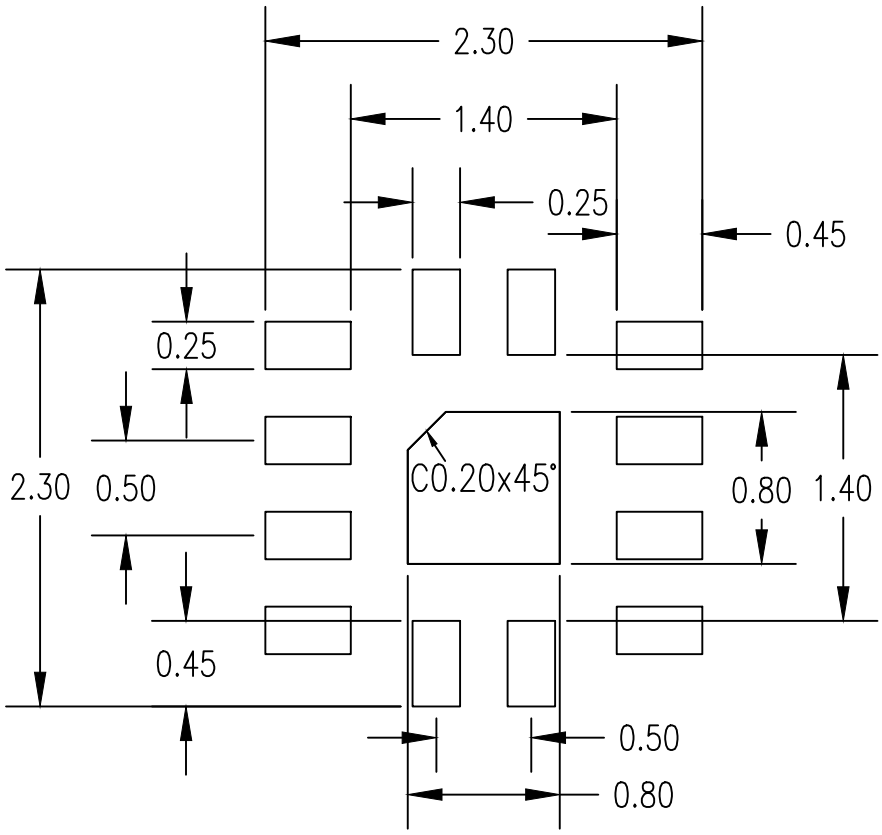
SIDE VIEW (ROTATE 90 DEG.)



BOTTOM VIEW

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASMEY14.5–2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 5, 2018	Rev 01	Add "K" Value Minimium 0.20 mm, Correct L/F Thickness
July 31, 2017	Rev 00	Initial Release

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