Description

The F1129LB is a single-ended input / differential output 1.4GHz to 3.2GHz high gain RF amplifier. The combination of impedance translation, high gain, high linearity, and low noise performance makes this device an ideal amplifier for a variety of receiver applications.

The F1129LB has been optimized to operate with a single 5V power supply and a nominal 61mA of I_{CC}. When operated at 2.5GHz, the device provides 20dB typical gain with 1.6dB noise figure and +36dBm OIP3.

The F1129LB is pin-compatible with Renesas' F1129xx family of RF amplifiers, offering additional frequency and output impedance options. Each F1129 variant is packaged in a 2 × 2 mm, 12-DFN, with a 50Ω single-ended RF input and 100Ω differential RF output impedances for ease of integration in the signal path.

F1129xx Base Part Number	Differential Output Impedance	Frequency Band	Frequency Coverage
F1129LB	100Ω	Low	1.4GHz to 3.2GHz
F1129MB	100Ω	Mid	3.0GHz to 4.2GHz
F1129HB	100Ω	High	4.0GHz to 6.0GHz

Competitive Advantage

- High gain
- Excellent gain flatness over frequency
- Near-constant gain versus temperature

Typical Applications

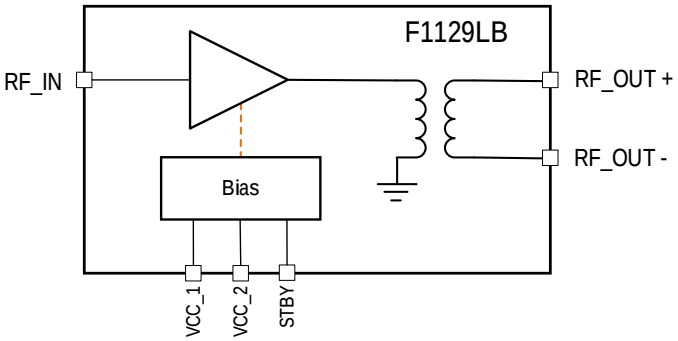
- 5G / Massive MIMO base stations
- 4G TDD and FDD base stations
- 2G/3G base stations
- Repeaters and DAS
- Point-to-point infrastructure
- Public-safety infrastructure
- Military handhelds

Features

- RF range: 1.4GHz to 3.2GHz
- Gain = 20dB typical at 2.5GHz
- Noise figure = 1.6dB typical at 2.5GHz
- OIP3 = +36dBm typical at 2.5GHz
- Output P1dB = +20.5dBm typical at 2.5GHz
- Gain variation over temperature = ±0.2dB typical
- 50Ω single-ended input impedance
- 100Ω differential output impedance
- 3.3V or 5V power supply
- I_{CC} = 61mA at 5V
- 1.4mA standby current
- 1.8V and 3.3V logic support for STBY control
- Operating temperature (T_{EP}) range: -40°C to +115°C
- 2 × 2 mm 12-DFN package

Block Diagram

Figure 1. F1129LB Block Diagram



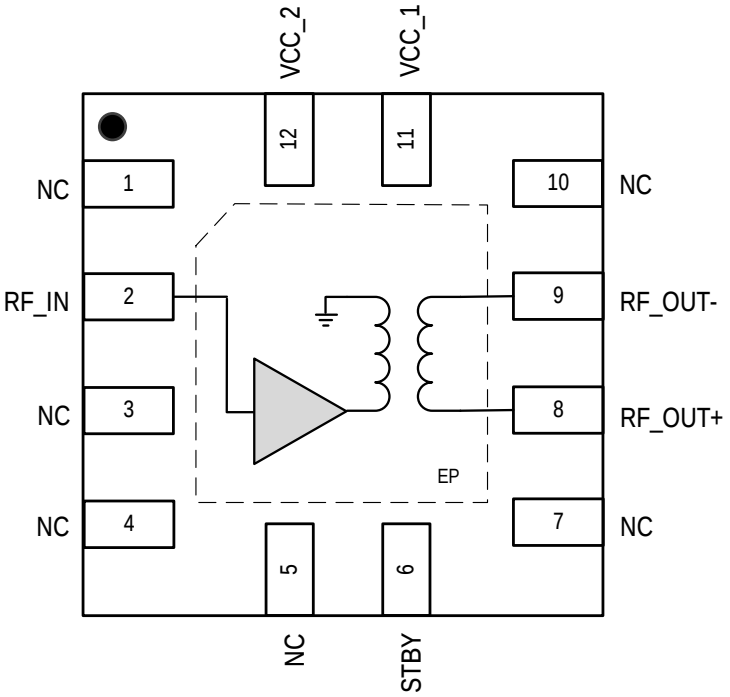
Contents

List of Figures

List of Tables

Pin Assignments

Figure 2. Pin Assignments for 2 × 2 × 0.75 mm 12-DFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 3, 4, 5, 7, 10	NC	No internal connection. It is highly recommended that these pins be connected to a ground via that is located as close to each pin as possible.
2	RF_IN	Single-ended RF input. An external DC block is required.
6	STBY	Standby. If this pin is not connected or is logic LOW, the F1129LB will operate under its normal operating condition. Apply a logic HIGH for STBY.
8	RF_OUT+	Differential RF output +. Internally tied to ground. Recommendation: Use an external DC block to prevent shorting of any DC voltage that may be present on the following RF stage.
9	RF_OUT-	Differential RF output -. Internally tied to ground. Recommendation: Use an external DC block to prevent shorting of any DC voltage that may be present on the following RF stage.
11	VCC_1	Connect to the supply voltage via a choke. An external bypass capacitor must be placed as close to the pin as possible.
12	VCC_2	Connect to V_{CC}. An external bypass capacitor must be placed as close to the pin as possible.
	EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the F1129LB into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1129LB at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VCC_1, VCC_2 to GND	V_{CC}	-0.3	+5.5	V
STBY	V_{STBY}	-0.3	Lower of (5V, V_{CC} + 0.25V)	V
RF Input Power applied for 24 Hours maximum (V_{CC} applied, f = 2.5GHz, T_{EP} = +115°C, and input/output VSWR = 1:1 based on a 100Ω system.) [a, b]	P_{MAX24}		+22	dBm
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – Human Body Model (HBM) (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		500	V
Electrostatic Discharge – Charge Device Model (CDM) (JEDEC 22-C101F)	V_{ESDCDM}		1500	V

[a] Exposure to these maximum RF levels can result in significant V_{CC} current draw due to overdriving the amplifier stages.

[b] Tested using an external 2:1 transformer at the RF output.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage [a]	V_{CC}	V_{CC} pins	4.75		5.25	V
Operating Temperature Range	T_{EP}	Exposed paddle temperature	-40		+115	°C
Junction Temperature	T_{JMAX}				150	°C
RF Frequency Range [b]	f_{RF}		1.4		3.2	GHz
RF_IN Source Impedance	Z_{RF_IN}	Single-ended		50		Ω
RF_OUT Load Impedance	Z_{RF_OUT}	Differential		100		Ω

[a] Although the device will operate with a minimum supply voltage of 3.15V, the performance of the device has been optimized to operate within a supply voltage range of 4.75V to 5.25V.

[b] To optimize RF performance, different matching components can be used as described in the BOM.

Electrical Characteristics – 5V Supply

See the F1129LB application circuit. Specifications apply when operated at V_{CC} = +5.0V, f_{RF} = 2.5GHz, T_{EP} = +25°C, STBY = logic LOW, Z_S = 50Ω single-ended, Z_L = 100Ω differential, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics with a 5V Supply

Note: See important notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH Threshold	V_{IH}		*1.17*[a]			V
Logic Input LOW Threshold	V_{IL}				*0.63*	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	*-5*		*+80*	µA
Supply Current	I_{CC}			61	*78*	mA
Standby Current	I_{CC_STBY}			1.4		mA
Settling Time	t_{SETTLE}	From 50% STBY control to within ±0.5dB of final gain		300		ns
RF Input Return Loss	RL_{IN}	f_{RF} = 1.4GHz		8		dB
		f_{RF} = 1.7GHz		9		
		f_{RF} = 2.0GHz		12		
		f_{RF} = 2.3GHz		17		
		f_{RF} = 2.5GHz		21		
		f_{RF} = 2.7GHz		18		
		f_{RF} = 3.2GHz		12		
RF Output Return Loss	RL_{OUT}	f_{RF} = 1.4GHz		8		dB
		f_{RF} = 1.7GHz		7		
		f_{RF} = 2.0GHz		9		
		f_{RF} = 2.3GHz		13		
		f_{RF} = 2.5GHz		22		
		f_{RF} = 2.7GHz		20		
		f_{RF} = 3.2GHz		8		
Gain	G	f_{RF} = 1.4GHz		19		dB
		f_{RF} = 1.7GHz		19.5		
		f_{RF} = 2.0GHz		19.5		
		f_{RF} = 2.3GHz		20		
		f_{RF} = 2.5GHz	*17*	20		
		f_{RF} = 2.7GHz		20		
		f_{RF} = 3.2GHz		19		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain Flatness (amplitude)	G_{VAR}	f_{RF} = 1.5GHz, ±100MHz		0.3		dB
		f_{RF} = 1.7GHz, ±100MHz		0.1		
		f_{RF} = 2.0GHz, ±100MHz		0.1		
		f_{RF} = 2.3GHz, ±100MHz		0.3		
		f_{RF} = 2.5GHz, ±100MHz		0.1		
		f_{RF} = 2.7GHz, ±100MHz		0.2		
		f_{RF} = 3.1GHz, ±100MHz		0.5		
Gain Variation over Temperature	G_{TEMP}	T_{EP} = -40°C to +115°C		±0.2		dB
Reverse Isolation	REV_{ISO}			31		dB
Amplitude Imbalance[b]	$IMBAL_{AMP}$	f_{RF} = 1.4GHz		0.1		dB
		f_{RF} = 1.7GHz		0.25		
		f_{RF} = 2.0GHz		0.45		
		f_{RF} = 2.3GHz		0.6		
		f_{RF} = 2.5GHz		0.6		
		f_{RF} = 2.7GHz		0.7		
		f_{RF} = 3.2GHz		0.7		
Phase Imbalance[c]	$IMBAL_{PH}$	f_{RF} = 1.4GHz		3		deg
		f_{RF} = 1.7GHz		2.3		
		f_{RF} = 2.0GHz		1.8		
		f_{RF} = 2.3GHz		1.6		
		f_{RF} = 2.5GHz		1.2		
		f_{RF} = 2.7GHz		1		
		f_{RF} = 3.2GHz		1		
Common Mode Rejection[d]	CMR	f_{RF} = 1.4GHz		31.5		dB
		f_{RF} = 1.7GHz		32.5		
		f_{RF} = 2.0GHz		30.5		
		f_{RF} = 2.3GHz		29		
		f_{RF} = 2.5GHz		28.5		
		f_{RF} = 2.7GHz		28		
		f_{RF} = 3.2GHz		28		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Noise Figure	NF	f_{RF} = 1.4GHz		1.3		dB
		f_{RF} = 1.7GHz		1.3		
		f_{RF} = 2.0GHz		1.4		
		f_{RF} = 2.3GHz		1.55		
		f_{RF} = 2.5GHz		1.55	1.65	
		f_{RF} = 2.7GHz		1.7		
		f_{RF} = 3.2GHz		2		
Noise Figure Variation over Temperature	NF_{TEMP}	T_{EP} = -40°C to +115°C		±0.5		dB
Output Third-Order Intercept Point[e]	OIP3	f_{RF} = 1.4GHz		33		dBm
		f_{RF} = 1.7GHz		33		
		f_{RF} = 2.0GHz		36		
		f_{RF} = 2.3GHz		38		
		f_{RF} = 2.5GHz, T_{EP} = 25°C		36		
		f_{RF} = 2.5GHz, T_{EP} = -40°C to +115°C	31			
		f_{RF} = 2.7GHz		35		
		f_{RF} = 3.2GHz		33		
Output P1dB	OP1dB	f_{RF} = 1.4GHz		20		dBm
		f_{RF} = 1.7GHz		21		
		f_{RF} = 2.0GHz		21		
		f_{RF} = 2.3GHz		20.5		
		f_{RF} = 2.5GHz	18	20.5		
		f_{RF} = 2.7GHz		20		
		f_{RF} = 3.2GHz		19		
2nd Order Harmonic Distortion[f]	HD2			-43		dBc
3rd Order Harmonic Distortion[f]	HD3			-80		dBc

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ amplitude.

[c] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ phase. Deviation is from ideal 180 degrees.

[d] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+.

[e] OIP3 test conditions: Tone spacing = 5MHz, P_{OUT} = +0dBm/tone.

[f] Harmonic Distortion test conditions: P_{OUT} = +0dBm/tone.

Electrical Characteristics – 3.3V Supply

See the F1129LB application circuit. Specifications apply when operated at V_{CC} = +3.3.0V, f_{RF} = 2.5GHz, T_{EP} = +25°C, STBY = logic LOW, Z_S = 50Ω single-ended, Z_L = 100Ω differential, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 5. Electrical Characteristics with a 3.3V Supply

Note: See important notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		1.17[a]			V
Logic Input Low Threshold	V_{IL}				0.63	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	-10		+100	µA
Supply Current	I_{CC}			31.2		mA
Settling Time	t_{SETTLE}	From 50% STBY control to within ±0.5dB of final gain.		0.5		µs
RF Input Return Loss	RL_{IN}	f_{RF} = 1.4GHz		7		dB
		f_{RF} = 1.7GHz		8		
		f_{RF} = 2.0GHz		10		
		f_{RF} = 2.3GHz		14		
		f_{RF} = 2.5GHz		16		
		f_{RF} = 2.7GHz		16		
		f_{RF} = 3.2GHz		14		
RF Output Return Loss	RL_{OUT}	f_{RF} = 1.4GHz		9		dB
		f_{RF} = 1.7GHz		8		
		f_{RF} = 2.0GHz		10		
		f_{RF} = 2.3GHz		16		
		f_{RF} = 2.5GHz		23		
		f_{RF} = 2.7GHz		16		
		f_{RF} = 3.2GHz		7		
Gain	G	f_{RF} = 1.4GHz		18		dB
		f_{RF} = 1.7GHz		18		
		f_{RF} = 2.0GHz		18		
		f_{RF} = 2.3GHz		19		
		f_{RF} = 2.5GHz		19		
		f_{RF} = 2.7GHz		19		
		f_{RF} = 3.2GHz		18		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Gain Flatness (amplitude)	G_{VAR}	f_{RF} = 1.5GHz, ±100MHz		0.3		dB
		f_{RF} = 1.7GHz, ±100MHz		0.1		
		f_{RF} = 2.0GHz, ±100MHz		0.2		
		f_{RF} = 2.3GHz, ±100MHz		0.3		
		f_{RF} = 2.5GHz, ±100MHz		0.1		
		f_{RF} = 2.7GHz, ±100MHz		0.2		
		f_{RF} = 3.1GHz, ±100MHz		0.5		
Gain Variation over Temperature	G_{TEMP}	T_{EP} = -40°C to +115°C		± 0.1		dB
Reverse Isolation	REV_{ISO}			30		dB
Amplitude Imbalance[b]	$IMBAL_{AMP}$	f_{RF} = 1.4GHz		0.1		dB
		f_{RF} = 1.7GHz		0.3		
		f_{RF} = 2.0GHz		0.45		
		f_{RF} = 2.3GHz		0.6		
		f_{RF} = 2.5GHz		0.6		
		f_{RF} = 2.7GHz		0.6		
		f_{RF} = 3.2GHz		0.5		
Phase Imbalance[c]	$IMBAL_{PH}$	f_{RF} = 1.4GHz		3.5		deg
		f_{RF} = 1.7GHz		3.4		
		f_{RF} = 2.0GHz		3.4		
		f_{RF} = 2.3GHz		3.4		
		f_{RF} = 2.5GHz		3.1		
		f_{RF} = 2.7GHz		2.7		
		f_{RF} = 3.2GHz		1.1		
Common Mode Rejection[d]	CMR	f_{RF} = 1.4GHz		30.5		dB
		f_{RF} = 1.7GHz		30		
		f_{RF} = 2.0GHz		28		
		f_{RF} = 2.3GHz		27		
		f_{RF} = 2.5GHz		27		
		f_{RF} = 2.7GHz		27.5		
		f_{RF} = 3.2GHz		28.5		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Noise Figure[e]	NF	f_{RF} = 1.4GHz		1.3		dB
		f_{RF} = 1.7GHz		1.2		
		f_{RF} = 2.0GHz		1.2		
		f_{RF} = 2.3GHz		1.3		
		f_{RF} = 2.5GHz		1.4		
		f_{RF} = 2.7GHz		1.5		
		f_{RF} = 3.2GHz		1.8		
Noise Figure Variation over Temperature[e]	NF_{TEMP}	T_{EP} = -40°C to +115°C		±0.5		dB
Output Third-Order Intercept Point[f]	OIP3	f_{RF} = 1.4GHz		23		dBm
		f_{RF} = 1.7GHz		24		
		f_{RF} = 2.0GHz		26		
		f_{RF} = 2.3GHz		28		
		f_{RF} = 2.5GHz		28		
		f_{RF} = 2.7GHz		27		
		f_{RF} = 3.2GHz		25		
Output P1dB[g]	OP1dB	f_{RF} = 1.4GHz		16.5		dBm
		f_{RF} = 1.7GHz		17.5		
		f_{RF} = 2.0GHz		17		
		f_{RF} = 2.3GHz		17		
		f_{RF} = 2.5GHz		16		
		f_{RF} = 2.7GHz		15.5		
		f_{RF} = 3.2GHz		15.5		

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ amplitude.

[c] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+ phase. Deviation is from ideal 180 degrees.

[d] Measures RF_IN to RF_OUT- and compares RF_IN to RF_OUT+.

[e] Measured using an external 2:1 transformer at the RF output.

[f] OIP3 test conditions: Tone spacing = 5MHz, POUT = +0dBm/tone.

[g] Harmonic Distortion test conditions: P_{OUT} = +0dBm/tone.

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction-to-Ambient Thermal Resistance.	θ_{JA}	112.57	°C/W
Junction-to-Case Thermal Resistance. (Case is defined as the exposed paddle.)	$\theta_{JC\text{-}BOT}$	27.6	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Evaluation kit connector and trace losses are de-embedded
- V_{CC} = 3.3V, 5.0V
- STBY = not connected (internally pulled to logic LOW)
- T_{EP} = 25°C
- Small signal parameters measured with P_{OUT} = 0dBm
- Two tone tests P_{OUT} = 0dBm/tone with 5MHz tone spacing
- All unused ports properly terminated.
- S-parameters (S11, S21, S12, and S22) measured using a de-embedded Differential Board (EVKit) with Z_S = single-ended 50Ω and Z_L = differential 100Ω. The inputs are mathematically combined using an ideal 1:2 (50Ω:100Ω) transformer to produce the 2-port S-parameters.
- OIP3, Output P1dB and Noise Figure measured using a Transformer Board EVKit with ZS = ZL = single-ended 50Ω.
- Amplitude and phase imbalances measures RF_IN to RF_OUT+ and compares to RF_IN to RF_OUT-.
- The phase imbalance is the deviation from an ideal 180 degrees.

Note: The use of the external transformer T1 is included for simple 2-port evaluation purposes. At some frequencies, the external transformer interacts with the on-chip balun affecting the gain and noise figure flatness responses. These interactions have been removed from the noise figure TOCs.

Typical Performance Characteristics – 5V

Figure 3. Gain

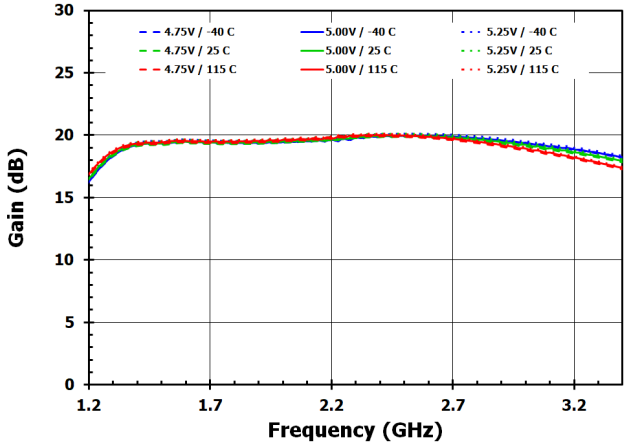


Figure 4. Reverse Isolation

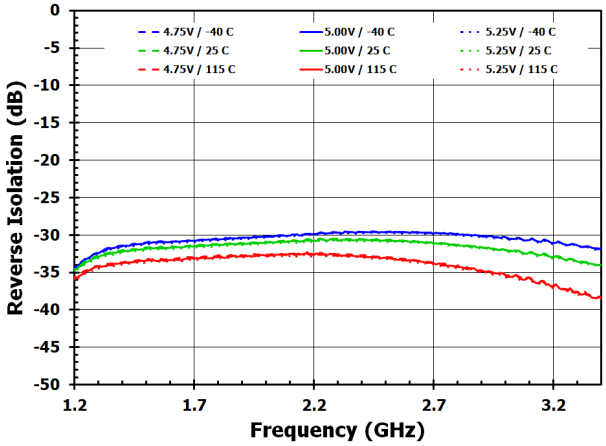


Figure 5. Input Return Loss

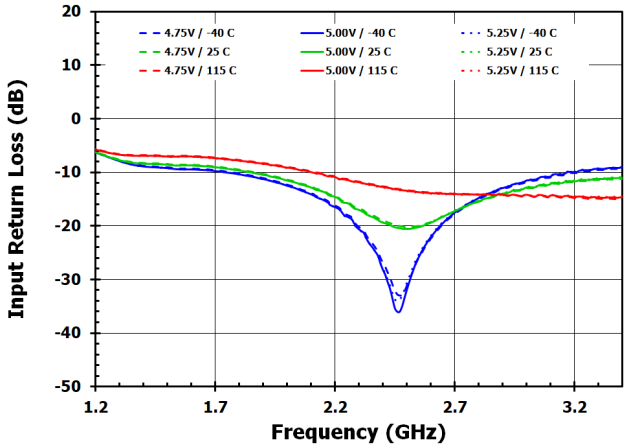


Figure 6. Output Return Loss

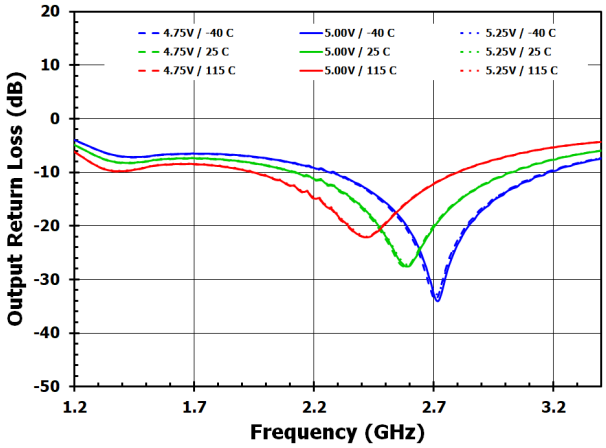


Figure 7. Output IP3

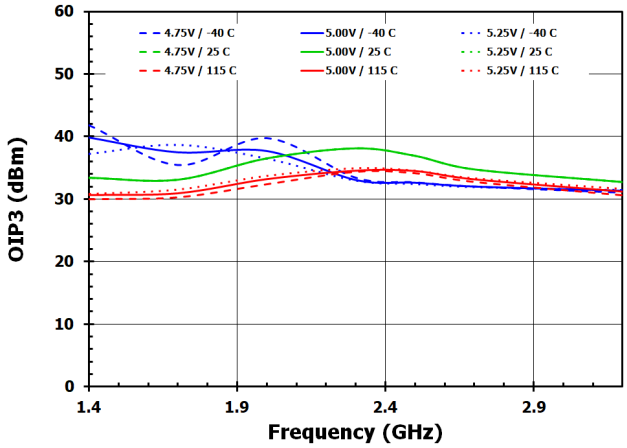


Figure 8. Output P1dB

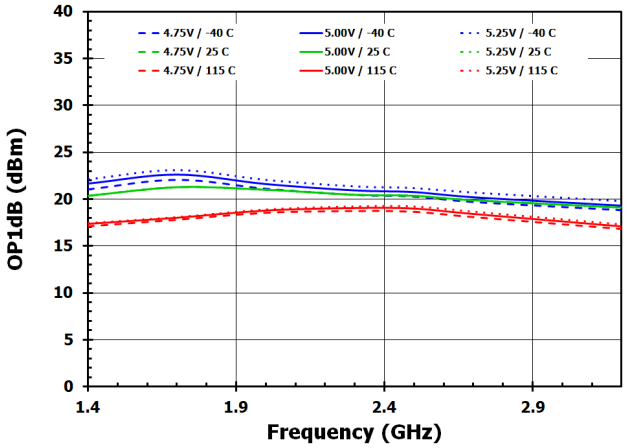


Figure 9. Noise Figure

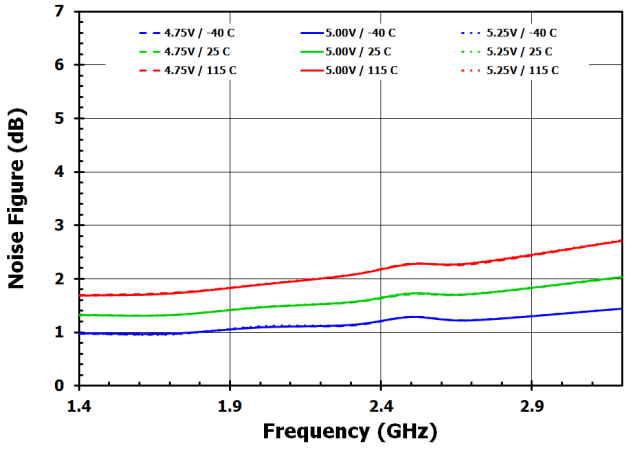


Figure 10. Gain Imbalance

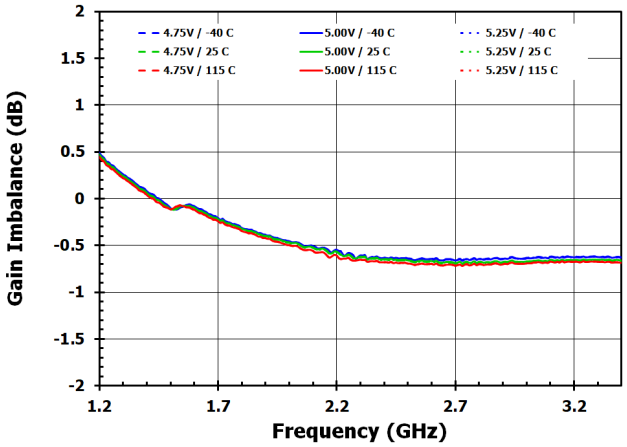


Figure 11. Phase Imbalance

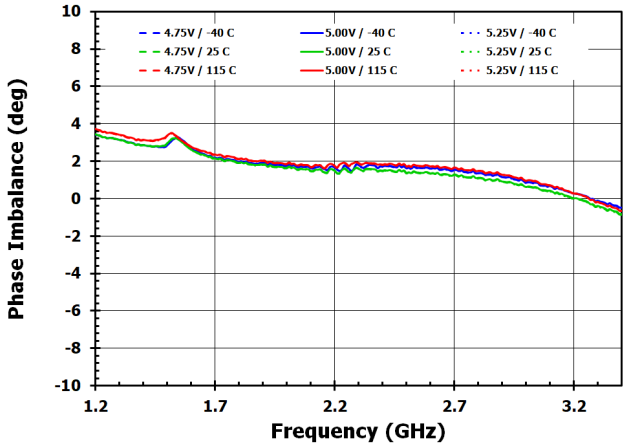
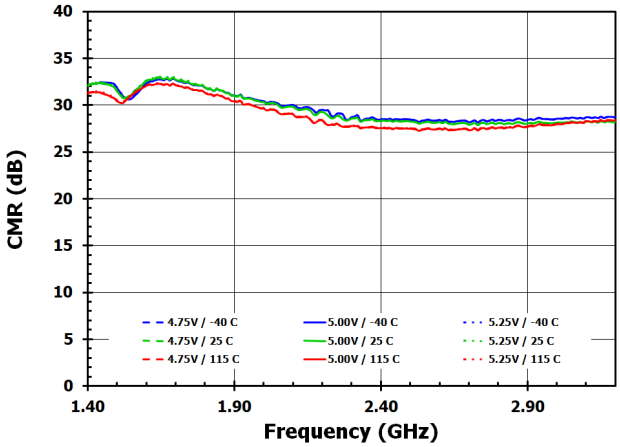


Figure 12. CMR



Typical Performance Characteristics – 3.3V

Figure 13. Gain

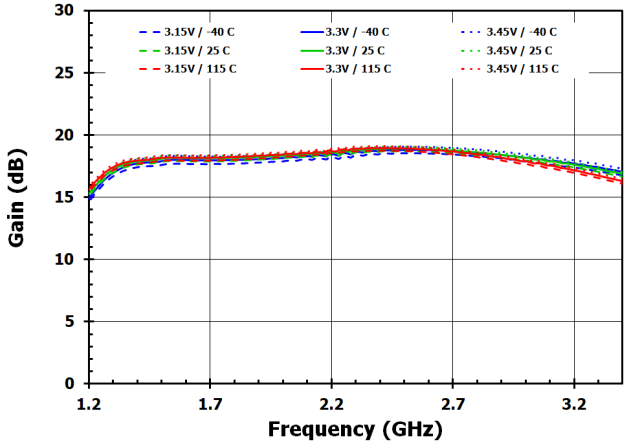


Figure 14. Reverse Isolation

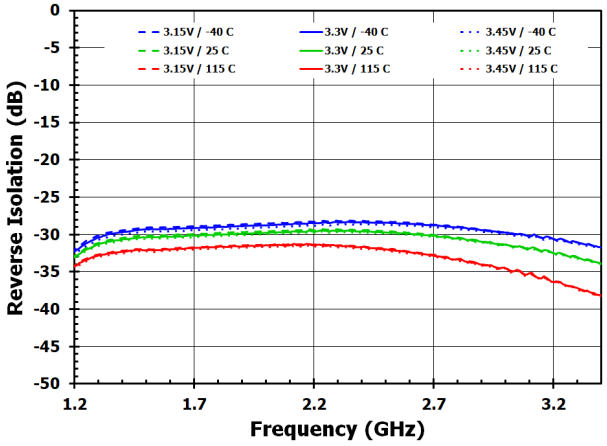


Figure 15. Input Return Loss

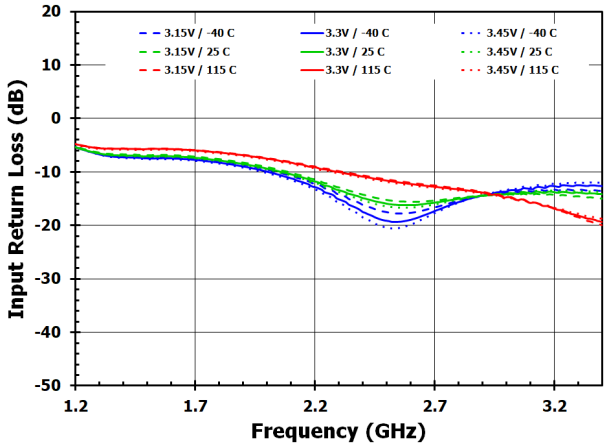


Figure 16. Output Return Loss

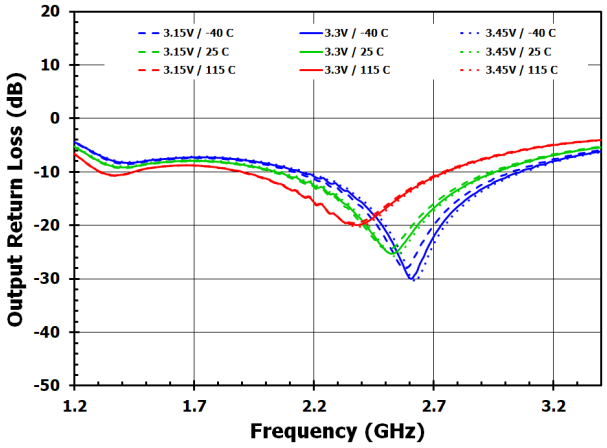


Figure 17. Output IP3

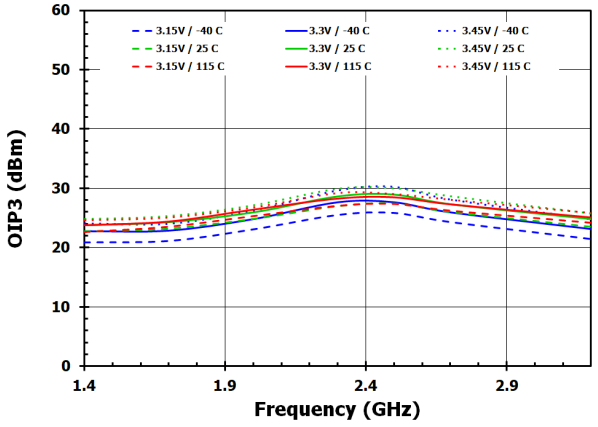


Figure 18. Output P1dB

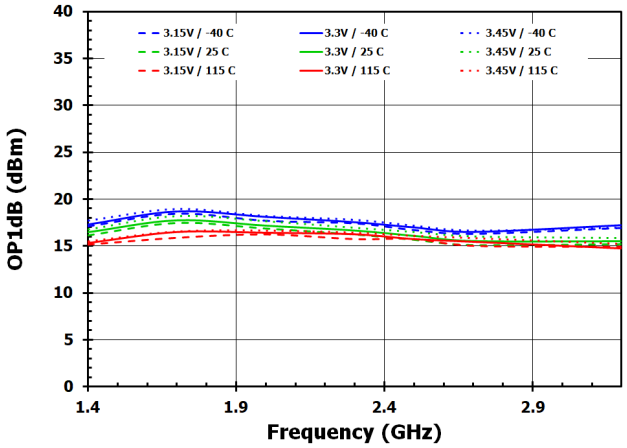


Figure 19. Noise Figure

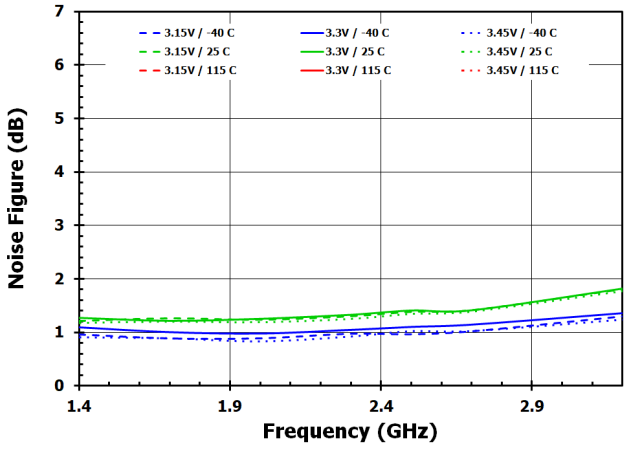


Figure 20. Gain Imbalance

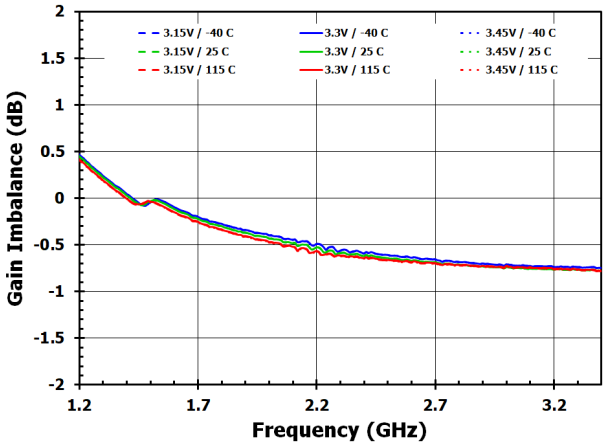


Figure 21. Phase Imbalance

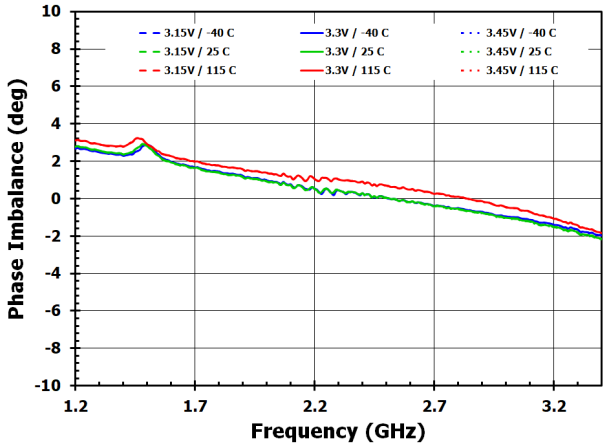
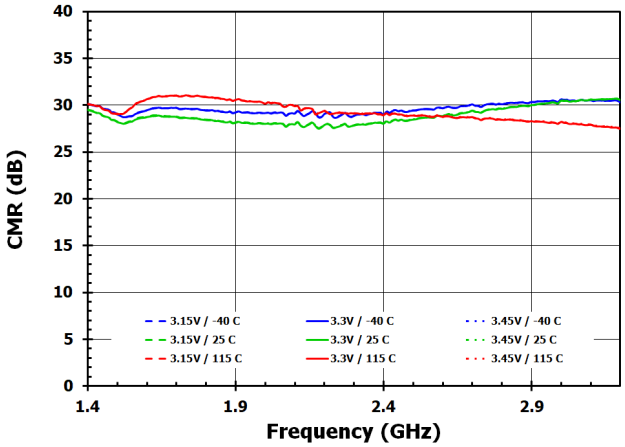


Figure 22. CMR



Evaluation Kit Picture

Figure 23. Evaluation Kit – Top View

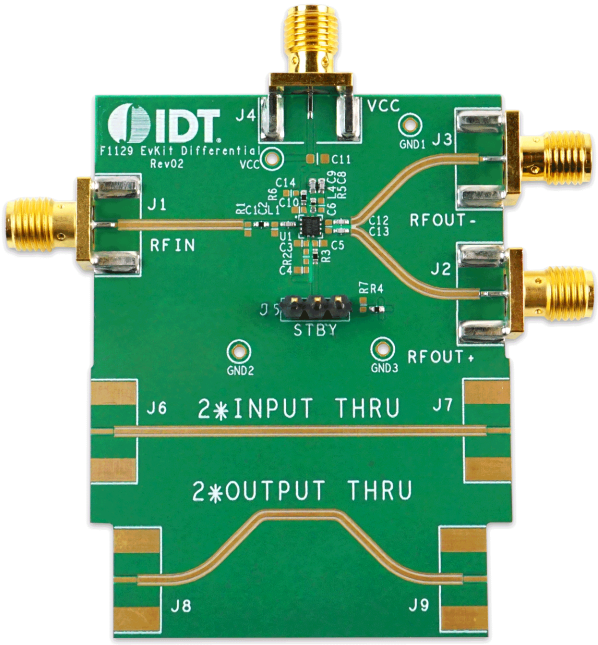
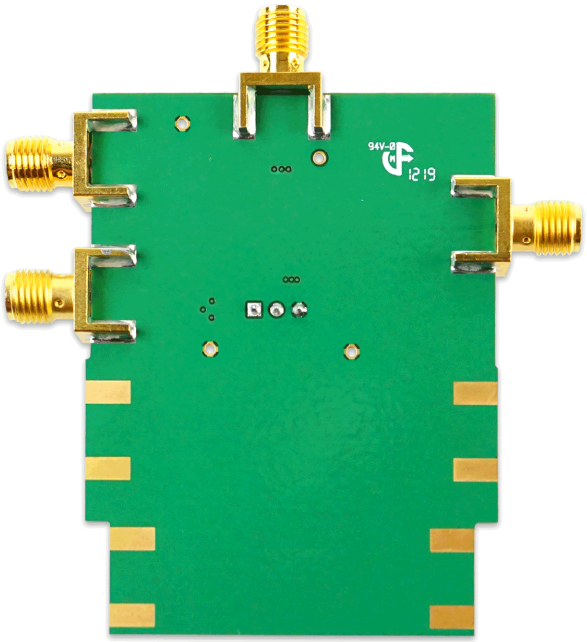


Figure 24. Evaluation Kit – Bottom View



Evaluation Kit Circuit

Figure 25. Evaluation Kit Electrical Schematic

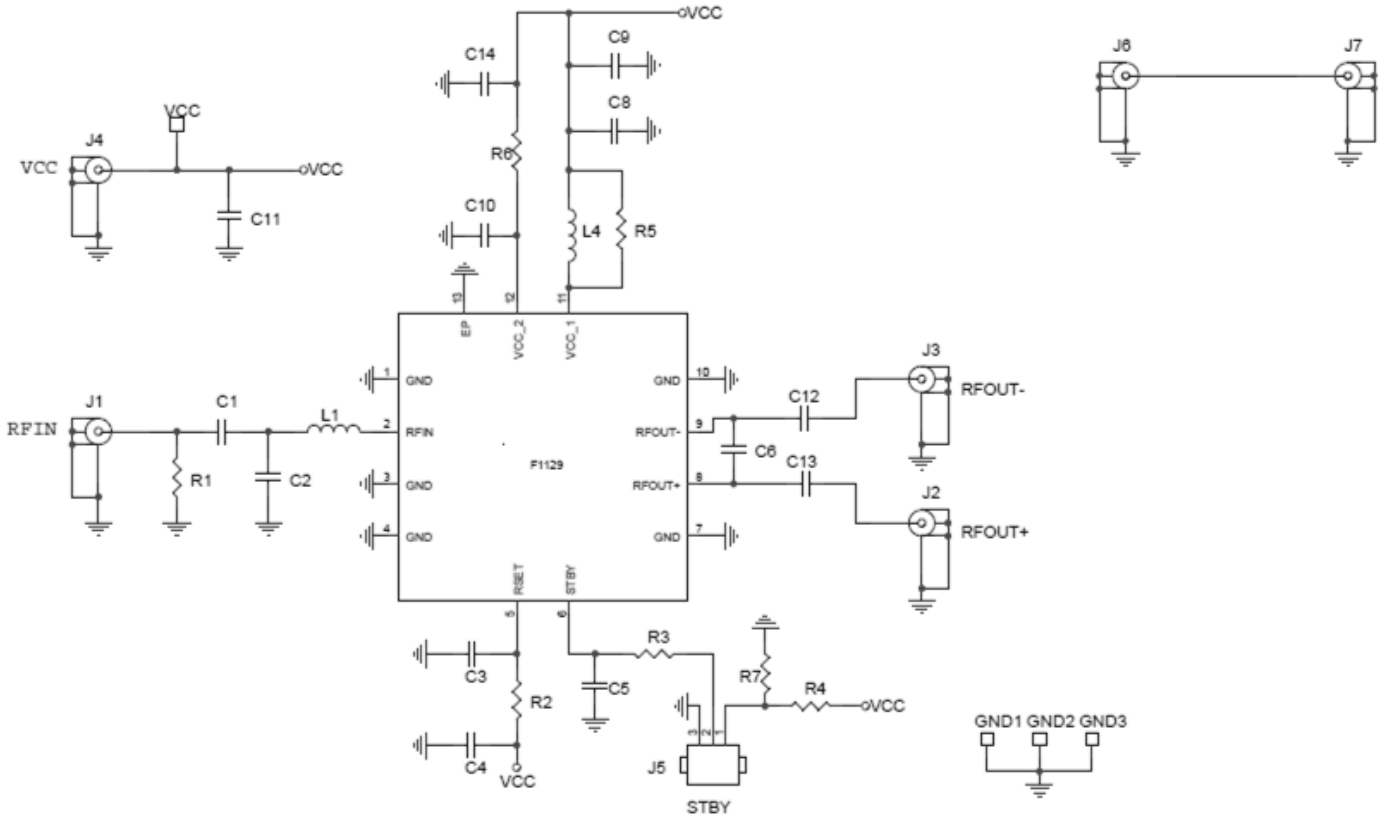


Table 7. Evaluation Kit Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1,R6,R3,R4	4	0 ohm Jumper 1/10W (0402)	ERJ2GE0R00X	Panasonic
C9	1	1000pF C0G 50v (0402)	GRM1555C1H102J	Murata
C8	1	100pF C0G 50v (0402)	GRM1555C1H101J	Murata
L1	1	10pF C0G 50v (0402)	GRM1555C1H100J	Murata
L4	1	1.5nH ±0.3 (0402)	LQG15HS1N5S02	Murata
C12,C13	2	5pF NP0 50V (0402)	GRM1555C1H50BA01D	Murata
J5	1	CONN HEADER VERT 1x3 POS 2.54MM	61300311121	Würth Elektronik
J1,J2, J3, J4, J6, J7, J8, J9	8	SMA Edge Mount	142-0701-851	Cinch Connectivity
C10,C11,C14,C2,,C3,C4,C5,C6,R1,R2,R5,R7	0	Do not Install		
U1	1	F1129LB 50Ω SE-In – 100Ω DIFF-Out Amplifier	F1129LBNELI	Renesas
	1	Printed Circuit Board	F1129 EVKIT DIFF. Rev.02	

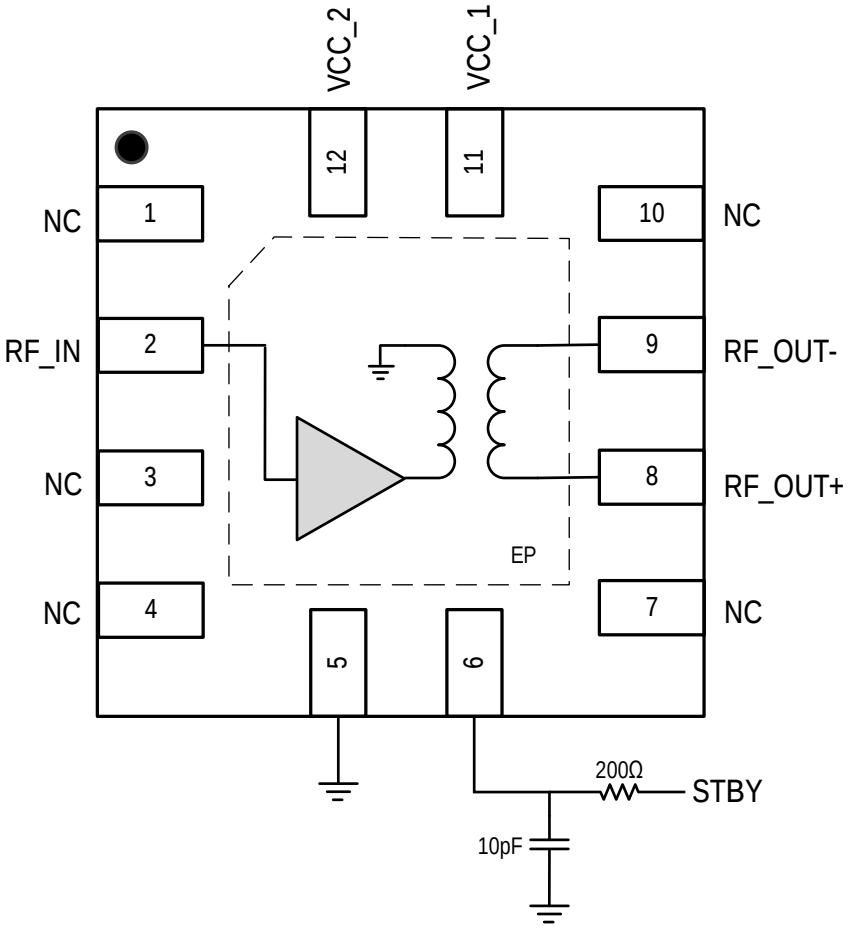
Application Information

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of the STBY control pin is recommended. This applies to the STBY pin as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV Kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

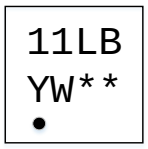
Figure 26. Control Pin Interface Schematic



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



Line 1: 11LB = abbreviated part number (F1129LB).
Line 2: Y = Year code, last digit of production year ("8" would correspond to 2018).
W = Work week code ("W" corresponds to week 30).
** = Sequential alpha characters for lot traceability.

Ordering Information

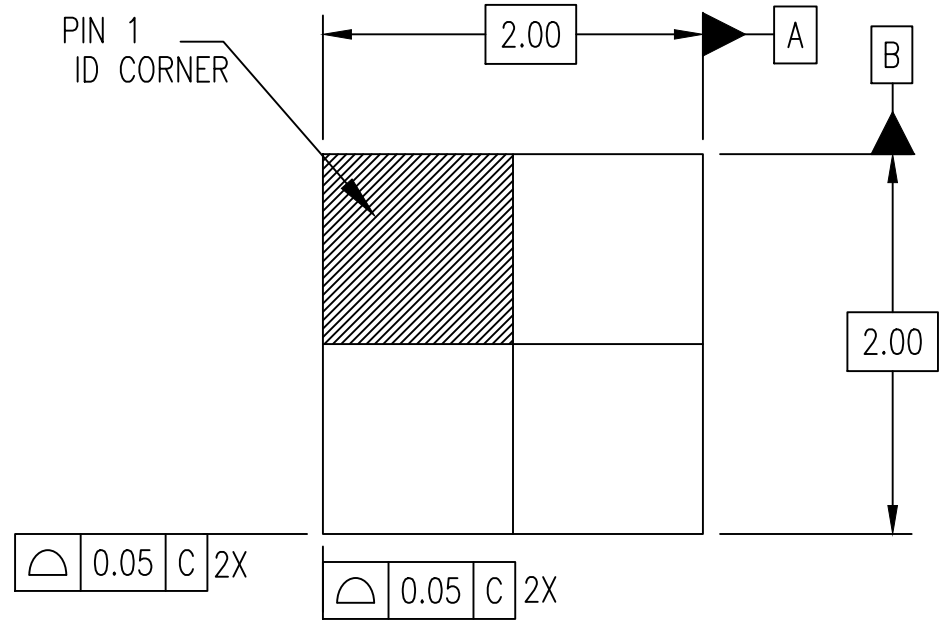
Orderable Part Number	Package	MSL Rating	Carrier Type	Temperature
F1129LBNELI	2 × 2 × 0.75 mm 12-DFN	1	Cut Reel	-40° to +115°C
F1129LBNELI8	2 × 2 × 0.75 mm 12-DFN	1	Reel	-40° to +115°C
F1129LBEVB	Evaluation Board			

Revision History

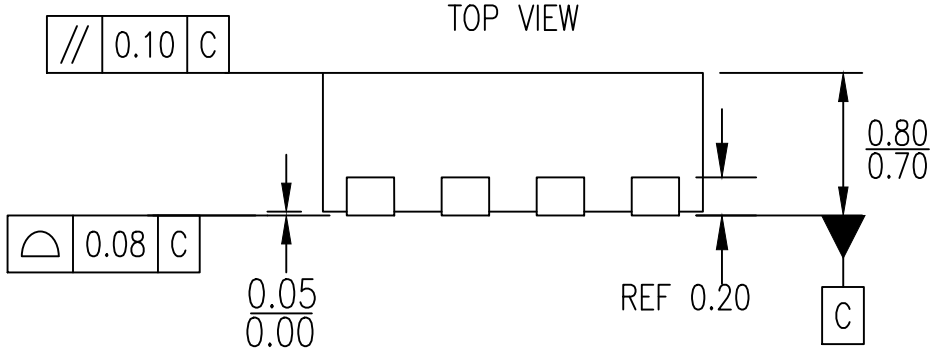
Revision Date	Description of Change
January 31, 2021	▪ Updated the Package Outline Drawings website link ▪ Updated the Carrier Type information in Ordering Information
May 21, 2020	Updated base part number table in Description.
April 29, 2020	Added Application Information section.
January 17, 2020	Updated Evaluation Kit pictures.
November 24, 2019	Updated the electrostatic discharge ratings in Table 2.
November 10, 2019	Initial release.

VFQFPN-12, Package Outline Drawing

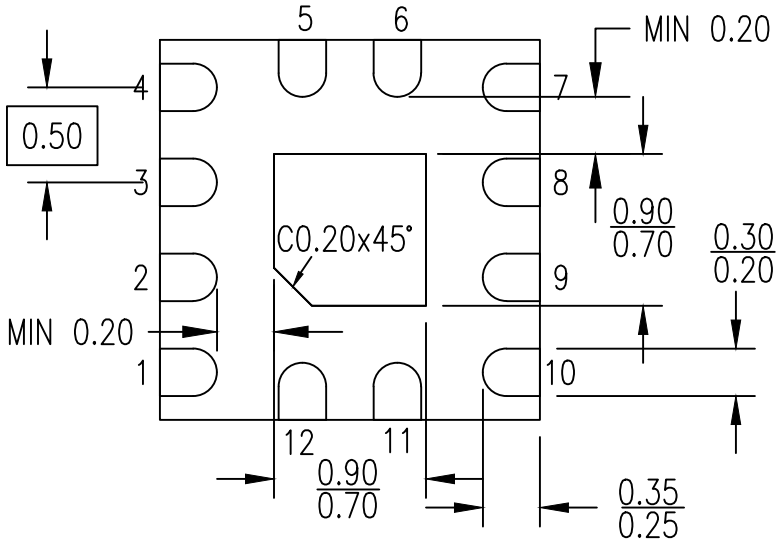
2.0 x 2.0 x 0.75 mm Body, 0.5mm Pitch Epad 0.80 x 0.80 mm



TOP VIEW



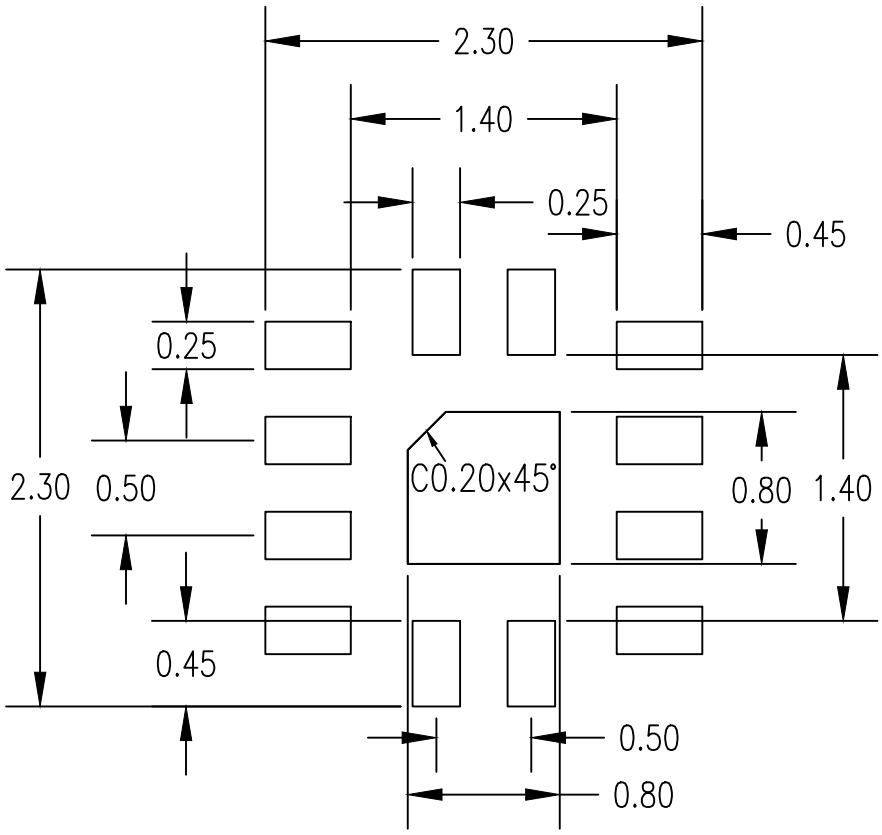
SIDE VIEW (ROTATE 90 DEG.)



BOTTOM VIEW

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASMEY14.5–2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 5, 2018	Rev 01	Add "K" Value Minimium 0.20 mm, Correct L/F Thickness
July 31, 2017	Rev 00	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.