February 2015

FPF2487
Dual Channel Over-Voltage Protection Load Switch

Features

- Dual Channel Power Switch (V_{BUS} and V_{IF})
- Surge Protection under IEC 61000-4-5
  - V_{BUS}: ±100 V
  - V_{IF}: ± 40 V
- Input Voltage Range
  - V_{BUS}: 2.5 V ~ 23 V
  - V_{IF}: 3.1 V ~ 5.5 V
- Max. Continuous Current Capability
  - V_{BUS}: 2.5 A
  - V_{IF}: 6 A
- Ultra Low On-Resistance
  - V_{BUS}: Typ. 33 mΩ
  - V_{IF}: Typ. 11 mΩ
- Over-Voltage Protection
  - V_{BUS}: 5.95 V ± 50 mV
  - V_{IF}: 5.25 V ± 250 mV
- LDO Output based V_{BUS_DET} for V_{BUS} Detection
- Active Low Control for V_{BUS} Path
- OTG Functionality on V_{BUS} Path
- Conditional Active High Control for V_{IF} Path
- Reverse-Current Blocking for V_{IF} Path

Applications

- Mobile Handsets and Tablets
- Wearable Devices

Description

The FPF2487 features a 2-channel power switch, which offers surge protection and Over-Voltage Protection (OVP), to protect downstream components and enhancing overall system robustness.

Channel one (V_{BUS}) is an active-low, 28 V/2.5 A rated, power MOSFET switch with an internal clamp supporting ±100 V surge protection, highly accurate fixed OVP at 5.95 V (±50 mV), and OTG functionality. Channel two (V_{IF}) is a conditional active-high, 6 V/6 A rated, power MOSFET switch with an integrated TVS supporting ±40 V surge protection and fixed OVP at 5.25 V (±250 mV). V_{IF} also provides Reverse Current Blocking (RCB) during its OFF state to minimize leakage current.

V_{BUS_DET} is paired with always ON LDO to power downstream devices even with V_{BUS} is greater than 2.5 V, even when disabled through the ONB pin. This provides power sequence control or a host controlled configuration in system.

The FPF2487 is available in a 15-bump, 1.6 mm x 2.2 mm Wafer-Level Chip-Scale Package (WLCSP) with 0.4 mm pitch.

Related Resources

- http://www.fairchildsemi.com/

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FPF2487UCX	-40°C – +85°C	GX	15-Ball, 0.4 mm Pitch WLCSP	Tape & Reel

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Application Diagram

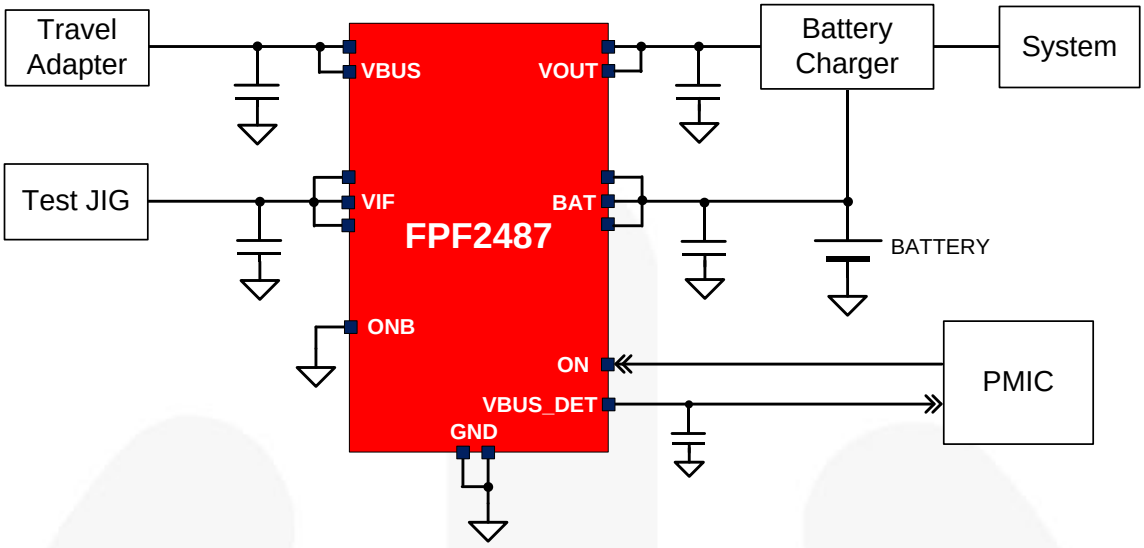

Figure 1. Typical Application

Block Diagram

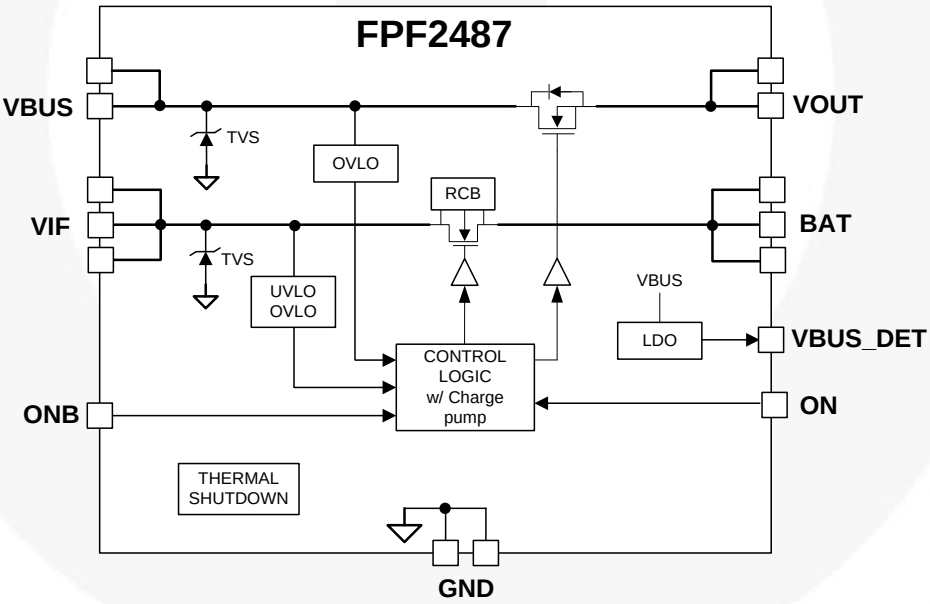

Figure 2. Functional Block Diagram

Pin Configuration

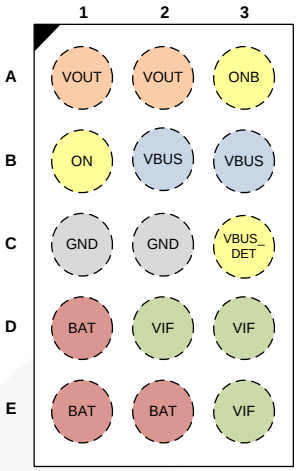

Figure 3. Pin Configuration (Top View)

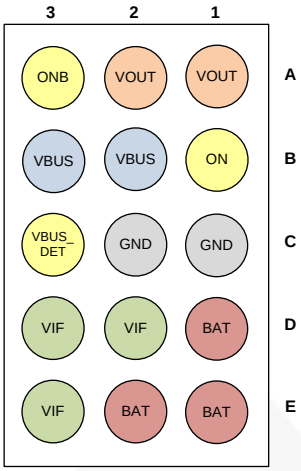

Figure 4. Pin Configuration (Bottom View)

Pin Definitions

Name	Bump	Type	Description
V_{BUS}	B2, B3	Input/Supply	Switch Input and Device Supply
V_{OUT}	A1, A2	Output	Switch Output to Load
V_{IF}	D2, D3, E3	Input/Supply	Switch Input and Device Supply
BAT	D1, E1, E2	Output	Switch Output to Battery
V_{BUS_DET}	C3	Output	Regulated Output according to V_{BUS}
ON	B1	Input	Active HIGH: V_{IF} path only and when BAT is valid prior to V_{IF}
ONB	A3	Input	Active LOW: V_{BUS} path only
GND	C1, C2	GND	Ground

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BUS}	V_{BUS} to GND & V_{BUS} to V_{OUT}=GND or Float			-0.3	29.0	V
V_{IF}	V_{IF} to GND			-2[1]	6	V
V_{OUT}	V_{OUT} to GND			-0.3	V_{IN} + 0.3	V
BAT	BAT to GND			-0.3	V_{IF} + 0.3	V
V_{BUS_DET}	V_{BUS_DET} to GND				8	V
$V_{ON(B)}$	ONB or ON to GND				6	V
I_{IN_VBUS}	Continuous V_{BUS} Current				2.5	A
	Peak V_{BUS} Current (5 ms)				5	A
I_{IN_VIF}	Continuous V_{IF} Current				6	A
	Peak V_{IF} Current (5 ms)				12	A
$I_{IN_VBUS_DET}$	Continuous V_{BUS_DET} Current				1	mA
t_{PD}	Total Power Dissipation at T_A=25°C				1.54	W
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient[2] (1-in.^{2} Pad of 2-oz. Copper)				81[2]	°C/W
ESD	Electrostatic Discharge Capability	IEC 61000-4-2 System Level ESD	Air Discharge	15		kV
			Contact Discharge	8		
		Human Body Model, ANSI/ESDA/JEDEC JS-001-2012	All Pins	2		
		Charged Device Model, JESD22-C101	All Pins	1		
Surge		IEC 61000-4-5, Surge Protection	V_{BUS}	±100		V
			V_{IF}	±40		

Notes:

1. Pulsed, 50 ms maximum non-repetitive.
2. Measured using 2S2P JEDEC std. PCB.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	Supply Voltage, V_{BUS}	2.5	23.0	V
V_{IF}	Supply Voltage, V_{IF}	3.1	5.5	V
C_{IN} / C_{OUT}	Input and Output Capacitance	0.1		µF
C_{VBUS_DET}	Output Capacitance	0.47		µF
T_A	Operating Temperature	-40	+85	°C

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Electrical Characteristics

Unless otherwise noted, V_{BUS}=2.5 to 23 V, V_{IF}=3.1 to 5.5 V, T_A=-40 to 85°C; Typical values are at V_{BUS}=5 V, I_{IN} ≤ 2 A, V_{IF}=4 V, C_{IN}=0.1 µF and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Basic Operation						
I_Q	Input Quiescent Current	V_{BUS}=5 V, ONB=0 V, V_{BUS_DET}=Floating		160	250	µA
		V_{IF}=4 V		100	150	µA
I_{IN_Q}	OVLO Supply Current	V_{BUS}=12 V, V_{OUT}=0 V, V_{BUS_DET}=Floating		150	205	µA
		V_{IF}=5.5 V, BAT=0 V		100	180	µA
T_{SDN}	Thermal Shutdown(3)			140		°C
T_{SDN_HYS}	Thermal Shutdown Hysteresis(3)			20		°C
V_{BUS} to V_{OUT} Switch						
V_{BUS_CLAMP}	Input Clamping Voltage	I_{IN}=10 mA		35		V
V_{BUS_OVLO}	Over-Voltage Trip Level	V_{BUS} Rising, T_A=-40 to 85°C	5.90	5.95	6.00	V
		V_{BUS} Falling, T_A=-40 to 85°C	5.8			V
R_{ON_VBUS}	On-Resistance	V_{BUS}=5 V, I_{OUT}=1 A, T_A=25°C		33	39	mΩ
		V_{BUS}=9 V, I_{OUT}=1 A, T_A=25°C		33	39	mΩ
t_{DEB_VBUS}	Debounce Time	Time from V_{BUS_MIN} < V_{BUS} < V_{BUS_OVLO} to V_{OUT}=0.1 × V_{BUS}		15		ms
t_{START_VBUS}	Soft-Start Time	Time from V_{BUS}=V_{BUS_MIN} to 0.1 × V_{BUS_DET}		30		ms
t_{ON_VBUS}	Switch Turn-On Time	R_L=100 Ω, C_L=22 µF, V_{OUT} from 0.1 × V_{BUS} to 0.9 × V_{BUS}		3		ms
t_{OFF_VBUS}	Switch Turn-Off Time	R_L=100 Ω, No C_L, V_{BUS} > V_{BUS_OVLO} to V_{OUT}=0.8 × V_{BUS}			150	ns
V_{IF} to BAT Switch						
V_{IF_CLAMP}	Input Clamping Voltage	I_{IN}=10 mA		6.4		V
V_{IF_UVLO}	Under-Voltage Trip Level	V_{IF} Rising, T_A=-40 to 85°C		2.85	3.05	V
		V_{IF} Falling, T_A=-40 to 85°C		2.7		V
V_{IF_OVLO}	Over-Voltage Trip Level	V_{IF} Rising, T_A=-40 to 85°C	5.00	5.25	5.50	V
		V_{IF} Falling, T_A=-40 to 85°C	4.8			V
R_{ON_VIF}	On-Resistance	V_{IF}=3.1 V, I_{OUT}=1 A, T_A=25°C		10	15	mΩ
I_{RCB}	Reverse Current	V_{IF}=0 V, BAT=4.4 V		3	7	µA
t_{DEB_VIF}	Debounce Time	Time from V_{IF_UVLO} < V_{IF} < V_{IF_OVLO} to BAT=0.1 × V_{IF}		15		ms
t_{QUAL_VIF}	Qualification Tim	BAT > VIH_BAT First, Time from ON > VIH_ON(B) to BAT Voltage Increase		2		ms
t_{ON_VIF}	Switch Turn-On Time	R_L=100 Ω, C_L=22 µF, V_{OUT} from 0.1 × V_{IF} to 0.9 × V_{IF}		2		ms
t_{OFF_VIF}	Switch Turn-Off Time	R_L=100 Ω, No C_L,V_{IN} > V_{OVLO} to V_{OUT}=0.8 × V_{IF}			150	ns

Note:

3. Guaranteed by characterization and design.

Continued on the following page…

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Electrical Characteristics (Continued)

Unless otherwise noted, V_{BUS}=2.5 to 23 V, V_{IF}=3.1 to 5.5 V, T_A=-40 to 85°C; Typical values are at V_{BUS}=5 V, I_{IN} ≤ 2 A, V_{IF}=4 V, C_{IN}=0.1 µF and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BUS_DET}						
V_{BUS_DET}	V_{BUS_DET} Output Voltage	V_{BUS}=6.5 V, I_{BUS_DET}=0 mA, T_A=25°C	6.0		6.5	V
		V_{BUS}=15 V, I_{BUS_DET}=0 mA, T_A=25°C	6.0	7.0	7.9	V
		V_{BUS}=6.5 V, I_{BUS_DET}=1 mA, T_A=25°C	6.0	6.3	6.5	V
		V_{BUS}=15 V, I_{BUS_DET}=1 mA, T_A=25°C	6.0	7.0	7.9	V
Digital Signals						
$V_{IH_ON(B)}$	Enable HIGH Voltage	V_{BUS}, V_{IF} Operating Range	1.2			V
$V_{IL_ON(B)}$	Enable LOW Voltage	V_{BUS}, V_{IF} Operating Range			0.5	V
V_{IH_BAT}	BAT Presence HIGH Voltage	BAT Rising	2.5			V
V_{IL_BAT}	BAT Presence LOW Voltage	BAT Falling			1.7	V
$I_{VBUS_DET_LEAK}$	V_{BUS_DET} Leakage Current	V_{VBUS_DET}=5 V, V_{BUS}=0 V			1	µA
ON(B)_Leak	ON(B) Leakage Current	V_{BUS}=5 V, V_{OUT}=Float			1	µA

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Timing Diagrams

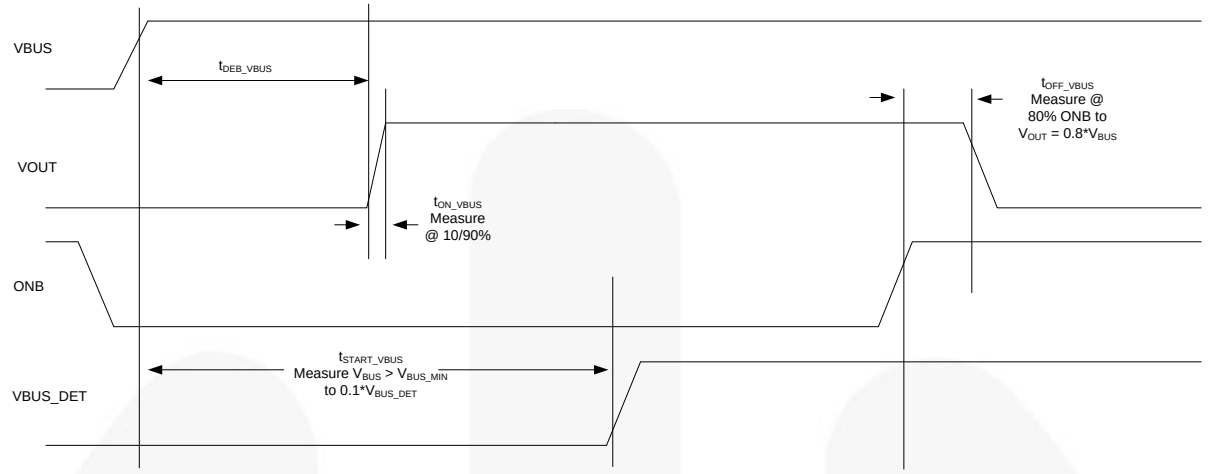

Figure 5. Timing for V_{BUS} Power Up/Down and Normal Operation

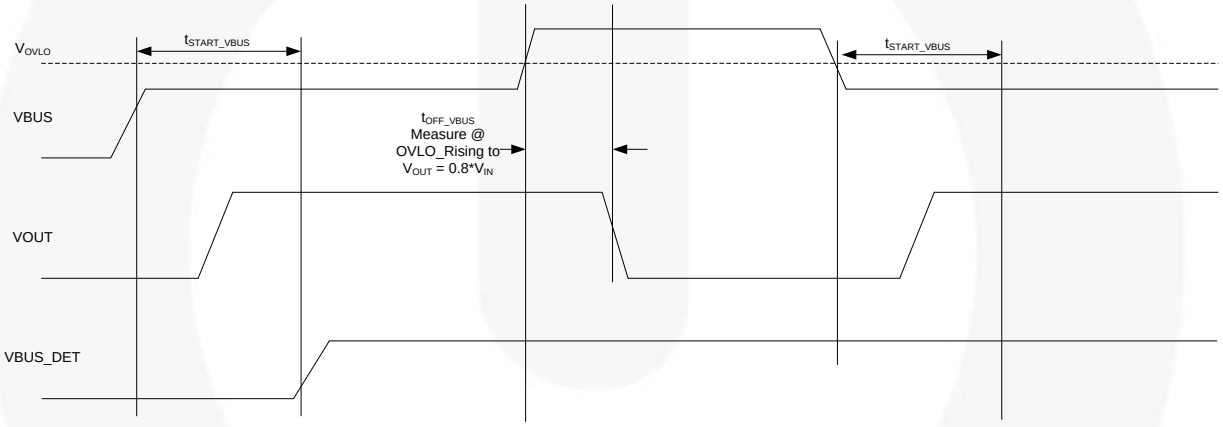

Figure 6. Timing for V_{BUS} OVLO Operation (ONB=LOW)

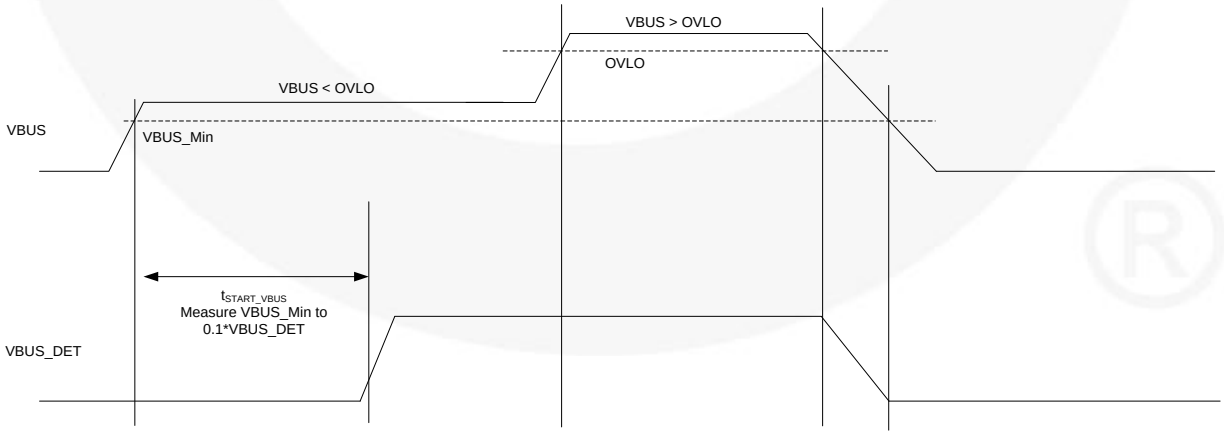

Figure 7. Always ON V_{BUS_DET} Operation (ONB=HIGH)

Timing Diagrams (Continued)

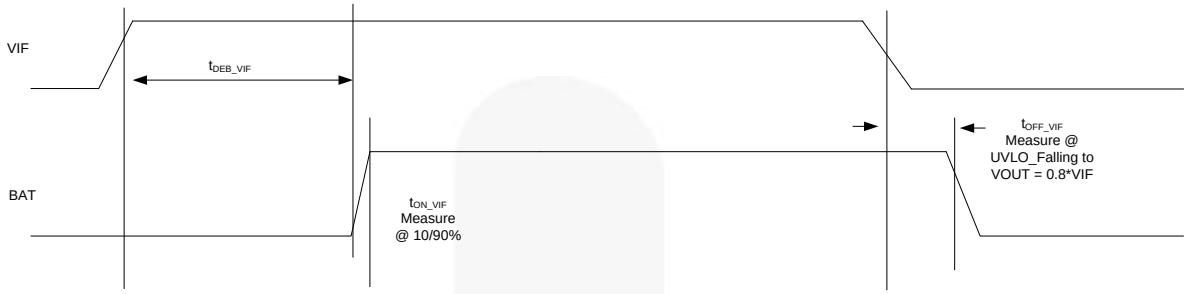

Figure 8. Timing for V_{IF} Power Up/Down and Normal Operation (ON=Don't Care)

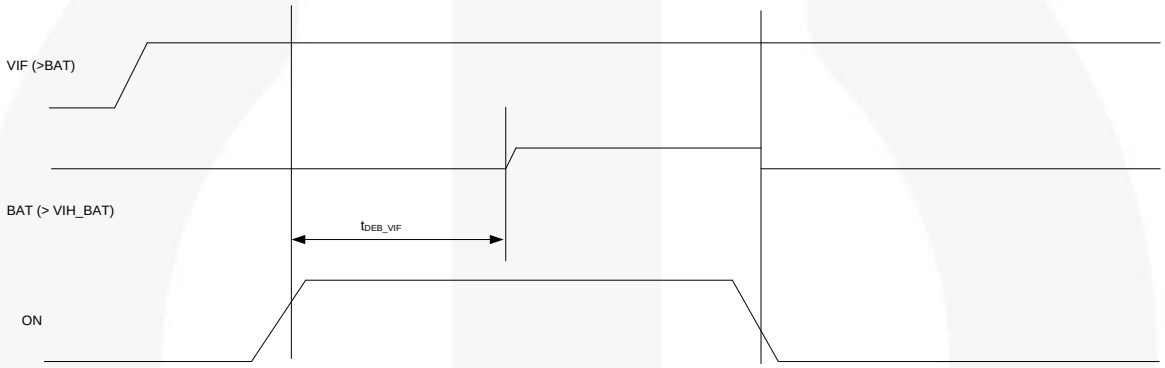

Figure 9. Timing for V_{IF} Power Up/Down and Normal Operation with ON Pin

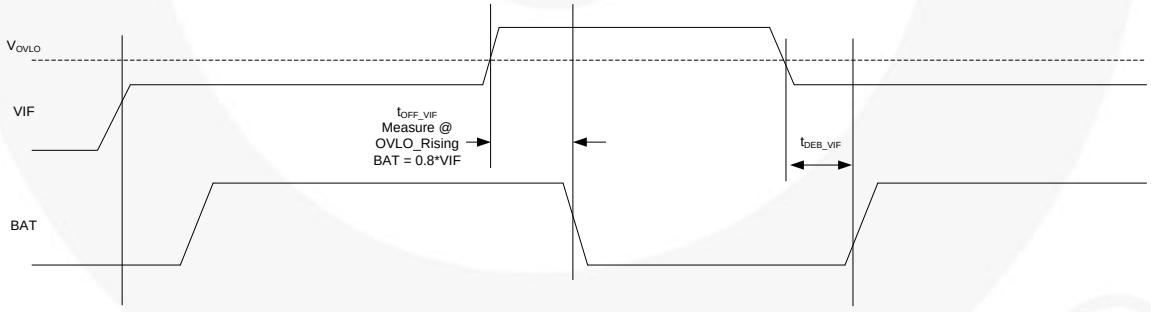

Figure 10. Timing for V_{IF} OVLO Operation (ON=Don't Care)

V_{IF} Turn-On Qualification State Diagram

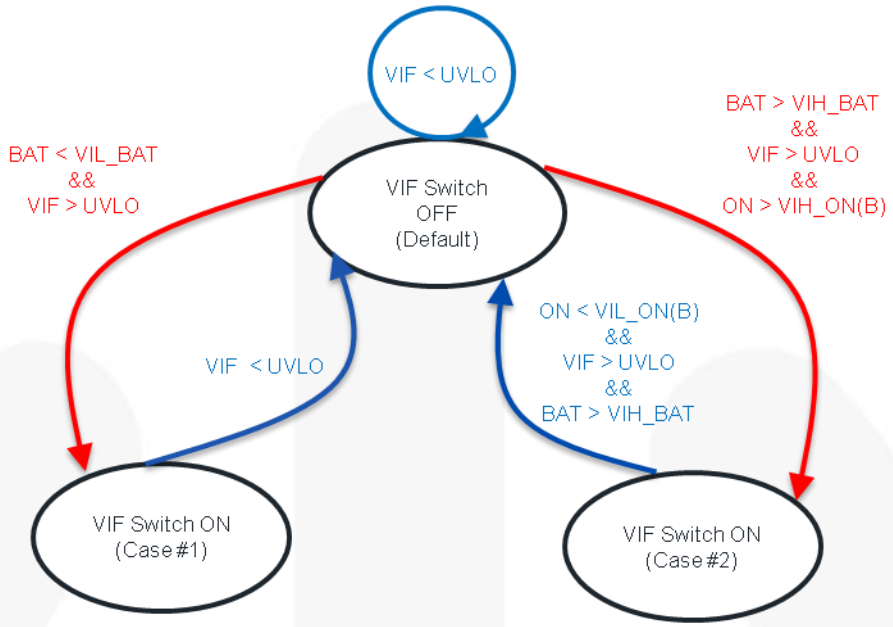

Figure 11. V_{IF} Turn-On Qualification State Diagram

Notes:

4. Case #1 is reflecting removable battery system without ON signal.
5. Case #2 is reflecting embedded battery system with ON signal.

Product-Specific Package Dimensions

D	E	X	Y
2200 µm ±30 µm	1600 µm ±30 µm	400 µm ±18 µm	300 µm ±18 µm

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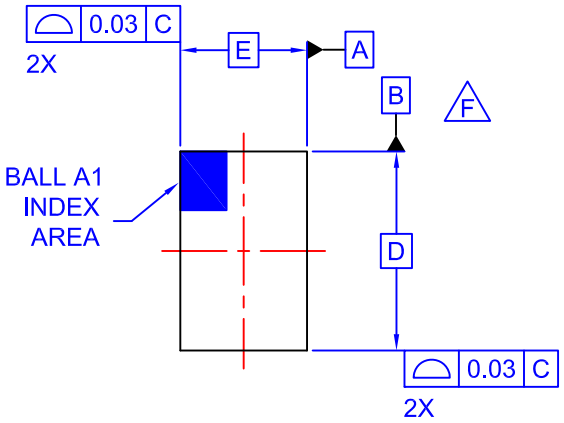
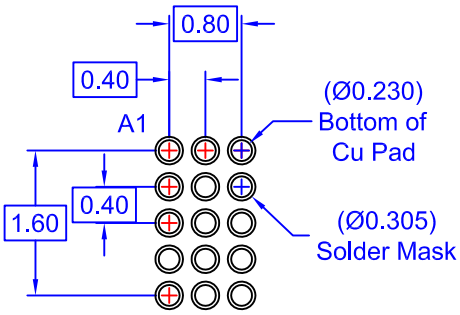
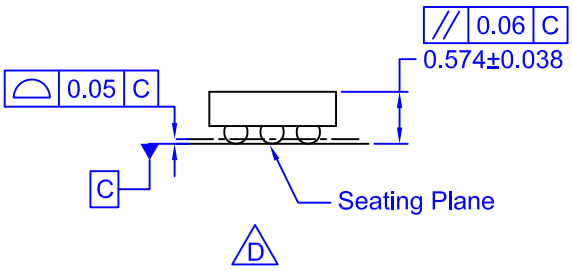
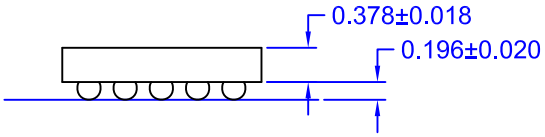


TOP VIEW

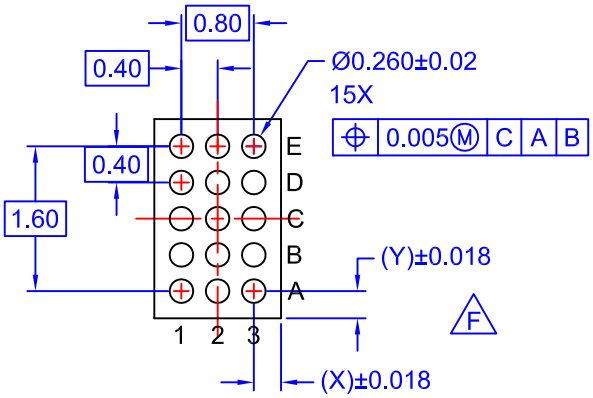


RECOMMENDED LAND PATTERN
(NSMD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 574 ± 38 MICRONS (536-612 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC015AC REV2.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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