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LC898123F40XC

Optical Image Stabilization (OIS) / Auto Focus (AF) Controller & Driver with 40 kB Flash Memory

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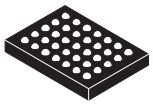


WLCSP35, 3.22x2.3

1. Overview

LC898123F40XC is a system solution integrating an ultra-low-power 32-bit DSP, Flash Memory, and analog peripherals for OIS (Optical Image Stabilization) /AF (Auto Focus) control, H-bridge, and linear drivers.

Available in a tiny 3.22 mm × 2.30 mm chipscale package, this device's 40 kB Flash memory enables high level commands and user data for greater system flexibility.

2. Features

■ On-chip ultra-low-power 32-bit DSP

- Built-in software digital servo filter
- Built-in software Gyro filter

■ Flash Memory

- 40 kByte Flash memory to store data and DSP software

■ Peripherals

- Built-in Hall op amp with internal 5×, 10×, 13×, 20×, 40×, and 60× adjustable gain
- 4-channel, 14-bit A/D converter for Hall input
- 3-channel, 3-bit D/A converter for Hall offset setting
- 3-channel, 8-bit D/A converter for Hall bias setting
- Built-in 1-MHz 2-wire serial interface with clock stretch function
- Digital Gyro interface for various types of gyro (SPI Bus)
- Built-in 41-MHz oscillator
- Built-in LDO (Low Drop-Out regulator)

■ Package

- WLP35 (35-bump chipscale)
- 3.22 mm × 2.30 mm , 0.45 mm thick
- 0.4 mm bump pitch
- Pb-Free and Halogen Free

■ Motor Driver

- OIS
  2-channel constant current linear driver (I_{full} = 200 mA)
  2-channel H-bridge PWM driver (I_{omax} = 220 mA)
- OP-AF (unidirection)
  1-channel constant current linear driver (I_{full} = 150 mA)
- OP-AF (bidirection)
  1-channel constant current linear driver (I_{full} = 150 mA)
- CL-AF
  1-channel constant current linear driver (I_{full} = 150 mA)
  1-channel H-bridge PWM driver (I_{omax} 150 mA)

■ Power supply voltage

- AD/DA/VGA/LDO/OSC :
  AVDD30 = 2.6 to 3.3 V
- Digital I/O (except Gyro I/F) :
  AVDD30 = 2.6 to 3.3 V
- Driver :
  VM = Constant current : 1.75 to 3.3 V
  H Bridge PWM : 2.6 to 3.3 V
- Core Logic / Gyro interface I/O generated by internal LDO :
  DVDD15 = 1.55 V output (typ)

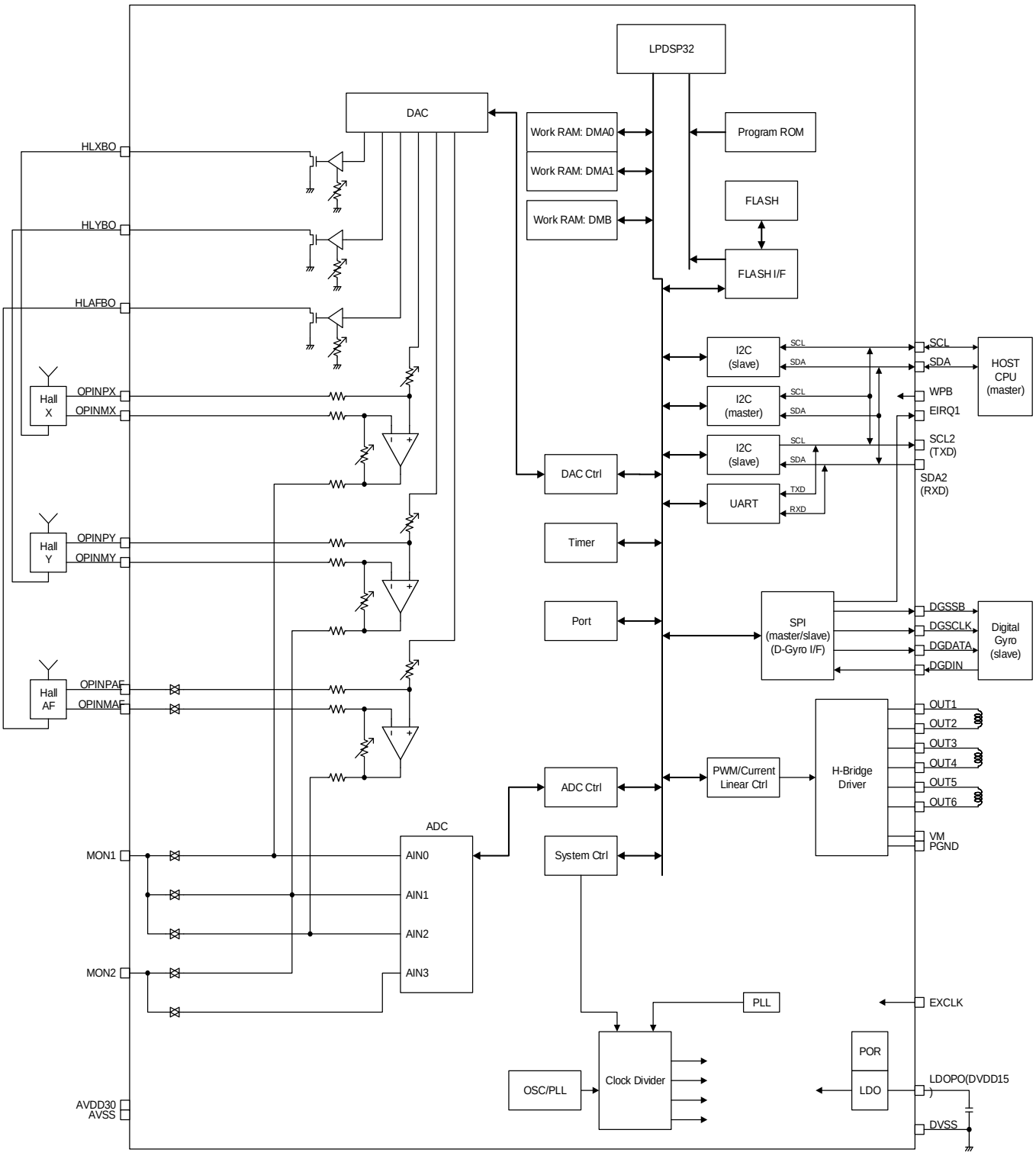
ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

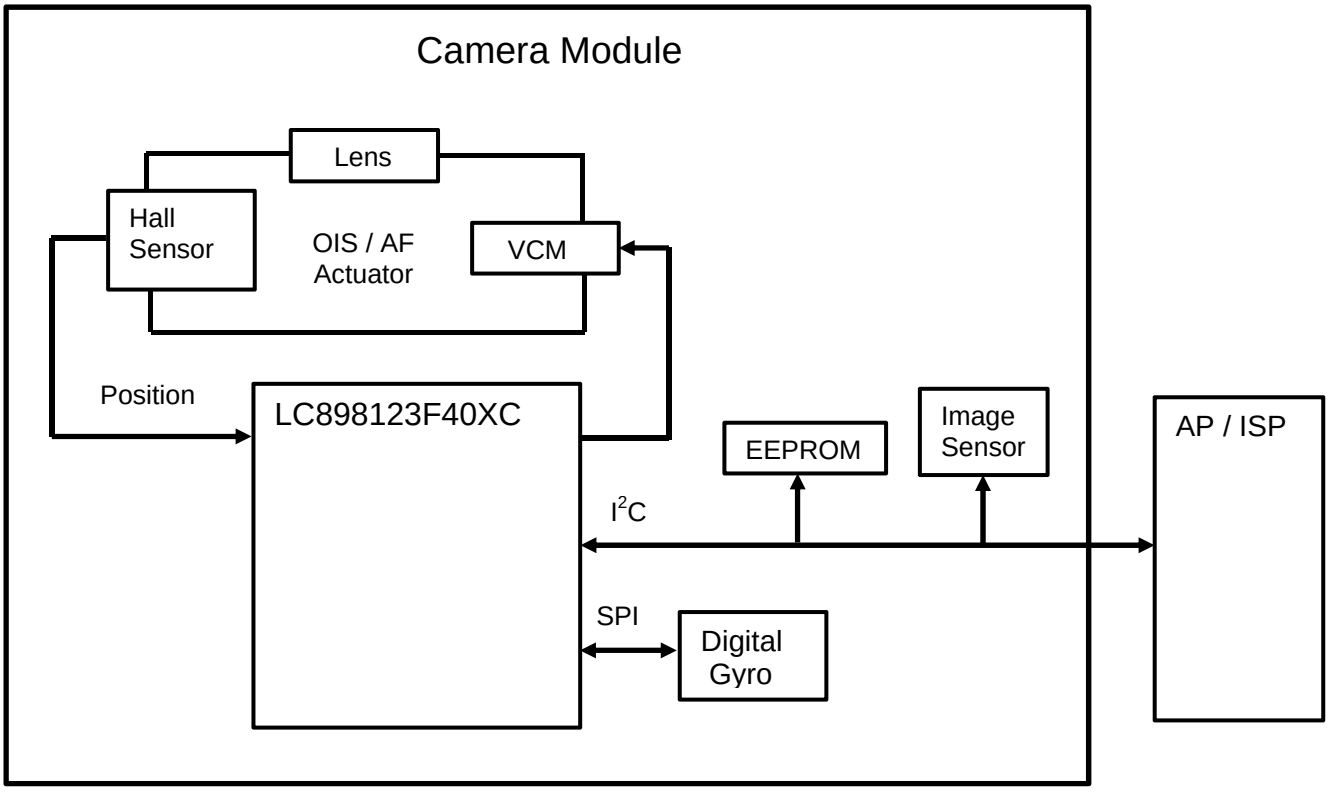
March 2017 - Rev. 3

Publication Order Number :
LC898123F40XC/D

3. Block Diagram



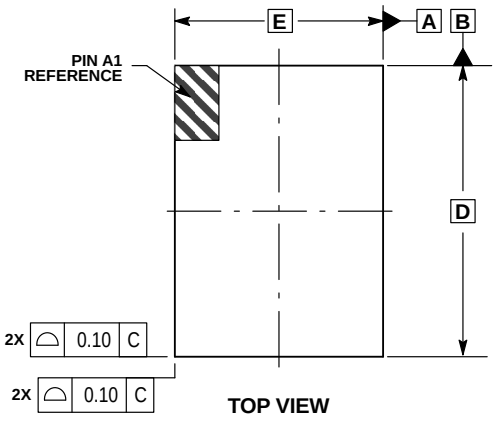
4. Application Diagram



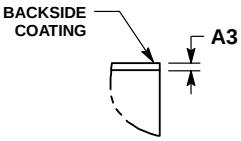
5. Package Dimensions

unit : mm

WLCSP35, 3.22x2.3
CASE 567LJ
ISSUE B



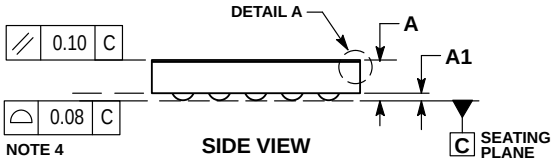
TOP VIEW



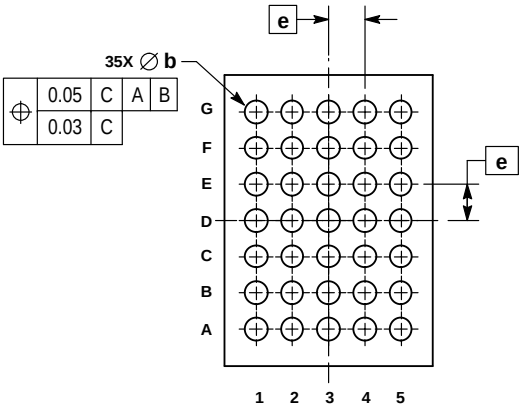
DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.35	0.45
A1	0.03	0.13
A3	0.025 REF	
b	0.15	0.25
D	3.22 BSC	
E	2.30 BSC	
e	0.40 BSC	

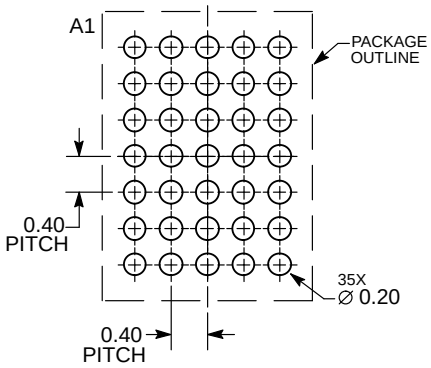


SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

6. Pin Assign

	1	2	3	4	5
G	OUT4	OUT3	OUT2	OUT1	VM
F	MON1	SDA2 (RXD)	WPB	PGND	OUT6
E	MON2	SCL2 (TXD)	DVSS	EXCLK	OUT5
D	DVDD15	EIRQ1	AVSS	SDA	SCL
C	AVDD30	HLAFBO	AVSS	HLYBO	HLXBO
B	DGDATA	DGSSB	OPINMAF	OPINMY	OPINMX
A	DGSCLK	DGDIN	OPINPAF	OPINPY	OPINPX

BOTTOM VIEW

- Driver output
- Driver V_{DD}
- Driver GND
- Analog V_{DD}
- Analog GND
- Digital GND
- Logic Core V_{DD} (Output)

7. Pin Descriptions

Pin Num	Pin	I/O Atr	I/O Pwr (V)	Primary Function (just after Reset)	Sub Functions	Init
A1	DGSCLK	B	1.55	Digital Gyro I/F Clock Input	Digital Gyro Clock Output	Z
				Digital Gyro I/F Clock Output	Internal Signal Monitor	
A2	DGDIN	B	1.55	Digital Gyro Data Input (4 Wired)	I^2C Data I/O for DAC Monitor	Z
					Internal Signal Monitor	
A3	OPINPAF	I	2.8	AF Hall Opamp Input Plus	–	–
A4	OPINPY	I	2.8	OIS Hall Y Opamp Input Plus	–	–
A5	OPINPX	I	2.8	OIS Hall X Opamp Input Plus	–	–
B1	DGDATA	B	1.55	GPIO Input	Digital Gyro I/F Data Output (4 Wired)	Z
					Digital Gyro I/F Data I/O (3 Wired)	
					Internal Signal Monitor	
B2	DGSSB	B	1.55	Digital Gyro I/F Chip Select Input	Digital Gyro I/F Chip Select Output	Z
				Digital Gyro I/F Chip Select Output	Internal Signal Monitor	
B3	OPINMAF	I	2.8	AF Hall OpAmp Input Minus	–	–
B4	OPINMY	I	2.8	OIS Hall Y Opamp Input Minus	–	–
B5	OPINMX	I	2.8	OIS Hall X Opamp Input Minus	–	–
C1	AVDD30	P	–	Analog Power (2.6 to 3.3 V)	–	–
C2	HLAFBO	O	2.8	AF Hall Bias Output	–	–
C3	AVSS	P		Analog GND	–	–
C4	HLYBO	O	2.8	OIS Hall Y Bias Output	–	–
C5	HLXBO	O	2.8	OIS Hall X Bias Output	–	–
D1	DVDD15	P	-	Internal LDO Power Output	–	–
D2	EIRQ1	B	2.8	External IRQ1	I^2C Data I/O for DAC Monitor	D
					UART Data Output (TXD)	
					SPI I/F Chip Select Output	
				External Clock Input	Internal Signal Monitor	
					Servo Monitor Analog Input	
D3	AVSS	P	–	Analog GND	–	–
D4	SDA	B	2.8	I^2C Data	–	Z
D5	SCL	B	2.8	I^2C Clock	–	Z
E1	MON2	B	2.8	(Debugger Data Input)	I^2C Data I/O for DAC Monitor	Z
					UART Data Input (RXD)	
					Servo Monitor Analog Out	
					Internal Signal Monitor	
E2	SCL2 (TXD)	B	2.8	I^2C Clock for 2nd I^2C	I^2C Data I/O for DAC Monitor	Z
					UART Data Output	
					Internal Signal Monitor	
E3	DVSS	P	–	Logic GND	–	–
E4	EXCLK	B	2.8	External Clock Input	I^2C Data I/O for DAC Monitor	D
				External IRQ1	Internal Signal Monitor	
E5	OUT5	O	2.8	AF Driver Output (H-Bridge, Linear)	–	–
F1	MON1	B	2.8	(Debugger Data Output)	I^2C Data I/O for DAC Monitor	L
					UART Data Output (TXD)	
					Servo Monitor Analog Out	
					Internal Signal Monitor	
F2	SDA2 (RXD)	B	2.8	I^2C Data for 2nd I^2C	I^2C Data I/O for DAC Monitor	Z
					UART Data Input	
					Internal Signal Monitor	
F3	WPB	I	2.8	Write Protect for Flash	–	D
F4	PGND	P	–	Driver GND	–	–
F5	OUT6	O	2.8	AF Driver Output (H-Bridge, Linear)	–	–
G1	OUT4	O	2.8	OIS Driver Output	–	–
G2	OUT3	O	2.8	OIS Driver Output	–	–
G3	OUT2	O	2.8	OIS Driver Output	–	–
G4	OUT1	O	2.8	OIS Driver Output	–	–
G5	VM	P	–	Driver Power (2.6 to 3.3 V)	–	–

8. Electrical Characteristics

Absolute Maximum Rating at AVSS = 0 V, DVSS = 0 V, PGND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	$V_{AD}30$ max	Ta ≤ 25°C	–0.3 to +4.6	V
	VM max	Ta ≤ 25°C	–0.3 to +4.6	V
Input voltage (Except DGDATA, DGSSB, DGSCLK, DGDIN)	$V_{AI}30$	Ta ≤ 25°C	–0.3 to $V_{AI}30$+0.3	V
Input voltage (DGDATA, DGSSB, DGSCLK, DGDIN)	$V_{LDO}18$	Ta = –30 to +85°C	–0.3 to +1.872	V
Storage temperature	Tstg		–55 to +125	°C
Operating temperature	Topr		–30 to +85	°C
Output continuous current	Iomax	OUT1 to 4	210	mA
		OUT5, OUT6	157.5	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ratings at Ta = –30 to +85°C, AVSS = 0 V, DVSS = 0 V, PGND = 0 V

3.0 V Power Supply (AVDD30)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage	$V_{AD}30$	2.6	2.8	3.3	V
Input voltage range	V_{IN}	0	–	$V_{AD}30$	V

3.0 V Power Supply (VM)

Parameter	Symbol	Min	Typ	Max	Unit
Power supply voltage (H-Bridge PWM)	V_M30	2.6	2.8	3.3	V
Power supply voltage (Constant current)		1.75	2.8	3.3	V
Input voltage range	V_{INM}	0	–	V_M30	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC Characteristics : Input/Output level at AVSS = 0 V, DVSS = 0 V, PGND = 0 V, V_{DD} = 2.6 to 3.6 V, Ta = –30 to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Applicable Pin
High-level input voltage	VIH	CMOS schmitt	1.36			V	SCL2(TXD), SDA2(RXD), EXCLK
Low-level input voltage	VIL				0.39	V	
High-level input voltage	VIH	CMOS schmitt	1.26			V	DGDIN, DGSSB, DGSCLK, DGDATA
Low-level input voltage	VIL				0.35		
High-level input voltage	VIH	CMOS schmitt	1.40				SCL, SDA
Low-level input voltage	VIL				0.40	V	
High-level input voltage	VIH	CMOS schmitt	1.48				EIRQ1, WPB
Low-level input voltage	VIL				0.37		
High-level input voltage	VIH	CMOS supported	1.40				MON1, MON2
Low-level input voltage	VIL				0.51		
High-level output voltage	VOH	IOH = –2 mA	AVDD30 –0.4			V	SCL2(TXD), SDA2(RXD), EXCLK, EIRQ1, MON1, MON2
High-level output voltage	VOH	IOH = –0.1 mA	1.32			V	DGDIN, DGSSB, DGSCLK, DGDATA
Low-level output voltage	VOL	IOL = 2 mA			0.2	V	SCL2(TXD), SDA2(RXD), DGDIN, DGSSB, DGSCLK, DGDATA, EXCLK, SDA, SCL
Low-level output voltage	VOL	IOL = 2 mA			0.4	V	MON1,MON2,EIRQ1
Analog input voltage	VAI		AVSS		AVDD30	V	OPINPX, OPINPY, OPINPAF, OPINMX, OPINMY, OPINMAF
PullUp resistor	Rup		50		200	kΩ	MON1, MON2, EIRQ1, SCL2(TXD), SD2(RXD)
PullUp resistor	Rup		180		800	kΩ	DGDATA, DGDIN, DGSSB, DGSCLK
PullDown resistor	Rdn		50		220	kΩ	MON1, MON2, EIRQ1, SCL2(TXD), SDA2(RXD), EXCLK, WPB
PullDown resistor	Rdn		120		500	kΩ	DGDATA, DGDIN, DGSSB, DGSCLK

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Driver output at Ta = –30 to +85°C, AVSS = 0 V, DVSS = 0 V, PGND = 0 V

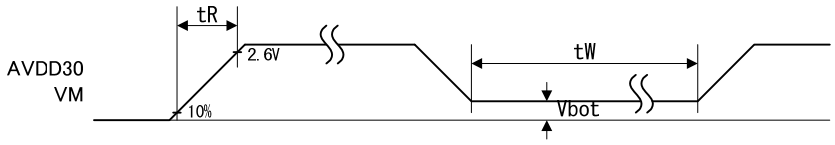
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Current OUT1 to OUT4	I_{full}	Full code		200		mA
Output Current OUT5, OUT6		Full Code OP-AF (bidirection / unidirection) CL-AF		150		mA

Non-volatile Memory Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Endurance	EN				1000	Cycles
Data retention	RT		10			Years

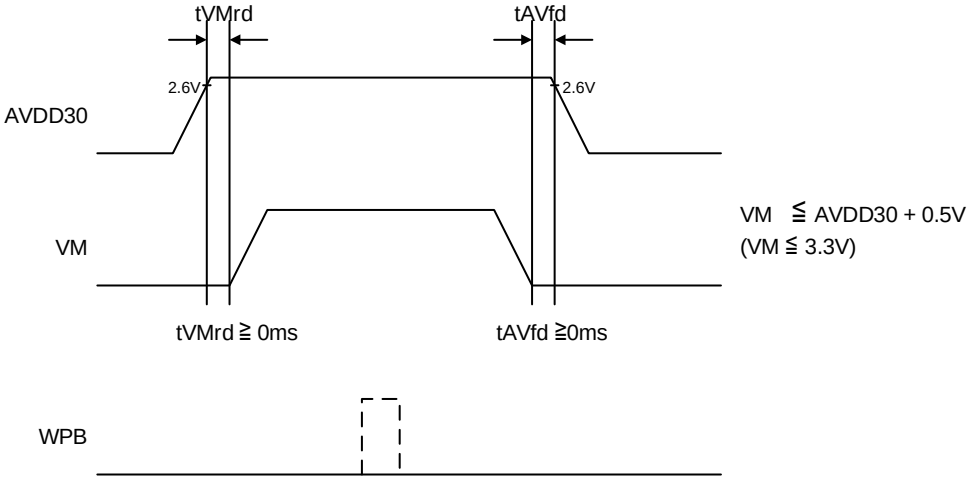
9. AC Characteristics

9-1 Power Sequence



Item	Symbol	Min	Typ	Max	Units
Rise time	tR			3	ms
Wait time	tW	100			ms
Bottom Voltage	Vbot			0.2	V

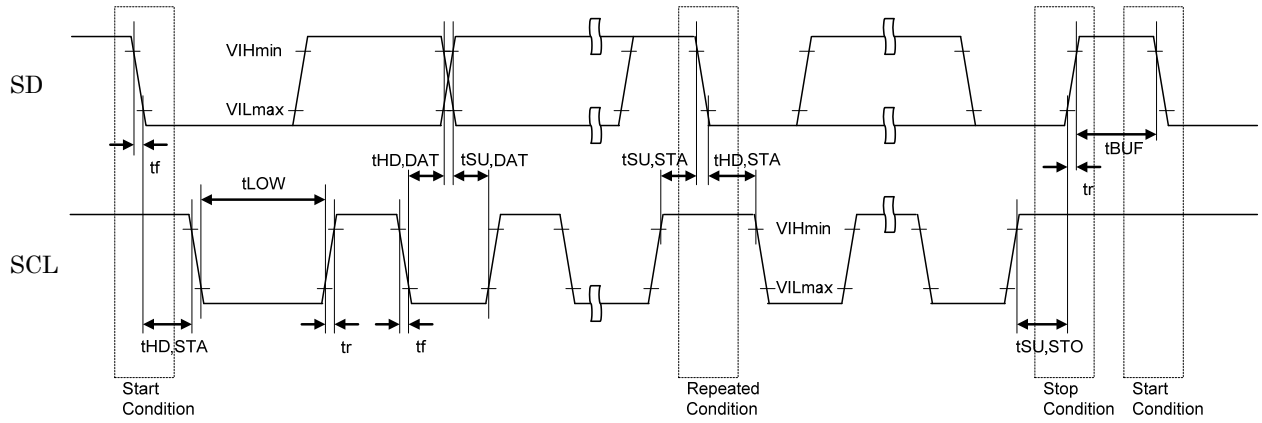
Injection order between AVDD30 and VM is below.



WPB must be open or pulled down normally. When Flash is erased or programmed, WPB must be held High.
SDA, SCL, EXCLK, and WPB will tolerate 3 V input at the time of power off.
Power must remain applied to the device during flash access in order to prevent unintentional rewriting of the flash memory.
Data in flash memory may be rewritten unintentionally if the specified power sequencing techniques are not kept.

9-2 Two Wire Serial Interface Timing

The device's communication protocol is compatible with I^{2}C (Fast mode Plus). This circuit has clock stretch function.



Item	Symbol	Pin name	Min	Typ	Max	Units
SCL clock frequency	Fscl	SCL			1000	kHz
START condition hold time	tHD,STA	SCL SDA	0.26			µs
SCL clock Low period	tLOW	SCL	0.5			µs
SCL clock High period	tHIGH	SCL	0.26			µs
Setup time for repetition START condition	tSU,STA	SCL SDA	0.26			µs
Data hold time	tHD,DAT	SCL SDA	0 (*1)		0.9	µs
Data setup time	tSU,DAT	SCL SDA	50			ns
SDA, SCL rising time	tr	SCL SDA			120	ns
SDA, SCL falling time	tf	SCL SDA			120	ns
STOP condition setup time	tSU,STO	SCL SDA	0.26			µs
Bus free time between STOP and START	tBUF	SCL SDA	0.5			µs

(*1) Although the I^{2}C specification defines a condition that 300 ns of hold time is required internally, LC898123F40XC is designed for a condition with typ. 40 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate countermeasure on board, such as inserting a resistor.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898123F40XC-VH	WLCSP35, 3.22x2.3 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF