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LC898219XI

Advance Information Auto Focus (AF) Controller



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Overview

This LSI is Closed-Auto Focus control LSI equipped with hall sensor. It consists of 1 system feedback circuit and constant current driver. It has also a built-in EEPROM and temperature sensor.

Features

- Built-in equalizer circuit using digital operation
 - AF control equalizer circuit
 - Any coefficient can be specified by 2-wire serial I/F (TWIF)
- 2-wire serial interface
(The communication protocol is compatible with I²C.)
- Built-in A/D converter
- Built-in D/A converter
 - Hall offset
 - Constant current bias
- Built-in Hall Sensor
 - Si Hall sensor
- Built-in VGA
 - Hall Amp
- Built-in EEPROM
 - 128 byte (16 byte/page)
- Built-in OSC
- Built-in Constant Current Driver
 - 140 mA
- Package
 - WL-CSP 8-pin
 - Pb-Free, Halogen Free
- Supply voltage
 - VDD (2.6 V to 3.3 V)



WLCSP8, 0.97x2.25x0.265

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

Pin Description

TYPE					
I	INPUT	P	Power supply, GND	NC	NOT CONNECT
O	OUTPUT				
B	BIDIRECTION				

■ 2-wire serial interface

SCL	I	2-wire serial interface clock pin
SDA	B	2-wire serial interface data pin

■ Driver interface

OUT1	O	Driver output (to Actuator)
OUT2	O	Driver output (to Actuator)

■ Power supply pin

VDD	P	Power supply
VSS	P	GND

■ Port pin

PORT	B	Convergence detection monitor output VSYNC input Test pin
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■ Test pin

TEST	O	Test pin
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*Process when pins are not used

PIN TYPE "O" – Ensure that it is set to OPEN.

PIN TYPE "I" – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused. (Please contact ON Semiconductor for more information about selection of VDD or VSS.)

PIN TYPE "B" – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

*In case of connecting PORT pin with HOST CPU

When LC898219XI is power off and HOST CPU is power on, a HOST CPU pin connected with PORT pin have to be fixed "L" level.

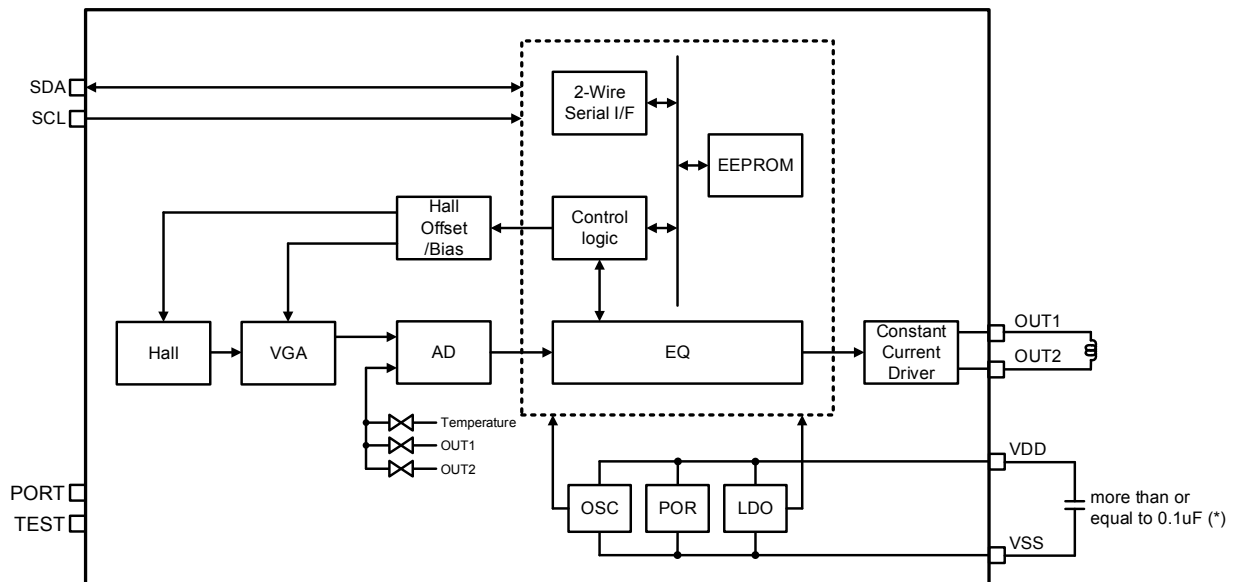
LC898219XI

Pin Layout

BOTTOM VIEW

	1	2	3	4
B	OUT1	VDD	SCL	SDA
A	OUT2	VSS	TEST	PORT

Block Diagram



(*) : Consider capacitance of capacitor between V_{DD} and V_{SS}. According to power source environment, attach an additional capacitor in camera module.

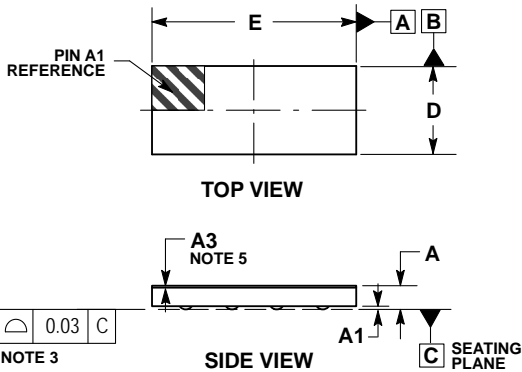
Package Dimensions

unit : mm

WLCSP8, 0.97x2.25X0.265

CASE 567TE

ISSUE A

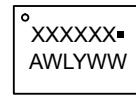


NOTES:

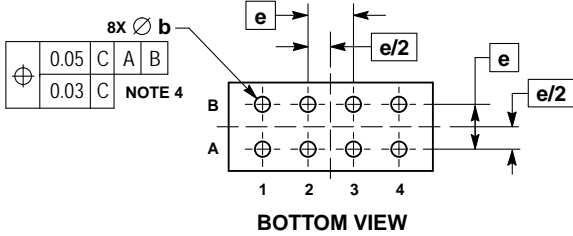
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM BALL DIAMETER PARALLEL TO DATUM C.
5. DIMENSION A3 IS AN OPTIONAL BACKSIDE COATING LAYER.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.24	0.265	0.29
A1	0.04 REF		
A3	0.025 REF		
b	0.12	0.17	0.22
D	0.92	0.97	1.02
E	2.20	2.25	2.30
e	0.50 BSC		

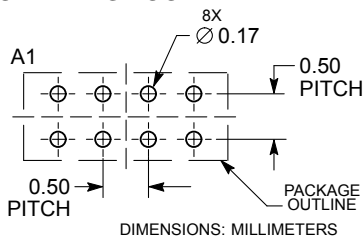
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- = Pb-Free Package



RECOMMENDED SOLDERING FOOTPRINT*



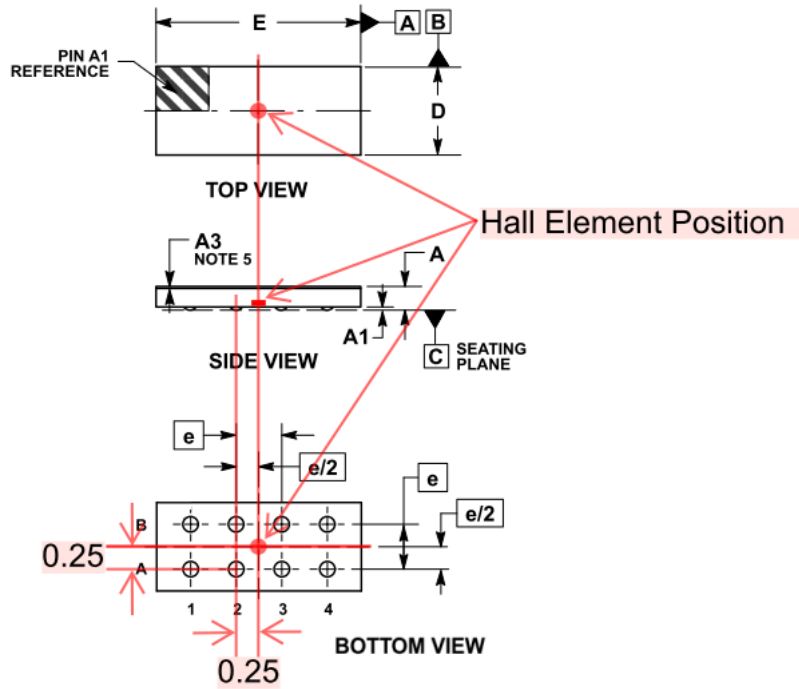
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic.

Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

About NOTE 5 : This product has "BACKSIDE COATING".

Hall Element Position



unit: mm(typ)

Figure. Hall element position

Please refer to package diagram for each dimension.

Electrical Characteristics

Absolute maximum rating at VSS = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V _{DD33} max	Ta ≤ 25°C	-0.3 to +4.6	V
Input/output voltage	V _{I33} , V _{O33}	Ta ≤ 25°C	-0.3 to V _{DD33} +0.3	V
Storage ambient temperature	Tstg		-55 to +125	°C
Operating ambient temperature	Topr		-30 to +70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Acceptable operation range at Ta = -30 to 70°C, VSS = 0 V

3 V power supply (V_{DD})

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD33}	2.6	2.8	3.3	V
Input voltage range	V _{IN}	0		V _{DD33}	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC characteristics : Input/output level at VSS = 0 V, V_{DD} = 2.6 V to 3.3 V, Ta = -30 to +70°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
High-level input voltage	V _{IH}	CMOS compliant Schmidt	1.4			V	SCL, SDA, PORT
Low-level input voltage	V _{IL}				0.4	V	
High-level output voltage	V _{OH}	I _{OH} = -2 mA	V _{DD} -0.4			V	PORT
Low-level output voltage	V _{OL}	I _{OL} = -2 mA			0.2	V	SDA, PORT
Pulldown resistor	R _{dn}		50		220	kΩ	PORT

Driver output (OUT1, OUT2) at VSS = 0 V, V_{DD} = 2.8 V, Ta = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable pins
Maximum current	I _{full}		133	140	147	mA	OUT1, OUT2

Non-volatile Memory Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable circuit
Endurance	EN				1000	Cycles	EEPROM
Data retention	RT		10			Years	
Write time	t _{WT}				20	ms	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC Characteristics

V_{DD} supply timing

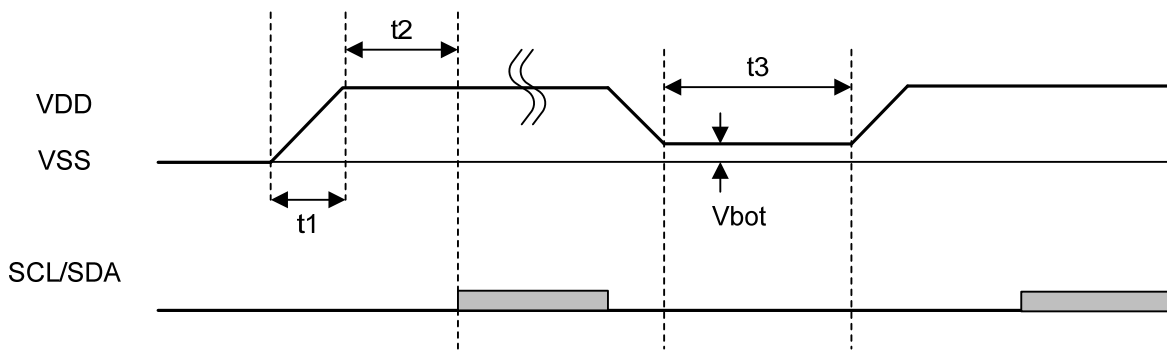


Figure. V_{DD} supply timing

It is available to use 2-wire serial interface 5 ms later for Power On Reset of V_{DD}.

Item	Symbol	Min	Typ	Max	Unit
V _{DD} turn on time	t1			3	ms
2-wire serial interface start time from V _{DD} on	t2	5			ms
V _{DD} off time	t3	100			ms
Bottom Voltage	Vbot			0.1	V

AC specification

The figure below shows interface timing definition and following table shows electric characteristics.

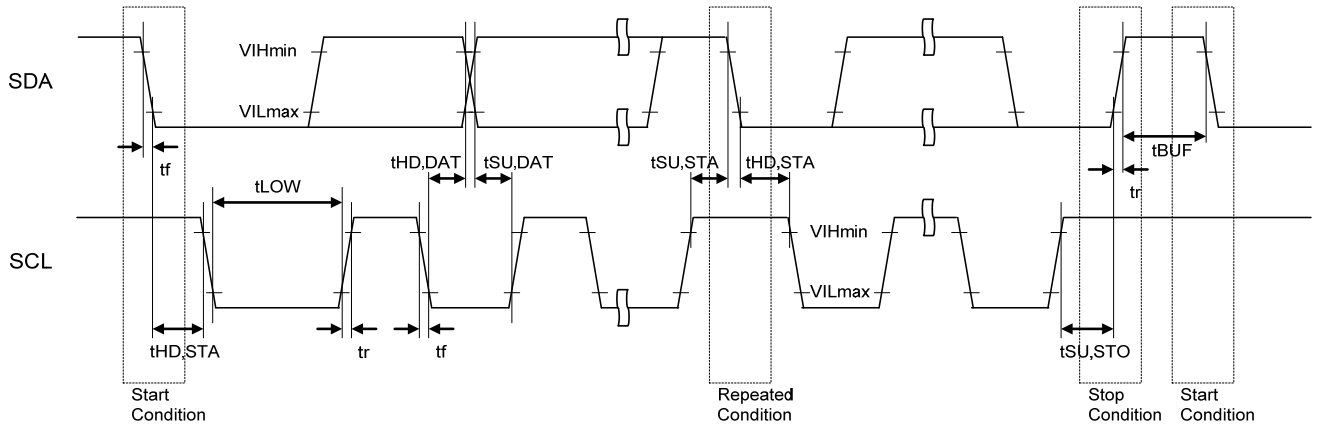


Figure. 2-wire serial interface timing definition

Table. Electric characteristics for 2-wire serial interface (AC characteristics)

Item	Symbol	Pin name	Fast-mode			Fast-mode Plus			Unit
			Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	FSCL	SCL			400			1000	kHz
START condition hold time	$t_{HD,STA}$	SCL SDA	0.6			0.26			μ s
SCL clock Low period	t_{LOW}	SCL	1.3			0.5			μ s
SCL clock High period	t_{HIGH}	SCL	0.6			0.26			μ s
Setup time for repetition START condition	$t_{SU,STA}$	SCL SDA	0.6			0.26			μ s
Data hold time	$t_{HD,DAT}$	SCL SDA	0 (*3)		0.9	0 (*3)			μ s
Data setup time	$t_{SU,DAT}$	SCL SDA	100			50			ns
SDA, SCL rising time	t_r	SCL SDA			300			120	ns
SDA, SCL falling time	t_f	SCL SDA			300			120	ns
STOP condition setup time	$t_{SU,STO}$	SCL SDA	0.6			0.26			μ s
Bus free time between STOP and START	t_{BUF}	SCL SDA	1.3			0.5			μ s

*3: LC898219XI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

LC898219XI

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC898219XI-MH	WLCSP8, 0.97x2.25x0.265 (Pb-Free / Halogen Free)	4000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF

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