19-3177; Rev 1; 3/05

EVALUATION KIT AVAILABLE

High-Efficiency CCFL Backlight Controller with SMBus Interface

General Description

The MAX8709/MAX8709A integrated backlight controller are optimized to drive cold-cathode fluorescent lamps (CCFLs) using a resonant full-bridge inverter architecture. The resonant operation maximizes striking capability and provides near-sinusoidal waveforms over the entire input range to improve CCFL lifetime. The controller operates over a wide input voltage range of 4.6V to 28V with high power-to-light efficiency. The device also includes safety features that effectively protect against many single-point fault conditions including lamp-out and short-circuit faults.

The MAX8709/MAX8709A achieve 10:1 dimming range by "chopping" the lamp current on and off using a digital pulse-width-modulation (DPWM) method. The minimum DPWM duty cycle of the MAX8709 is 9.375% and the minumum duty cycle of the MAX8709A is 12.5%. The brightness is controlled with a 2-wire SMBus™-compatible interface. The device directly drives the four external N-channel power MOSFETs of the full-bridge inverter. An internal 5.3V linear regulator powers the MOSFET drivers, the DPWM oscillator, and most of the internal circuitry. The MAX8709/MAX8709A are available in a space-saving 28-pin thin QFN package and operates over a -40°C to +85°C temperature range.

Applications

Notebook Computer Displays

LCD Monitors

LCD TVs

Automotive Displays

SMBus is a trademark of Intel Corp.

Features

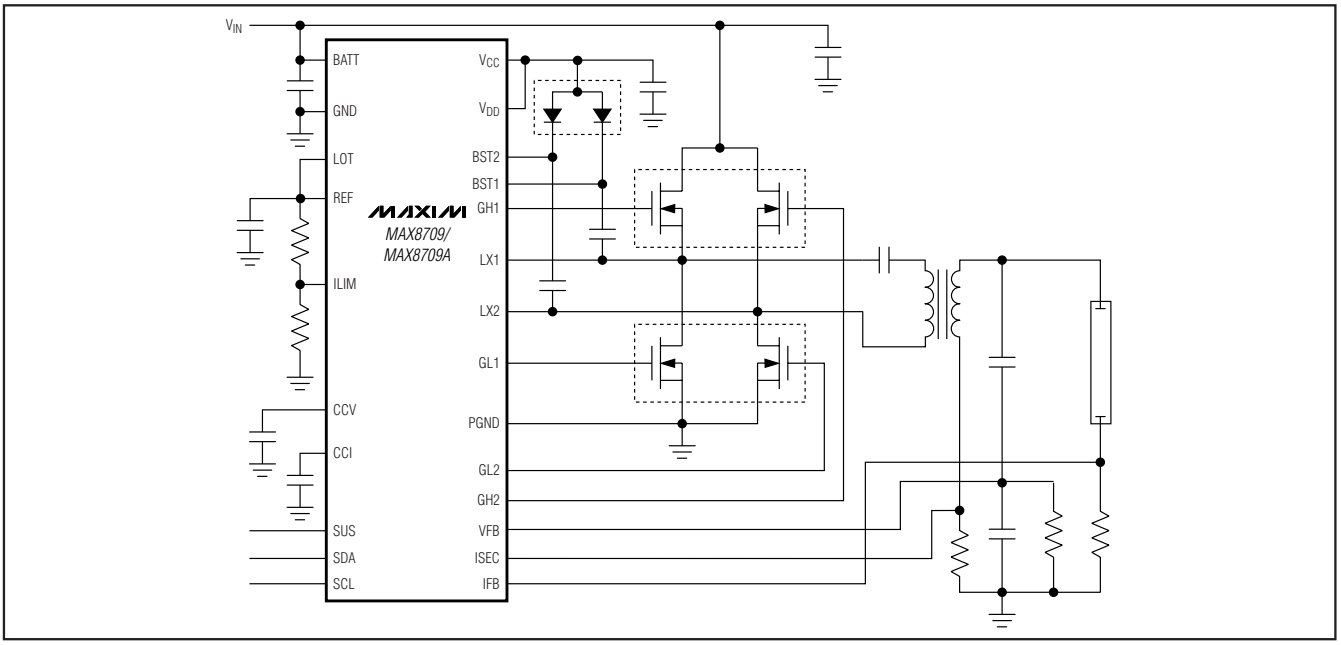
- **Synchronized to Resonant Frequency**
  - **Longer Lamp Life**
  - **Guaranteed Striking Capability**
  - **High Power-to-Light Efficiency**
- **Wide Input Voltage Range (4.6V to 28V)**
- **Feed Forward for Excellent Line Rejection**
- **SMBus Dimming Control Interface**
- **10:1 Dimming Range**
- **Guaranteed 200Hz to 220Hz DPWM Frequency**
- **Secondary Voltage Limit Reduces Transformer Stress**
- **Adjustable Lamp-Out Protection with 1s Timer**
- **Secondary Current Limit Protects Against High-Voltage Short Circuits to Ground**
- **Small 5mm x 5mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8709ETI	-40°C to +85°C	28 Thin QFN 5mm x 5mm
MAX8709AETI	-40°C to +85°C	28 Thin QFN 5mm x 5mm

Pin Configuration appears at end of data sheet.

Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

High-Efficiency CCFL Backlight Controller with SMBus Interface

ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to +30V
BST1, BST2 to GND .....-0.3V to +36V
BST1 to LX1, BST2 to LX2 .....-0.3V to +6V
GH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
GH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
V_{CC}, V_{DD} to GND .....-0.3V to +6V
REF, ILIM to GND .....-0.3V to (V_{CC} + 0.3V)
GL1, GL2 to GND .....-0.3V to (V_{DD} + 0.3V)
CCI, CCV, LOT to GND .....-0.3V to +6V
IFB, ISEC, VFB to GND .....-6V to +6V
SDA, SCL, SUS to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derate 20.84mW/°C above +70°C) ..1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BATT} Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28.0	
V_{BATT} Quiescent Current	V_{SUS} = 5.5V	V_{BATT} = 28V		1.5	3	mA
		V_{BATT} = V_{CC} = 5V			3	
V_{BATT} Quiescent Current, Shutdown	SUS = GND			6	20	µA
V_{CC} Output Voltage, Normal Operation	V_{SUS} = 5.5V, 6V < V_{BATT} < 28V, 0 < I_{LOAD} < 20mA		5.0	5.35	5.5	V
V_{CC} Output Voltage, Shutdown	SUS = GND, no load		3.5	4.6	5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)				4.5	V
	V_{CC} falling (entering lockout)		4.0			
V_{CC} Undervoltage-Lockout Hysteresis				200		mV
V_{CC} Power-On Reset (POR) Threshold	Rising edge		0.90	1.75	2.70	V
V_{CC} POR Hysteresis				50		mV
REF Output Voltage, Normal Operation	4.5V < V_{CC} < 5.5V, I_{LOAD} = 40µA		1.96	2.00	2.04	V
GH1, GH2, GL1, GL2 On-Resistance	I_{TEST} = 100mA, V_{CC} = V_{DD} = 5.3V			9	18	Ω
GH1, GH2, GL1, GL2 Output Current				0.5		A
BST1, BST2 Leakage Current	$V_{BST\_}$ = 12V, $V_{LX\_}$ = 7V				5	µA
Input Resonant Frequency	Guaranteed by design		25		300	kHz
Minimum Off-Time			180	280	380	ns
Maximum Off-Time			18	28	38	µs
Current-Limit Threshold LX1 - GND, LX2 - GND (Fixed)	ILIM = V_{CC}		180	200	220	mV
Current-Limit Threshold LX1 - GND, LX2 - GND (Adjustable)	V_{ILIM} = 0.5V		80	100	120	mV
	V_{ILIM} = 2.0V		370	400	430	
Minimum Current Threshold LX1 - GND, LX2 - GND				6		mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOT Input Voltage Range		0.5		V_{REF}	V
LOT Input Bias Current		-2		+2	µA
IFB Input Voltage Range		-1.7		+1.7	V
IFB Regulation Point		380	400	420	mV
IFB Input Bias Current	V_{IFB} = 0.4V	-2		+2	µA
IFB Lamp-Out Threshold	LOT = REF	500	600	700	mV
IFB to CCI Transconductance	1V < V_{CCI} < 2.5V		100		µS
CCI Output Impedance			20		MΩ
ISEC Input Voltage Range		-2		+2	V
ISEC Regulation Threshold		1.20	1.25	1.30	V
ISEC Input Bias Current	V_{ISEC} = 1.25V	-2		+2	µA
VFB Input Voltage Range		-2		+2	V
VFB Input Bias Current	V_{VFB} = 0.5V	-0.5		+0.5	µA
VFB Regulation Point		490	510	530	mV
VFB to CCV Transconductance	1V < V_{CCV} < 2.7V		40		µS
VFB Zero-Voltage Crossing Threshold		-10		+10	mV
CCV Output Impedance			20		MΩ
Digital PWM Chopping Frequency	MAX8709	200	210	220	Hz
	MAX8709A	204	210	216	
Lamp-Out Detection Timeout Timer	V_{IFB} < 0.1V (Note 1)	1.14	1.22	1.30	s
SDA, SCL, SUS Input Low Voltage				0.8	V
SDA, SCL, SUS Input High Voltage		2.1			V
SDA, SCL, SUS Input Hysteresis			300		mV
SDA, SCL, SUS Input Bias Current		-1		+1	µA
SDA Output Low Sink Current	V_{SDA} = 0.4V	4			mA
SCL Serial Clock High Period	T_{HIGH}	4			µs
SCL Serial Clock Low Period	T_{LOW}	4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$	4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$	4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking-In Data	$t_{SU:DAT}$	250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$	0			ns
SCL Falling Edge to SDA Valid, Reading Out Data	T_{DV}		700		ns

High-Efficiency CCFL Backlight Controller with SMBus Interface

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BATT} Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28.0	
V_{BATT} Quiescent Current	V_{SUS} = 5.5V	V_{BATT} = 28V			3	mA
		V_{BATT} = V_{CC} = 5V			3	
V_{BATT} Quiescent Current, Shutdown	SUS = GND				20	µA
V_{CC} Output Voltage, Normal Operation	V_{SUS} = 5.5V, 6V < V_{BATT} < 28V, 0 < I_{LOAD} < 20mA		5.0		5.5	V
V_{CC} Output Voltage, Shutdown	SUS = GND, no load		3.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)				4.5	V
	V_{CC} falling (entering lockout)		4.0			
V_{CC} Power-On Reset (POR) Threshold	Rising edge		0.90		2.70	V
REF Output Voltage, Normal Operation	4.5V < V_{CC} < 5.5V, I_{LOAD} = 40µA		1.95		2.05	V
GH1, GH2, GL1, GL2 On-Resistance	I_{TEST} = 100mA, V_{CC} = V_{DD} = 5.3V				18	Ω
BST1, BST2 Leakage Current	$V_{BST\_}$ = 12V, $V_{LX\_}$ = 7V				5	µA
Input Resonant Frequency	Guaranteed by design		25		300	kHz
Minimum Off-Time			180		380	ns
Maximum Off-Time			18		38	µs
Current-Limit Threshold LX1 - GND, LX2 - GND (Fixed)	ILIM = V_{CC}		180		220	mV
Current-Limit Threshold LX1 - GND, LX2 - GND (Adjustable)	V_{ILIM} = 0.5V		80		120	mV
	V_{ILIM} = 2.0V		370		430	
Current-Limit Leading-Edge Blanking			250		450	ns
LOT Input Voltage Range			0.5		V_{REF}	V
LOT Input Bias Current			-2		+2	µA
IFB Input Voltage Range			-1.7		+1.7	V
IFB Regulation Point			380		420	mV
IFB Input Bias Current	V_{IFB} = 0.4V		-2		+2	µA
IFB Lamp-Out Threshold	LOT = REF		500		700	mV
ISEC Input Voltage Range			-2		+2	V
ISEC Regulation Point			1.20		1.30	V
ISEC Input Bias Current	V_{ISEC} = 1.25V		-2		+2	µA
VFB Input Voltage Range			-2		+2	V
VFB Input Bias Current	V_{VFB} = 0.5V		-0.5		+0.5	µA
VFB Regulation Point			490		530	mV
VFB Zero-Voltage Crossing Threshold			-10		+10	mV
Digital PWM Chopping Frequency	MAX8709		200		220	Hz
	MAX8709A		204		216	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

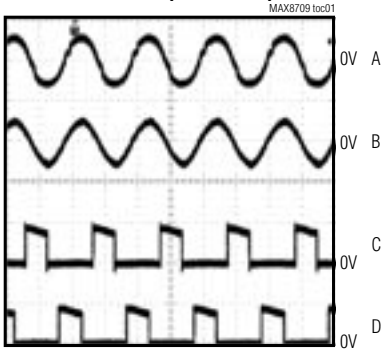
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Lamp-Out Detection Timeout Timer	V_{IFB} < 0.1V (Note 1)	1.14		1.30	s
SDA, SCL, SUS Input Low Voltage				0.8	V
SDA, SCL, SUS Input High Voltage		2.1			V
SDA, SCL, SUS Input Bias Current		-1		+1	µA
SDA Output Low Sink Current	V_{SDA} = 0.4V	4			mA
SCL Serial Clock High Period	T_{HIGH}	4			µs
SCL Serial Clock Low Period	T_{LOW}	4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$	4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$	4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking-In Data	$t_{SU:DAT}$	250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$	0			ns

Note 1: Corresponds to 256 DPWM cycles.
Note 2: Specifications to -40°C are guaranteed by design based on final characterization results.

Typical Operating Characteristics

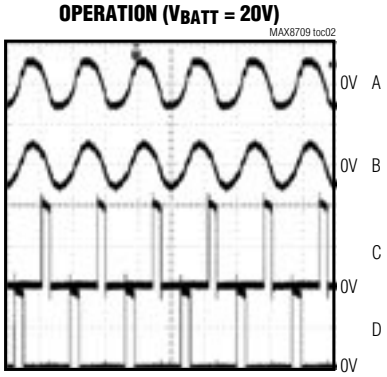
(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, T_A = +25°C, unless otherwise noted.)

LOW INPUT-VOLTAGE OPERATION (V_{BATT} = 8V)



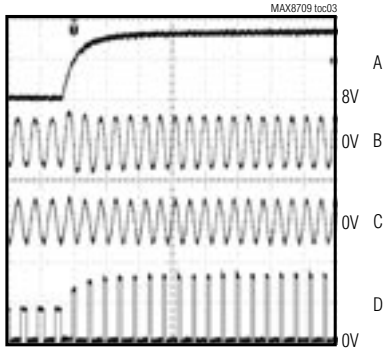
A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{LX1}, 10V/div
D: V_{LX2}, 10V/div

HIGH INPUT-VOLTAGE OPERATION (V_{BATT} = 20V)



A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{LX1}, 10V/div
D: V_{LX2}, 10V/div

LINE-TRANSIENT RESPONSE



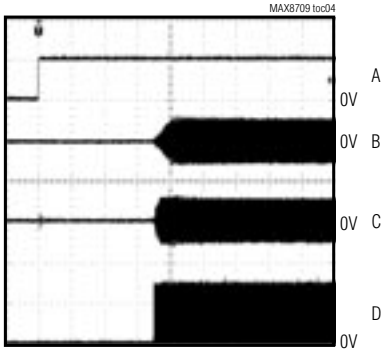
A: V_{BATT}, 5V/div
B: V_{IFB}, 2V/div
C: V_{VFB}, 2V/div
D: V_{LX1}, 10V/div

High-Efficiency CCFL Backlight Controller with SMBus Interface

Typical Operating Characteristics (continued)

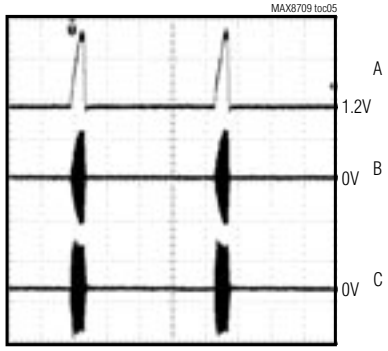
(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, T_A = +25°C, unless otherwise noted.)

STARTUP



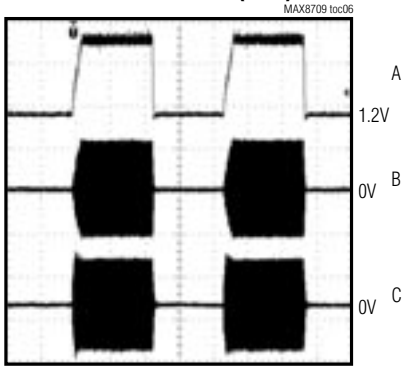
A: V_{SUS}, 5V/div
B: V_{IFB}, 2V/div
C: V_{VFB}, 2V/div
D: V_{LX1}, 10V/div

DPWM OPERATION (10%)



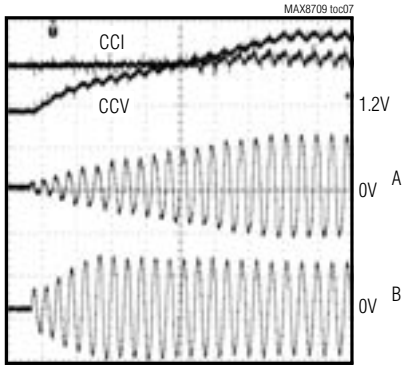
A: V_{CCV}, 200mV/div
B: V_{IFB}, 1V/div
C: V_{VFB}, 1V/div

DPWM OPERATION (50%)



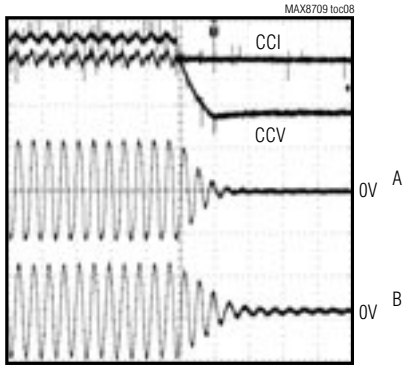
A: V_{CCV}, 200mV/div
B: V_{IFB}, 1V/div
C: V_{VFB}, 1V/div

DPWM SOFT-START



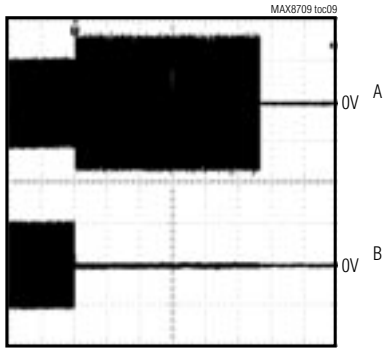
A: V_{IFB}, 1V/div
B: V_{VFB}, 1V/div

DPWM SOFT-STOP



A: V_{IFB}, 1V/div
B: V_{VFB}, 1V/div

LAMP-OUT VOLTAGE LIMITING AND TIMEOUT

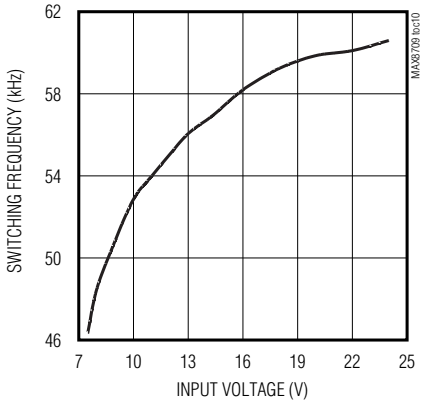


A: V_{VFB}, 1V/div
B: V_{IFB}, 1V/div

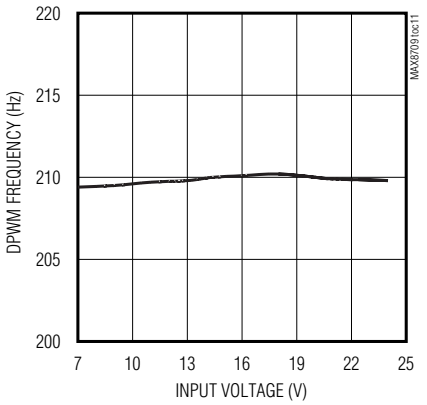
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{LOT} = V_{REF}, V_{CC} = V_{DD}, V_{SUS} = 5.3V, T_A = +25°C, unless otherwise noted.)

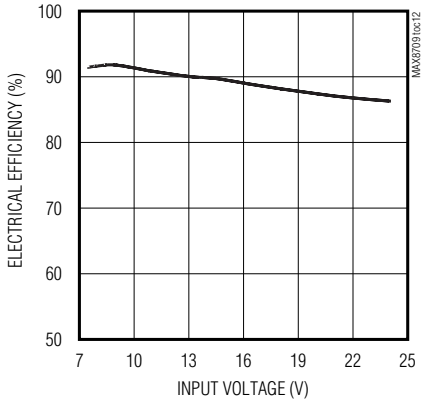
SWITCHING FREQUENCY vs. INPUT VOLTAGE



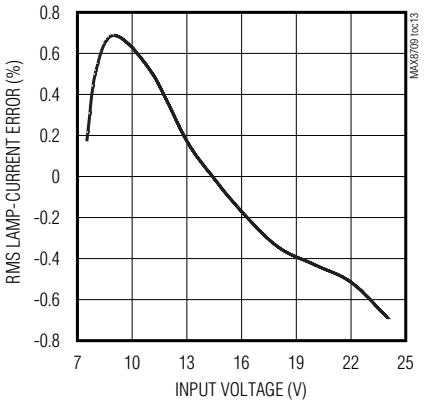
DPWM FREQUENCY vs. INPUT VOLTAGE



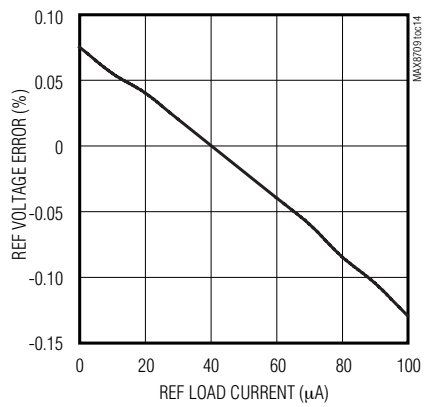
ELECTRICAL EFFICIENCY vs. INPUT VOLTAGE



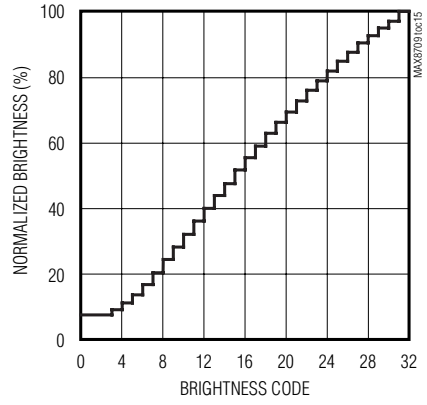
NORMALIZED RMS LAMP CURRENT vs. INPUT VOLTAGE



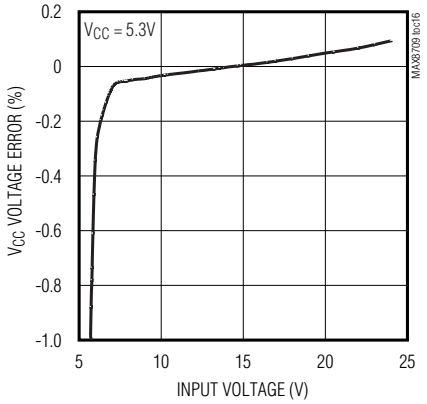
REF LOAD REGULATION



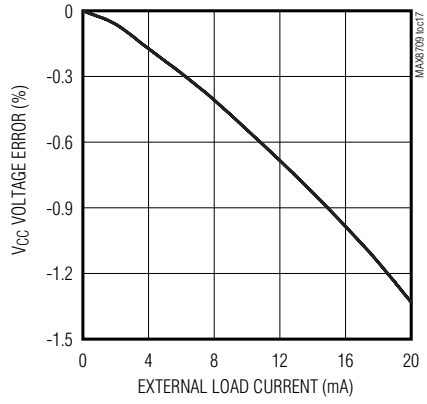
NORMALIZED BRIGHTNESS vs. BRIGHTNESS CODE



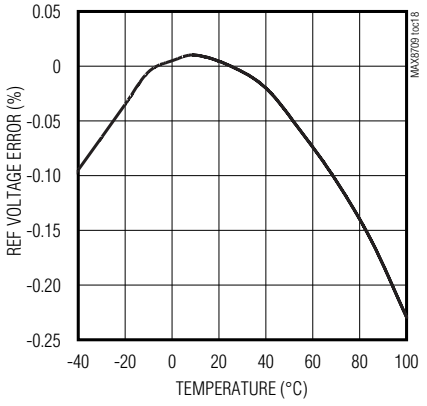
NORMALIZED V_{CC} LINE REGULATION



V_{CC} LOAD REGULATION



REF OUTPUT vs. TEMPERATURE



High-Efficiency CCFL Backlight Controller with SMBus Interface

Pin Description

PIN	NAME	FUNCTION
1	ILIM	Current-Limit Threshold Adjustment. Connect a resistive voltage-divider between REF or V_{CC} and GND. The current-limit threshold measured between LX_ and GND is 1/5th the voltage forced at ILIM. The ILIM adjustment range is 0 to 3V. Connect ILIM to V_{CC} to select the default current-limit threshold of 0.2V.
2	REF	2V Reference Output. Bypass REF to GND with a 0.1µF ceramic capacitor. REF is discharged to GND during shutdown.
3	LOT	Lamp-Out Threshold Adjustment. The lamp-out threshold is 30% of the voltage at LOT. The LOT adjustment range is from 0.5V to V_{REF}.
4	GND	Analog Ground. The ground return for V_{CC}, REF, and other analog circuitry. Connect GND to PGND under the IC at the IC's backside exposed metal pad.
5	ISEC	Secondary Current-Limit Sense Input. The secondary current limit controls the transformer secondary current even if the IFB sense resistor is shorted. See the *Secondary Current Limit (ISEC)* section.
6	SDA	SMBus Serial Data Input
7	SCL	SMBus Serial Clock Input
8	SUS	SMBus Suspend Input
9, 10, 11, 23	N.C.	No Connection. Not internally connected.
12	V_{DD}	Gate-Driver Supply Input. Connect V_{DD} to V_{CC}, the output of the linear regulator. Bypass V_{DD} with a 0.1µF capacitor to PGND.
13	PGND	Power Ground. Gate-driver current flows through this pin.
14	GL2	Low-Side MOSFET NL2 Gate-Driver Output
15	GL1	Low-Side MOSFET NL1 Gate-Driver Output
16	GH1	High-Side MOSFET NH1 Gate-Driver Output
17	LX1	Switching Node Connection. LX1 is the internal gate driver's (GH1's) source connection for the high-side MOSFET NH1. LX1 is also the sense input to the current comparators.
18	BST1	Driver Bootstrap Input for High-Side MOSFET NH1. Connect BST1 through a diode to V_{DD} and through a 0.1µF capacitor to LX1 (Figure 1).
19	BST2	Driver Bootstrap Input for High-Side MOSFET NH2. Connect BST2 through a diode to V_{DD} and through a 0.1µF capacitor to LX2 (Figure 1).
20	LX2	Switching Node Connection. LX2 is the internal gate driver's (GH2's) source connection for the high-side MOSFET NH2. LX2 is also the sense input to the current comparators.
21	GH2	High-Side MOSFET NH2 Gate-Driver Output
22	VFB	Lamp Output Feedback Sense Input. The average value on VFB is regulated during startup and open-lamp conditions to 0.5V by controlling the on-time of high-side switches. A capacitive voltage-divider between the CCFL lamp output and GND is sensed to set the maximum average lamp output voltage.
24	IFB	Lamp Current-Sense Input. The voltage on IFB is used to regulate the lamp current. If the IFB input falls below 30% of the LOT voltage for 1.22s, then the MAX8709/MAX8709A activate the lamp-out fault latch.
25	CCI	Current-Loop Compensation Pin. CCI is the output of the current-loop transconductance amplifier (GMI) that regulates the CCFL current. The CCI voltage controls the time interval during which the full bridge applies the input voltage (BATT) to the transformer primary. Connect CCI to GND through a 0.1µF capacitor. CCI is internally discharged to GND in shutdown.

Pin Description (continued)

PIN	NAME	FUNCTION
26	CCV	Voltage-Loop Compensation Pin. CCV is the output of the voltage-loop transconductance amplifier (GMV) that regulates the maximum average secondary transformer voltage. The CCV voltage controls the time interval during which the full bridge applies the input voltage (BATT) to the transformer primary. The CCV capacitor also sets the rise time and fall time of the lamp current in DPWM. Connect CCV to GND with a 6.8nF capacitor. CCV is internally discharged to GND in shutdown.
27	BATT	MAX8709/MAX8709A Supply Input. Input to the internal 5.3V linear regulator (V_{CC}) that provides power to the device. Bypass BATT to GND with a 0.1µF capacitor.
28	V_{CC}	5.3V Linear-Regulator Output. V_{CC} is the supply voltage for the MAX8709/MAX8709A. Bypass V_{CC} to GND with a 0.47µF ceramic capacitor. V_{CC} can also be connected to BATT if V_{BATT} < 5.5V.

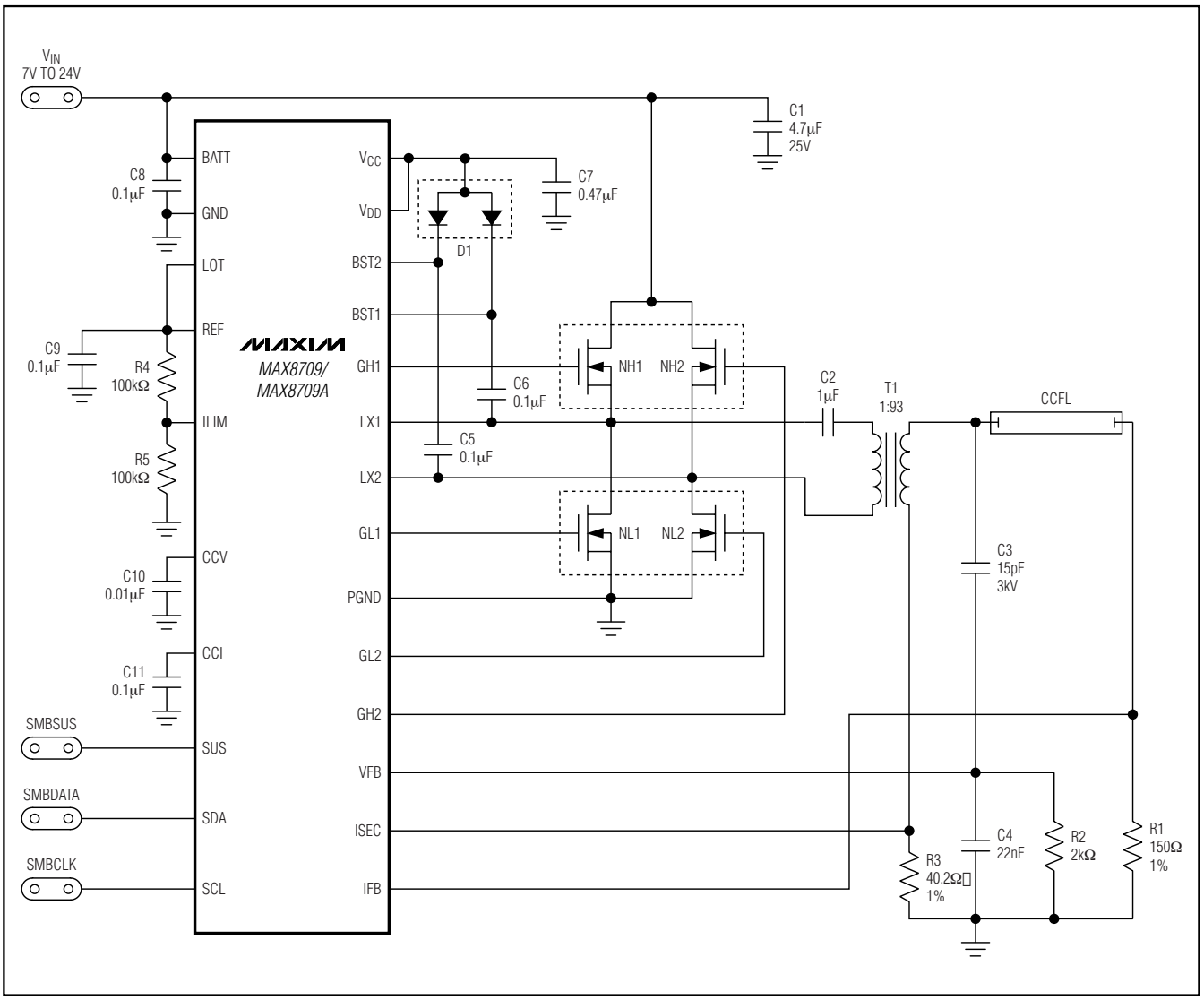


Figure 1. Typical Operating Circuit of the MAX8709/MAX8709A

High-Efficiency CCFL Backlight Controller with SMBus Interface

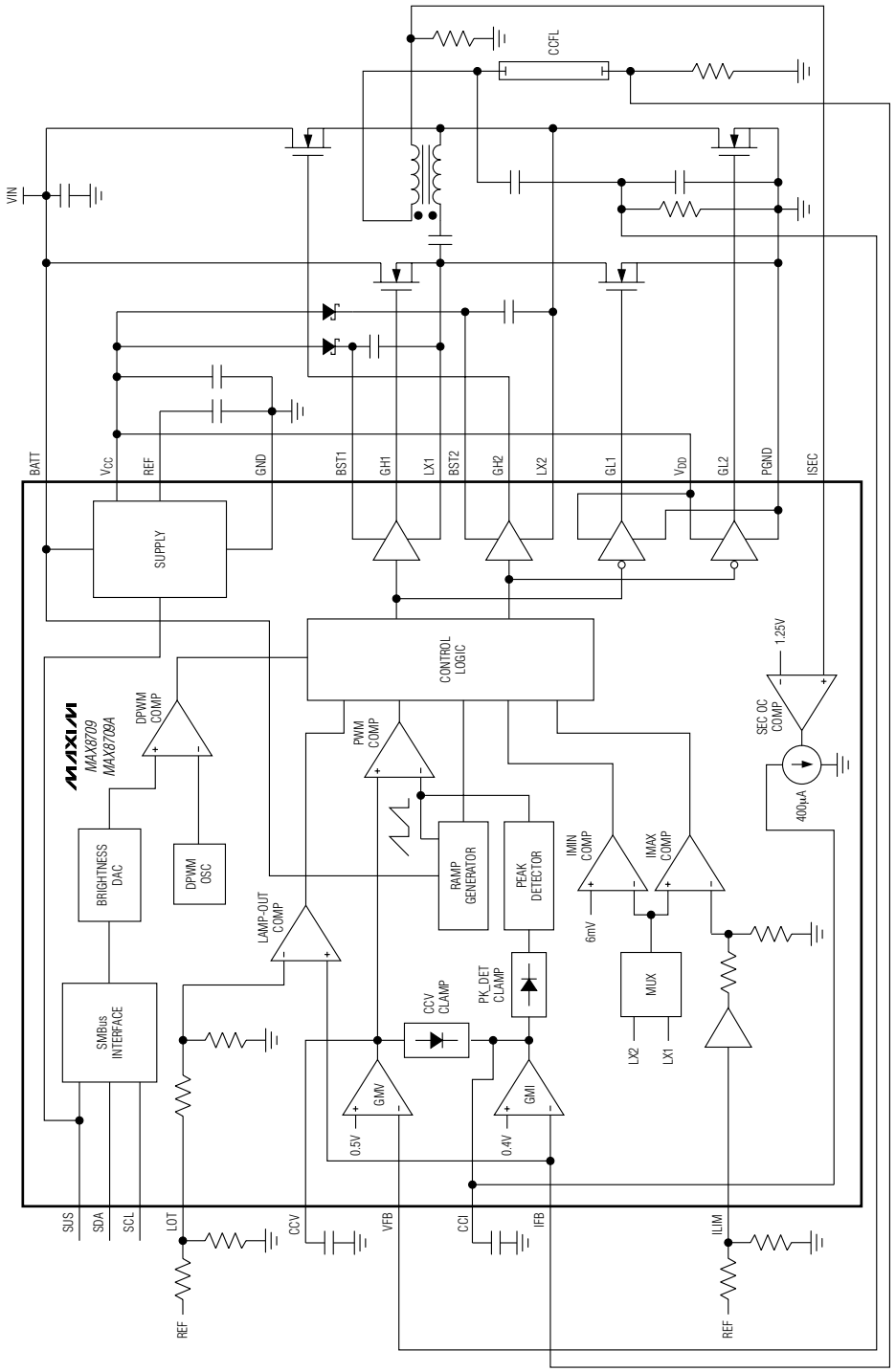


Figure 2. MAX8709/MAX8709A Functional Diagram

Table 1. Component List

DESIGNATION	DESCRIPTION
C1	4.7µF ±20%, 25V X5R ceramic capacitor (1210) Murata GRM32RR61E475K Taiyo Yuden TMK325BJ475MN TDK C3225X7R1E475M
C2	1µF ±10%, 25V X7R ceramic capacitor (1206) Murata GRM31MR71E105K Taiyo Yuden TMK316BJ105KL TDK C3216X7R1E105K
C3	15pF ±1pF, 3kVhigh-voltage ceramic capacitor (1808) Murata GRM42D1X3F150J TDK C4520C0G3F150F
C4	0.022µF ±10%, 16V X7R ceramic capacitor (0402) Murata GRP155R71C223K Taiyo Yuden EMK105BJ223KV TDK C1005X7R1C223K
C5, C6, C8, C9	0.1µF ±10%, 25V X7R ceramic capacitors (0603) Murata GRM188R71E104K Taiyo Yuden TMK107BJ104KA TDK C1608X7R1E104K
C7	0.47µF ±10%, 10V X5R ceramic capacitor (0603) Taiyo Yuden LMK107BJ474KA TDK C1608X5R1A474K
D1	Dual silicon switching diode, common anode (SOT-323) Central Semiconductor CMSD2836 Diodes Incorporated BAW56W
NH1/2, NL1/2	30V, 0.095 dual N-channel MOSFETs (6-pin SOT23) Fairchild FDC6561AN
R1	150Ω ±1% resistor (0603)
R2	2kΩ ±5% resistor (0603)
R3	39Ω ±1% (resistor (0603)
R4, R5	100kΩ ±5% resistors (0603)
T1	CCFL transformer, 1:93 turns ratio Sumida 5371-400-W1423 TOKO T912MG-1018

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
Murata	www.murata.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.components.tdk.com

Typical Operating Circuit

The *Typical Operating Circuit* of the MAX8709/MAX8709A (Figure 1) is a complete CCFL backlight inverter for notebook TFT LCD panels. The circuit works over an input voltage range of 7V to 24V with an RMS lamp current of 6mA. The circuit's maximum RMS open-lamp voltage is limited to 1600V. Table 1 lists recommended component options, and Table 2 lists the component suppliers' contact information.

Detailed Description

The MAX8709/MAX8709A control a full-bridge resonant inverter to convert an unregulated DC input into a near-sinusoidal AC output for powering CCFLs. The lamp brightness is adjusted by turning the lamp on and off with an internal DPWM signal. The duty cycle of the DPWM signal is set through an SMBus-compatible 2-wire serial interface. Figure 2 shows the functional diagram of the MAX8709/MAX8709A.

Resonant Operation

The MAX8709/MAX8709A drive the four N-channel power MOSFETs that make up the zero-voltage-switching (ZVS) full-bridge inverter as shown in Figure 3. Assume that NH1 and NL2 are turned on at the beginning of a switching cycle as shown in Figure 3(a). The primary current flows through MOSFET NH1, DC blocking cap C2, the primary side of transformer T1, and MOSFET NL2. During this interval, the primary current ramps up until the controller turns off NH1. When NH1 turns off, the primary current forward biases the body diode of NL1, which clamps the LX1 voltage just below ground as shown in Figure 3(b). When the controller turns on NL1, its drain-to-source voltage is near zero because its forward-biased body diode clamps the drain. Since NL2 is still on, the primary current flows through NL1, C2, the primary side of T1, and NL2. Once the primary current drops to the minimum current threshold (6mV / $R_{DS(ON)}$), the controller turns off NL2. The remaining energy in T1 charges up the LX2

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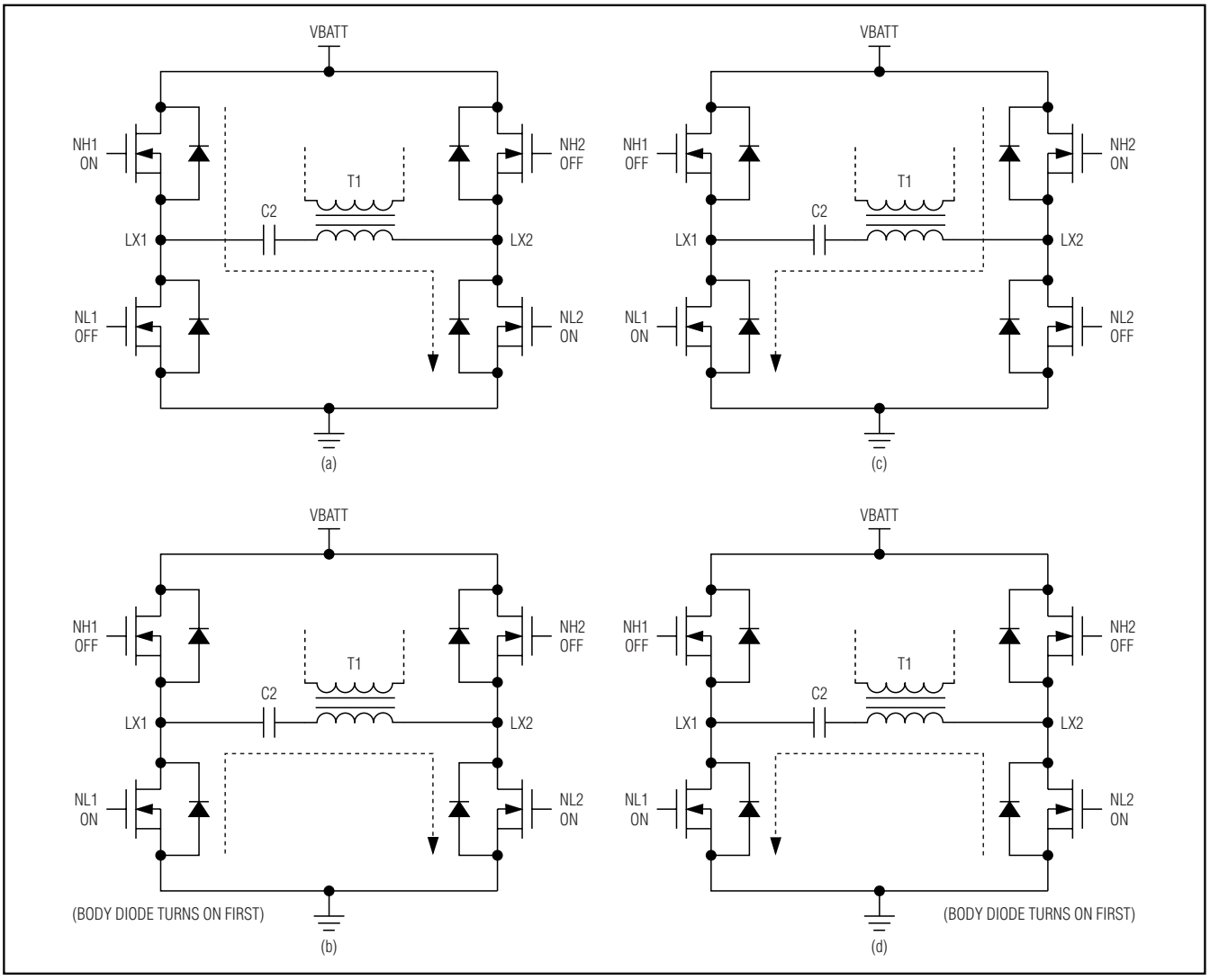

Figure 3. Resonant Operation

node until the body diode of NH2 is forward biased.

When NH2 turns on, it does so with near-zero drain-to-source voltage. The primary current reverses polarity as shown in Figure 3(c), beginning a new cycle with the current flowing in the opposite direction, with NH2 and NL1 on. The primary current ramps up until the controller turns off NH2. When NH2 turns off, the primary current forward biases the body diode of NL2, which clamps the LX2 voltage just below ground as shown in Figure 3(d). After the LX2 node goes low, the controller losslessly turns on NL2. Once the primary current drops to the minimum current threshold, the controller turns off NL1. The remaining energy charges up the LX1 node until the body diode of NH1 is forward biased. Finally, NH1 losslessly turns on, beginning a new cycle as shown in Figure 3(a). Note that switching transitions on all four power MOSFETs occur under ZVS conditions, which reduce transient power losses and EMI.

The simplified CCFL inverter circuit is shown in Figure 4(a). The full-bridge power stage is simplified and represented as a square-wave AC source. The resonant tank circuit can be further simplified to Figure 4(b) by removing the transformer. C_S is the primary series capacitor, C'_S is the series capacitance reflected to the secondary, C_P is the secondary parallel capacitor, N is the transformer turns ratio, L is the transformer sec-

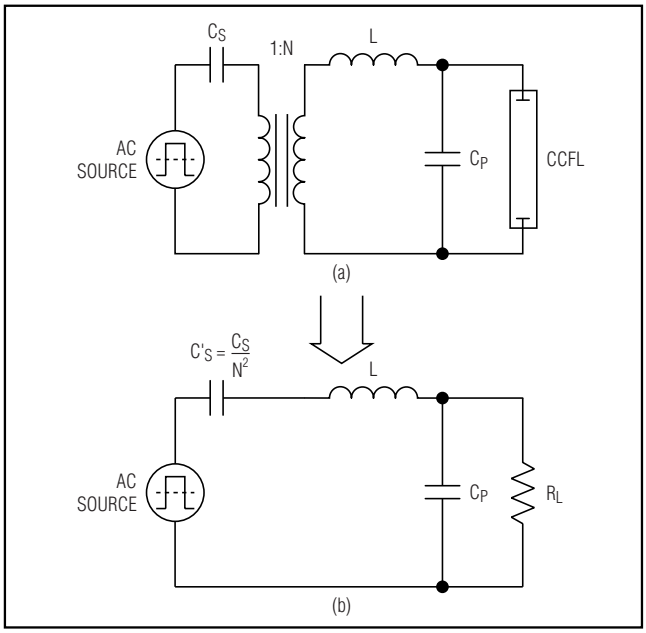

Figure 4. Equivalent Resonant Tank Circuit

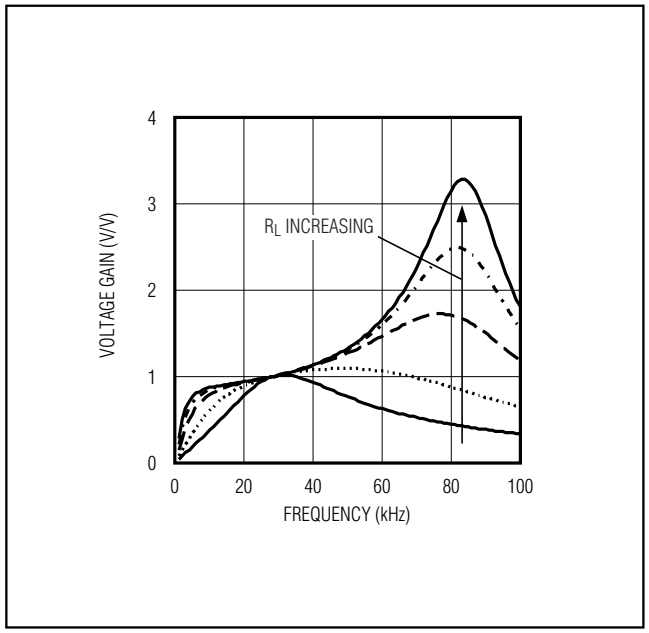

Figure 5. Frequency Response of the Resonant Tank

ondary leakage inductance, and R_L is an idealized resistance that models the CCFL in normal operation.

Figure 5 shows the frequency response of the resonant tank's voltage gain under different load conditions. The primary series capacitor is 1µF, the secondary parallel capacitor is 15pF, the transformer turns ratio is 1:93, and the secondary leakage inductance is 260mH. Notice there are two peaks, f_S and f_P, in the frequency response. The first peak, f_S, is the series resonant peak determined by the reflected series capacitor and the secondary leakage inductance:

$$f_S = \frac{1}{2\pi\sqrt{LC'_S}}$$

The second peak, f_P, is the parallel resonant peak determined by the reflected series capacitor, the parallel capacitor, and the secondary leakage inductance:

$$f_P = \frac{1}{2\pi\sqrt{L\frac{C'_S C_P}{C'_S + C_P}}}$$

These two frequencies set the lower and upper boundaries of resonant operation. When the lamp is off, the operating point of the resonant tank is close to the parallel resonant peak due to the infinite lamp impedance. The circuit displays the characteristics of a parallel-loaded resonant converter, acting like a voltage source to generate the necessary striking voltage. Theoretically, the output voltage of the resonant converter keeps going until the lamp is ionized.

Once the lamp is ionized, the equivalent load resistance decreases rapidly and the operating point moves toward the series resonant peak. The series resonant operation causes the circuit to behave like a current source.

Current and Voltage Control Loops (CCI, CCV)

The MAX8709/MAX8709A use a current loop and a voltage loop to control the power delivered to the CCFL. The current loop is the dominant loop in regulating the lamp current. The voltage loop limits the transformer secondary voltage and is active during startup, the DPWM off-time, and open-lamp fault.

Both the current and the voltage loops use transconductance error amplifiers for regulation. The AC lamp current is measured with a sense resistor in series with the CCFL. The voltage across this resistor is applied to the IFB input and is internally half-wave rectified. The current-loop transconductance error amplifier compares the rectified IFB voltage with a 400mV internal threshold to create an error current. The error current charges and discharges a capacitor connected between CCI and ground to generate an error voltage V_{CCI}. Similarly, the AC voltage across the transformer secondary winding is measured through a capacitive voltage-divider. The sense voltage is applied to the VFB input and is internally half-wave rectified. The volt-

High-Efficiency CCFL Backlight Controller with SMBus Interface

age-loop transconductance error amplifier compares the rectified VFB voltage with a 500mV internal threshold to create an error current. The error current charges and discharges a capacitor connected between CCV and ground to generate an error voltage V_{CCV}. The lower of V_{CCI} and V_{CCV} takes control and is compared with an internal ramp signal to set the high-side MOSFET switch on-time (t_{ON}).

Lamp Startup

A CCFL is a gas discharge lamp that is normally driven in the avalanche mode. To start ionization in a nonionized lamp, the applied voltage (striking voltage) must be increased to the level required for the start of avalanche. The striking voltage can be several times the typical operating voltage.

Because of the resonant topology, the striking voltage is guaranteed regardless of the temperature. Before the lamp is ionized, the lamp impedance is infinite. The transformer secondary leakage inductance and the high-voltage parallel capacitor determine the unloaded resonant frequency. Since the unloaded resonant circuit has a high Q, it is easy to generate high voltages across the lamp.

Operation during startup differs from the steady-state condition described in the *Current and Voltage Control Loops* section. Upon power-up, V_{CCI} slowly rises, increasing the duty cycle, which provides soft-start. During this time, V_{CCV} is limited to 150mV above V_{CCI}. Once the secondary voltage reaches the strike voltage, the lamp current begins to increase. When the lamp current reaches the regulation point, V_{CCI} exceeds V_{CCV} and it reaches steady state.

Feed-Forward Control and Dropout Operation

The MAX8709/MAX8709A are designed to maintain tight control of the transformer secondary under all transient conditions including dropout. The feed-forward control instantaneously adjusts the t_{ON} time for changes in input voltage (V_{BATT}). This feature provides immunity to input voltage variations and simplifies loop compensation over wide input voltage ranges. The feed-forward control also improves the line regulation for short DPWM on-times and makes startup transients less dependent on the input voltage.

Feed-forward control is implemented by increasing the PWM's internal voltage ramp rate for higher V_{BATT}. This has the effect of varying t_{ON} as a function of the input voltage while maintaining about the same signal levels at V_{CCI} and V_{CCV}. Since the required voltage change across the compensation capacitors is minimal, the controller's response to input voltage changes is essentially instantaneous.

To maximize run time, it may be desirable to allow the circuit to operate in dropout if the backlight's performance is not critical. When V_{BATT} is very low, the controller loses current regulation and runs at maximum duty cycle. Under these circumstances, a transient overvoltage condition could occur when the AC adapter is suddenly applied to power the circuit. The feed-forward circuitry minimizes variations in lamp voltage due to such input voltage steps. The regulator also clamps the voltage on V_{CCI}. These two features together ensure that overvoltage transients do not appear on the transformer when leaving dropout.

The V_{CCI} clamp is unique in that it limits V_{CCI} to the peak voltage of the PWM ramp. As the circuit reaches dropout, V_{CCI} approaches the PWM ramp's peak in order to reach maximum t_{ON}. If V_{BATT} decreases further, the control loop loses regulation and V_{CCI} tries to reach its positive supply rail. The clamp on V_{CCI} prevents this from happening and V_{CCI} rides just above the PWM ramp's peak. If V_{BATT} continues to decrease, the feed-forward control reduces the amplitude of the PWM ramp and the clamp pulls V_{CCI} down. When V_{BATT} suddenly steps out of dropout, V_{CCI} is still low and maintains the drive on the transformer at the old dropout level. The control loop then slowly corrects and increases V_{CCI} to bring the circuit back into regulation.

DPWM Dimming Control

The MAX8709/MAX8709A control the brightness of the CCFL by "chopping" the lamp current on and off using an internal DPWM signal. The frequency of the DPWM signal is 210Hz. The brightness code set through the SMBus interface determines the duty cycle of the DPWM signal. A brightness code of 0b00000 corresponds to a 9.375% DPWM duty cycle for MAX8709, and a 12.5% duty cycle for MAX8709A. A brightness code of 0b11111 corresponds to a 100% DPWM duty cycle. The duty cycle changes by 3.125% per step, but codes 0b00000 to 0b00010 all produce 9.375% for MAX8709 as shown in Figure 6. Codes 0b00000 to 0b00011 all produce 12.5% for MAX8709A.

In DPWM operation, the CCI and CCV control loops work together to regulate the lamp current, limit the secondary voltage, and control the rising and falling of the lamp current. During the DPWM off-cycle, the output of the voltage-loop error amplifier (CCV) is set to 1.15V and the current-loop error-amplifier output (CCI) is high impedance. The high-impedance output acts like a sample-and-hold circuit to keep V_{CCI} from changing during the off-cycles. At the beginning of the DPWM on-cycle, V_{CCV}

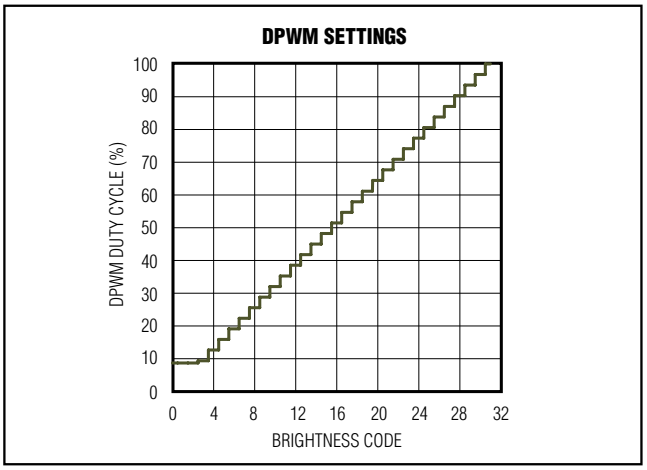

Figure 6. DPWM Settings

linearly rises, gradually increasing t_{ON}, which provides soft-start. Once V_{CCV} exceeds V_{CCI}, the current-loop error amplifier takes control and starts to regulate the lamp current. In the meantime, V_{CCV} continues to rise and is limited to 150mV above V_{CCI}. At the end of the DPWM on-cycle, the CCV capacitor discharges linearly, gradually decreasing t_{ON} and providing soft-stop.

POR and UVLO

The MAX8709/MAX8709A include power-on-reset (POR) and undervoltage-lockout (UVLO) circuits. The POR resets all internal registers such as DAC outputs, fault latches, and all SMBus registers. POR occurs when V_{CC} is below 1.5V. The SMBus input logic thresholds are only guaranteed to meet electrical characteristic limits for V_{CC} as low as 3.5V, but the interface continues to function down to the POR threshold.

The UVLO is activated and disables both high-side and low-side switch drivers when V_{CC} is below 4.2V (typ).

Low-Power Shutdown (SUS)

When the MAX8709/MAX8709A are placed in shutdown, all functions of the IC are turned off except for the 5.3V linear regulator that powers all internal registers and the SMBus interface. The SMBus interface is accessible in shutdown. In shutdown, the linear-regulator output voltage drops to about 4.5V and the supply current is 6µA (typ), which is the required power to maintain all internal register states. While in shutdown, lamp-out detection and short-circuit detection latches are reset. The device can be placed into shutdown either by writing to the shutdown-mode register or pulling SUS low.

Lamp-Out Protection

For safety, the MAX8709/MAX8709A monitor the lamp-current feedback (IFB) to detect faulty or open CCFL tubes and secondary short circuits in the lamp and IFB sense resistor. If the voltage on IFB is continuously below 30% of the LOT voltage for greater than 1.22s (typ), the MAX8709/MAX8709A latch off the full bridge. Unlike the normal shutdown mode, the linear-regulator output (V_{CC}) remains at 5.3V. Toggling SUS or cycling the input power reactivates the device.

During the 1.22s delay, V_{CCI} slowly rises, increasing t_{ON} in an attempt to maintain lamp current regulation. As V_{CCI} rises, V_{CCV} rises with it until the secondary voltage reaches its preset limit. At this point, V_{CCV} stops and limits the secondary voltage by limiting t_{ON}. Because V_{CCV} is limited to 150mV above V_{CCI}, the voltage control loop is able to quickly limit the secondary voltage. Without this clamping feature, the transformer voltage overshoots to dangerous levels because V_{CCV} takes time to slew down from its supply rail.

Primary Overcurrent Protection (ILIM)

The MAX8709/MAX8709A sense primary current in each switching cycle. When the regulator turns on the low-side MOSFET, a comparator monitors the voltage drop from LX_ to GND. If the voltage exceeds the current-limit threshold, the regulator turns off the high-side switch at the opposite side of the primary to prevent the transformer primary current from increasing further.

The current-limit threshold can be adjusted using the ILIM input. Connect a resistive voltage-divider between REF or V_{CC} and GND with the midpoint connected to ILIM. The current-limit threshold measured between LX_ and GND is 1/5th the voltage at ILIM. The ILIM adjustment range is 0 to 3V. Connect ILIM to V_{CC} to select the default current-limit threshold of 0.2V.

Secondary Current Limit (ISEC)

The secondary current limit provides failsafe current limiting in case a failure, such as a short circuit or leakage from the lamp high-voltage terminal to ground, prevents the CCI current control loop from functioning properly. ISEC monitors the voltage across a sense resistor placed between the transformer's low-voltage secondary terminal and ground. The ISEC voltage is internally half-wave rectified and continuously compared to the ISEC regulation threshold (1.25V typ). Any time the ISEC voltage exceeds the threshold, a controlled current is drawn from CCI to reduce the on-time of the bridge's high-side switches.

Reference Output (REF)

The reference output is nominally 2V, and can source at least 40µA (see the *Typical Operating Characteristics*).

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Write-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are writing to

Data Byte: data goes into the register set by the command byte

Read-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	

Slave Address

Command Byte: selects which register you are reading from

Slave Address: repeated due to change in data-flow direction

Data Byte: reads from the register set by the command byte

Send-Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	P
	7 bits	1b	1b	8 bits	1b	

Command Byte: sends command with no data; usually used for one-shot command

Receive-Byte Format

S	ADDRESS	RD	ACK	DATA	///	P
	7 bits	1b	1b	8 bits	1b	

Slave Address

Data Byte: reads data from the register commanded by the last read-byte or write-byte transmission; also used for SMBus Alert Response return address

S = Start condition
P = Stop condition

Shaded = Slave transmission
Ack= Acknowledged = 0
/// = Not acknowledged = 1

WR = Write = 0
RD = Read =1

Figure 7. SMBus Protocols

Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

Linear-Regulator Output (VCC)

The internal linear regulator steps down the DC input voltage to 5.3V (typ). The linear regulator supplies power to the internal control circuitry of the MAX8709/MAX8709A and can also be used to power the MOSFET drivers by connecting V_{CC} directly to V_{DD}. The V_{CC} voltage drops to 4.5V in shutdown.

SMBus Interface (SDA, SCL)

The MAX8709/MAX8709A support an Intel SMBus-compatible 2-wire digital interface. SDA is the bidirectional data line and SCL is the clock line of the 2-wire interface corresponding respectively to SMBDATA and SMBCLK lines of the SMBus. SDA and SCL are Schmidt-triggered inputs that can accommodate slow edges; however, the rising and falling edges should still be faster than 1µs and 300ns, respectively. The MAX8709/MAX8709A use the write-byte, read-byte, and receive-byte protocols (Figure 7). The SMBus protocols are documented in *System Management Bus Specification V1.1* and are available at http://www.SMBus.org/.

The MAX8709/MAX8709A are slave-only devices and respond to the 7-bit address 0b01011000 (i.e., with the R/$\overline{W}$ bit clear indicating a write, this corresponds to 0x58). The MAX8709/MAX8709A have three functional registers: a 5-bit brightness register (BRIGHT4–BRIGHT0), a 3-bit shutdown-mode register (SHMD2–SHMDE0), and a 2-bit status register (STATUS1–STATUS0). In addition, the device has three identification (ID) registers: an 8-bit chip ID register, an 8-bit chip revision register, and an 8-bit manufacturer ID register.

Communication starts with the master signaling the beginning of a transmission with a START condition, which is a high-to-low transition on SDA while SCL is high. When the master has finished communicating with the slave, the master issues a STOP condition, which is a low-to-high transition on SDA while SCL is high. The bus is then free for another transmission. Figures 8 and 9 show the timing diagrams for signals on the 2-wire interface. The address byte, command byte, and data byte are transmitted between the START and STOP conditions. The SDA state is allowed to change only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit words and is sampled on the

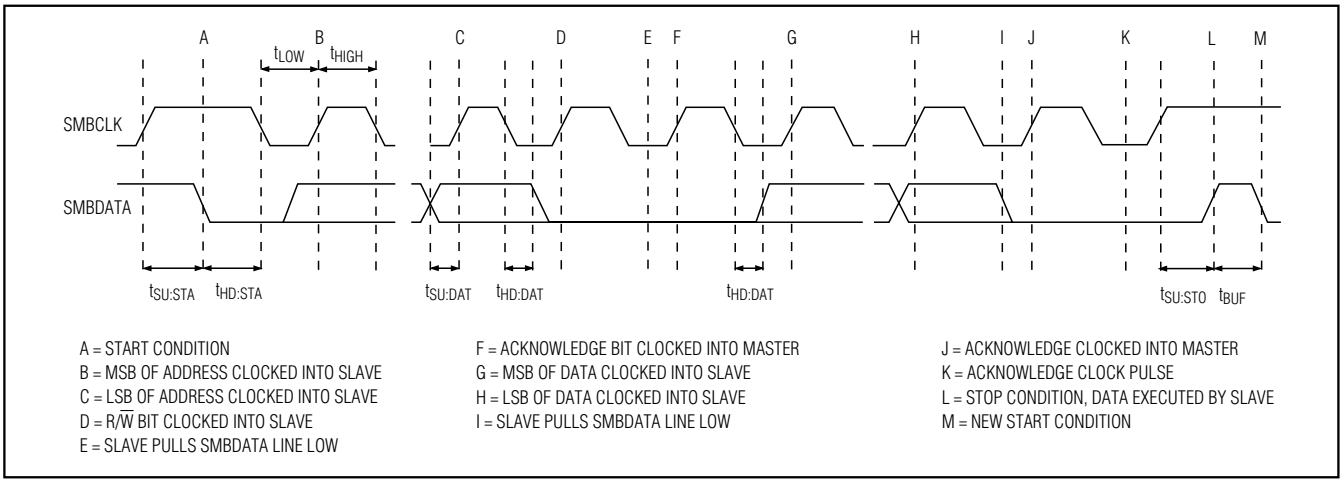

Figure 8. SMBus Write Timing

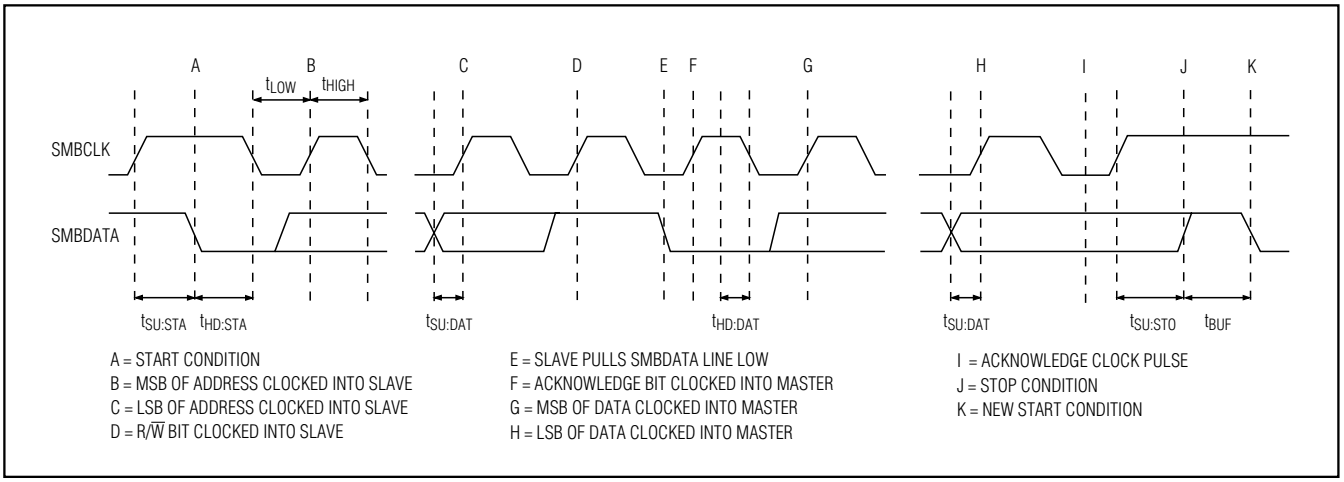

Figure 9. SMBus Read Timing

rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the MAX8709/MAX8709A since either the master or the slave acknowledges the receipt of the correct byte during the ninth clock. If the MAX8709/MAX8709A receive the correct slave address followed by R/$\overline{W}$ = 0, it expects to receive 1 or 2 bytes of information (depending on the protocol). If the device detects a START or STOP condition prior to clocking in the bytes of data, it considers this an error condition and disregards all of the data.

If the transmission is completed correctly, the registers are updated immediately after a STOP (or RESTART) condition. If the MAX8709/MAX8709A receives its correct slave address followed by R/$\overline{W}$ = 1, it expects to clock out the register data selected by the previous command byte.

SMBus Commands

The MAX8709/MAX8709A registers are accessible through several different redundant commands (i.e., the command byte in the read-byte and write-byte protocols), which can be used to read or write the brightness, SHMD, status, or ID registers.

Table 3 summarizes the command byte's register assignments, as well as each register's power-on state.

High-Efficiency CCFL Backlight Controller with SMBus Interface

Table 3. Commands Description

SMBus PROTOCOL	COMMAND BYTE*	POR STATE	DATA REGISTER BIT ASSIGNMENT							
			BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Read and Write	0x01 0b0XXX XX01	0x17	0	0	0	BRIGHT4 (MSB)	BRIGHT3	BRIGHT2	BRIGHT1	BRIGHT0 (LSB)
Read and Write	0x02 0b0XXX XX10	0xF9	STATUS1	STATUS0	1	1	1	SHMD2	SHMD1	SHMD0
Read Only	0x03 0b0XXX XX11	0x0C	ChipID7 0	ChipID6 0	ChipID5 0	ChipID4 0	ChipID3 1	ChipID2 1	ChipID1 0	ChipID0 1
Read Only	0x04 0b0XXX XX00	0x00	ChipRev7 0	ChipRev6 0	ChipRev5 0	ChipRev4 0	ChipRev3 0	ChipRev2 0	ChipRev1 0	ChipRev0 0
Read and Write	0xAA 0b10XX XXX0	0x40	$\overline{\text{BRIGHT4}}$ (MSB)	$\overline{\text{BRIGHT3}}$	$\overline{\text{BRIGHT2}}$	$\overline{\text{BRIGHT1}}$	$\overline{\text{BRIGHT0}}$ (LSB)	0	$\overline{\text{STATUS1}}$	$\overline{\text{STATUS0}}$
Read and Write	0XA9 0b10XX XXX1	0x40	$\overline{\text{BRIGHT4}}$ (MSB)	$\overline{\text{BRIGHT3}}$	$\overline{\text{BRIGHT2}}$	$\overline{\text{BRIGHT1}}$	$\overline{\text{BRIGHT0}}$ (LSB)	0	$\overline{\text{STATUS1}}$	$\overline{\text{STATUS0}}$
Read Only	0xFE 0b11XX XXX0	0x4D	MfgID7 0	MfgID6 1	MfgID5 0	MfgID4 0	MfgID3 1	MfgID2 1	MfgID1 0	MfgID0 1
Read Only	0xFF 0b11XX XXX1	0x0C	ChipID7 0	ChipID6 0	ChipID5 0	ChipID4 0	ChipID3 1	ChipID2 1	ChipID1 0	ChipID0 1

**The hexadecimal command byte shown is recommended for maximum forward compatibility with future products.*
X = Don't care.

Table 4. SHMD Register Bit Descriptions

BIT	NAME	POR STATE	DESCRIPTION
2	SHMD2	0	SHMD2 = 1 forces the lamp off and sets STATUS1. SHMD2 = 0 allows the lamp to operate, although it may still be shut down by SUS (depending on the state of SHMD1 and SHMD0).
1	SHMD1	0	When SUS = 0, this bit has no effect. SUS = 1 and SHMD1 = 1 forces the lamp off and sets STATUS1. SUS = 1 and SHMD1 = 0 allows the lamp to operate, although it may still be shut down by the SHMD2 bit.
0	SHMD0	1	When SUS = 1, this bit has no effect. SUS = 0 and SHMD0 = 1 forces the lamp off and sets STATUS1. SUS = 0 and SHMD0 = 0 allows the lamp to operate, although it may still be shut down by the SHMD2 bit.

The MAX8709/MAX8709A also support the receive-byte protocol for quicker data transfers. This protocol accesses the register configuration pointed to by the last command byte. Immediately after power-up, the data byte returned by the receive-byte protocol is the inverted contents of the brightness register, left justified (i.e., $\overline{\text{BRIGHT4}}$ is in the most-significant-bit position of the data byte) with the 3 remaining bits containing a one, $\overline{\text{STATUS1}}$, and $\overline{\text{STATUS0}}$. This gives the same result as using the read-word protocol with 0b10XXXXXX (0xAA and 0xA9) command. Use caution with the shorter protocols in multimaster systems, since a second master could overwrite the command byte without informing the first master. During shutdown the serial interface remains fully functional.

Table 5. SUS and SHMD Register Truth Table

SUS	SHMD2	SHMD1	SHMD0	OPERATING MODE
0	0	X	0	Operate
0	0	X	1	Shutdown, STATUS1 set
1	0	0	X	Operate
1	0	1	X	Shutdown, STATUS1 set
X	1	X	X	Shutdown, STATUS1 set

X = Don't care.

Brightness Register [BRIGHT4 – BRIGHT0] (POR = 0b10111)

The 5-bit brightness register corresponds to the 5-bit brightness code used in dimming control (See the *Dimming Control* section). BRIGHT4 - BRIGHT0 = 0b11111 sets minimum brightness and BRIGHT4 - BRIGHT0 = 0b00000 sets maximum brightness. Note that the brightness-register polarity of command bytes 0xA9 and 0xAA are inverted from that of command byte 0x01.

Shutdown-Mode Register [SHMD2–SHMD0] (POR = 0b001)

The 3-bit shutdown-mode register configures the operation of the device when the SUS pin is toggled as described in Table 4. The shutdown-mode register can also be used to directly shut off the CCFL regardless of the state of SUS (Table 5).

Status Register [STATUS1–STATUS0] (POR = 0b11)

The status register returns information on fault conditions. If the MAX8709/MAX8709A detect that V_{IFB} does not exceed 30% of V_{LOT} continuously for 1.22s, the IC latches STATUS1 to zero. STATUS1 is reset to 1 by toggling SUS or by toggling the input power.

STATUS0 reports 1 as long as no overcurrent conditions are detected. If an overcurrent condition is detected in any given digital PWM period, STATUS0 is cleared for the duration of the following digital PWM period. If an overcurrent condition is not detected in any given digital PWM period, STATUS0 is set for the duration of the following digital PWM period. Note that the status-register polarity of command bytes 0xA9 and 0xAA are inverted from that of command byte 0x02.

ID Registers

The ID registers return information on the manufacturer chip ID and the chip revision number. The MAX8709/MAX8709A are the first-generation advanced CCFL controller and its ChipRev is 0x00. Reading from MfgID register returns 0x4D, which is the ASCII code for M (for Maxim). The ChipID register returns 0x0D. Writing to these registers has no effect.

Applications Information

To select the correct component values for the MAX8709/MAX8709A, several CCFL parameters must be specified. (Table 7)

MOSFETs

The MAX8709/MAX8709A require four external N-channel power MOSFETs (NL1, NL2, NH1, and NH2) to form a full-bridge inverter circuit to drive the transformer primary. The regulator senses the on-state drain-to-source voltage of the two low-side MOSFETs NL1 and NL2 to detect the transformer primary current, so the $R_{DS(ON)}$ of NL1 and NL2 should be matched. For instance, if dual MOSFETs are used to form the full bridge, NL1 and NL2 should be in one package. Select dual logic-level N-channel MOSFETs with low $R_{DS(ON)}$ to minimize conduction loss for NL1/NL2 and NH1/NH2. The regulator utilizes the energy stored in the transformer's primary leakage inductance to softly turn on each of four switches in the full bridge zero voltage switching (ZVS) occurs when the external power MOSFETs are turned on when their respective drain-to-source voltages are near 0V. ZVS effectively eliminates the instantaneous turn-on loss of MOSFETs caused by C_{OSS} (drain-to-source capacitance) and parasitic capacitance discharge, and improves efficiency and reduces switching-related EMI.

Table 6. Status-Register Bit Descriptions (Read Only, Writes Have No Effect)

BIT	NAME	POR STATE	DESCRIPTION
1	STATUS1	1	STATUS1 = 0 (or $\overline{STATUS1}$ = 1) means that a lamp-out condition has been detected. The STATUS1 bit stays clear even after the lamp-out condition has gone away. The only way to set STATUS1 is to shut off the lamp by programming the shutdown-mode register or by toggling SUS.
0	STATUS0	1	STATUS0 = 0 (or $\overline{STATUS0}$ = 1) means that an overcurrent condition was detected during the previous digital PWM period. STATUS0 = 1 means that an overcurrent condition was not detected during the previous digital PWM period.

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Setting the Lamp Current

The MAX8709/MAX8709A sense the lamp current flowing through a resistor R1 (Figure 1) connected between the low-voltage terminal of the lamp and ground. The voltage across R1 is fed to IFB and is internally rectified. The MAX8709/MAX8709A control the desired lamp current by regulating the average of the half-wave rectified IFB voltage. To set the RMS lamp current, determine R1 as follows:

$$R1 = \frac{\pi \times 400mV}{\sqrt{2} \times I_{LAMP(RMS)}}$$

where $I_{LAMP(RMS)}$ is the desired RMS lamp current and 400mV is the typical value of the IFB regulation point specified in the *Electrical Characteristics* table. To set the RMS lamp current to 6mA, the value of R1 should be 148Ω. The closest standard 1% resistors are 147Ω and 150Ω. The precise shape of the lamp-current waveform, which is dependent on lamp parasitics, influences the actual RMS lamp current. Use a true RMS current meter to make final adjustments to R1.

Setting the Secondary Voltage Limit

The MAX8709/MAX8709A limit the transformer secondary voltage during lamp striking and lamp-out faults. The secondary voltage is sensed through the capacitive voltage-divider formed by C3 and C4 (Figure 1). The voltage on VFB is proportional to the CCFL voltage. The selection of the parallel resonant capacitor C3 is described in the *Transformer Design and Resonant Component Selection* section. C3 is usually between 10pF to 22pF. After the value of C3 is determined, select C4 using the following equation to set the desired maximum RMS secondary voltage $V_{LAMP(RMS)\_MAX}$:

$$C4 = \left(\frac{\sqrt{2} \times V_{LAMP(RMS)\_MAX}}{\pi \times 510mV} - 1 \right) \times C3$$

where 510mV is the typical value of the VFB regulation threshold specified in the *Electrical Characteristics* table. If C3 is 15pF, C4 needs to be 21.2nF to set the desired maximum RMS secondary voltage to 1600V. The closest standard value of C4 is 22nF.

The resistor R2 is used to set the VFB DC bias point to 0V. Choose the value of R2 as follows:

$$R2 = \frac{10}{2\pi \times f_{SW} \times C4}$$

where f_{SW} is the nominal resonant operating frequency.

Setting the Secondary Current Limit

The MAX8709/MAX8709A limit the secondary current even if the IFB sense resistor is shorted or transformer secondary current finds its way to ground without passing through R1. ISEC monitors the voltage across the sense resistor R3 connected between the low-voltage terminal of the transformer secondary winding and ground. Determine the value of R3 using the following equation:

$$R3 = \frac{1.25V}{\sqrt{2} \times I_{SEC(RMS)\_MAX}}$$

where $I_{SEC(RMS)\_MAX}$ is the desired maximum RMS transformer secondary current during fault conditions, and 1.25V is the typical value of the ISEC regulation point specified in the *Electrical Characteristics* table.

Transformer Design and Resonant Component Selection

The transformer is the most important component of the resonant tank circuit. The first step in designing the transformer is to determine the transformer turns ratio. The ratio must be high enough to support the CCFL operating voltage at the minimum supply voltage. The transformer turns-ratio N can be calculated as follows:

$$N = \frac{V_{LAMP(RMS)}}{0.9 \times V_{IN(MIN)}}$$

where $V_{LAMP(RMS)}$ is the maximum RMS lamp voltage in normal operation, and $V_{IN(MIN)}$ is the minimum DC input voltage.

The next step in the design procedure is to determine the desired operating frequency range. The MAX8709/MAX8709A are synchronized to the natural resonant frequency of the resonant tank. The resonant frequency changes with operating conditions, such as the input voltage, lamp impedance, etc. Therefore, the switching frequency varies over a certain range. To ensure reliable operation, the resonant frequency range must be within the operating frequency range specified by the CCFL lamp transformer manufacturers. As discussed in the *Resonant Operation* section, the resonant frequency range is determined by the transformer secondary leakage inductance L, the primary series DC-blocking capacitor C2, and the secondary parallel resonant capacitor C3. Since it is difficult to control the transformer leakage inductance, the resonant tank design should be based on the existing secondary leakage inductance of the selected CCFL transformer. The leakage inductance values usually have large tolerance and significant variations among different batches. It is best to work directly with transformer vendors

Table 7. CCFL Specifications

SPECIFICATION	SYMBOL	UNITS	DESCRIPTION
CCFL Minimum Striking Voltage (Kick-Off Voltage)	V_{STRIKE}	V_{RMS}	Although CCFLs typically operate at less than $550V_{RMS}$, a higher voltage ($1000V_{RMS}$ and up) is required initially to start the tube. The strike voltage is typically higher at cold temperatures and at the end of life of the tube. Resonant operation and the high Q of the resonant tank generate the required strike voltage of the lamp.
CCFL Typical Operating Voltage (Lamp Voltage)	V_{LAMP}	V_{RMS}	Once a CCFL has been struck, the lamp voltage required to maintain light output falls to approximately $550V_{RMS}$. Short tubes may operate on as little as $250V_{RMS}$. The operating voltage of the CCFL stays relatively constant, even as the tube's brightness is varied.
CCFL Operating Current (Lamp Current)	I_{LAMP}	mA_{RMS}	The desired RMS AC current through a CCFL is typically $6mA_{RMS}$. DC current is not allowed through CCFLs. The sense resistor, R1, sets the lamp current.
CCFL Maximum Frequency (Lamp Frequency)	f	kHz	The maximum AC-lamp-current frequency. The circuit should be designed to operate the lamp below this frequency. The MAX8709/MAX8709A are designed to operate between 20kHz and 100kHz.

on leakage inductance requirements. The MAX8709/MAX8709A work best when the secondary leakage inductance is between 250mH and 350mH. The series capacitor C2 sets the minimum operating frequency, which is approximately two times the series resonant peak frequency. Choose:

$$C2 \le \frac{N^2}{\pi^2 \times f^2_{MIN} \times L}$$

where f_{MIN} is the minimum operating frequency range. The parallel capacitor C3 sets the maximum operating frequency, which is also the parallel resonant peak frequency. Choose:

$$C3 \ge \frac{C2}{(4\pi^2 \times f^2_{MAX} \times L \times C2) - N^2}$$

The transformer core saturation also needs to be considered when selecting the operating frequency. The primary winding should have enough turns to prevent transformer saturation under all operating conditions. Use the following expression to calculate the minimum number of turns (N1) of the primary winding:

$$N1 > \frac{D_{MAX} \times V_{IN(MAX)}}{B_S \times S \times f_{MIN}}$$

where D_{MAX} is the maximum duty cycle (approximately 0.8) of the high-side switches, $V_{IN(MAX)}$ is the maximum DC input voltage, B_S is the saturation flux density of the core, and S is the minimal cross-section area of the core.

Compensation Design

The CCI capacitor sets the speed of the current loop that is used during startup, maintaining lamp current regulation, and during transients caused by changing the input voltage. The typical CCI value is 0.1µF. Larger values increase the transient-response delays. Smaller values speed up transient response, but extremely small values can cause loop instability.

The CCV capacitor sets the speed of the voltage loop that affects soft-start and soft-stop during DPWM operation, and voltage loop stability during startup and open-lamp conditions. The typical CCV capacitor value is 10nF. Use the smallest value of CCV that gives an acceptable fault transient response and does not cause excessive ringing at the beginning of a DPWM pulse.

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Larger CCV values reduce transient overshoot but can reduce light output at low-DPWM duty cycles by increasing the time required to reach the tube strike voltage.

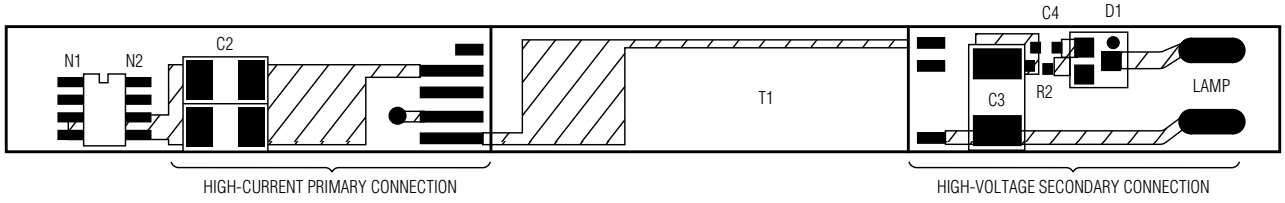
Other Components

The external bootstrap circuits formed by D1 and C5/C6 in Figure 1 power the high-side MOSFET drivers. Connect BST1/BST2 through a signal-level silicon diode to V_{DD}, and bypass it to LX1/LX2 with a 0.1µF ceramic capacitor.

Layout Guidelines

Careful PC board layout is critical to achieve stable operation. The high-voltage section and the switching section of the circuit require particular attention. The high-voltage sections of the layout need to be well separated from the control circuit. Most layouts for single-lamp notebook displays are constrained to the long and narrow form factor, so this separation occurs naturally. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation, and high efficiency.
2) Utilize a star-ground configuration for power and analog grounds. The power and analog grounds should be completely isolated—meeting only at the center of the star. The center should be placed at the exposed backside pad to the QFN package. Using separate copper islands for these grounds may simplify this task. Quiet analog ground is used for REF, CCV, CCI, and ILIM (if a resistive voltage-divider is used).
3) Route high-speed switching nodes away from sensitive analog areas (CCI, CCV, REF, V_{FB}, I_{FB}, I_{SEC}, ILIM). Make all pin-strap control input connections (ILIM, etc.) to analog ground or V_{CC} rather than power ground or V_{DD}.
4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.
5) The current-sense paths for LX1 and LX2 to GND must be made using Kelvin-sense connections to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting GND and LX inside (underneath) the 8-pin SO package.
6) Ensure the feedback connections are short and direct. To the extent possible, IFB, VFB, and ISEC connections should be far away from the high-voltage traces and the transformer.
7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent lossy capacitive coupling.
8) The traces to the capacitive voltage-divider on the transformer's secondary need to be widely separated to prevent arcing. Moving these traces to opposite sides of the board can be beneficial in some cases (see Figure 10).

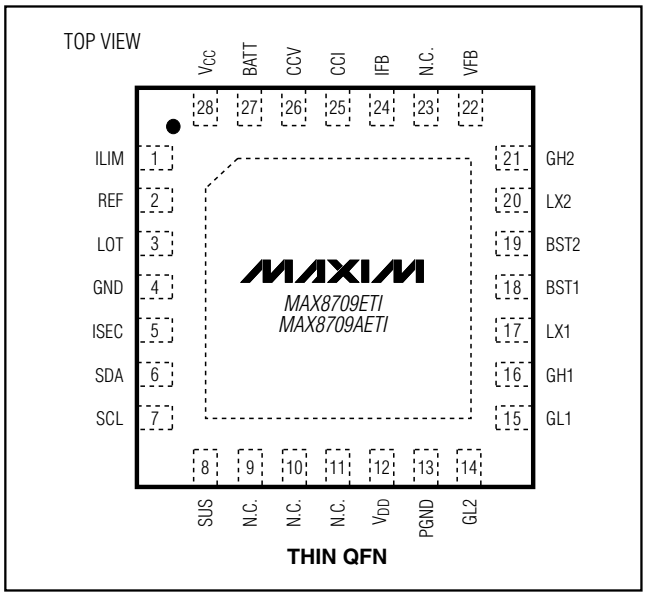


NOTE: DUAL MOSFET N2 IS MOUNTED ON THE BOTTOM SIDE OF THE PC BOARD DIRECTLY UNDER N1.

Figure 10. High-Voltage Components Layout Example

High-Efficiency CCFL Backlight Controller with SMBus Interface

Pin Configuration



THIN QFN

Chip Information

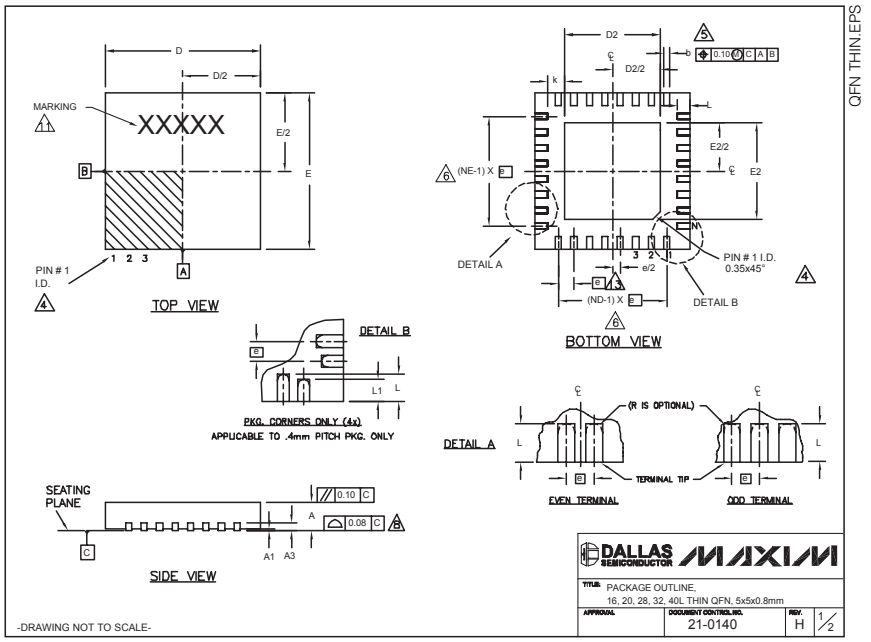
TRANSISTOR COUNT: 7116

PROCESS: BiCMOS

High-Efficiency CCFL Backlight Controller with SMBus Interface

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm
21-0140
H
2/2

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