ecoSwitch™
Advanced Load Management

Controlled Load Switch with Low R_{ON}

NCP45610

The NCP45610 series of load management devices provide a component and area−reducing solution for efficient power domain switching with inrush current limit via soft start. These devices are designed to integrate control and driver functionality with a high performance low on−resistance power MOSFET in a single package offering safeguards and monitoring via fault protection and power−good signaling. This cost effective solution is ideal for power management and disconnect functions in USB ports and power management applications requiring low power consumption in a small footprint.

Features

- Advanced Controller with Charge Pump
- Integrated N−Channel MOSFET with Low R_{ON}
- Soft−Start via Controlled Slew Rate
- Adjustable Slew Rate Control
- Power Good Output
- Thermal Shutdown
- Under Voltage Lockout
- Over Current Protection
- Input Voltage Range 1 V to 13.5 V
- Extremely Low Standby Current
- Load Bleed (Quick Discharge)
- This is a Pb−free Device

Typical Applications

- Notebook and Tablet Computers
- Handheld & Mobile Electronics
- Portable Medical Devices
- Hard Drives
- Peripheral Ports

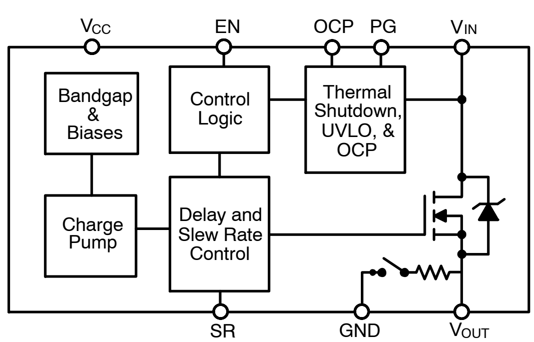


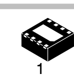
Figure 1. Block Diagram

ON Semiconductor®

www.onsemi.com

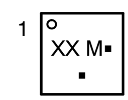
R_{ON} TYP	V_{CC}	V_{IN}	DC I_{MAX}
14.0	3.3 V	1.0 V	8 A
14.5	3.3 V	5 V	
15.9	3.3 V	12 V	

*IMAX is defined as the maximum steady state current the load switch can pass at room ambient temperature without entering thermal lockout.



DFN8, 2x2
CASE 506CN

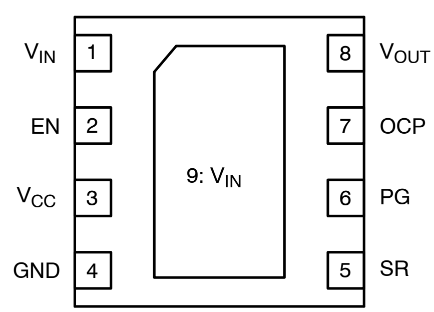
MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION
2x2 DFN



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP45610IMNTWG	DFN8	TBD

Table 1. PIN DESCRIPTION

Pin	Name	Function
1, 9	V_{IN}	Input voltage (1 V – 13.5 V)
2	EN	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to GND.
3	V_{CC}	Driver supply voltage (3.0 V – 5.5 V)
4,	GND	Driver ground
5	SR	Slew rate adjustment made with an external capacitor to GND; float if not used
6	PG	Power Good Output; Open drain, should be tied to VCC with a pullup resistor (100kΩ typical)
7	OCP	Over−current protection trip point adjustment made with a voltage applied (1 V – 1.2 V), pin has an internal pull up resistor to EN; float if over−current protection is needed
8	V_{OUT}	Source of MOSFET connected to load. Includes an internal bleed resistor to GND.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
Input Voltage Range	V_{IN}	−0.3 to 18	V
Output Voltage Range	V_{OUT}	−0.3 to 18	V
EN Input Voltage Range	V_{EN}	−0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 2)	V_{PG}	−0.3 to 6	V
OCP Input Voltage Range	V_{OCP}	−0.3 to 6	V
Thermal Resistance, Junction−to−Ambient, Steady State (Note 1)	$R_{\theta JA}$	59.9	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	7.9	°C/W
Continuous MOSFET Current @ T_A = 25°C (Note 1)	I_{MAX}	24	A
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above T_A = 25°C	P_D	3.49 34.9	W mW/°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Note 3 and 4)	ESD_{HBM}	2.0	kV
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	1.0	kV
Latch−up Current Immunity (Note 3 and 4)	LU	100	mA
OFF to ON Transition Energy Dissipation Limit (See application section)	E_{TRANS}	50	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
2. PG is an open−drain output that requires an external pull−up resistor > 1 kΩ to an external voltage source.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78
4. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3	5.5	V
Input Voltage	V_{IN}	1	13.5	V
OCP Input Voltage	V_{OCP}	0	1	V
Ground	GND		0	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
MOSFET						
On−Resistance	V_{CC} = 3.3 V; V_{IN} = 1 V	R_{ON}		14.0	16.5	mΩ
	V_{CC} = 3.3 V; V_{IN} = 5 V			14.5	17	
	V_{CC} = 3.3 V; V_{IN} = 12 V			15.9	18.5	
	V_{CC} = 3.3 V; V_{IN} = 13.5 V			17.4	21	
Leakage Current (Note 5)	V_{EN} = 0 V; V_{IN} = 13.5 V	I_{LEAK}		10	100	nA
CONTROLLER						
Supply Standby Current (Note 6)	V_{EN} = 0 V	I_{STBY}		2.7	5	μA
Supply Dynamic Current (Note 7)	V_{EN} = V_{CC} = 3 V; V_{IN} = 12 V	I_{DYN}		430	750	μA
	V_{EN} = V_{CC} = 5.5 V; V_{IN} = 1 V			800	1000	
Internal Load Bleed Resistance (Note 8)	V_{EN} = 0 V	R_{BLEED}	300	600	1000	Ω
Internal Bleed Leakage Current		I_{BLEED}		14	80	μA
EN Input High Voltage		V_{IH}	2			V
EN Input Low Voltage		V_{IL}			0.8	V
EN Pull Down Resistance		R_{PD}	80	100	120	kΩ
PG Output Low Voltage	I_{SINK} = 5 mA	V_{OL}		0.13	0.2	V
PG Output Leakage Current	V_{TERM} = 3.3 V	I_{OH}		5	100	nA
Slew Rate Control Constant (Note 9)	V_{IN} = 5 V; V_{CC} = 3 V	K_{SR}	22	31	38	μA
FAULT PROTECTIONS						
Thermal Shutdown Threshold (Note 10)		T_{SDT}		155		°C
Thermal Shutdown Hysteresis (Note 10)		T_{HYS}		20		°C
V_{IN} Undervoltage Lockout Threshold	V_{IN} falling	V_{UV_FA}	670	710	750	mV
V_{IN} Undervoltage Lockout Hysteresis	V_{IN} rising	V_{UV_RI}	755	795	840	mV
Over−Current Protection Trip Current (Note 12)	V_{OCP} = 0 V	I_{TRIP_OCP}		3.5		A
Over−Current Protection Blanking Time	V_{CC} = 3 V	t_{OCP}	2.0	3.5	5.0	ms
OCP Pull Up Resistance (Note 11)		R_{OCP}	200	250	300	kΩ
Short−Circuit Protection Trip Voltage	V_{IN} < 4.5 V	V_{SC_LVIN}	110	150	190	mV
	V_{IN} > 4.5 V	V_{SC_HVIN}	135	160	190	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
6. Average current from V_{CC} to GND with MOSFET turned off.
7. Average current from V_{CC} to GND after charge up time of MOSFET.
8. Resistance from VOUT to GND when the MOSFET driver is disabled.
9. See Applications Information section for details on how to adjust the gate slew rate.
10. Operation above T_J = 125°C is not guaranteed.
11. Internal resistor from OCP to EN used to pull up on OCP pin if not driven.
12. Min and max trip OCP trip currents are not guaranteed but typically are accurate within ±1.5 A.

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Notes 13 and 14)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate − Default	V_{CC} = 3.0 V; V_{IN} = 1.0 V	SR		18.5		V/ms
	V_{CC} = 5.5 V; V_{IN} = 1.0 V			18		
	V_{CC} = 3.0 V; V_{IN} = 5.0 V		11	19.3	25	
	V_{CC} = 3.0 V; V_{IN} = 13.5 V			22		
	V_{CC} = 5.5 V; V_{IN} = 13.5 V			23		
Output Turn−on Delay	V_{CC} = 3.0 V; V_{IN} = 1.0 V	T_{ON}		140		μs
	V_{CC} = 5.5 V; V_{IN} = 1.0 V			110		
	V_{CC} = 3.0 V; V_{IN} = 5.0 V		50	165	230	
	V_{CC} = 3.0 V; V_{IN} = 13.5 V			200		
	V_{CC} = 5.5 V; V_{IN} = 13.5 V			190		
Output Turn−off Delay	V_{CC} = 3.0 V; V_{IN} = 1.0 V	T_{OFF}		2.1		μs
	V_{CC} = 5.5 V; V_{IN} = 1.0 V			1.6		
	V_{CC} = 3.0 V; V_{IN} = 13.5 V	T_{OFF}		0.5		
	V_{CC} = 5.5 V; V_{IN} = 13.5 V			0.4		
Power Good Turn−on Time	V_{CC} = 3.0 V; V_{IN} = 1.0 V	$T_{PG,ON}$		0.70		ms
	V_{CC} = 5.5 V; V_{IN} = 1.0 V			0.65		
	V_{CC} = 3.0 V; V_{IN} = 5.0 V		0.4	0.8	1.8	
	V_{CC} = 3.0 V; V_{IN} = 13.5 V			1.33		
	V_{CC} = 5.5 V; V_{IN} = 13.5 V			0.9		
Power Good Turn−off Time	V_{CC} = 3.0 V; V_{IN} = 1.0 V	$T_{PG,OF}$		21		ns
	V_{CC} = 5.5 V; V_{IN} = 1.0 V			15		
	V_{CC} = 3.0 V; V_{IN} = 13.5 V			21		
	V_{CC} = 5.5 V; V_{IN} = 13.5 V			15		

13. See below figure for Test Circuit and Timing Diagram.
14. Tested with the following conditions: V_{TERM} = V_{CC}; R_{PG} = 100 kΩ; R_L = 10 Ω; C_L = 0.1 μF.

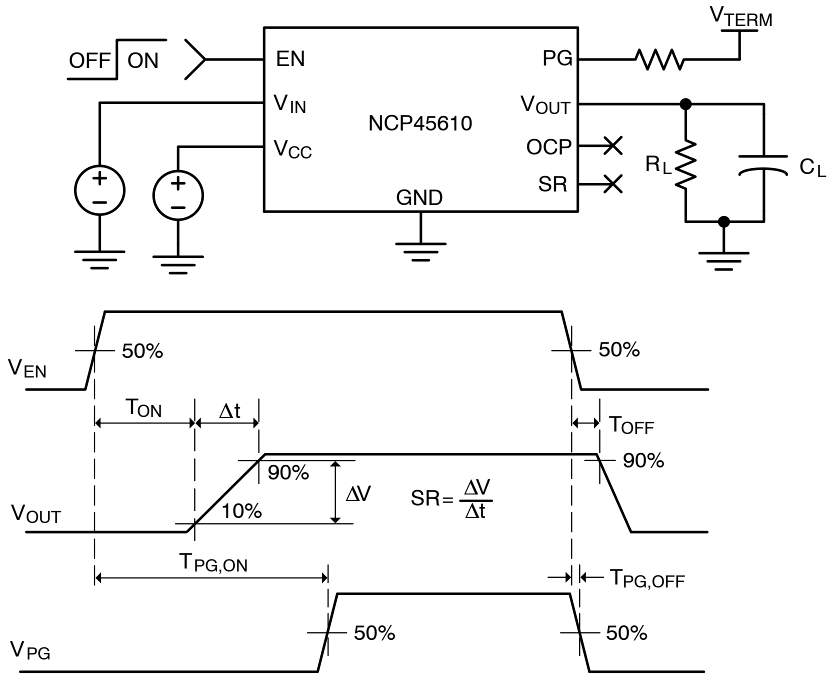


Figure 2. Switching Characteristics Test Circuit and Timing Diagram

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise specified)

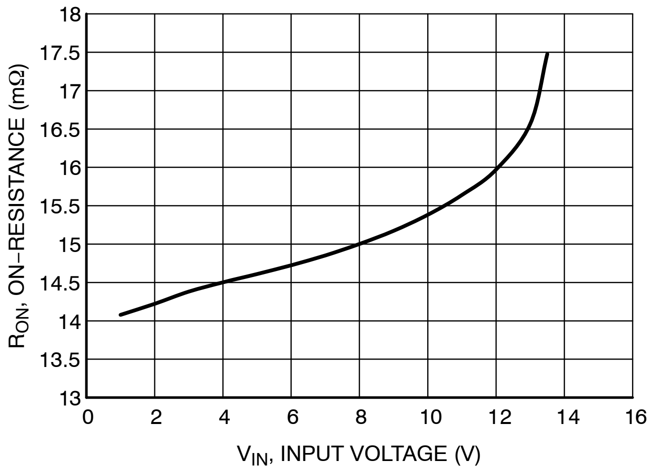


Figure 3. On−Resistance vs. Input Voltage

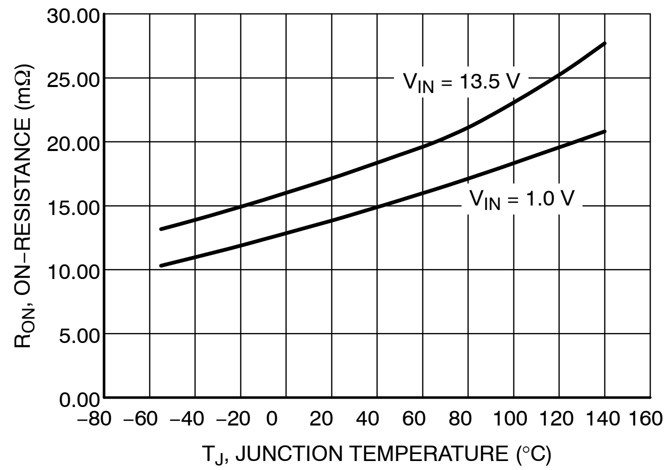


Figure 4. On−Resistance vs. Temperature

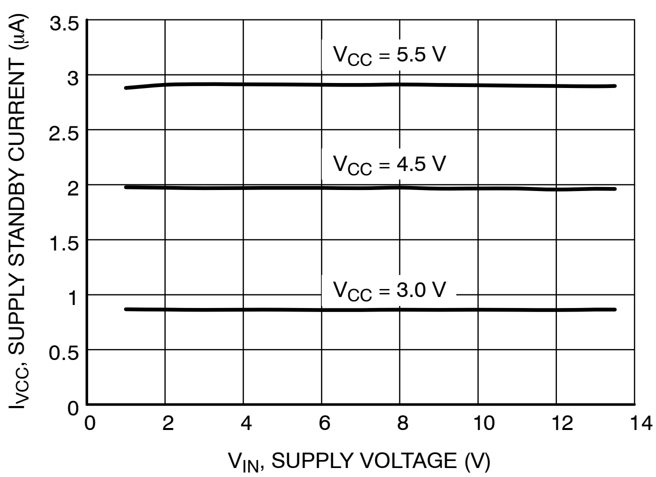


Figure 5. Supply Standby Current vs. Supply Voltage

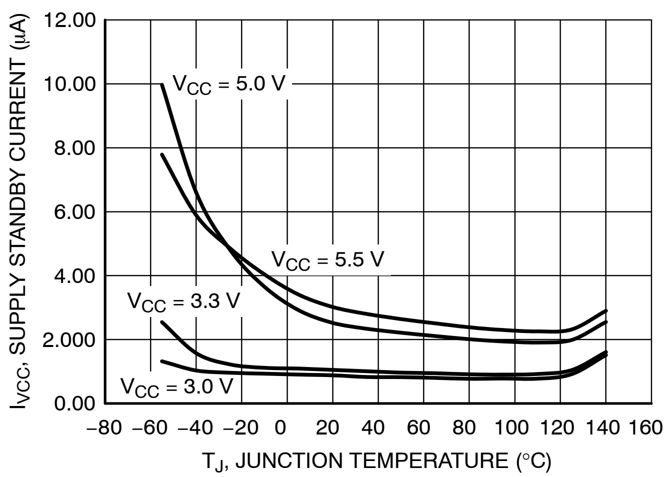


Figure 6. Supply Standby Current vs. Temperature

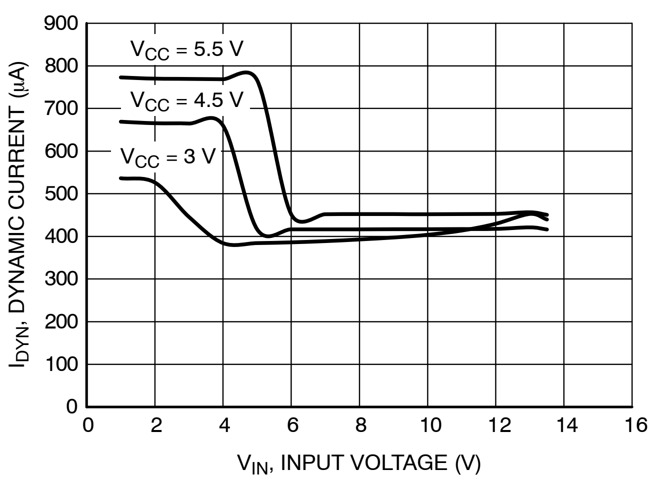


Figure 7. Dynamic Current vs. Input Voltage

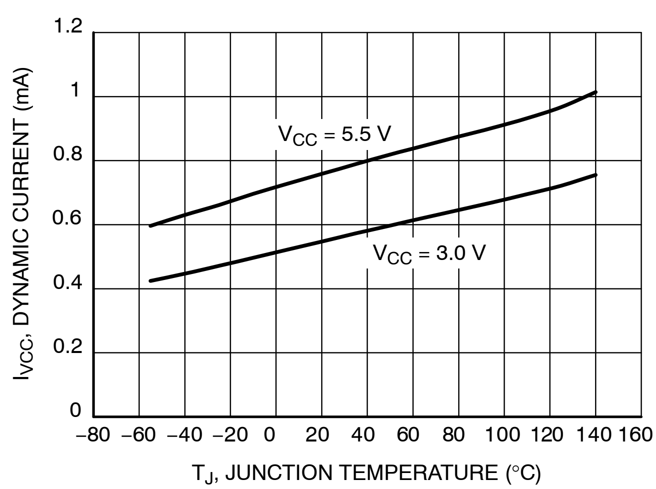


Figure 8. Supply Dynamic Current vs. Temperature

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise specified)

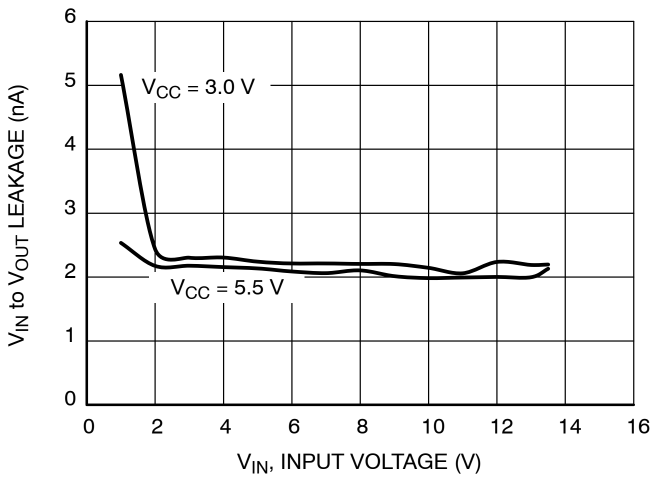


Figure 9. V_{IN} to V_{OUT} Leakage with EN = 0 V

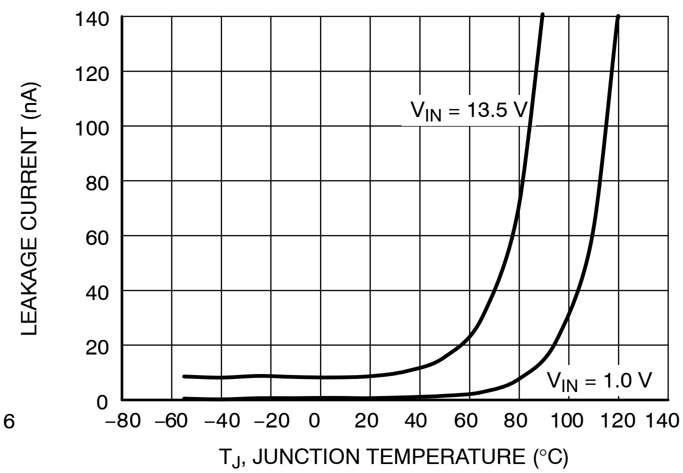


Figure 10. V_{IN} to V_{OUT} Leakage Over Temperature (EN = 0 V)

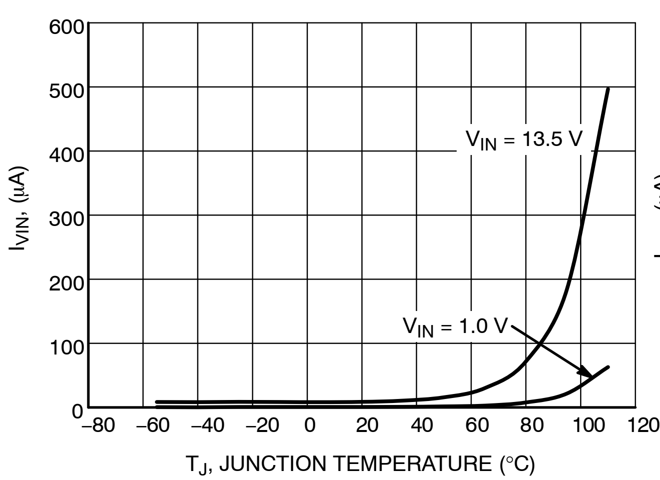


Figure 11. V_{IN} Controller Current vs. Temperature (EN = 0 V)

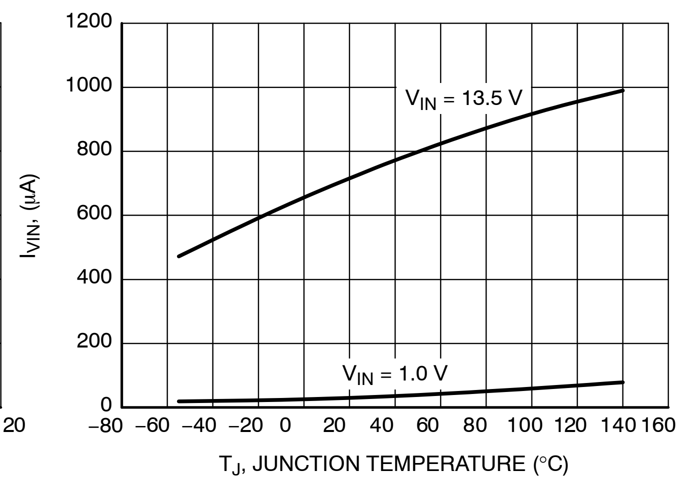


Figure 12. V_{IN} Controller Current vs. Temperature (EN = HIGH)

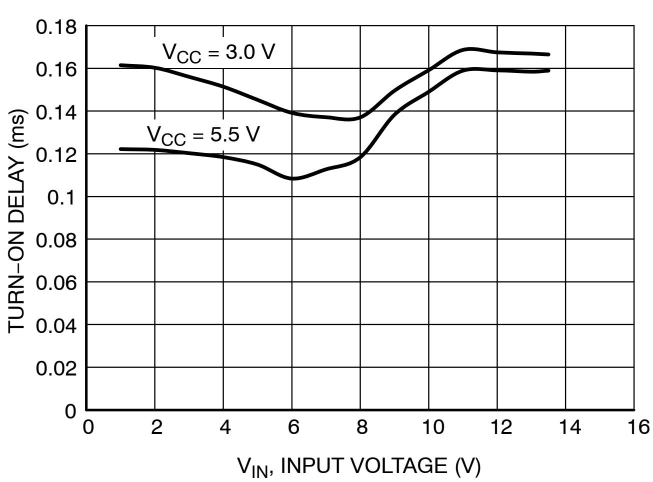


Figure 13. Output Turn−on Delay vs. Input Voltage

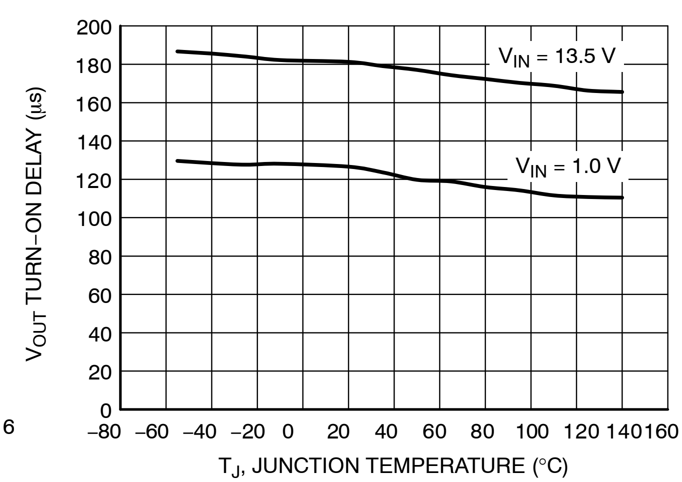


Figure 14. Output Turn−on Delay vs. Temperature

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise specified)

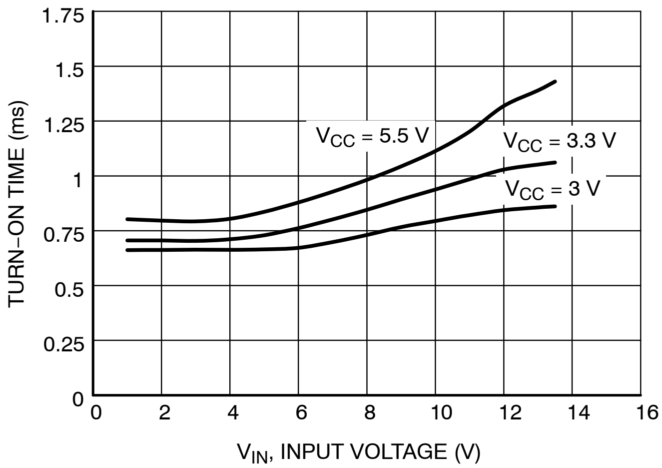


Figure 15. Power Good Turn On Turn vs. Input Voltage

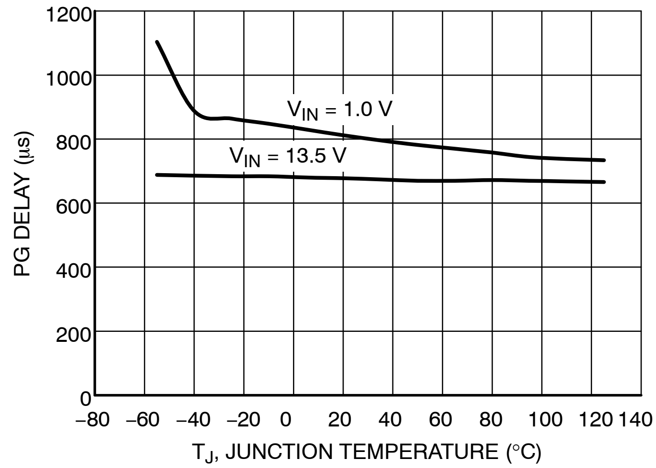


Figure 16. Power Good Turn−on Delay vs. Temperature

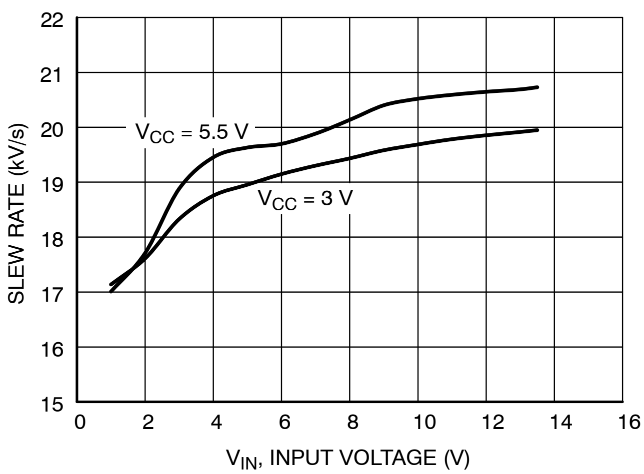


Figure 17. Default Slew Rate vs. Input Voltage (SR pin = Floating)

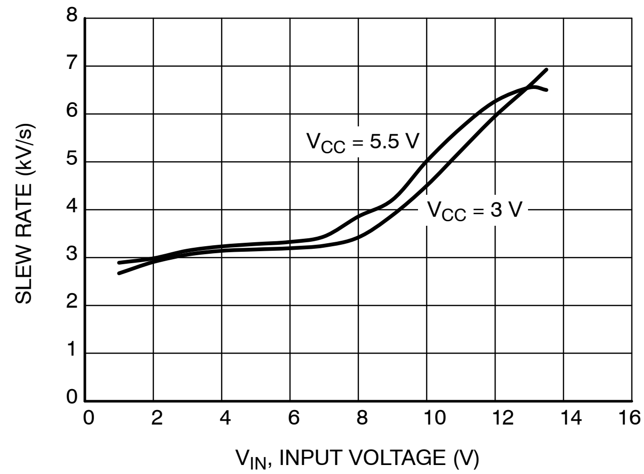


Figure 18. Slew Rate vs. Input Voltage (SR Pin = 10 nF to GND)

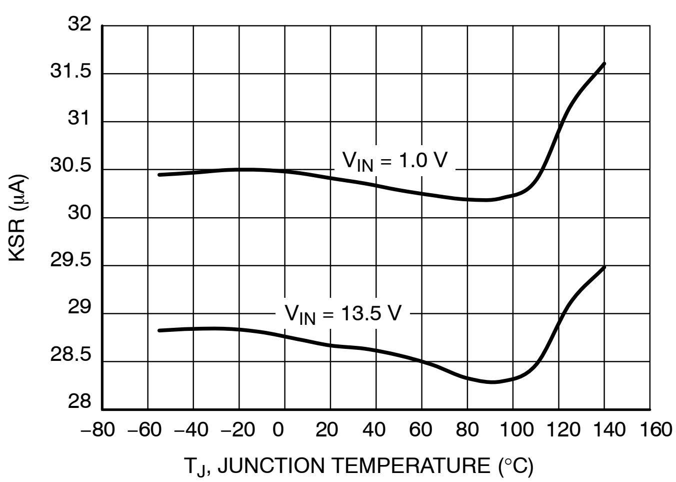


Figure 19. KSR vs. Temperature

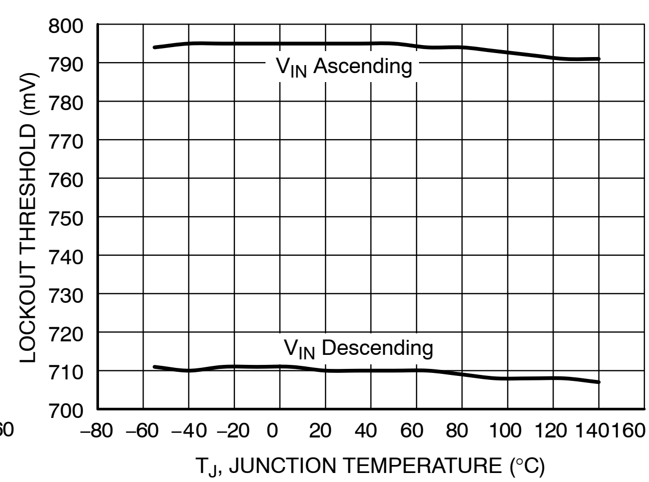


Figure 20. UVLO Trip Voltage vs. Temperature

APPLICATIONS INFORMATION

Power Sequencing

The NCP45610 will function with any power sequence, but the output turn−on delay and slew rate performance may vary from what is specified. To achieve the specified performance, there are two recommended power sequences:

1. $V_{CC} \rightarrow V_{IN} \rightarrow V_{EN}$
2. $V_{IN} \rightarrow V_{CC} \rightarrow V_{EN}$

V_{CC} must be at 2 V or higher when EN is asserted to ensure proper operation.

Enable Control

The NCP45610 part allows for enabling the MOSFET in an active−high configuration. When the EN pin is at a logic high level and the VCC supply pin has an adequate voltage applied, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. After disabling the NCP45610 at least 400 ms must pass before the part is enabled again to ensure proper slew rate. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

Load Bleed

The NCP45610 device has an on−chip bleed resistor that is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. Delays are added to the enable of this switch to ensure that both the MOSFET and the bleed switch are not concurrently active.

Over−Current and Short−Circuit protection

The NCP45610 devices are equipped with short−circuit protection and an optional over−current protection that are used to help protect the part and the system from a sudden high−current event, such as the output, V_{OUT}, being shorted to ground. This circuitry is only active when the gate of the MOSFET is fully driven.

Once active, the circuitry monitors the difference in the voltage on the V_{IN} pin and the voltage on the V_{OUT} pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is immediately turned off and the load bleed is activated. The part remains latched in this off state until the V_{CC}− supply voltage is cycled. When latched off the behavior of the part if EN is toggled is not defined. After the V_{CC} supply voltage is cycled and EN is high, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The over−current protection can be enabled to allow for protection before the short−circuit threshold. If this lower threshold is not needed, then OCP can be left floating. By tying the OCP pin to ground the NCP45610 will enable the over−current protection. In the event the OCP threshold is exceeded, the MOSFET will shut down after the blanking time if the voltage difference remains greater than the threshold. Like the short−circuit protection, the part remains latched in this off state until the V_{CC}− supply voltage is cycled. When latched off the behavior of the part if EN is toggled is not defined. After the V_{CC} supply voltage is cycled and EN is high, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Thermal Shutdown

The thermal shutdown of the NCP45610 device protects the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over−temperature condition is detected, the MOSFET is immediately turned off and the load bleed is activated.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Under Voltage Lockout

The under voltage lockout of the NCP45610 device turns the MOSFET off and activates the load bleed when the input voltage, V_{IN}, drops below the undervoltage lockout threshold. This circuitry is disabled when EN is not active to reduce standby current.

If the V_{IN} voltage rises above the undervoltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The NCP45610 devices have a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, R_{PG}, greater than or equal to 100 kΩ to an external voltage source, that is compatible with input levels of all devices connected to this pin.

The power good output can be used as the enable signal for other active-high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

Slew Rate Control

The NCP45610 device is equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}}\ [\text{V/s}] \qquad \text{(eq. 1)}$$

where K_{SR} is the specified slew rate control constant, found on page 3, and C_{SR} is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified I_{max}. CL (capacitive load) should be less then C_{max} as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \qquad \text{(eq. 2)}$$

where I_{max} is the maximum load current, and SR_{typ} is the typical default slew rate when no external load capacitor is added to the SR pin.

OFF to ON Transition Energy Dissipation

The energy dissipation due to load current traveling from V_{IN} to V_{OUT} is very low during steady state operation due to the low R_{ON}. When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from V_{IN} to V_{OUT} transitions from high impedance to RON, and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot \left(I_{INRUSH} + 0.8 \cdot I_{LOAD}\right) \cdot dt \qquad \text{(eq. 3)}$$

Where V_{IN} is the voltage on the V_{IN} pin, I_{INRUSH} is the inrush current caused by capacitive loading on VOUT, and dt is the time it takes V_{OUT} to rise from 0 V to V_{IN}. I_{INRUSH} can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \qquad \text{(eq. 4)}$$

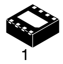
Where dv/dt is the programmed slew rate, and C_L is the capacitive loading on V_{OUT}. To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to E_{TRANS} listed in absolute maximum ratings table.

ecoSWITCH LAYOUT GUIDELINES

Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSWITCH products.

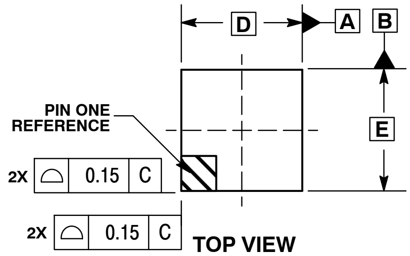
Power Planes: The ecoSWITCH is optimized for extremely low Ron resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the VIN and VOUT pins of the ecoSWITCH to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSWITCH requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. Direct coupling of VIN to VOUT should be avoided, as this will adversely affect slew rates.



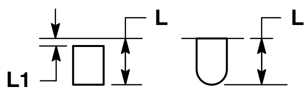
SCALE 2:1

DFN8 2x2, 0.5P
CASE 506CN
ISSUE O

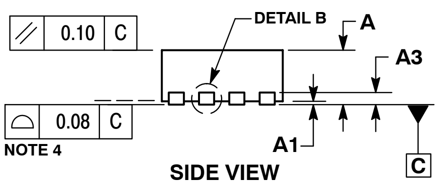
DATE 17 JUL 2013



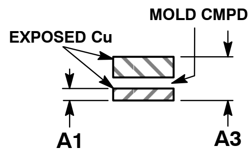
TOP VIEW



DETAIL A
ALTERNATE CONSTRUCTIONS



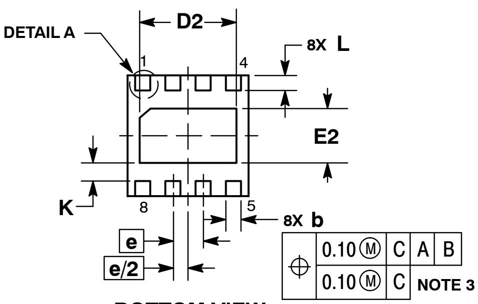
SIDE VIEW



DETAIL B
ALTERNATE CONSTRUCTION

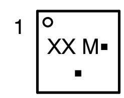
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
K	0.27 REF	
L	0.17	0.38
L1	---	0.15



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

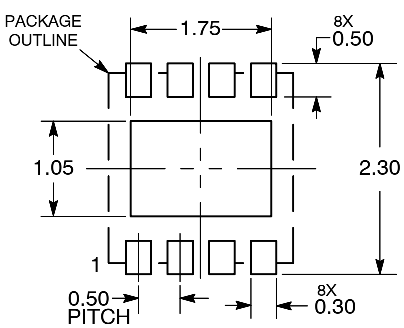


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON76135F	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	DFN8 2X2, 0.5P	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊