

MC33363B

High Voltage Switching Regulator

The MC33363B is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on-chip 700 V/1.0 A SENSEFET® power switch, 500 V active off-line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle-by-cycle current limiting, input undervoltage lockout with hysteresis, overvoltage protection, and thermal shutdown. This device is available in a 16-lead dual-in-line and wide body surface mount packages.

Features

- On-Chip 700 V, 1.0 A SENSEFET Power Switch
- Rectified 240 Vac Line Source Operation
- On-Chip 500 V Active Off-Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle-By-Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Over-Voltage Protection
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown
- These are Pb-Free Devices*

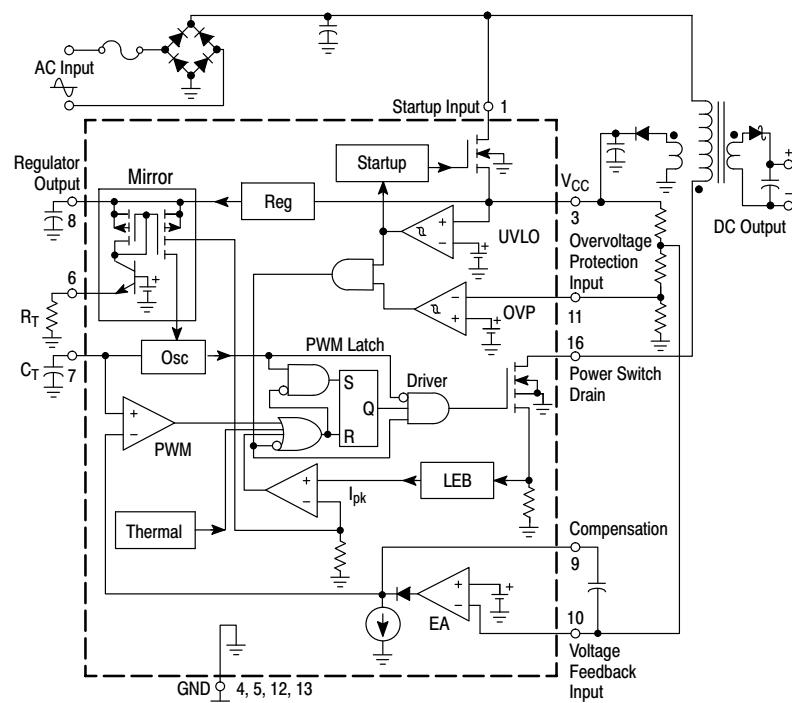


Figure 1. Simplified Application

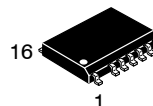
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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MARKING DIAGRAMS

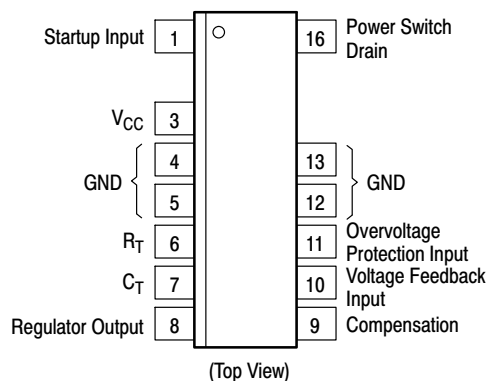


SO-16WB
DW SUFFIX
CASE 751N



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
MC33363BDWG	SO-16WB (Pb-Free)	47 Units/Rail
MC33363BDWR2G	SO-16WB (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Switch (Pin 16) Drain Voltage Drain Current	V_{DS} I_{DS}	700 1.0	V A
Startup Input Voltage (Pin 1, Note 2)	V_{in}	500	V
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	-1.0 to V_{reg}	V
Thermal Characteristics P Suffix, Dual-In-Line Case 648E Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case DW Suffix, Surface Mount Case 751G Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case	$R_{\theta JA}$ $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JC}$	80 15 95 15	$^{\circ}C/W$
Operating Junction Temperature	T_J	-25 to +150	$^{\circ}C$
Storage Temperature	T_{stg}	-55 to +150	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- This device series contains ESD protection and exceeds the following tests:
Human Body Model 2000 V per JEDEC Standard JESD22, Method A114E.
Machine Model Method 200 V per JEDEC Standard JESD22, Method A115A.
- Maximum power dissipation limits must be observed.
- Tested junction temperature range for the MC33363B: $T_{low} = -25^{\circ}C$ $T_{high} = +125^{\circ}C$

ELECTRICAL CHARACTERISTICS ($V_{CC} = 20$ V, $R_T = 10$ k, $C_T = 390$ pF, $C_{Pin\ 8} = 1.0$ μ F, for typical values $T_J = 25^{\circ}C$, for min/max values T_J is the operating junction temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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REGULATOR (Pin 8)

Output Voltage ($I_O = 0$ mA, $T_J = 25^{\circ}C$)	V_{reg}	5.5	6.5	7.5	V
Line Regulation ($V_{CC} = 20$ V to 40 V)	Reg_{line}	-	30	500	mV
Load Regulation ($I_O = 0$ mA to 10 mA)	Reg_{load}	-	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	-	8.0	V

OSCILLATOR (Pin 7)

Frequency $C_T = 390$ pF $T_J = 25^{\circ}C$ ($V_{CC} = 20$ V) $T_J = T_{low}$ to T_{high} ($V_{CC} = 20$ V to 40 V) $C_T = 2.0$ nF $T_J = 25^{\circ}C$ ($V_{CC} = 20$ V) $T_J = T_{low}$ to T_{high} ($V_{CC} = 20$ V to 40 V)	f_{OSC}	260 255	285 -	310 315	kHz
Frequency Change with Voltage ($V_{CC} = 20$ V to 40 V)	$\Delta f_{OSC}/\Delta V$	-	0.1	2.0	kHz

ERROR AMPLIFIER (Pins 9, 10)

Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation ($V_{CC} = 20$ V to 40 V, $T_J = 25^{\circ}C$)	Reg_{line}	-	0.6	5.0	mV
Input Bias Current ($V_{FB} = 2.6$ V, $T_J = 0$ - $125^{\circ}C$)	I_{IB}	-	20	500	nA
Open Loop Voltage Gain ($T_J = 25^{\circ}C$)	A_{VOL}	70	82	94	dB
Gain Bandwidth Product ($f = 100$ kHz, $T_J = 25^{\circ}C$)	GBW	0.85	1.0	1.15	MHz
Output Voltage Swing High State ($I_{Source} = 100$ μ A, $V_{FB} < 2.0$ V) Low State ($I_{Sink} = 100$ μ A, $V_{FB} > 3.0$ V)	V_{OH} V_{OL}	4.0 -	5.3 0.2	- 0.35	V

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 20\text{ V}$, $R_T = 10\text{ k}$, $C_T = 390\text{ pF}$, $C_{Pin\ 8} = 1.0\text{ }\mu\text{F}$, for typical values $T_J = 25^\circ\text{C}$, for min/max values T_J is the operating junction temperature range that applies (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OVERVOLTAGE DETECTION (Pin 11)

Input Threshold Voltage	V_{th}	2.47	2.6	2.73	V
Input Bias Current ($V_{in} = 2.6\text{ V}$, $T_J = -25 - 125^\circ\text{C}$)	I_{IB}	–	100	500	nA

PWM COMPARATOR (Pins 7, 9)

Duty Cycle Maximum ($V_{FB} = 0\text{ V}$) Minimum ($V_{FB} = 2.7\text{ V}$)	$DC_{(max)}$ $DC_{(min)}$	48 –	50 0	52 0	%
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POWER SWITCH (Pin 16)

Drain–Source On–State Resistance ($I_D = 200\text{ mA}$) $T_J = 25^\circ\text{C}$ $T_J = T_{low}$ to T_{high}	$R_{DS(on)}$	– –	15 –	17 39	Ω
Drain–Source Off–State Leakage Current ($V_{DS} = 650\text{ V}$) $T_J = 25^\circ\text{C}$ $T_J = T_{low}$ to T_{high}	$I_{D(off)}$	– –	0.25 –	1.0 50	μA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns

OVERCURRENT COMPARATOR (Pin 16)

Current Limit Threshold ($R_T = 10\text{ k}$)	I_{lim}	0.5	0.72	0.9	A
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STARTUP CONTROL (Pin 1)

Peak Startup Current ($V_{in} = 50\text{ V}$) ($T_J = -25 - 100^\circ\text{C}$) $V_{CC} = 0\text{ V}$ $V_{CC} = (V_{th(on)} - 0.2\text{ V})$	I_{start}	2.0 2.0	5.0 5.0	8.0 8.0	mA
Off–State Leakage Current ($V_{in} = 50\text{ V}$, $V_{CC} = 20\text{ V}$)	$I_{D(off)}$	–	40	200	μA

UNDERVOLTAGE LOCKOUT (Pin 3)

Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	15.2	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V

TOTAL DEVICE (Pin 3)

Power Supply Current Startup ($V_{CC} = 10\text{ V}$, Pin 1 Open) Operating	I_{CC}	– –	0.25 3.2	0.5 5.0	mA
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THERMAL SHUTDOWN

Shutdown (Junction Temperature Increasing)	T_{sd}	–	135	–	$^\circ\text{C}$
Hysteresis (Junction Temperature Decreasing)	T_H	–	30	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Tested junction temperature range for the MC33363B: $T_{low} = -25^\circ\text{C}$ $T_{high} = +125^\circ\text{C}$

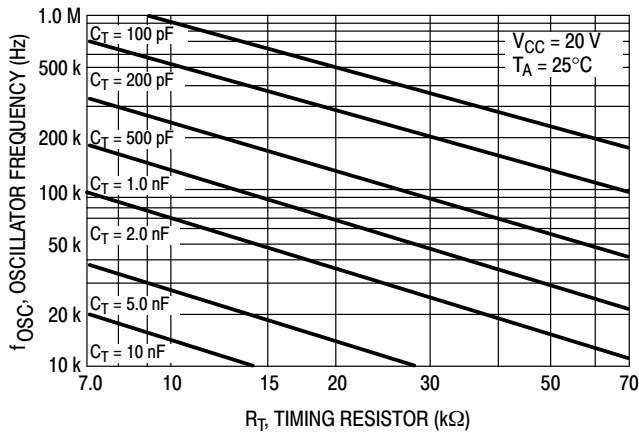


Figure 2. Oscillator Frequency versus Timing Resistor

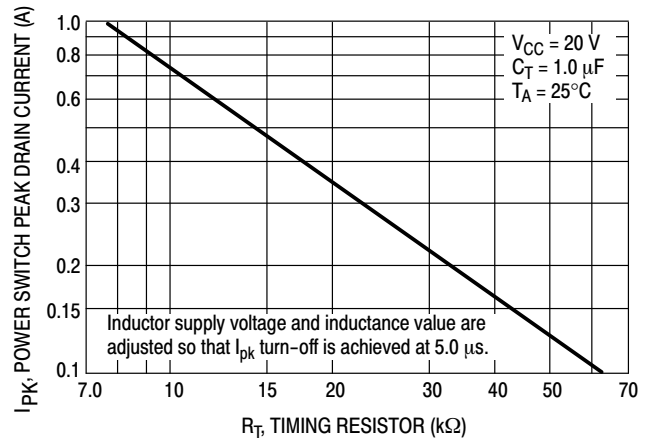


Figure 3. Power Switch Peak Drain Current versus Timing Resistor

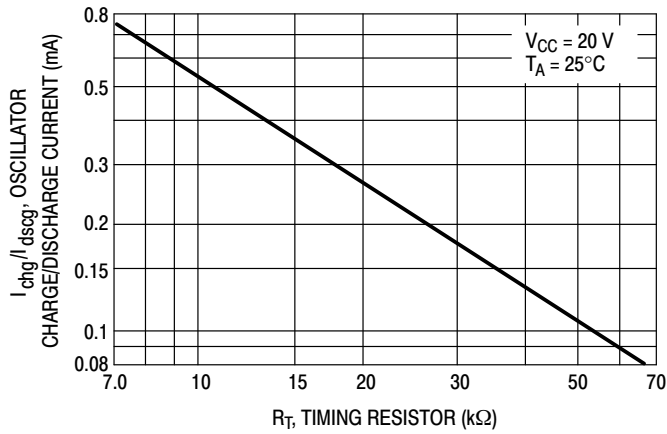


Figure 4. Oscillator Charge/Discharge Current versus Timing Resistor

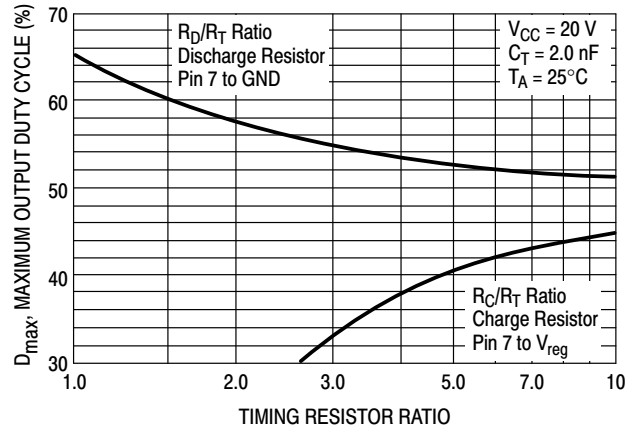


Figure 5. Maximum Output Duty Cycle versus Timing Resistor Ratio

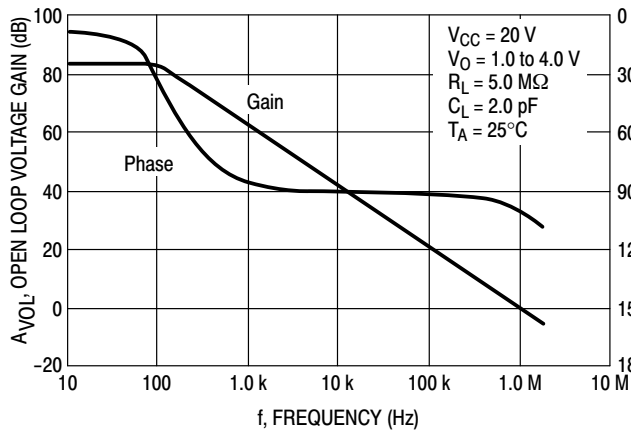


Figure 6. Error Amp Open Loop Gain and Phase versus Frequency

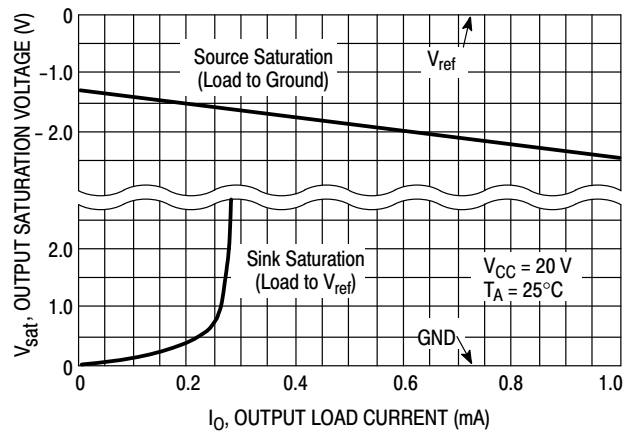


Figure 7. Error Amp Output Saturation Voltage versus Load Current

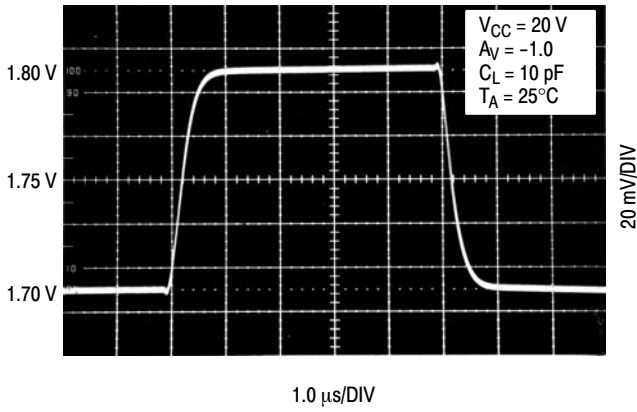


Figure 8. Error Amplifier Small Signal Transient Response

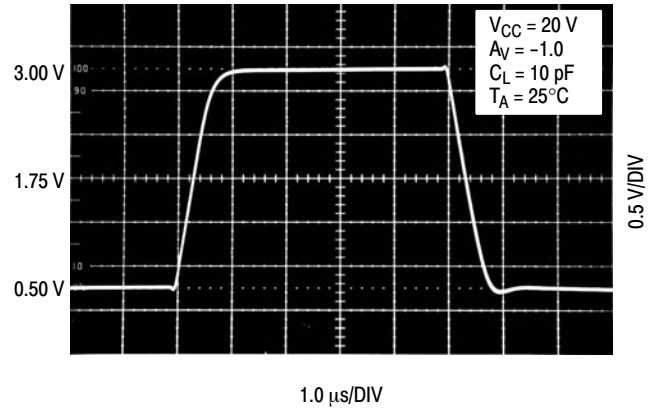


Figure 9. Error Amplifier Large Signal Transient Response

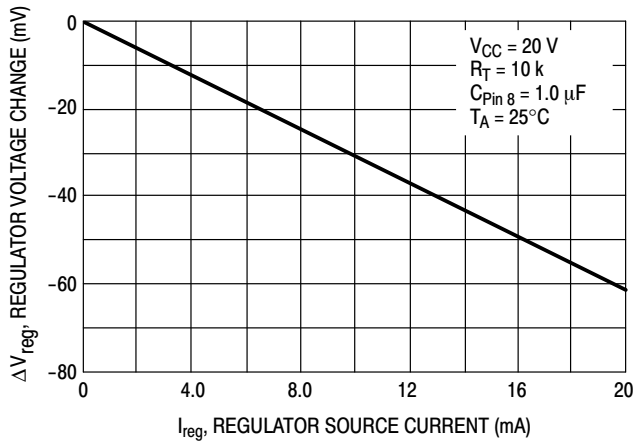


Figure 10. Regulator Output Voltage Change versus Source Current

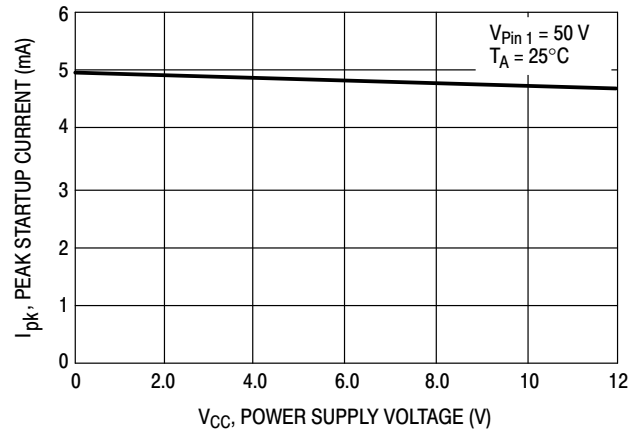


Figure 11. Peak Startup Current versus Power Supply Voltage

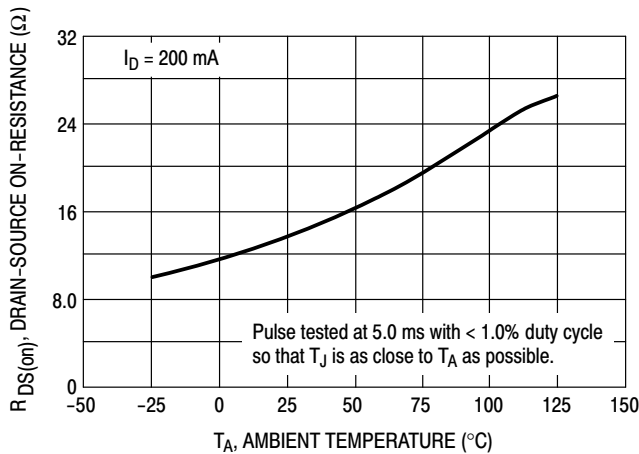


Figure 12. Power Switch Drain-Source On-Resistance versus Temperature

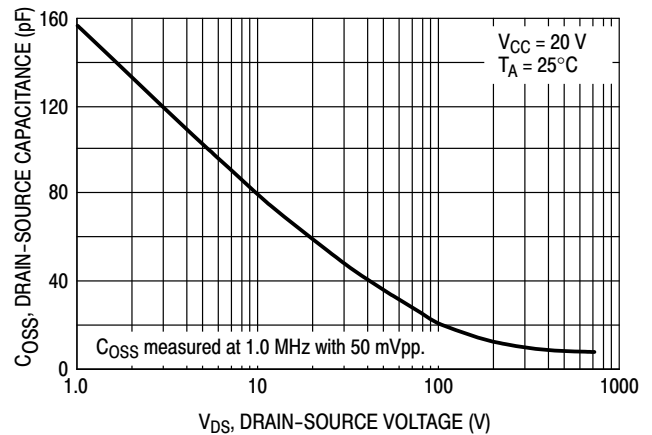


Figure 13. Power Switch Drain-Source Capacitance versus Voltage

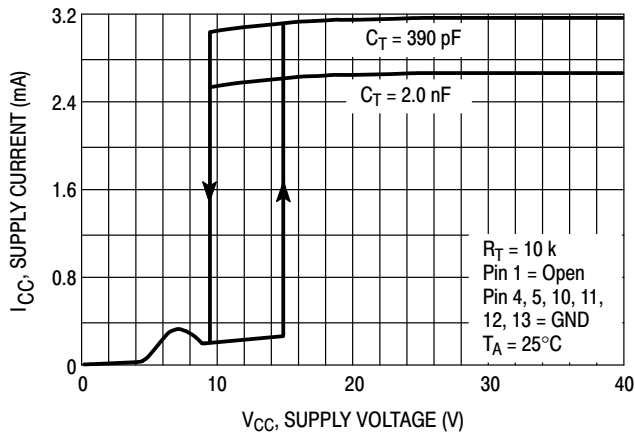


Figure 14. Supply Current versus Supply Voltage

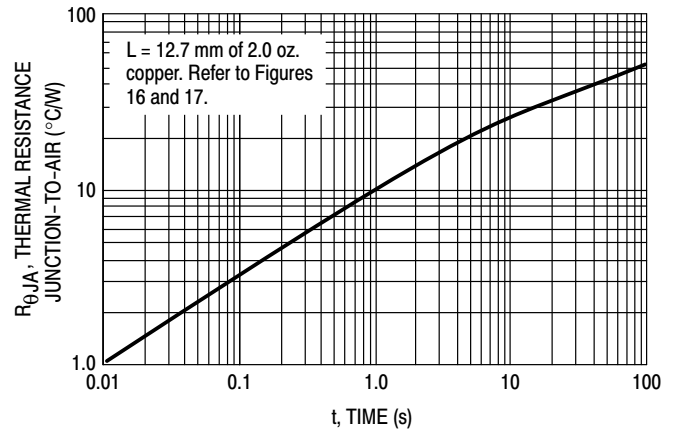


Figure 15. DW and P Suffix Transient Thermal Resistance

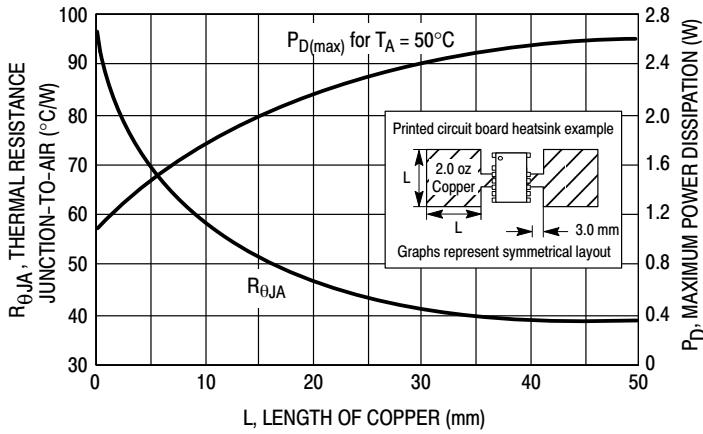


Figure 16. DW Suffix (SOP-16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

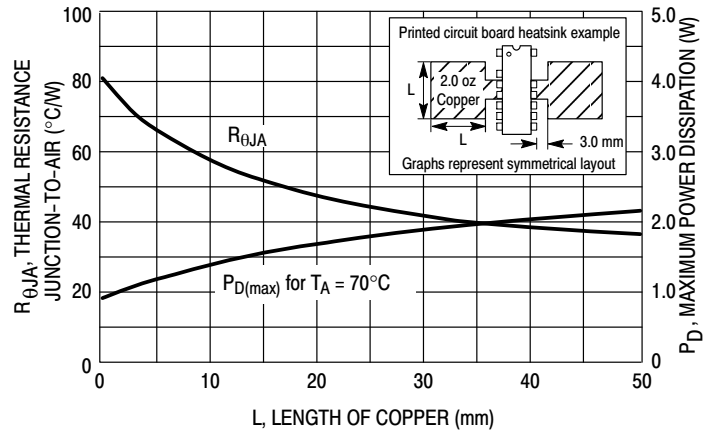


Figure 17. P Suffix (DIP-16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T , programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 μ F for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Overvoltage Protection Input	This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A.

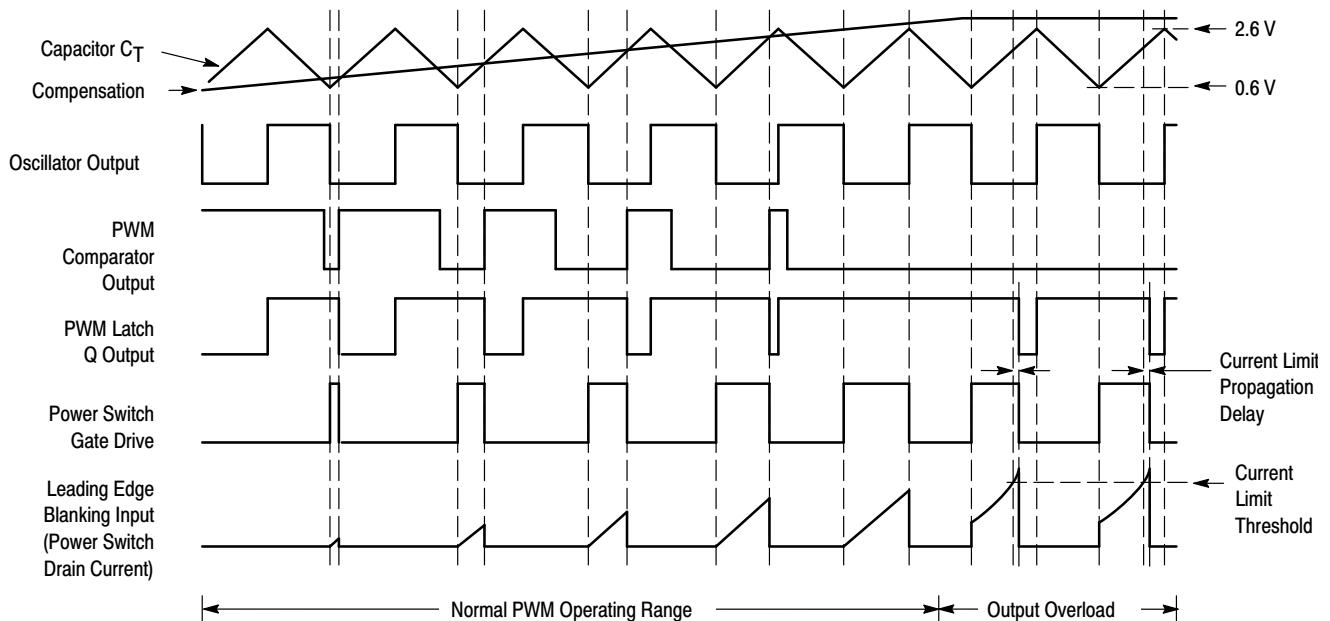


Figure 18. Timing Diagram of Normal Operation

MC33363B

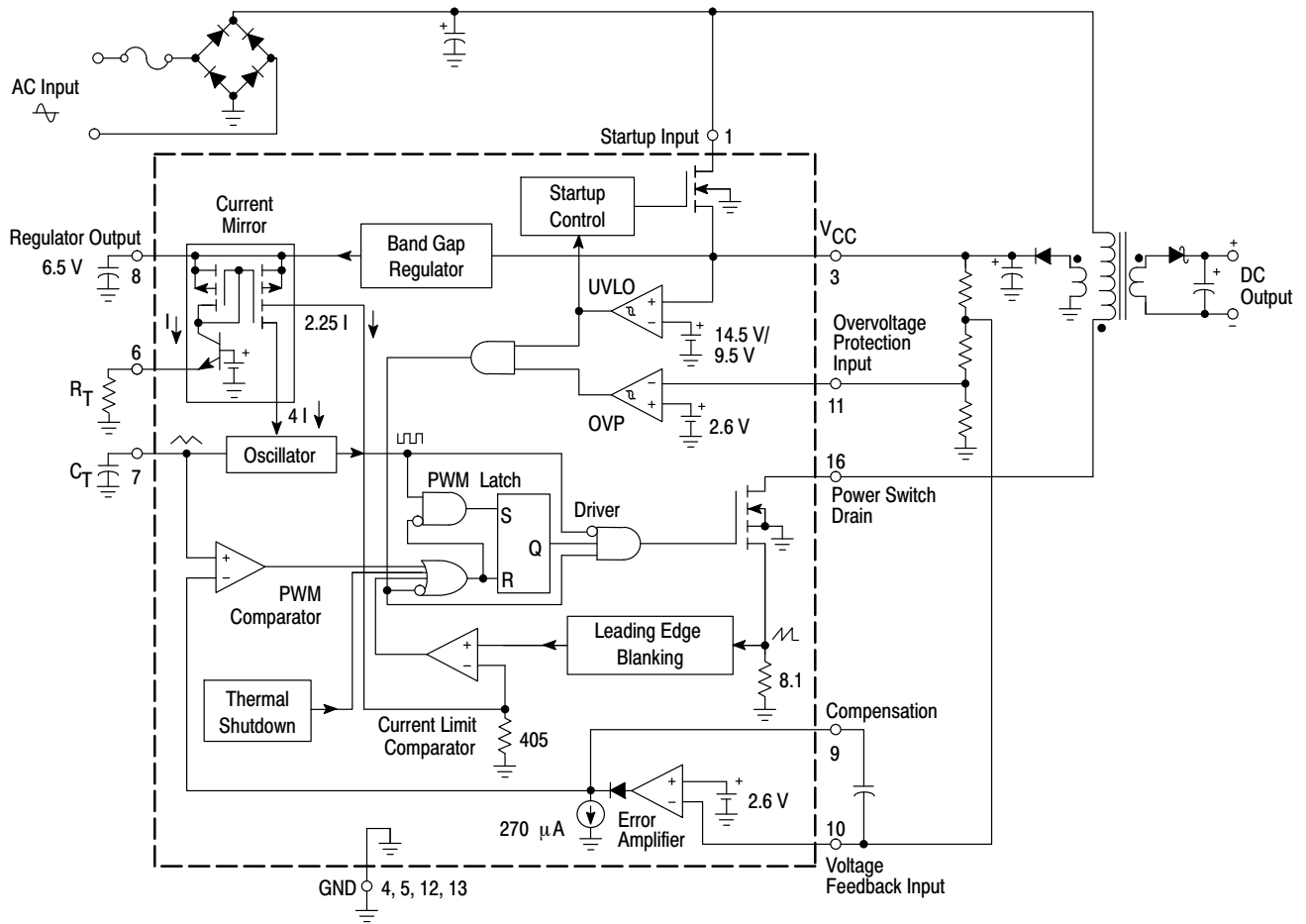


Figure 19. Representative Block Diagram

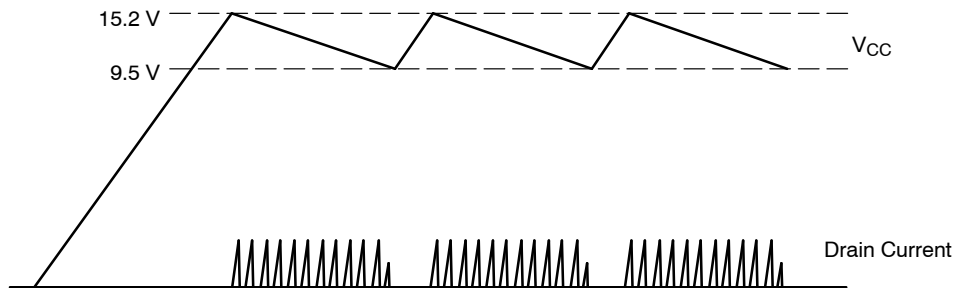


Figure 20. Timing Diagram of Short-Circuit Condition

OPERATING DESCRIPTION

Introduction

The MC33363B represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 19, 18 and 20.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T . Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 4. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T , the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T , Figure 21. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 5 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T .

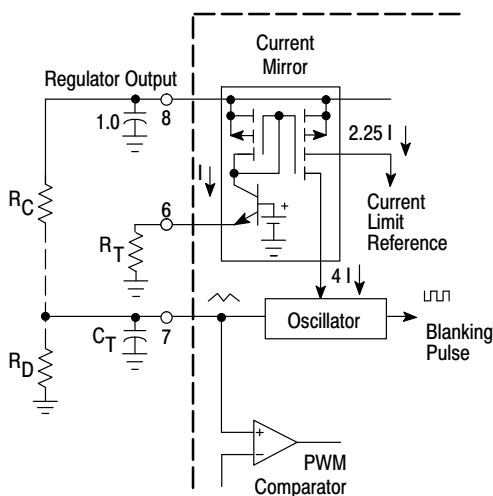


Figure 21. Maximum Duty Cycle Modification

The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T , refer to Figure 2. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{\text{chg/dscg}} = \frac{5.4}{R_T} \quad f \approx \frac{I_{\text{chg/dscg}}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non-inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp-up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33363B uses cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The Power Switch is constructed as a SENSEFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1462 cells, of which 36 are connected to a 8.1 Ω ground-referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 405 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T . Therefore when selecting the values for R_T and C_T , R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 3 with the related formula below.

$$I_{\text{pk}} = 8.8 \left(\frac{R_T}{1000} \right)^{-1.077}$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn-on transition is completed. The current limit propagation delay time is typically 262 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn-off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 19. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 6. The noninverting input is internally biased at $2.6\text{ V} \pm 3.1\%$ and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of $270\text{ }\mu\text{A}$, allowing it to be easily overridden with a pullup resistor. This is desirable in applications that require secondary side voltage sensing.

Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side V_{CC} voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V , the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363B. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its

associated power dissipation, commonly used in most off-line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 15.2 V , the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide a steady current of 1.7 mA , Figure 11, as V_{CC} increases or shorted to ground. The startup MOSFET is rated at a maximum of 400 V with V_{CC} shorted to ground, and 500 V when charging a V_{CC} capacitor of $1000\text{ }\mu\text{F}$ or less.

Output Short-Circuit Condition

When the output is short-circuited, the V_{CC} is powered by the internal startup circuit instead of the V_{CC} auxiliary winding. The internal startup circuit turns on and charges up V_{CC} voltage when V_{CC} reaches its UVLO lower threshold of 9.5 V . It turns off and V_{CC} voltage drops when V_{CC} reaches its UVLO upper threshold of 15.2 V . The device only delivers drain current for the time when V_{CC} goes from 15.2 V to 9.5 V . No drain current is delivered when V_{CC} goes from 9.5 V to 15.2 V . As a result, some of the switching cycle is missed as shown in Figure 20. The drain current limit is limited by the cycle-by-cycle current limit.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short-circuit protection. This output requires an external bypass capacitor of at least $1.0\text{ }\mu\text{F}$ for stability.

Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 135°C , the Latch is forced into a 'reset' state, disabling the Power Switch. The Latch is allowed to 'set' when the Power Switch temperature falls below 105°C . This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

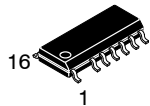
The MC33363B is contained in a heatsinkable plastic dual-in-line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single-sided board with two ounce per square foot of copper.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

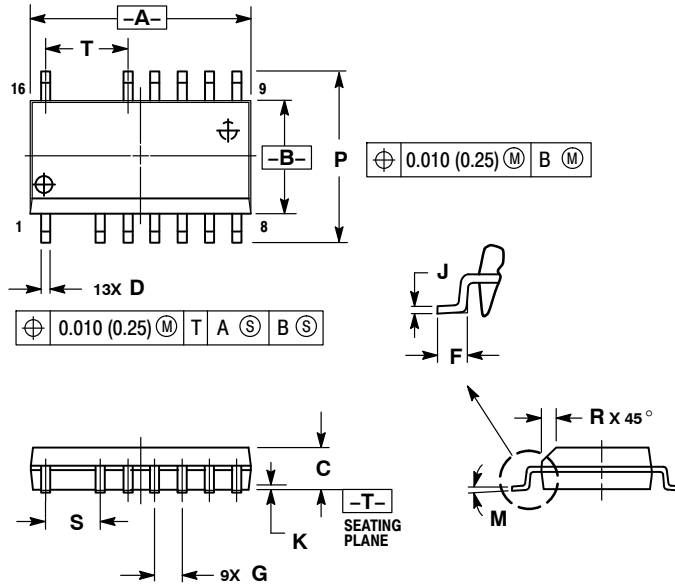
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SCALE 1:1

SOIC-16 MINUS PINS, 2, 14, 15 CASE 751N-01 ISSUE O

DATE 02/28/95



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029
S	2.54 BSC		0.100 BSC	
T	3.81 BSC		0.150 BSC	

DOCUMENT NUMBER: 98ASH70300A

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DESCRIPTION: SOIC-16 MINUS PINS, 2, 14, 15

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