ON Semiconductor®

FAN7093
High-Current PN Half-Bridge Driver

Features

- Path Resistance for a Full-Bridge Configuration: Max. 30.5 mΩ at 150°C
- PWM Capability: > 60 kHz[1] Combined with Active Free Wheeling
- Switched-Mode Current Limitation for Reduced Power Dissipation In Over-Current Condition
- Current Limit Protection: Typ. 43 A
- Independent Current-Sense Output and Diagnostic Flag for High and Low Sides
- Over-Temperature Protection (OTP) with Latch
- Shorted-Load Protection with Latch Behavior
- Over-Voltage Protection (OVP) with Lockout
- Under-Voltage Protection (UVP)
- Logic Level Control Inputs
- Adjustable Slew Rates for Optimized EMI
- Typical Slew Rate of 1 V/µs with Open Slew Rate Pin

Description

The FAN7093 is an integrated high-current half-bridge driver for electric motor drive applications. It contains one P-channel high-side MOSFET and one N-channel low-side MOSFET with an integrated control IC in one package. With the P-channel high-side switch, the need for a charge pump is eliminated, which minimizes EMI.

Pins IN and /INH are logic-level inputs and control the half-bridge output. The diagnostic and current sense IS pin outputs a current that is proportional to the current flowing through the half-bridge MOSFETs. The IS pin output represents current for the P-channel or the N-channel, depending on which is active.

The part is protected against a short to battery or ground of the out pin, over-current, over-temperature, over-voltage, and under-voltage conditions. The FAN7093 provides a cost- and space-optimized solution for protected high-current PWM motor drives.

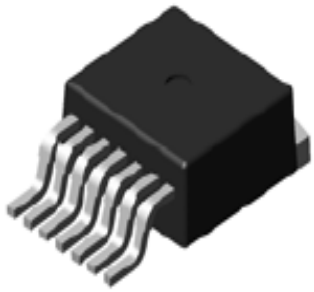


Figure 1. TO263-7L

[1] The *minimum* duty cycle is 34% when V_{BATT}=14 V, R_{SR} is shorted, and the following parameters are at their typical values: $t_{d(ON)HS}$, $t_{d(ON)LS}$, $t_{Slew(on)HS}$, and $t_{Slew(on)LS}$.

August-2017, Rev. 2

Publication order number:
FAN7093-F085/D

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN7093-F085	-40 to +150°C	8-Lead, TO263, Molded, JEDEC Variation CA	Tape & Reel

Block Diagram

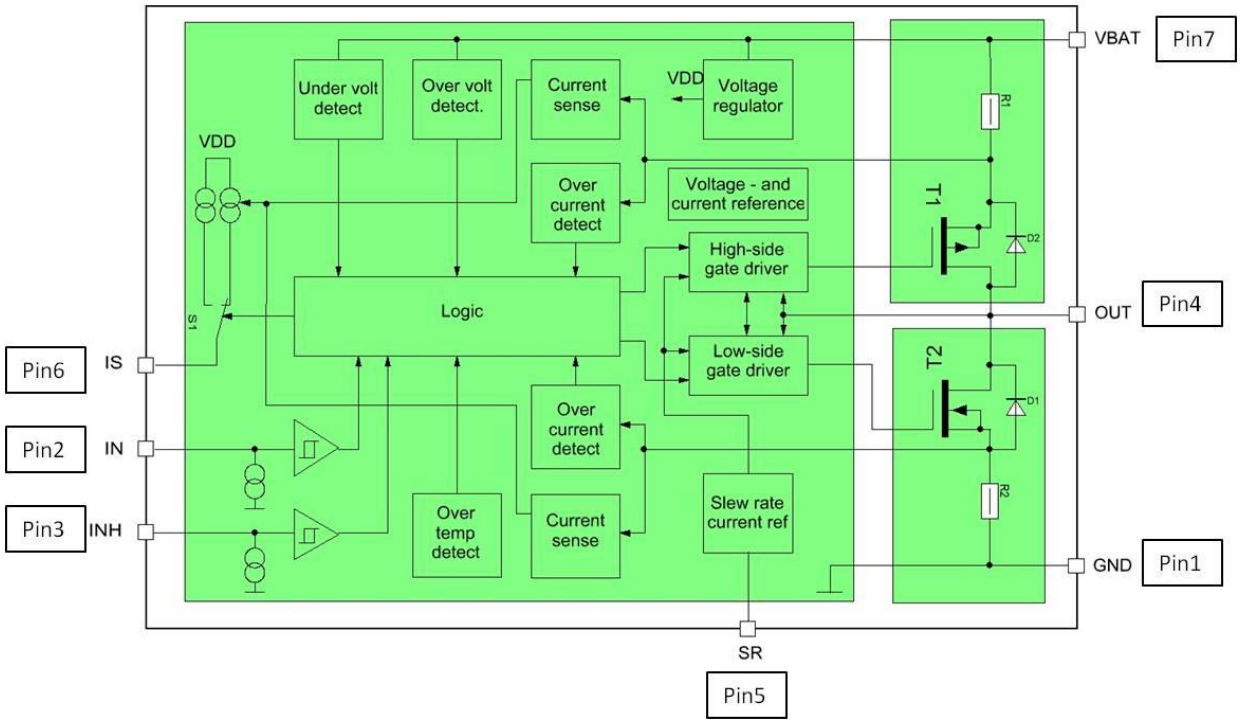


Figure 2. Block Diagram

The FAN7093 is a high-current half-bridge that contains three separate chips in one package: one P-channel high-side MOSFET, one N-channel low-side MOSFET, and with a control IC. All three chips are mounted on one common lead frame, using chip-on-chip and chip–by-chip technologies. The power MOSFETs are vertical MOS transistors to ensure minimum on-state resistance.

Using a P-channel high-side switch eliminates a charge pump and reduces EMI. A microcontroller is able to control the logic level inputs of IN and /INH of the half-bridge. The diagnostic pin IS is a current output stage that delivers a proportional current through the P-channel and N-channel MOSFETS, depending on which is being activated, with the IN or /INH pin forcing conditions. In case of a short to VBATT or ground, the IS pin acts as an error flag. The error flag can be detected as a logic HIGH level through an attached microcontroller. In an over-current situation, the control IC turns off the MOSFETs and tries to turn them back on after a cool down time of 140 µs (typical). The control IC protects the MOSFETs against over-voltage, under–voltage, and over–temperature conditions. The dead time, to prevent shoot-through between the P- and N-channel MOSFET, is also generated by the control IC. The slew rate of the outputs can be adjusted through an external resistor connected to the SR pin. The FAN7093 can be combined with another FAN7093 to form a full-bridge drive. Multiple FAN7093 can be combined in full- or half-bridge three-phase drive configurations.

Pin Configuration

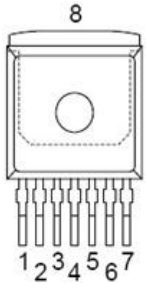


Figure 3. Pin Assignments

Pin Definitions

Pin	Symbol	I/O	Function
1	GND(1)		Ground
2	IN	I	Input. Defines whether the high-side (HS) or low-side (LS) switch is activated.
3	/INH	I	Inhibit. When set to LOW, the device enters Sleep Mode and resets Over-Temperature Protection (OTP) and the HS and LS short latch.
4, 8	OUT(1)	O	Power output of the bridge
5	SR	I	Slew rate. The slew rate of the power switches can be adjusted by connecting a resistor between the SR and GND pins.
6	IS	O	Current sense and diagnostics
7	V_{BATT}(1)		Supply

Note:
1. This pin needs power wiring.

Table 1. Truth Table

Device State	/INH	IN	HS	LS	IS	Mode
Normal Operation	LOW	X	OFF	OFF	LOW	Standby Mode
	HIGH	LOW	OFF	ON	CS	LS Active
	HIGH	HIGH	ON	OFF	CS	HS Active
Over-Voltage $I_{OUT} \le I_{CP}$	X	X	ON	OFF	HIGH	Shutdown of LS, HS Activated, Error Detected
Over-Voltage $I_{OUT} > I_{CP}$	X	X	OFF	OFF	HIGH	Shutdown of LS, HS Error Detected Reset with /INH HIGH to LOW to HIGH when condition no longer exists
Under-Voltage	X	X	OFF	OFF	LOW	UV Lockout
Over-Temperature or Shorted LS or HS	LOW	X	OFF	OFF	LOW	Standby Mode, Reset of Latch
Over-Temperature or Shorted LS or HS	HIGH	X	OFF	OFF	HIGH	Shutdown with Latch, Error Detected
Current Limit	HIGH	HIGH	OFF	ON	HIGH	Switched Mode, Error Detected(2)
	HIGH	LOW	ON	OFF	HIGH	Switched Mode, Error Detected(2)

Notes:
2. Device resumes normal operation after t_{CLS}. The error signal is reset after 2 x t_{CLS}.
3. X=Don't care input and CS=Current Sense Mode status flag.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_J = -40°C to +150°C; all voltages with respect to ground, and positive current flowing into pin (unless otherwise specified).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{BATT}	Supply Voltage[4]		-0.3		45	V
V_{IN} /V_{INH}	Logic Input Voltage[4]		-0.3		45	V
V_{SR}	Voltage at SR Pin[4]		-0.3		1.5	V
V_{IS}	Voltage at IS Pin[4]		-0.3		7.5	V
$I_{D(HS)}$, $I_{D(LS)}$	HS/LS Continuous Drain Current[4,5]	T_C < 85°C		-46/46		A
$I_{D(HS)}$, $I_{D(LS)}$	HS/LS Pulsed Drain Current[4,5]	T_C < 85°C Single Pulse < 5 µs		-90/90		A
$I_{D(HS)}$, $I_{D(LS)}$	HS/LS PWM Current[4,5]	T_C < 125°C f=1 kHz, DC=50%		-55/55		A
Temperatures						
T_J	Junction Temperature[4]		-40		150	°C
T_{STG}	Storage Temperature[4]		-55		150	°C
Electrostatic Discharge Capability (ESD)						
ESD	Human Body Model, JESD22-A114[6]	IN, /INH, SR, IS	-2		2	kV
		OUT, GND, VBATT	-6		6	

Notes:

4. Not subject to production testing, specified by design.
5. Maximum reachable current may be smaller, depending on current-limit level.
6. ESD susceptibility, HBM according to AEC-Q100-0042 / JESD22-A114-B (1.5 kΩ, 100 pF).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. On Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{BATT(NOM)}$	Supply Voltage Range for Nominal Operation		7		18	V
$V_{BATT(EXT)}$	Supply Voltage Range for Extended Operation	Parameter Deviations Possible	5.5		28.0	V
T_J	Junction Temperature		-40		150	°C
$\Theta_{JC(LS)}$	Thermal Resistance, Junction-Case, Low-Side Switch $\Theta_{JC(LS)}=\Delta T_J$ (LS) / P_V (LS)[Error! Reference source not found.]			0.8		°C/W
$\Theta_{JC(HS)}$	Thermal Resistance, Junction-Case, High-Side Switch $\Theta_{JC(HS)}=\Delta T_J$ (HS) / P_V (HS)[Error! Reference source not found.]			0.45		°C/W
Θ_{JA}	Thermal Resistance, Junction-Ambient[Error! Reference source not found.]	Using Pad Area of One Square Inch of Two-Ounce		40		°C/W

		Copper				

Note:

7. Not subject to production test; specified by design

Electrical Characteristics

Unless otherwise specified, V_{BATT} = 7 V to 18 V, T_J = -40°C to +150°C, I_L = 0 A, all voltages with respect to ground, and positive current flowing into pin.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{V_{BATT(ON)}}$	Supply Current	V_{INH}=5 V, V_{IN}=5 V, R_{SR}=0 Ω, DC-Mode, No Fault Condition			5.0	mA
$I_{V_{BATT(OFF)}}$	Quiescent Current	V_{INH}=0 V, V_{IN}=0 V			450	µA

Power Stage Characteristics

The power stages of the FAN7093 consist of a P-channel vertical DMOS transistor for the high-side switch and an N-channel vertical DMOS transistor for the low-side switch. All protection and diagnostic functions are located in the control die. Both switches can be operated up to 60 kHz[2], allowing active freewheeling and minimizing power dissipation in the forward operation of the integrated diodes.

The on-state resistance, $R_{DS(ON)}$, is dependent on the supply voltage V_{BATT} as well as on the junction temperature, T_J.

Power Stages — Static Characteristics

Unless otherwise specified, V_{BATT}=7 V to 18 V, T_J=-40°C to +150°C, all voltages with respect to ground, and positive current flowing into pin.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
High-Side Switch						
$R_{DS(ON)\_HS}$	On-State High-Side Resistance	I_{OUT}=-20 A; V_{BATT}=14 V[8]			12.3	mΩ
$I_{LEAK(HS)}$	Leakage Current	V_{INH}=0 V, V_{OUT}=0 V			50	µA
V_{RDF}	Reverse Diode Forward-Voltage[9]	I_{OUT}=-9 A			1.5	V
Low-Side Switch						
$R_{DS(ON)\_LS}$	On-State Low-Side Resistance	I_{OUT}=20 A; V_{BATT}=14 V[8]			18.2	mΩ
$I_{Leak(LS)}$	Leakage Current	V_{INH}=0 V, V_{OUT}=V_{BATT}			10	µA
	Reverse Diode Forward-Voltage[9]	I_{OUT}=9 A			-1.5	V

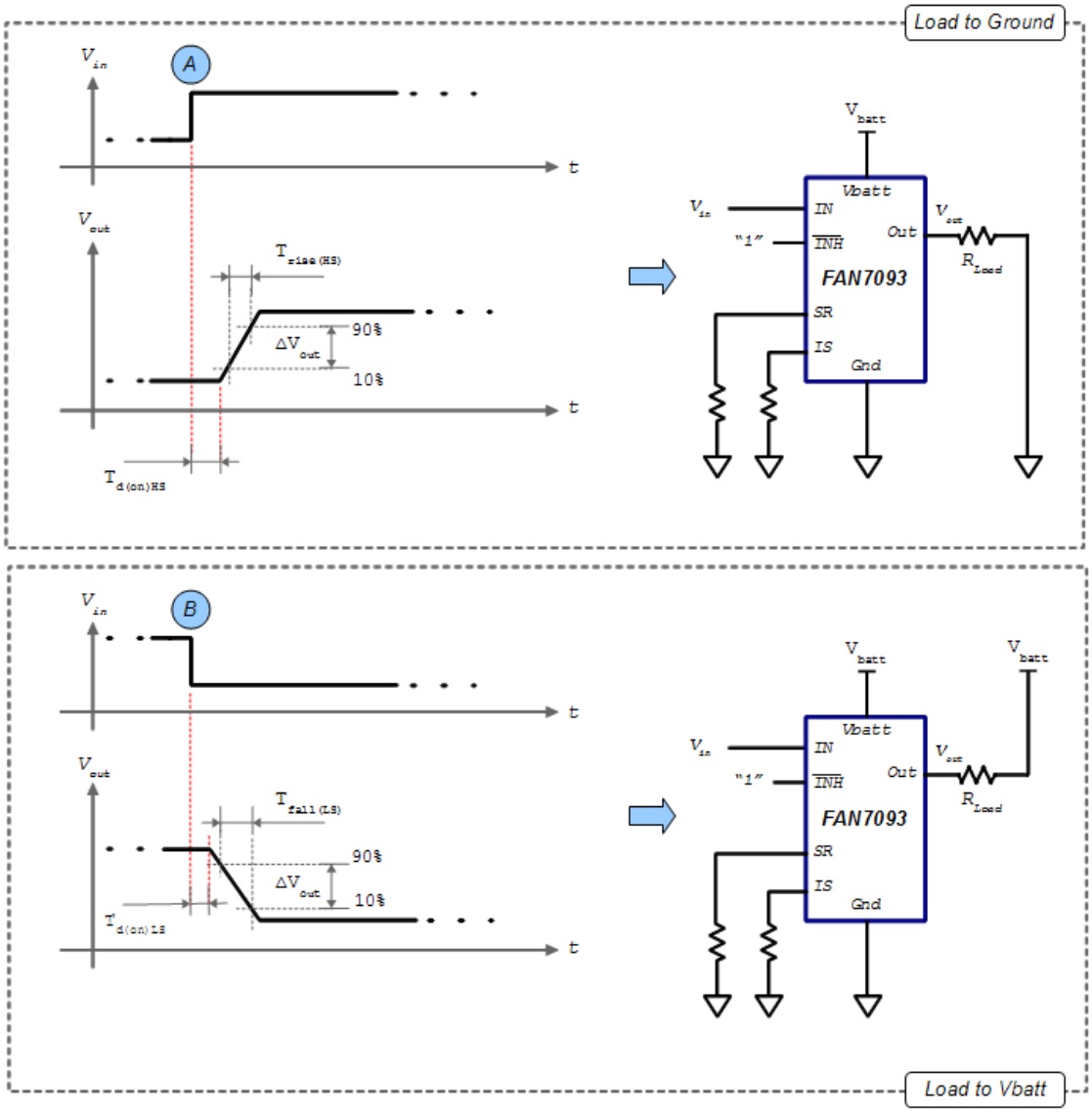
Notes:

8. Specified $R_{DS(ON)}$ value is related to normal soldering points; $R_{DS(ON)}$ values are specified for FAN7093-F085: pin 1,7 to pin 8 (tab, backside).
9. Due to active freewheeling, the diode is conducting only for a few µs, depending on the value of the external R_{SR} resistor.

[2] The *minimum* duty cycle is 34% when V_{BATT}=14 V, R_{SR} is shorted and the following parameters are at their typical values: $t_{d(ON)HS}$, $t_{d(ON)LS}$, $t_{Slew(on)HS}$, and $t_{Slew(on)LS}$.

Switching Times

Due to the timing differences for the rising and the falling edges, there is a slight difference between the length of the input pulse and the length of the output pulse, as shown in Figure 4.



$$T_{rise(HS)} = T_{rise(LS)} = \frac{\Delta V_{Out}}{V_{slew(on)HS}} \qquad T_{fall(LS)} = T_{fall(HS)} = \frac{\Delta V_{Out}}{V_{slew(on)LS}}$$

Where $V_{slew(on)HS}$ & $V_{slew(on)LS}$ have the units: $\frac{V}{\mu S}$

Figure 4. Timing Diagrams

Power Stages - Dynamic Characteristics

Unless otherwise specified; V_{BATT}=7 V - 14 V, T_J=-40°C to +150°C, R_L=2 Ω, /INH HIGH, all voltages with respect to ground, and positive current flowing into pin.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
High-Side Switch Dynamic Characteristics						
$V_{Slew(ON)HS}$	Slew Rate[10]	R_{SR}=0Ω	15	19	24	V/µs
		R_{SR}=5.1 kΩ	12	15	17	
		R_{SR}=51 kΩ	5	6	7	
		R_{SR}=Open, R_L to GND	0.8	1.0	1.2	
$t_{d(ON)HS}$	Turn-On Delay	/INH High; IN LOW to HIGH; OUT with RL to GND *(see Figure 4 top)*	0.45	2.10	4.20	µs
Low-Side Switch Dynamic Characteristics						
$V_{Slew(ON)LS}$	Slew Rate[10]	R_{SR}=0Ω	18	21	24	V/µs
		R_{SR}=5.1 kΩ	13	17	19	
		R_{SR}=51 kΩ	5	7	7	
		R_{SR}=Open, R_L to VBATT	0.8	1.2	1.2	
$t_{d(ON)LS}$	Turn-On Delay	/INH HIGH; IN HIGH to LOW; OUT with RL to V_{BATT} *(see Figure 4 bottom)*	0.45	2.10	4.20	µs

Note:

10. Not production tested.

Protection Functions

The device provides several integrated protection functions designed to prevent IC damage in fault conditions. Fault conditions are considered as “outside” the normal operating range. Protection functions are not for continuous or repetitive operation, with the exception of current-limit protection. In a fault condition, the FAN7093 applies the highest slew rate possible, independent of the connected slew rate resistor (R_{SR}). Over-voltage, over-temperature, and over-current situations are indicated by a fault current flag $I_{IS(LIM)}$ at the IS pin. The following describes the protection functions in order of priority. Over-voltage protection overrides all other protections.

Over-Voltage Protection (OVP)

To ensure a high immunity against over-voltage conditions like load dump, the device turns off the low-side MOSFET and turns on the high-side MOSFET when the supply voltage exceeds the over-voltage protection level $V_{OV(OFF)}$. The control IC returns to normal operation t_{lock}=140 µs (Typ.) after the supply voltage decreases below the over-voltage lockout level, $V_{OV(ON)}$. In H-bridge configurations, this behavior leads to freewheeling in the high side during over-voltage condition. If the load current exceeds I_{CP} in over-voltage lockout, the IC turns off the high-side driver and latches this state. See Table 1, which shows the condition of the IS pin flag. This state can be reset (if the conditions no longer exist) when /INH goes from HIGH to LOW to HIGH again.

Under-Voltage Protection (UVP)

To avoid uncontrolled motion; for example, a driven motor at low voltages; the control IC turns off all MOSFETS when the supply voltage drops below the turn-off voltage, $V_{UV(OFF)}$. The control IC resumes to normal operation when the supply voltage rises above the turn-on voltage $V_{UV(ON)}$. Notice that the IS pin does NOT flag this fault condition.

Over-Temperature Protection (OTP)

The FAN7093 is protected against over-temperature by an integrated temperature sensor in the control IC. Over-temperature protection turns off both output stages. This state is latched until the device is reset by a LOW signal with a minimum pulse length of t_{reset} at the /INH pin, assuming the control IC temperature decreased by at least the thermal hysteresis. Repetitive use of the over-temperature protection decreases product life.

Current Limitation

The current is measured in both MOSFETS. As soon as the current reaches the limit I_{CL}, the low-side or high-side MOSFET is deactivated and the other MOSFET activated for t_{CLS}. During that time, changes at the IN pin are ignored. The /INH pin can still be used to turn off both MOSFETs. After t_{CLS}, the MOSFETS return to their initial setting. The error signal at the IS pin is reset after 2 x t_{CLS}. Unintentional triggering of the current-limit circuitry through short current spikes (e.g. inflicted by EMI coming from a motor) is suppressed by an internal filter. Reaction delay of the filter circuitry affects the current limit level I_{CL}, depending on slew rate of the load current dI/dt.

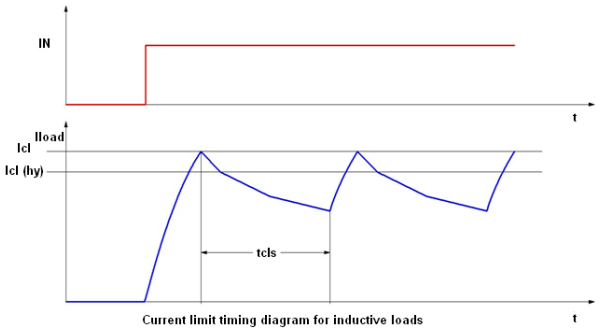


Figure 5. Current Limitation Timing Diagram (Inductive Load)

In combination with a typical inductive load, such as a motor, this results in a switched-mode current limitation. This method of limiting current has the advantage of greatly reduced power dissipation compared to driving the MOSFET in linear mode. Therefore, it is possible to use the current limitation for a short time without exceeding the maximum allowed junction temperature (e.g. for limiting the inrush current during motor startup). However, regular use of the current limitation is only allowed as long as the specified maximum junction temperature is not exceeded. Exceeding this temperature reduces the life of the device.

Short-Circuit Protection (SCP)

The device is short-circuit protected against:

- Output Shorted to Ground
- Output Shorted to Battery Voltage
- Short-Circuit between the Load Connections

The short-circuit protection is a combination of current limit and over-temperature shutdown of the device.

Electrical Characteristics - Protection Functions

Unless otherwise specified; V_{BATT}=7 V to 18 V, T_J=-40°C to +150°C, all voltages with respect to ground, and positive current flowing into pin.

Symbol	Parameter	Condition	Limit Values			Unit
			Min.	Typ.	Max.	
Under-Voltage Shutdown						
$V_{UV(ON)}$	Turn-Off Voltage	V_{BATT} Increasing			5.6	V
$V_{UV(OFF)}$	Turn-On Voltage	V_{BATT} Decreasing	4.9			V
$V_{UV(HY)}$	Hysteresis			0.15		V
Over-Voltage Lockout						
$V_{OV(ON)}$	Turn-Off Voltage	V_{BATT} Decreasing	28			V
$V_{OV(OFF)}$	Turn-On Voltage	V_{BATT} Increasing	27		35	V
$V_{OV(HY)}$	Hysteresis			1.0		V
t_{lock}	Lockout Time			140		µs
Current Limitation						
I_{CL}	Current Limit Detection Level High and Low Side		35	43	55	A
I_{CP}	Peak Current Limit Detection Level High and Low Side(11)		72	88	105	A
Current Limitation Timing						
t_{CLS}	Shut-Off Time for HS and LS		100	150	200	µs
Thermal Shutdown						
$T_{SD(SENSE)}$	Turn-Off Temperature Sense		170		190	°C
$T_{SD(SENSE)}$	Turn-On Temperature Sense		150		170	°C
$T_{SD(HYS)}$	Thermal Hysteresis			15		K
t_{reset}	Reset Pulse at /INH Pin (/INH LOW)		4			µs

Note:

11. Not production tested; specified by design.

Control and Diagnostics

Input Circuit

The internal gate drivers for the MOSFETS are controlled through inputs IN and /INH and are TTL / CMOS-compatible Schmitt triggers with hysteresis. Setting the /INH pin to HIGH enables the device. In this condition, one of the two power MOSFETS turn on, depending on the input level of the IN pin. To deactivate both switches, the /INH pin must be set LOW. No external driver is needed. The FAN7093 can interface directly with a microcontroller as long as the maximum ratings are not exceeded.

Dead-Time Generation

The dead time is generated on the control IC to prevent shoot-through between the power MOSFETS. The dead-time is independent of the selected slew rate to reach a high PWM frequency of 60 kHz.

Adjustable Slew Rate

To optimize electromagnetic emission (EMI), the switching speed of the MOSFETs is adjustable by an external resistor. The slew rate pin, SR, allows designers to optimize the balance between emission and power dissipation within the application by connecting an external resistor R_{SR} to GND. If the SR pin is open by design or if intermittent disconnect occurs, the slew rate is set to the value shown in the Power Stages - Dynamic Characteristics table.

Status Flag Diagnostic with Current-Sense Capability

The status pin, IS, is used as a combined current sense and error flag output. In normal operation (Current-Sense Mode), a current source in the control IC is connected to the status pin, which delivers a current proportional to the forward load current flowing through the active high-side or low-side MOSFET. Current flow in the reverse direction cannot be detected except for a marginal leakage current $I_{IS(LK)}$. External resistor R_{IS} determines the voltage per output current. The current-sense ratio value is shown in the Electrical Characteristics – Control and Diagnostics table. In case of a fault condition, the status output is connected to a current source independent of the load current and provides $I_{IS(lim)}$. The maximum voltage at the IS pin is determined by the choice of the external resistor and the supply voltage. When in a current-limit condition, $I_{IS(lim)}$, is active for a time 2 x t_{CLS}; the flag indicates the error for time t_{CL} after the condition no longer exists, but constantly stays active as long as the current-limit condition exists.

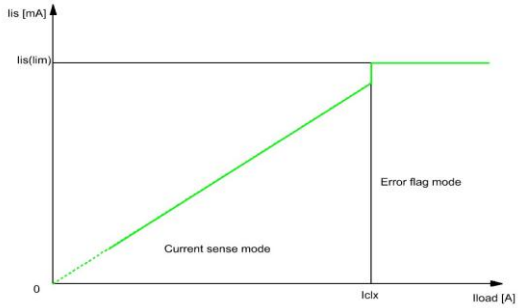


Figure 6. Sense Current vs. Load Current and Flag Current

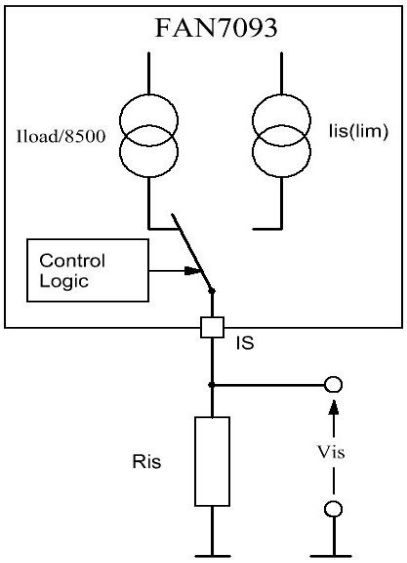


Figure 7. Current Sense Mode, Normal Operation

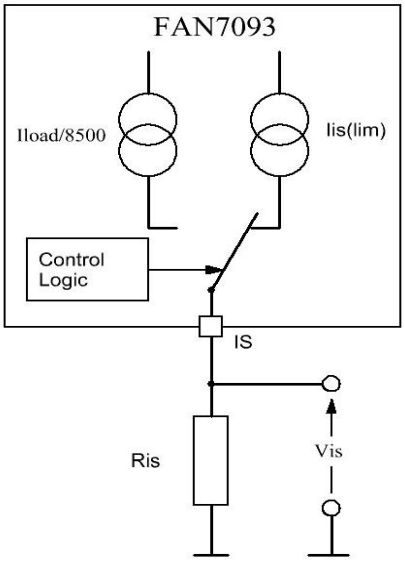


Figure 8. Error Flag Mode, Fault Condition

Electrical Characteristics - Control and Diagnostics

Unless otherwise specified, V_{BATT}=7V to 18V, T_J=-40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{INXL}	Low Level Voltage, /INH, IN		1.5			V
V_{INXH}	High Level Voltage, /INH, IN				3.5	V
$V_{INXH(HYS)}$	Input Voltage Hysteresis		500			mV
I_{INXH}	Input Current High Level	$V_{INH}=V_{IN}$=0.4 V to 5.3 V	20		80	µA
KILIS	Current Sense Ratio in Static on-Condition KILIS=I_L/I_{IS}	R_{IS}=800 Ω	4.5	8.5	13.5	10^3
		I_L=8 A to 50 A				
		I_L=1.1 A to 8 A	3.5			
$I_{IS(LIM)}$	Maximum Analog Sense Current	R_{IS}=800 Ω	4.5		5.5	mA
$I_{IS(FAULT)}$	Sense Current in Fault Condition[12]	R_{IS}=800 Ω	5.5		7.0	mA
$V_{IS(FAULT)}$	Maximum IS Output Voltage	R_{IS} ≥ 3 kΩ			7.5	V
I_{ISLEAK}	I_{SENSE} Leakage Current	/INH HIGH, IN=X, I_L=0 A			300	µA
t_{SET}	Settling time[12,13]	Resistive Load, V_{BATT}=14 V, I_L=3 A, /INH HIGH, SR to GND			4	µs

Notes:

12. Not subject to production test; specified by design.
13. The settling time is from when IN transitions 0 to 1 (the low-side goes OFF and the high-side goes ON) and 1 to 0 (the high-side goes OFF and the low-side goes ON) to when $V_{(IS)}$ reaches 90% of its final value.

Application Information

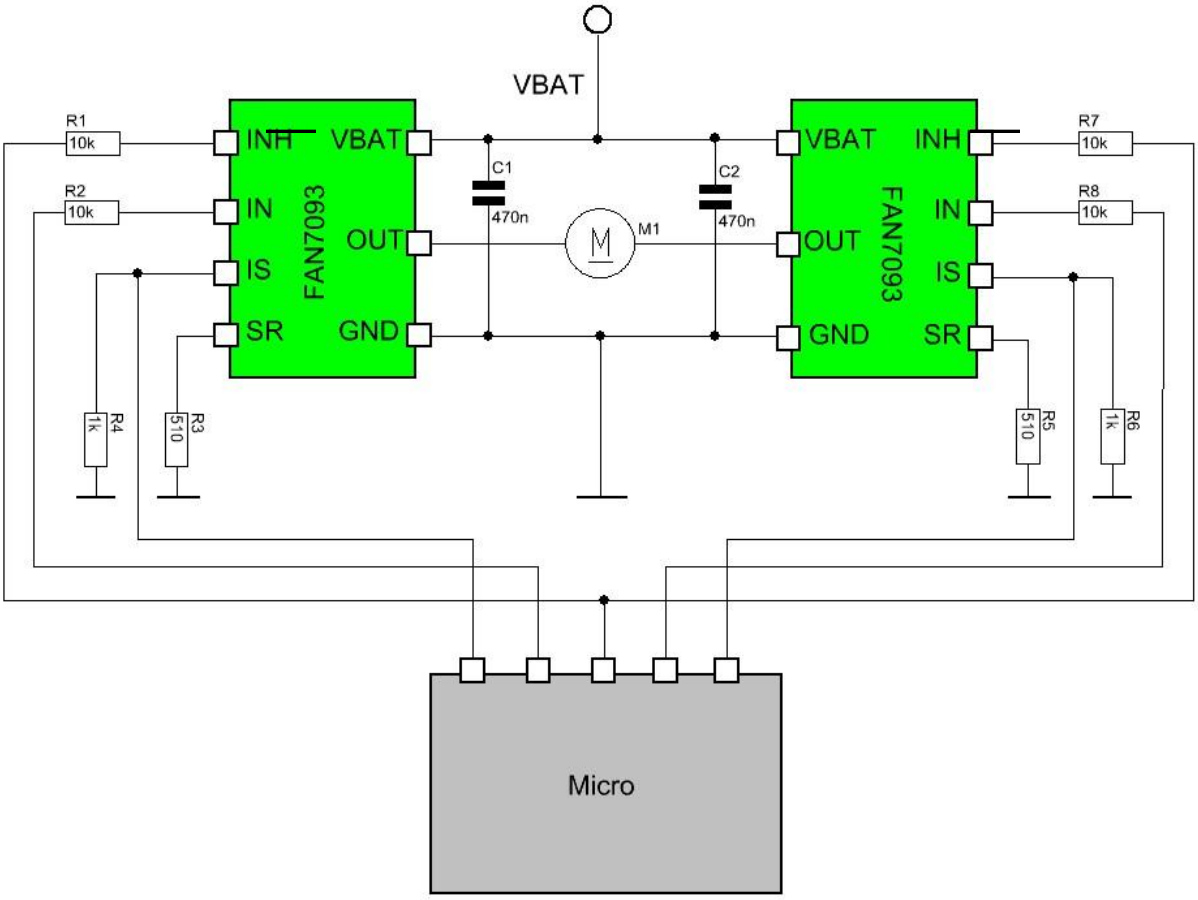


Figure 9. Full-Bridge Motor Application

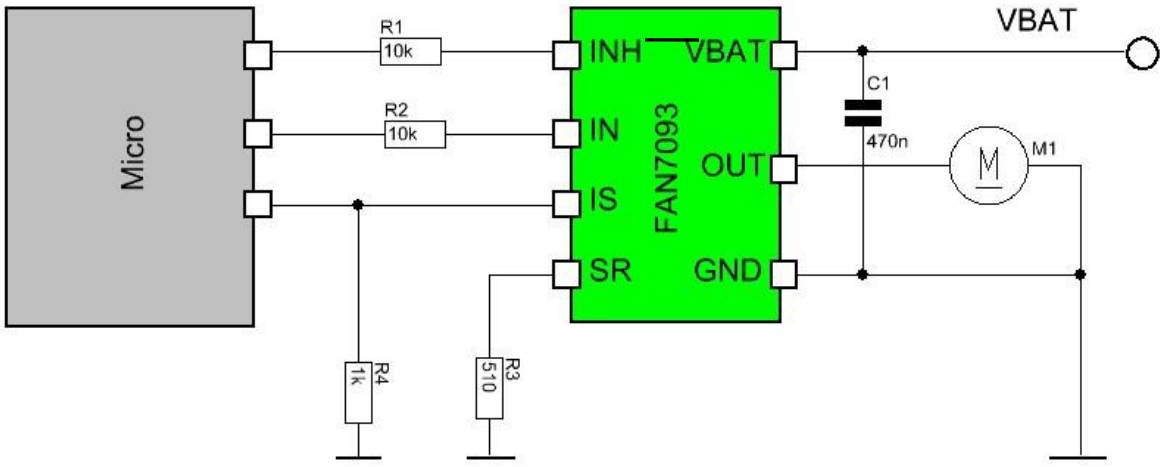


Figure 10. Half-Bridge Motor Application

Physical Dimensions

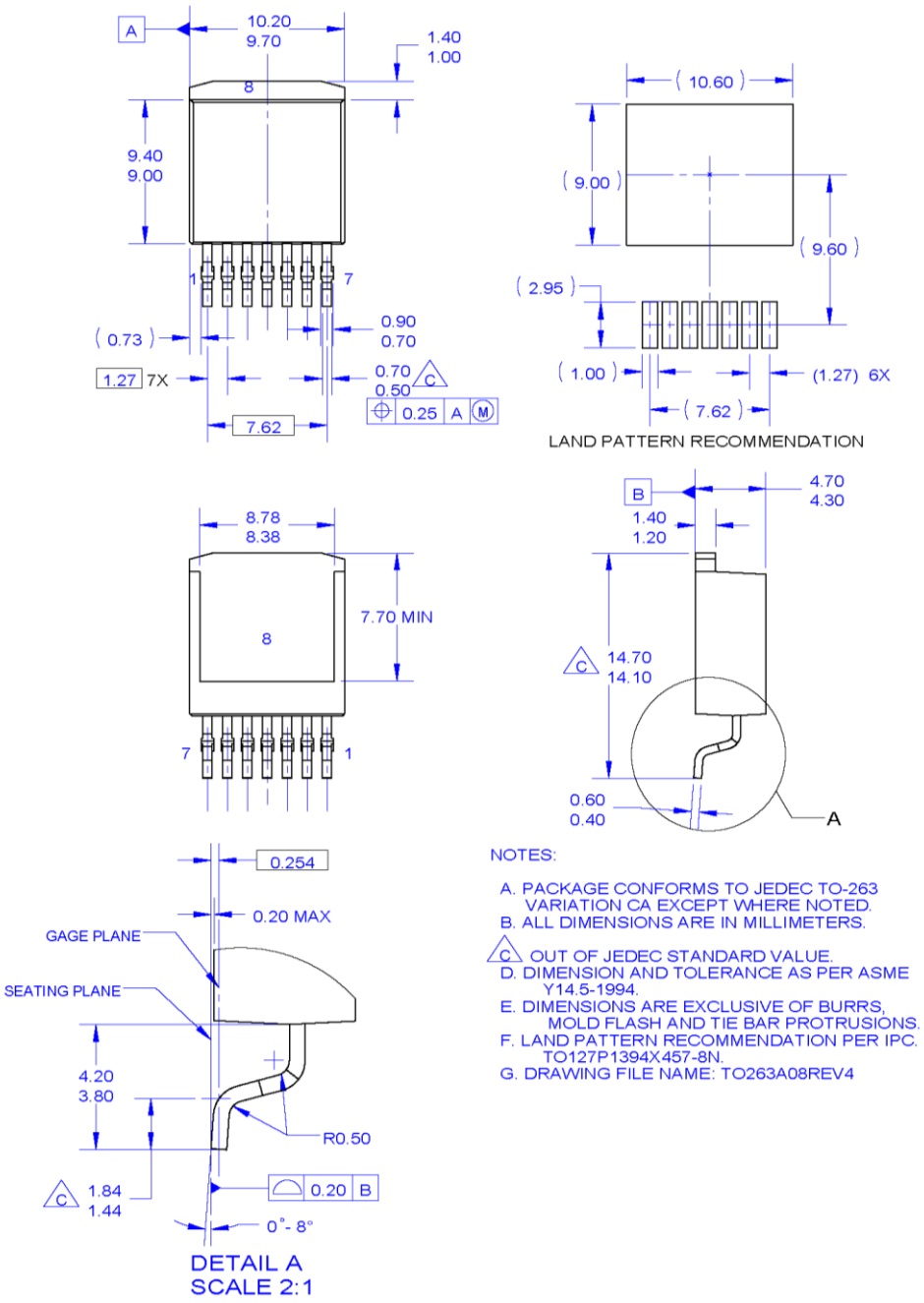


Figure 11. 8-Lead, TO263, Molded, JEDEC Variation CA

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