Dual Outputs AMOLED Display Power Supply

Check for Samples: TPS65630, TPS65630A

FEATURES

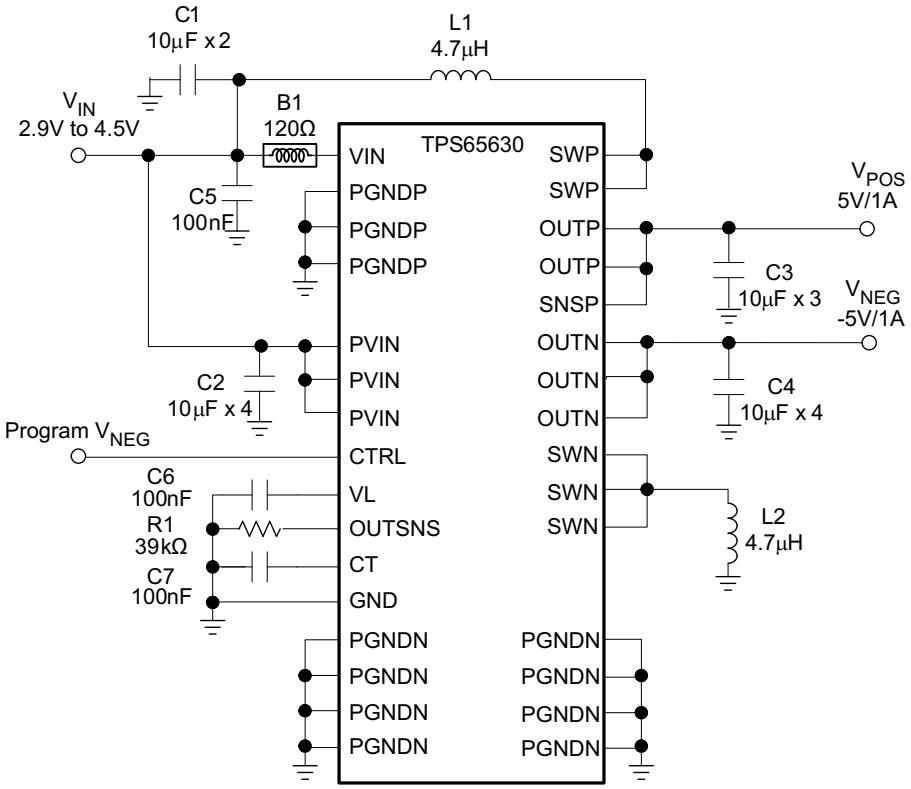
- **2.9V to 4.5V Input Voltage Range**
- **Fixed 5V V_{POS} Output Voltage**
- **0.6% Accuracy V_{POS} at 25°C to 85ºC**
- **External Output Sense Pin for V_{POS}**
- **Excellent Line Transient Regulation**
- **1A Output Current**
- **Digitally Programmable V_{NEG}**
  - **TPS65630: -1.5 to -5.5V, Default -4V**
  - **TPS65630A: -2.4 to -6.4V, Default -5V**
- **Programmable V_{POS} Output Current**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **6 x 3mm 32 pin QFN package**

APPLICATIONS

- **Active Matrix OLED**

DESCRIPTION

The TPS65630 is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring positive and negative supply rails. The device integrates a boost converter for V_{POS} and an inverting buck boost converter for V_{NEG} which are suitable for battery operated products. The digital control pin (CTRL) allows programming the negative output voltage in digital steps. The TPS65630 uses a novel technology enabling excellent line and load regulation.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERING PART NUMBER
-40°C to 95°C	32-Pin 6x3 QFN	TPS65630ARTGR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	VIN, SWP, OUTP, SNSP, PVIN		5.5	V
	OUTN		–6.5	
	SWN	–6.5	4.8	
	VL, OUTSNS, CTRL		5.5	
	CT		3.6	
ESD rating	HBM		±2	kV
	MM		±200	V
	CDM		±500	V
Operating junction temperature range, T_J		–40	50	°C
Operating ambient temperature range, T_A		–40	95	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND pin

THERMAL INFORMATION

THERMAL METRIC(1)		RTG	UNITS
		32-PINS	
θ_{JA}	Junction-to-ambient thermal resistance	35.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	24.8	
θ_{JB}	Junction-to-board thermal resistance	6.4	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	6.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.9	3.7	4.5	V
T_A	Operating ambient temperature	–40	25	95	°C
T_J	Operating junction temperature	–40	85	125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.7V, CTRL = V_{IN}, V_{POS} = 5V, V_{NEG} = –5V, T_A = –40°C to 95°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current and Thermal Protection						
V_{IN}	Input voltage range		2.9		4.5	V
I_{SD}	Shutdown current into V_{IN}	CTRL = GND		0.1		µA
V_L	Output of internal regulator			5		V
V_{UVLO}	Under-voltage lockout threshold	VIN falling			2.1	V
		VIN rising			2.4	V
	Thermal shutdown			145		°C
Output V_{POS}						
V_{POS}	Positive output voltage			5		V
	Positive output voltage regulation	T_A = 25°C to 95°C	–0.6%		0.6%	
		T_A = –40°C to 95°C	–0.8%		0.8%	
$r_{DS(on)}$	SWP MOSFET on-resistance	I_{SWN} = 500mA		130		mΩ
	SWN MOSFET rectifier on-resistance + Output current sense resistance	I_{SWN} = 500mA		200		mΩ
f_{SWP}	SWP Switching frequency	I_{POS} = 0mA		1.3		MHz
I_{SWP}	SWP switch current limit	Inductor valley current	2.5	3		A
$V_{P(SCP)}$	Short circuit threshold in operation	V_{POS} falling		4		V
$t_{P(SCP)}$	Short circuit detection time in operation			3		ms
$R_{P(DCG)}$	V_{POS} Discharge resistance	CTRL = GND, I_{POS} = 1mA		30		Ω
I_{LMIT}	Output current limit	R_{OUTSNS} = 36 KΩ	1.15	1.27	1.39	A
	Line regulation	I_{POS} = 400mA		0.016		%/V
	Load regulation			0.15		%/A

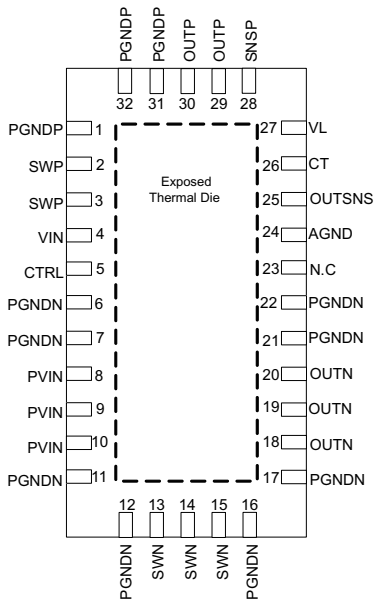
ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.7V, CTRL = V_{IN}, V_{POS} = 5V, V_{NEG} = –5V, T_A = –40°C to 95°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output V_{NEG}						
V_{NEG}	Negative output voltage default	TPS65630		–4		V
		TPS65630A		–5		V
	Negative output voltage range	TPS65630	–1.5		–5.5	V
		TPS65630A	–2.4		–6.4	V
	Negative output voltage regulation	T_A = 25°C to 95°C	–50		50	mV
$r_{DS(on)}$	SWN MOSFET on-resistance	I_{SWN} = 1 A		30		mΩ
	SWN MOSFET rectifier on-resistance	I_{SWN} = 1 A		30		mΩ
f_{SWN}	SWN Switching frequency	I_{NEG} = 0 mA		1.6		MHz
	SWN switch current limit	V_{IN} = 2.9 V	4.8			A
$V_{N(SCP)}$	Short circuit threshold in operation	Voltage drop from programmed V_{NEG}		550		mV
	Short circuit threshold in start-up		180	200	230	mV
$t_{N(SCP)}$	Short circuit detection time in start-up			10		ms
	Short circuit detection time in operation			3		ms
$R_{N(DCG)}$	V_{NEG} Discharge resistance	CTRL = GND, I_{NEG} = 1 mA		50		Ω
	Line regulation	I_{NEG} = 400 mA		0.018		%/V
	Load regulation			0.14		%/A
CTRL Interface						
V_H	Logic high-level voltage		1.2			V
V_L	Logic low-level voltage				0.4	V
R	Pull down resistor		150	400	860	KΩ
t_{INIT}	Initialization time			300	400	µs
t_{OFF}	Shutdown time period		30		80	µs
t_{HIGH}	Pulse high level time period		2	10	25	µs
t_{LOW}	Pulse low level time period		2	10	25	µs
t_{STORE}	Data storage/accept time period		30		80	µs
R_T	C_T pin output impedance		150	300	500	kΩ

DEVICE INFORMATION

(TOP VIEW)

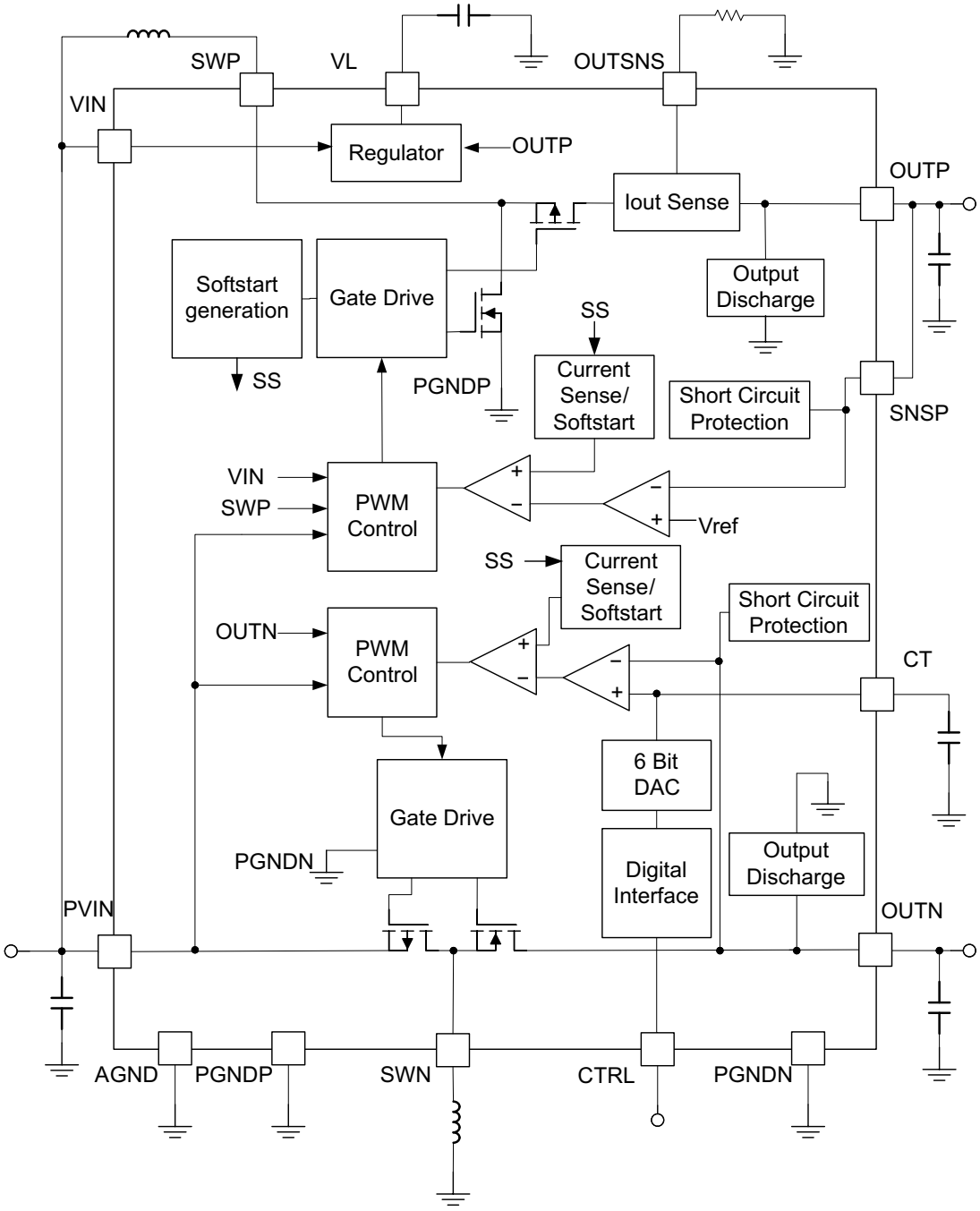


PIN FUNCTIONS

NUMBER	NAME	TYPE(1)	DESCRIPTION
1, 31, 32	PGNDP	G	Power ground of the boost converter
2, 3	SWP	I	Switch pin of the boost converter
4	VIN	I	Input voltage supply pin for analog circuit
5	CTRL	O	Combined enable device and V_{NEG} program pin.
6, 7	PGNDN	G	Power ground of buckboost converter
8 - 10	PVIN	I	Input supply for the negative buck boost converter generating V_{NEG}
11, 12	PGND	G	Power ground of buckboost converter
13 - 15	SWN	I	Switch pin of the negative buck boost converter
16, 17	PGND	G	Power ground of buckboost converter
18 - 20	OUTN	O	Output of the inverting buck boost converter
21, 22	PGND	G	Power ground of buckboost converter
23	N.C		Not connected
24	AGND	G	Analog ground
25	OUTSNS	O	Set the output current limit of V_{POS}
26	CT	O	Sets the settling time for the voltage on V_{NEG} when programmed to a new value.
27	VL	O	Output of internal regulator
28	SNSP	I	V_{POS} sense input
29, 30	OUTP	O	Output of the boost converter
	Exposed thermal pad	G	Connect this pad to analog GND.

(1) G = Ground, I = Input, O = Output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Table 1. TABLE OF GRAPHS

TITLE	TEST CONDITIONS	FIGURE
Efficiency versus Output current (Output current is from V_{POS} to V_{NEG}.)	V_{POS} 5 V, V_{NEG} -5 V	Figure 1
Start-up	V_{POS} 5 V, V_{NEG} -5 V	Figure 2
Switch pins and output waveforms	I_{OUT} 300 mA, Boost	Figure 3
	I_{OUT} 300 mA, BuckBoost	Figure 4
	I_{OUT} 900 mA, Boost	Figure 5
	I_{OUT} 900 mA, BuckBoost	Figure 6

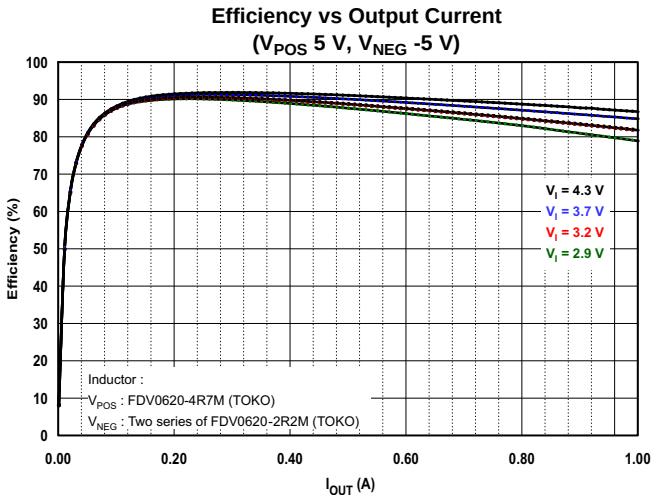


Figure 1.

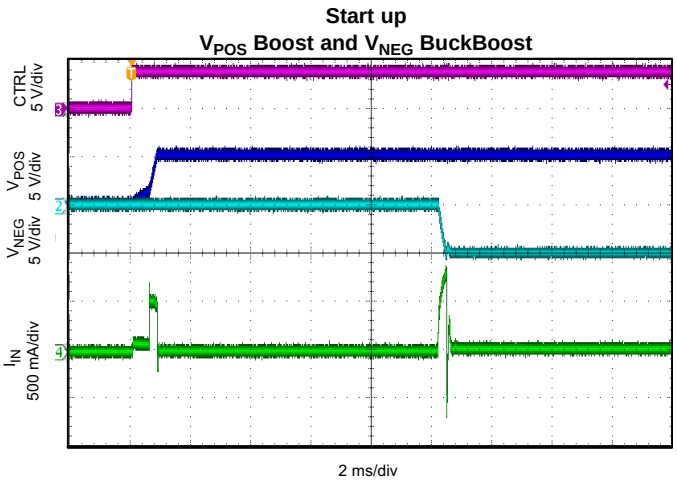


Figure 2.

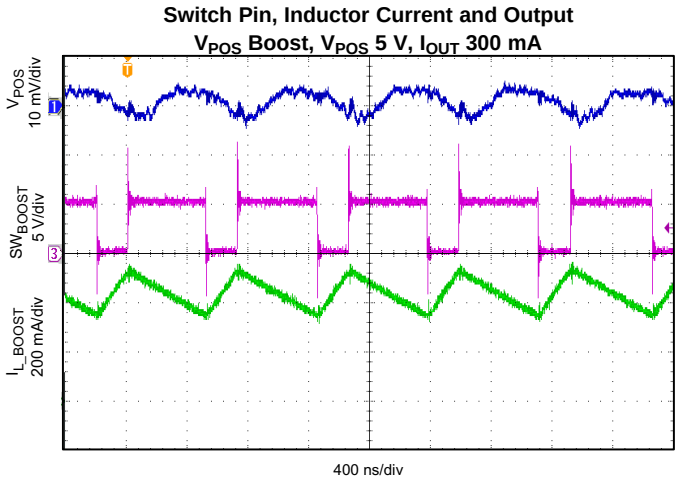


Figure 3.

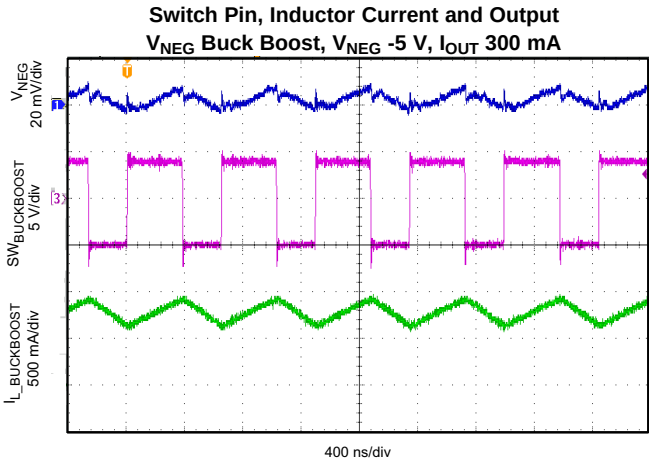


Figure 4.

Switch Pin, Inductor Current and Output
V_{POS} Boost, V_{POS} 5 V, I_{OUT} 900 mA

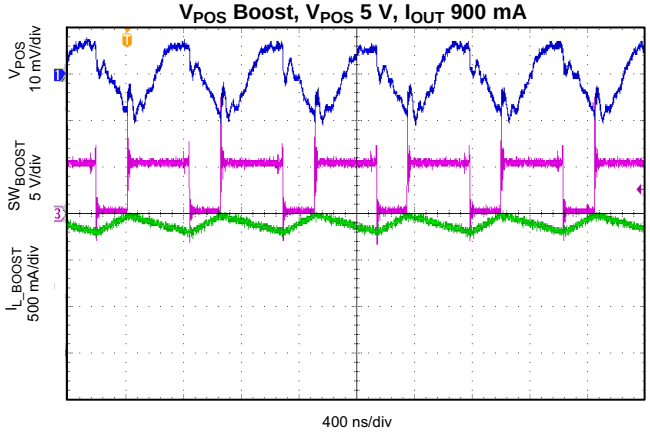


Figure 5.

Switch Pin, Inductor Current and Output
V_{NEG} Buck Boost, V_{NEG} -5 V, I_{OUT} 900 mA

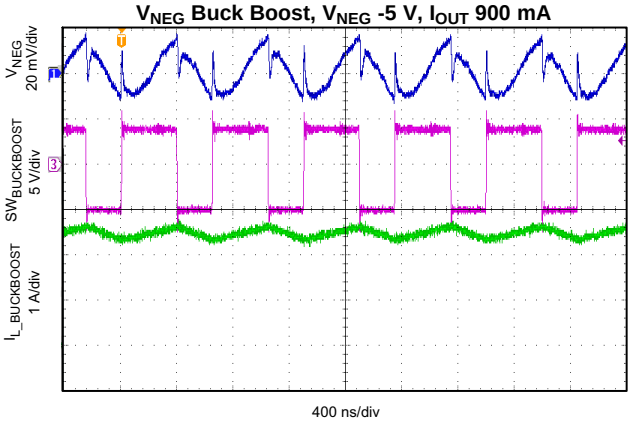


Figure 6.

APPLICATION INFORMATION

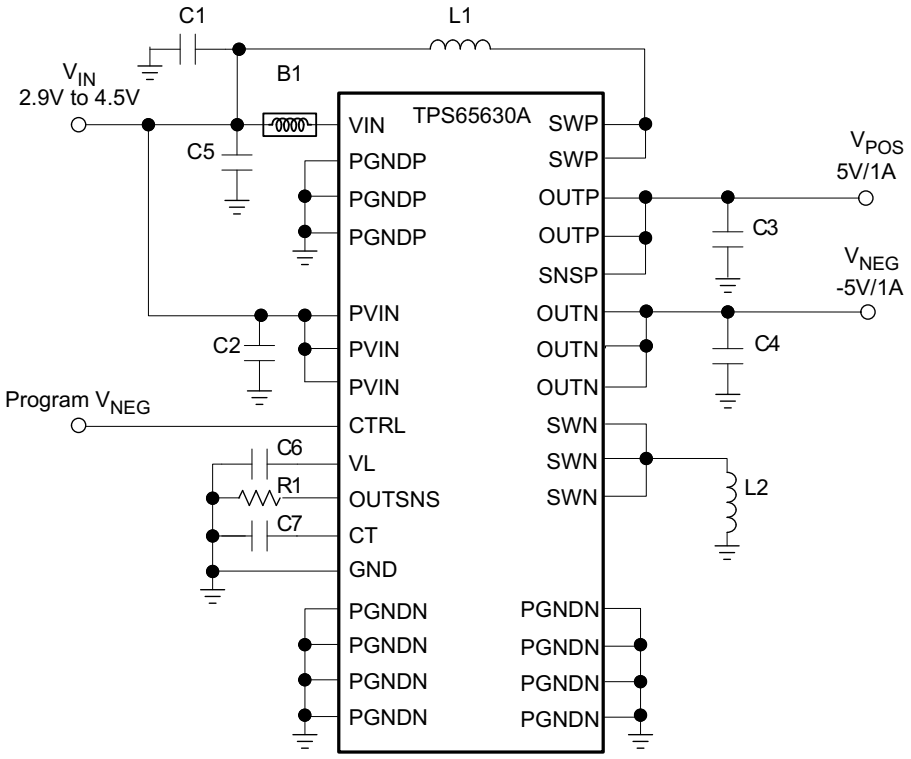


Figure 7. Application for Typical Characteristics

Table 2. Bill of Materials for Typical Characteristics

	Value	Part Number	Manufacturer
C1	2 x 10 µF	GRM21BR71A106KE51	Murata
C2	4 x 10 µF	GRM21BR71A106KE51	Murata
C3	3 x 10 µF	GRM21BR71A106KE51	Murata
C4	4 x 10 µF	GRM21BR71A106KE51	Murata
C5, C6, C7	100 nF	GRM21BR71E104KA01	Murata
B1	120 Ω	BLM18BD121SN1	Murata
R1	39 kΩ	Standard	Standard
L1	4.7 µH	FDV0620-4R7M	TOKO
L2	Two series 2.2 µH	FDV0620-2R2M	TOKO

DETAIL DESCRIPTION

The TPS65630 consists of a boost converter and an inverting buck boost converter. The positive output is fixed at 5 V. The negative output is programmable by a digital interface. TPS65630 has the negative output range of –1.5 to –5.5 V with the default of –4 V. TPS65630A has the negative output range of –2.4 to –6.4 V with the default of –5 V. The transition time of the negative output is adjustable by the CT pin capacitor.

SOFT START and START-UP SEQUENCE

The device has soft start to limit in rush current. When the device is enabled by CTRL pin going HIGH, the boost converter starts with reduced switch current limit. 10 ms after CTRL HIGH, Buck boost converter starts with the default value. V_{NEG} default is –4 V for TPS65630 and –5 V for TPS65630A. The typical start-up sequence is shown in Figure 8.

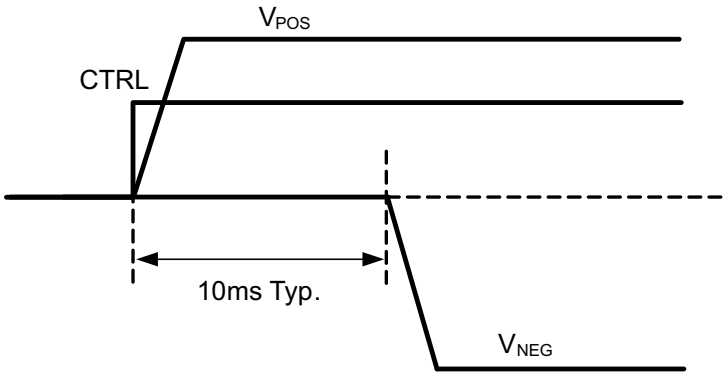


Figure 8. Start-up Sequence

ENABLE (CTRL PIN)

The CTRL pin serves two functions. One is to enable and disable the device and the other is the output programming of V_{NEG}. If the digital interface is not required the CTRL pin can be used as a standard enable pin for the device. When CTRL is pulled high, the device is enabled and the device is shut down with CTRL low.

SHORT CIRCUIT PROTECTION

The device is protected against short circuits of the outputs to ground and short circuit of the outputs each other. During normal operation, an error condition is detected if V_{POS} falls below 4 V for more than 3 ms or V_{NEG} is pulled above the programmed nominal output by 550 mV for longer than 3 ms. In either case, the device goes into shutdown and this state is latched. Input and outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

During start up, an error condition is detected in the following cases:

- V_{POS} is not in regulation 10ms after CTRL goes HIGH.
- V_{NEG} is higher than threshold level of 200mV 10ms after CTRL goes HIGH.
- V_{NEG} is not in regulation 20ms after CTRL goes HIGH.

For these cases, the device goes into shutdown and this state is latched. Input and outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or CTRL has to toggle LOW and HIGH.

PROGRAMMABLE BOOST OUTPUT CURRENT LIMIT

The device can limit boost output current and the output current limit is programmable with the external resistor to OUTSNS pin. When boost output current reaches the programmed limit value, the device goes into shutdown. This state is latched and input and outputs are disconnected. To resume normal operation, V_{IN} has to cycle below UVLO or EN has to toggle LOW and HIGH. Output current limit value with different external resistor to OUTSNS pin is shown in Table 3.

Table 3. Boost Output Current Limit Value vs. R_{OUTSNS}

Limit Value	Typ.	800 mA	820 mA	850 mA	890 mA	910 mA	950 mA	1000 mA	1100 mA	1200 mA
	Tolerance	± 120mA								
R_{OUTSNS}		56 KΩ	55 KΩ	53 KΩ	51 KΩ	50 KΩ	48 KΩ	46 KΩ	41 KΩ	38 KΩ

BEAD FILTER ON VIN PIN

The inverting buck boost converter generates the discontinuous current on the input rail. It causes big switching noise on input rail. The switching noise can couple into boost converter internal control loop through V_{IN} pin, and this can result the interference between boost converter and inverting buck boost converter. To avoid the interference, it is required to add the bead filter to VIN pin. Impedance of 120 Ω to 220 Ω bead is enough to minimize the interference. For more detail, see the PCB layout design guideline. Recommended beads are shown in Table 4.

Table 4. Recommended Beads

Impedance (at 100 MHz)	Part number	Supplier
120 Ω ±25%	BLM18BD121SN1	MURATA
150 Ω ±25%	BLM18BD151SN1	
220Ω ±25%	BLM18BD221SN1	

DIGITAL INTERFACE (CTRL PIN)

The digital interface allows programming the negative output voltage V_{NEG} in digital steps. The digital output voltage programming is implemented by a simple digital interface with the timing shown in Figure 9.

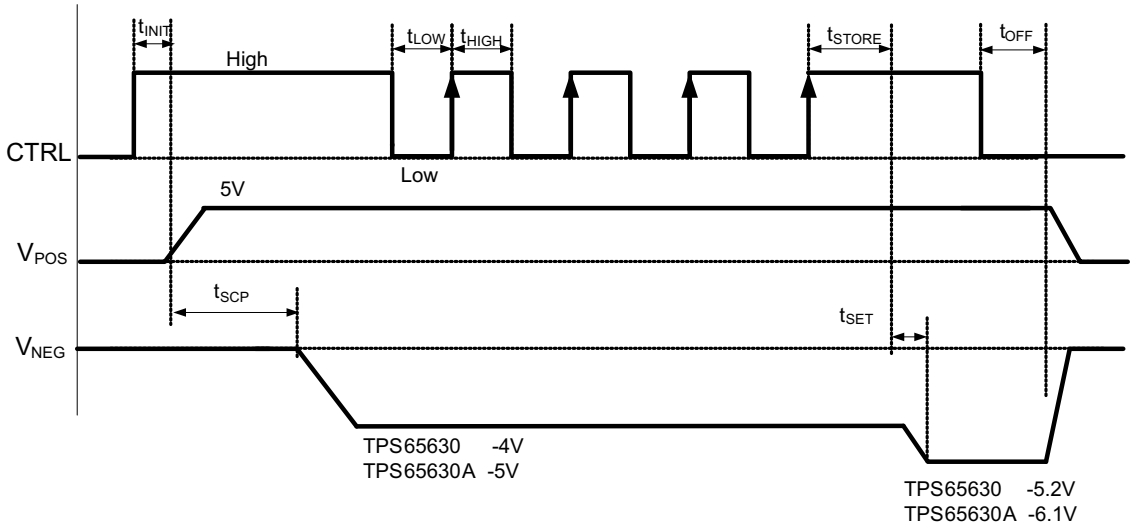


Figure 9. Digital Interface Using CTRL

Once CTRL is pulled high the device will come up with its default voltage. The device has a 6 bit DAC implemented with the corresponding output voltages as given in the table below. The interface counts now the rising edges applied to CTRL pin once the device is enable. For the programming table shown in Table 5, V_{NEG} is programmed to –5.2 V for TPS65630 and –6.1 V for TPS65630A, since 4 rising edges are detected. Other output voltages are programmed according Table 5.

Table 5. Programming Table for V_{NEG}

Bit / Rising edges	V_{NEG}		DAC Value	Bit / Rising edges	V_{NEG}		DAC Value
	TPS65630	TPS65630A			TPS65630	TPS65630A	
0/ no pulse	-4.0 V	-5 V	000000	21	-3.5 V	-4.4 V	010101
1	-5.5 V	-6.4 V	000001	22	-3.4 V	-4.3 V	010110
2	-5.4 V	-6.3 V	000010	23	-3.3 V	-4.2 V	010111
3	-5.3 V	-6.2 V	000011	24	-3.2 V	-4.1 V	011000
4	-5.2 V	-6.1 V	000100	25	-3.1 V	-4.0 V	011001
5	-5.1 V	-6.0 V	000101	26	-3.0 V	-3.9 V	011010
6	-5.0 V	-5.9 V	000110	27	-2.9 V	-3.8 V	011011
7	-4.9 V	-5.8 V	000111	28	-2.8 V	-3.7 V	011100
8	-4.8 V	-5.7 V	001000	29	-2.7 V	-3.6 V	011101
9	-4.7 V	-5.6 V	001001	30	-2.6 V	-3.5 V	011110
10	-4.6 V	-5.5 V	001010	31	-2.5 V	-3.4 V	011111
11	-4.5 V	-5.4 V	001011	32	-2.4 V	-3.3 V	100000
12	-4.4 V	-5.3 V	001100	33	-2.3 V	-3.2 V	100001
13	-4.3 V	-5.2 V	001101	34	-2.2 V	-3.1 V	100010
14	-4.2 V	-5.1 V	001110	35	-2.1 V	-3.0 V	100011
15	-4.1 V	-5.0 V	001111	36	-2.0 V	-2.9 V	100100
16	-4.0 V	-4.9 V	010000	37	-1.9 V	-2.8 V	100101
17	-3.9 V	-4.8 V	010001	38	-1.8 V	-2.7 V	100110
18	-3.8 V	-4.7 V	010010	39	-1.7 V	-2.6 V	100111
19	-3.7 V	-4.6 V	010011	40	-1.6 V	-2.5 V	101000
20	-3.6 V	-4.5 V	010100	41	-1.5 V	-2.4 V	101001

SETTING TRANSITION TIME t_{set} for V_{NEG}

The device allows setting the transition time t_{set} using an external capacitor connected to pin CT. The transition time is the time period required to move V_{NEG} from one voltage level to the next programmed voltage level. The capacitor connected to pin CT does not influence on the soft start time t_{ss} of V_{NEG} default value. When the CT pin is left open then the shortest possible transition time is programmed. When connecting a capacitor to the CT pin then the transition time is given by the R-C time constant. This is given by the output impedance of the CT pin typically 300 kΩ and the external capacitance. Within one τ the output voltage of V_{NEG} has reached 70% of its programmed value. An example is given when using 100nF for C_T.

$$\tau \approx t_{set\ 70\%} = 300k\Omega \times C_T = 300k\Omega \times 100nF = 30ms \quad (1)$$

The V_{NEG} programmed voltage is almost in nominal value after 3 τ.

PCB LAYOUT DESIGN GUIDELINES

Figure 10 and Figure 11 show the example of PCB layout design.

1. Place the input capacitor on PVIN and the output capacitor on OUTN as close as possible to device. Use short and wide traces to connect the input capacitor on PVIN and the output capacitor on OUTN.
2. VIN traces should be separated from PVIN traces. PVIN rail has big switching noises by the discontinuous current of inverting buck boost. The separation of VIN from PVIN will ensure stable operation of boost converter.
3. Place the output capacitor on OUTP as close as possible to device. Use short and wide traces to connect the output capacitor on OUTP.
4. Connect input ground and output ground on the same board layer, not through via hole.
5. AGND should be separated from PGND and connected only to exposed thermal pad. Connect AGND and PGND with exposed thermal pad.
6. Connect the ground of C_T pin capacitor and OUTSNS pin resistor with AGND, pin 24 directly.

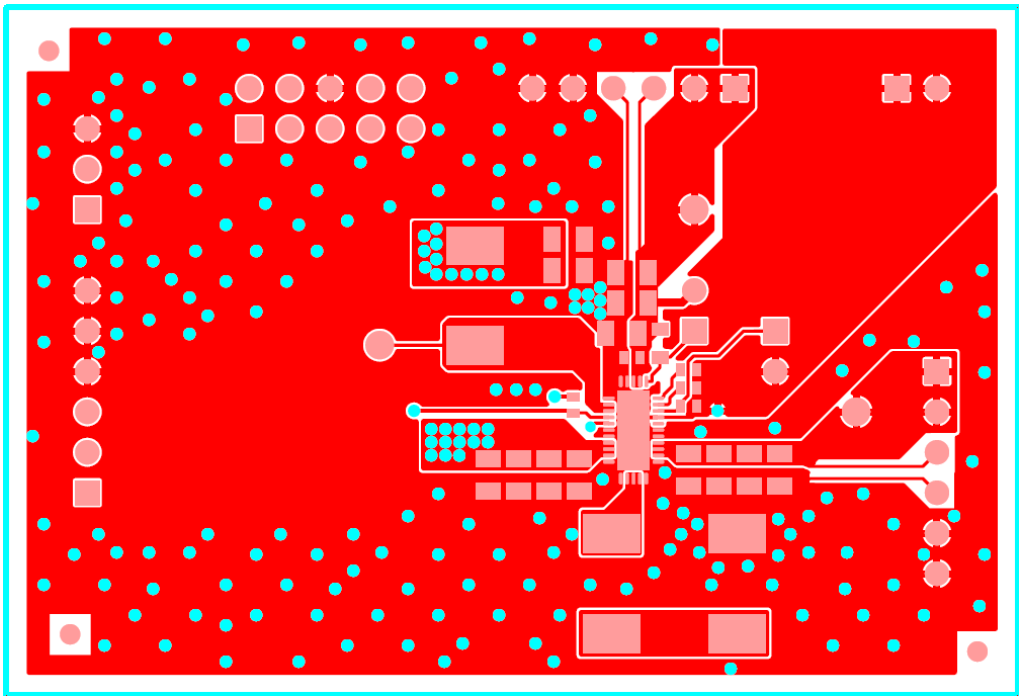


Figure 10. Example of Board Layout. Top Layer

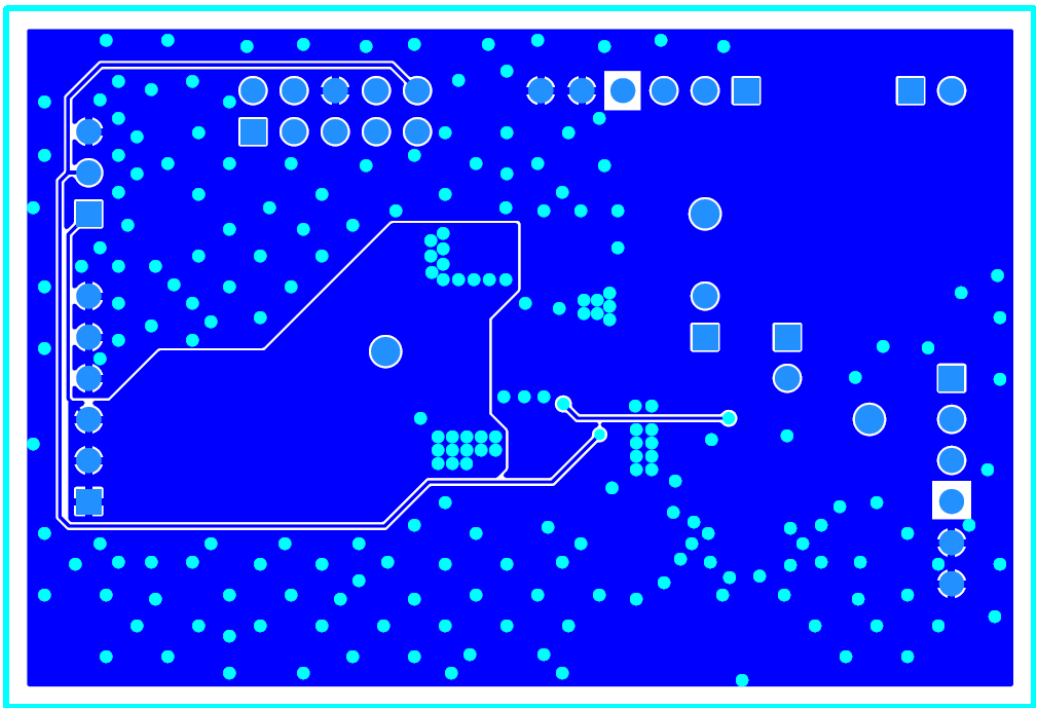


Figure 11. Example of Board Layout. Bottom Layer

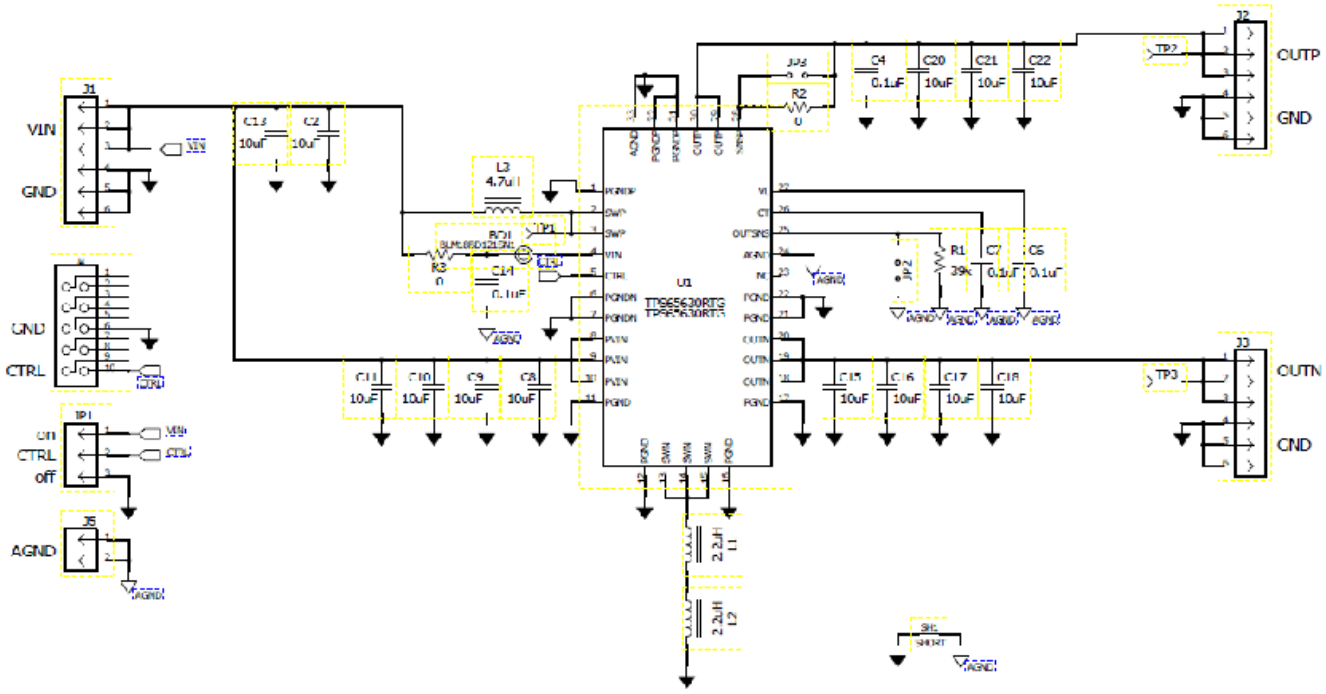


Figure 12. Schematic of Board Layout Example

PACKAGING INFORMATION

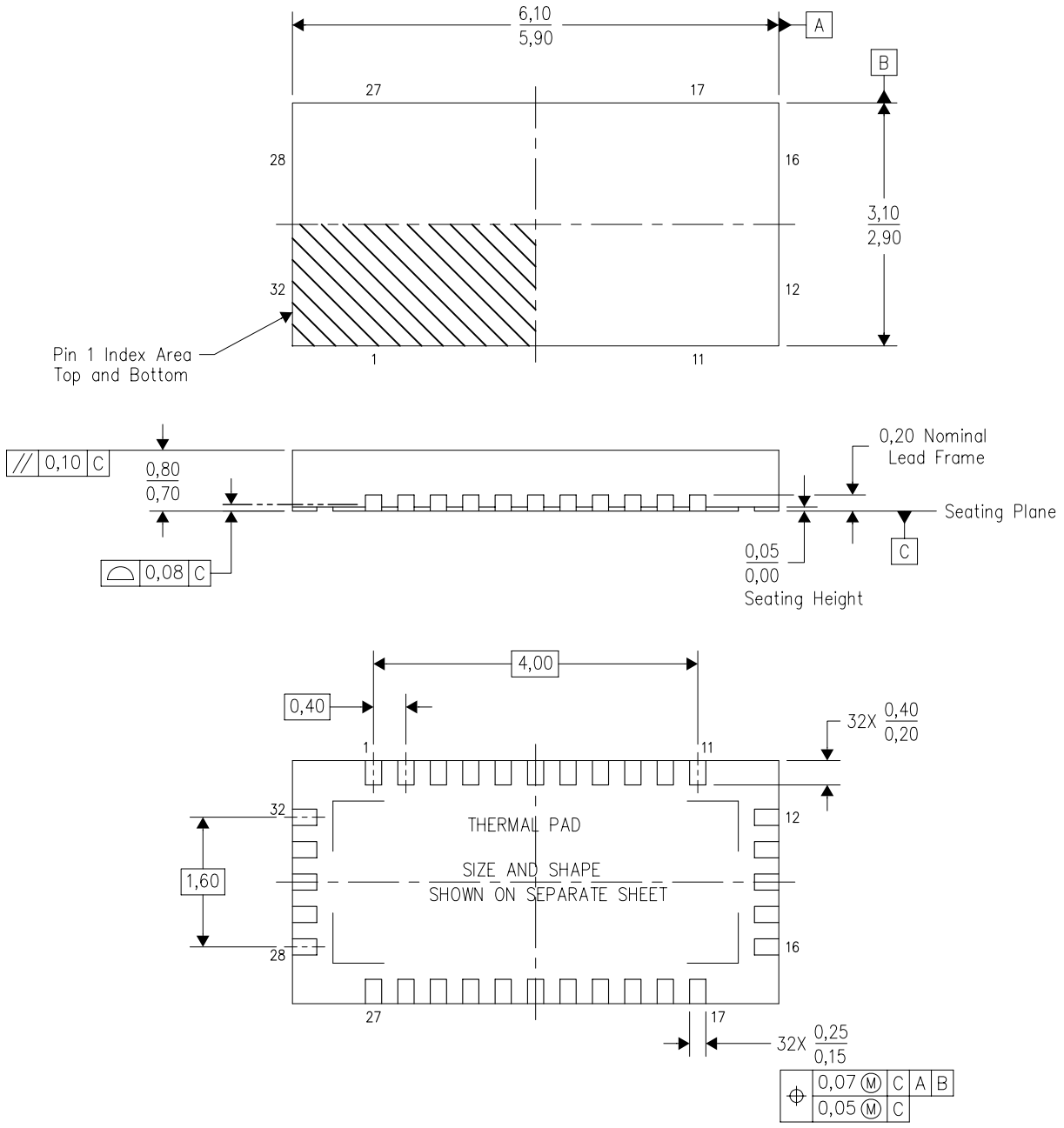
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65630ARTGR	PREVIEW	WQFN	RTG	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Reference JEDEC MO–220.

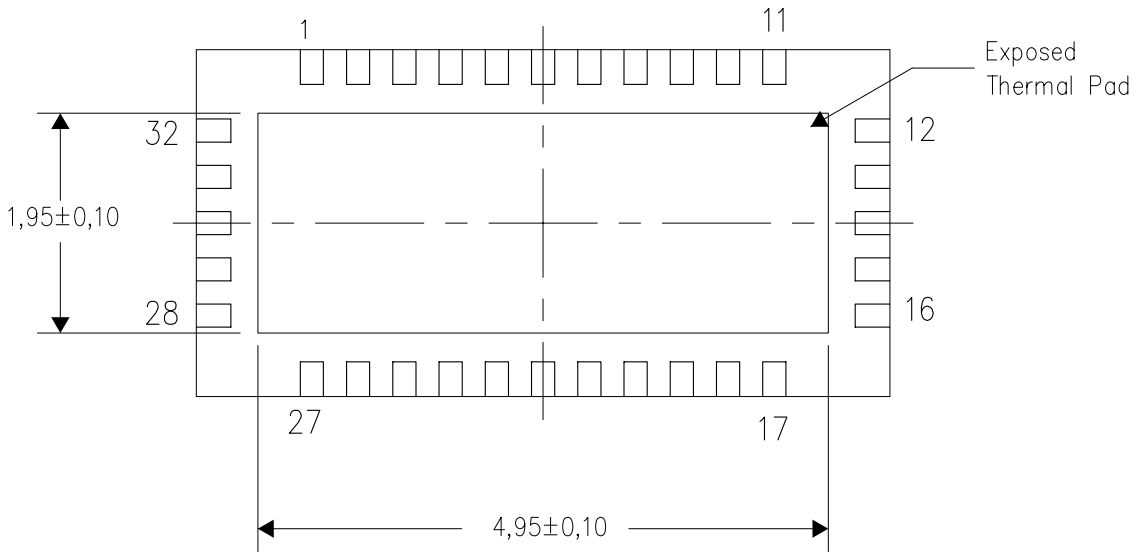
RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



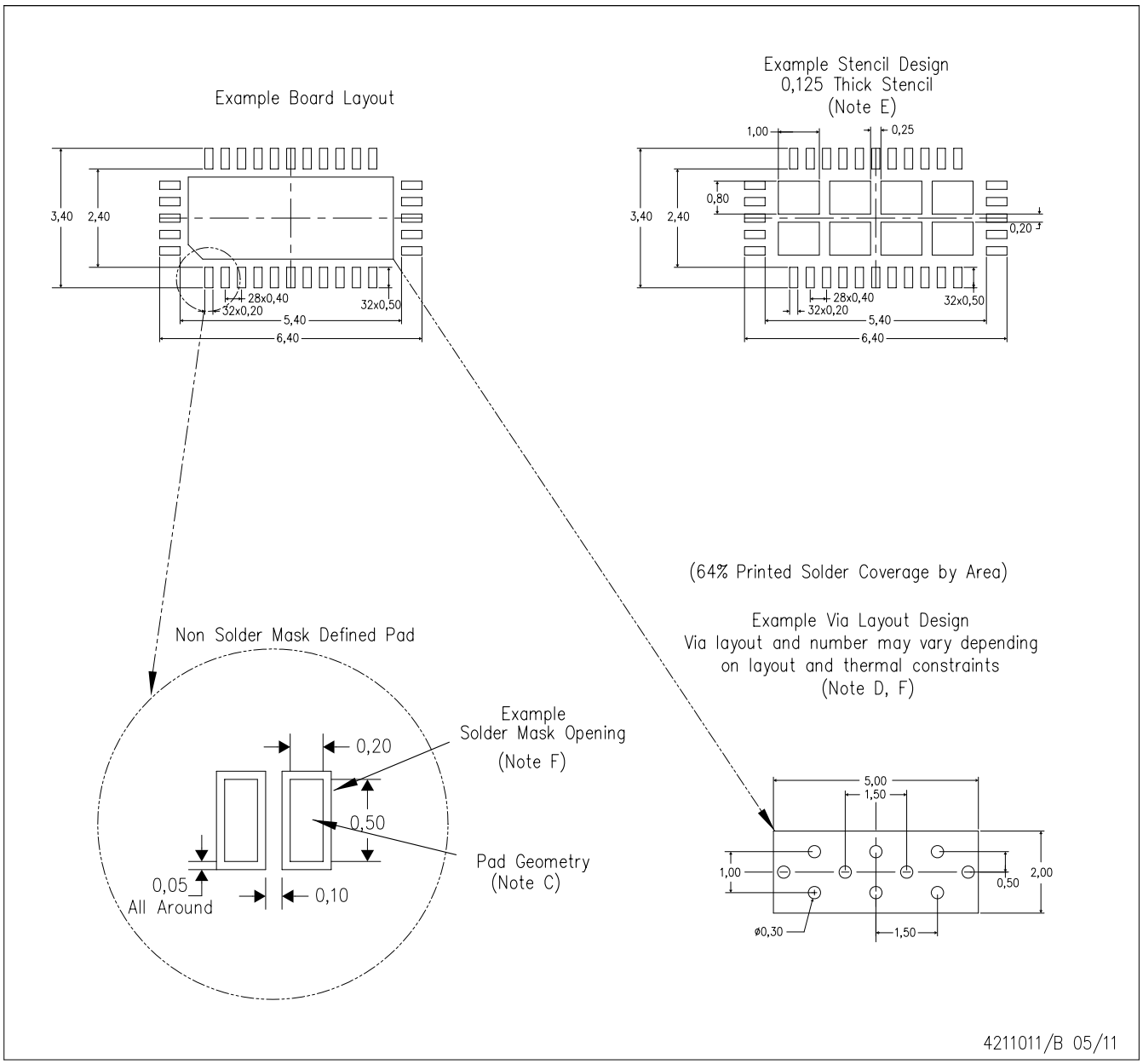
Bottom View

Exposed Thermal Pad Dimensions

4210534/C 05/11

NOTE: All linear dimensions are in millimeters

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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