Description

The F1975 Digital Step Attenuator (DSA) is a product in IDT's *Glitch-Free™* DSA Family, which is optimized for the demanding requirements of CATV and satellite systems. It operates in the frequency range of 5MHz to 3000MHz. This device is offered in a compact 4mm × 4mm, 20-pin Thin QFN package with a 75Ω impedance for ease of integration.

Advantages

Digital step attenuators are used in receivers and transmitters to provide gain control. The F1975 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (+64dBm IIP3). The device has pinpoint attenuation accuracy. Most importantly, the F1975 includes IDT's *Glitch-Free™* technology, which results in low overshoot and ringing during most significant bit (MSB) transitions.

- *Glitch-Free™* technology protects the power amplifier or analog-to-digital converter (ADC) from damage during transitions between attenuation states
- Extremely accurate attenuation levels
- Ultra-low distortion
- Low insertion loss for best signal-to-noise ratio (SNR)

Typical Applications

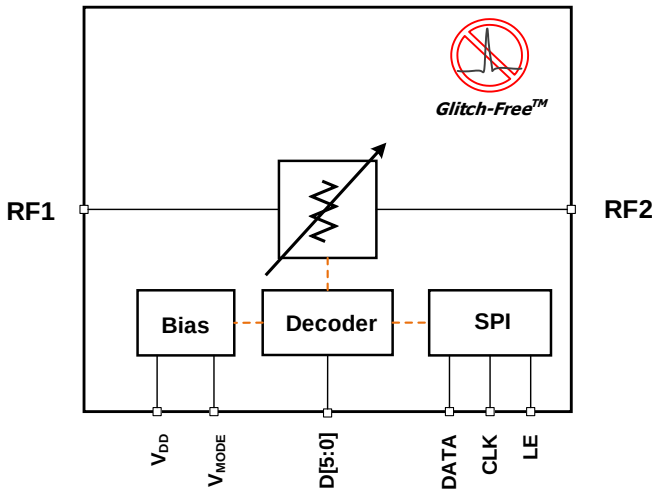
- CATV infrastructure
- CATV set-top boxes
- CATV satellite modems
- Data network equipment
- Fiber networks

Features

- Frequency: 5MHz to 3000MHz
- Serial and 6-bit parallel interface
- 31.5dB control range
- 0.5dB step
- *Glitch-Free™* technology, low transient overshoot
- 3.0V to 5.25V supply
- 1.8V or 3.3V control logic
- Attenuator step error: 0.1dB at 1GHz
- Low insertion loss: 1.2dB at 1GHz
- Ultra-linear IIP3: +64dBm
- IIP2: +125dBm typical
- Stable integral non-linearity over temperature
- Low current consumption: 550µA typical
- Bi-directional
- Operating temperature: -40°C to +105°C
- 4mm × 4mm, 20-pin QFN package

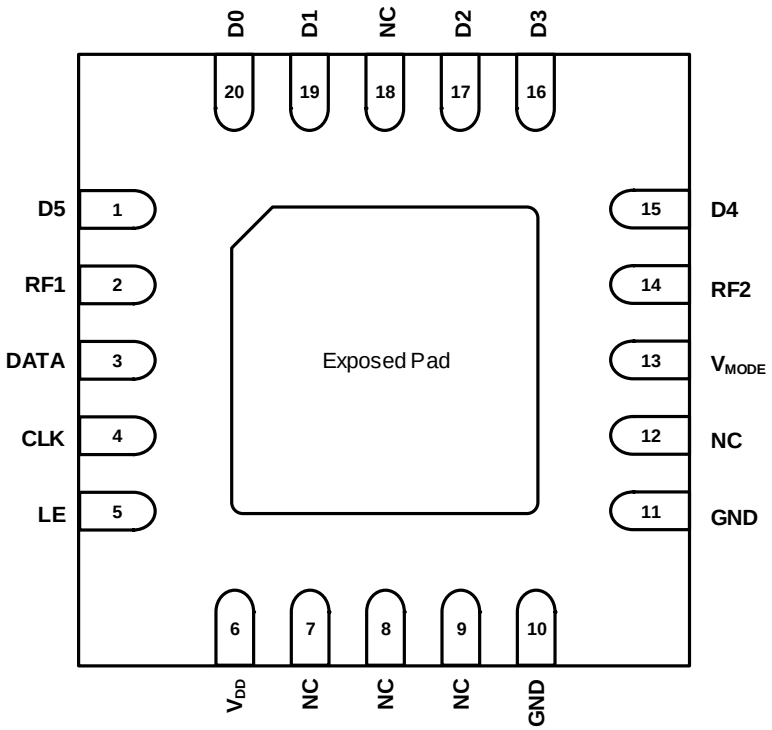
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4mm × 4mm × 0.75mm, 20-pin QFN Package – Top View (Through Package)



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	D5	16dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
2	RF1	Device RF input or output (bi-directional).
3	DATA	Serial interface data input.
4	CLK	Serial interface clock input.
5	LE	Serial interface latch enable input. Internal pull-up (100kΩ). See “Programming” section for proper usage of this line.
6	V_{DD}	Power supply pin.
7–9, 12, 18	NC	No internal connection. These pins can be left unconnected, have a voltage applied, or be connected to ground (recommended)
10, 11	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to the pin with thru vias.
13	V_{MODE}	Pull this pin HIGH for Serial Control Mode. Ground this pin for Parallel Control Mode.
14	RF2	Device RF input or output (bi-directional).
15	D4	8dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
16	D3	4dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
17	D2	2dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
19	D1	1dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
20	D0	0.5dB attenuation control bit. This pin is activated by logic HIGH (see Table 11). [a]
	EPAD	Exposed paddle. Internally connected to ground (GND). Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

[a] There is a 100kΩ pull-up resistor to the internally regulated 2.5V power supply.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1975 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions could affect device reliability.

Table 2. Absolute Maximum Ratings

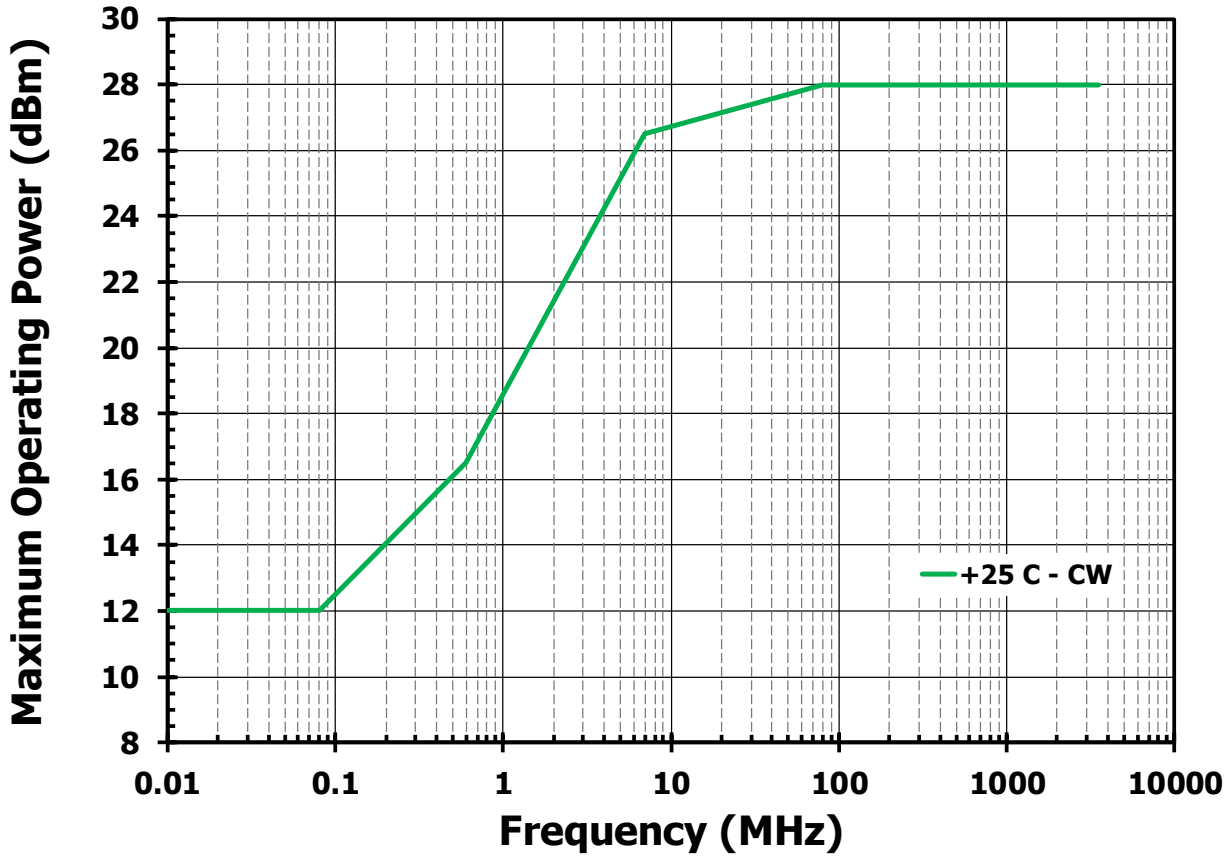
Parameter	Symbol	Minimum	Maximum	Units
V_{DD} to GND	V_{DD}	-0.3	+5.5	V
DATA, LE, CLK, D[5:0], V_{MODE}	V_{Logic}	-0.3	Minimum (V_{DD}+0.3, 3.6)	V
RF1, RF2	V_{RF}	-0.3	+0.3	V
Maximum Input Power Applied to RF1 or RF2 (>100MHz)	P_{RF}		+34	dBm
Continuous Power Dissipation	P_{diss}		1.75	dBm
Junction Temperature	T_J		+140	°C
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)			+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		250 (Class C1)	V

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage(s)	V_{DD}		3.00		5.25	V
Frequency Range	f_{RF}		5		3000	MHz
Operating Temperature Range	T_{EP}	Exposed paddle	-40		105	°C
RF CW Input Power	P_{CW}	RF1 or RF2			See Figure 3	dBm
RF1 Impedance	Z_{RF1}	Single-ended		75		Ω
RF2 Impedance	Z_{RF2}	Single-ended		75		Ω

Figure 3. Maximum Continuous Operating RF Input Power versus Input Frequency (+25°C)



Electrical Characteristics

The specifications in Table 4 apply at V_{DD} = +3.3V, T_{EP} = +25°C, f_{RF} = 1000MHz, P_{IN} = 0dBm, Serial Mode, Z_S = Z_L = 75Ω, Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted.

Table 4. Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}	All control pins				V
		V_{DD} > 3.6V	***1.17*** [a]		***3.6***	
		3.0V ≤ V_{DD} ≤ 3.6V	***1.17***		V_{DD}	
Logic Input Low Threshold	V_{IL}	All control pins			***0.63***	V
Logic Current	I_{IH}, I_{IL}	All control pins	***-35***		***+35***	µA
Supply Current [b]	I_{DD}	V_{DD} = 3.3V		550	***830***	µA
		V_{DD} = 5.0V		620	***900***	
RF1 Return Loss	S_{11}			18		dB
RF2 Return Loss	S_{22}			18		dB
Attenuation Step	LSB	Least significant bit		0.5		dB
Insertion Loss (Minimum Attenuation)	A_{MIN}	D[5:0]=[000000_{BIN}] (IL State)		1.2	2.0	dB
Attenuation Range	A_{RANGE}	D[5:0]=[111111_{BIN}]=31.5dB	30.5	31.1	31.7	dB
Step Error	DNL			0.1		dB
Absolute Error	INL	D[5:0]=[100111_{BIN}]= 19.5dB	***-0.7***		***+0.5***	dB
Insertion Phase Delta	Φ_Δ	f_{RF} = 0.5GHz (A_{MAX} to A_{MIN})		10		deg
		f_{RF} = 1.0GHz (A_{MAX} to A_{MIN})		20		
Input IP3	IIP3	P_{IN} = +10dBm/tone, f_1 = 900MHz, f_2 = 950MHz				
		Attn = 0.0dB, RF_{IN} = RF1	60	64		dBm
		Attn =15.5dB, RF_{IN} = RF1	59	62		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] Current is tested using the Serial Mode with parallel pins floating. If parallel pins are grounded, add 25µA per pin.

Electrical Characteristics (continued)

The specifications in Table 5 apply at V_{DD} = +3.3V, T_{EP} = +25°C, f_{RF} = 1000MHz, P_{IN} = 0dBm, Serial Mode, Z_S = Z_L = 75Ω, Evaluation Board (EVKit) trace and connector losses are de-embedded, unless otherwise noted.

Table 5. Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input IP2	IIP2	P_{IN} = +12dBm/tone f_1= 945MHz, f_2 = 949MHz $f_1 + f_2$ = 1894MHz RF_{IN} = RF1		125		dBm
Second Harmonic	H2	P_{IN} = +15dBm RF_{IN} = 945MHz RF_{OUT} = 1890MHz RF_{IN} = RF1		108		dBc
Input 0.1dB Compression [c]	$IP_{0.1}$	D[5:0] = [000000] = A_{MIN}, RF_{IN} = RF1		30.5		dBm
MSB Step Time	t_{LSB}	Start at LE rising edge End ±0.10dB P_{out} settling for 15.5dB to 16.0dB transition		500		ns
Maximum Spurious Level on any RF Port [d]	$SPUR_{MAX}$			-130		dBm
Maximum Switching Rate	SW_{RATE}			25		kHz
DSA Settling Time [e]	τ_{SET}	Maximum to minimum attenuation to settle to within 0.5dB of final value		0.9		µs
		Maximum to minimum attenuation to settle to within 0.5dB of final value		1.8		
Control Interface	SPI_{BIT}			6		bit
Serial Clock Speed	SPI_{CLK}				***25***	MHz

[c] The input 0.1dB compression point is a linearity figure of merit. Refer to “Absolute Maximum Ratings” section for the maximum RF input power. This specification is measured in a 50Ω system.

[d] Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

[e] Speeds are measured after SPI programming is completed (data latched with LE = HIGH).

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	50	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	3	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- V_{DD} = +3.3V
- $Z_L = Z_S$ = 75Ω single-ended
- T_{EP} = +25°C
- f_{RF} = 1GHz
- P_{IN} = 0dBm for single tone measurements
- P_{IN} = +10dBm/tone for multi-tone measurements
- Tone spacing = 50MHz
- Evaluation Board connector and board losses are de-embedded
- Measured in a 75Ω system unless otherwise specified

Typical Performance Characteristics

Figure 4. Insertion Loss vs. Frequency

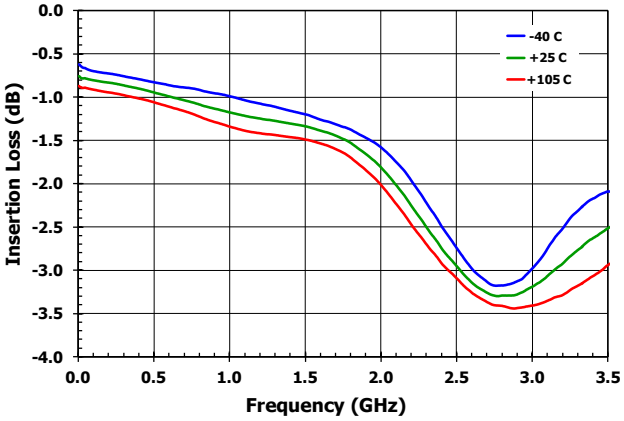


Figure 5. Insertion Loss vs. Attenuation State

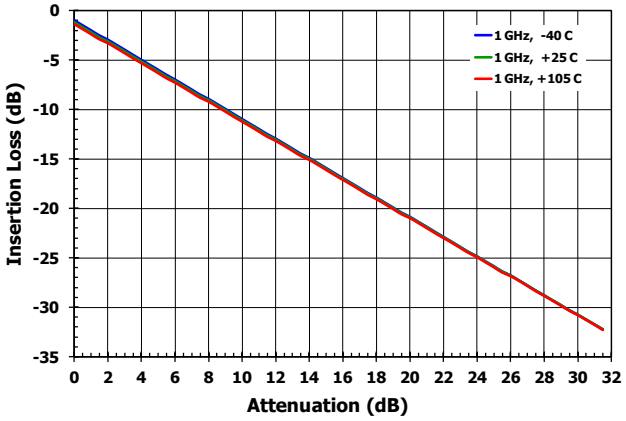


Figure 6. RF1 Return Loss vs. Frequency (All States)

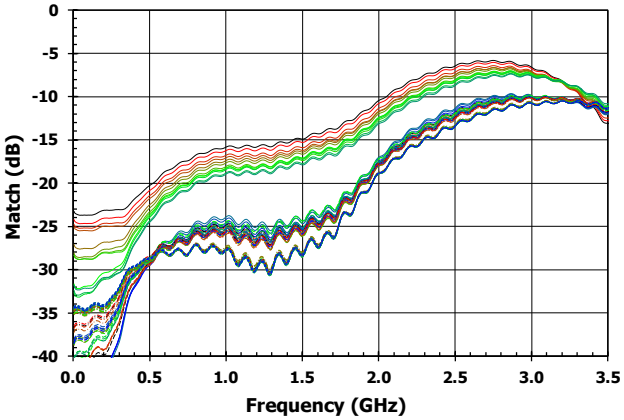


Figure 7. RF1 Return Loss vs. Attenuation State

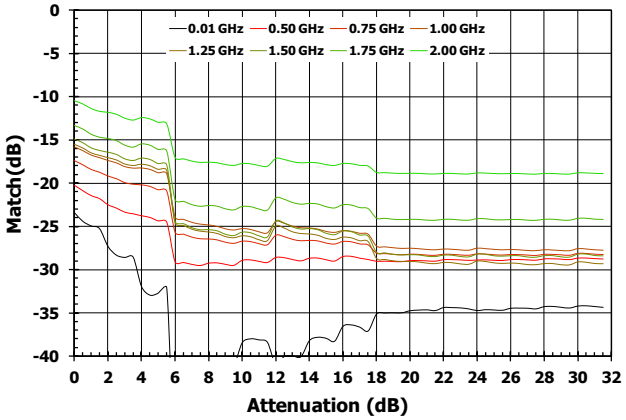


Figure 8. RF2 Return Loss vs. Frequency (All States)

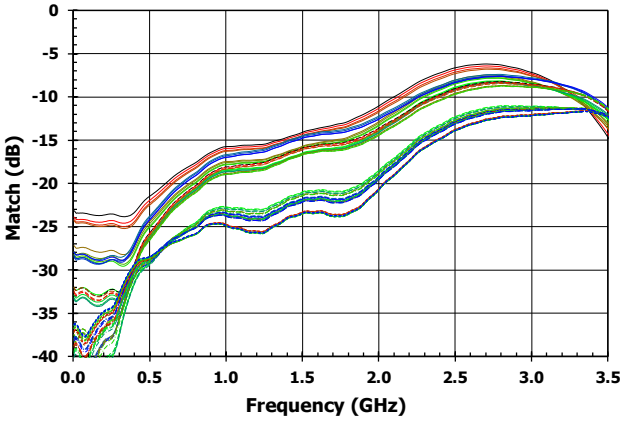
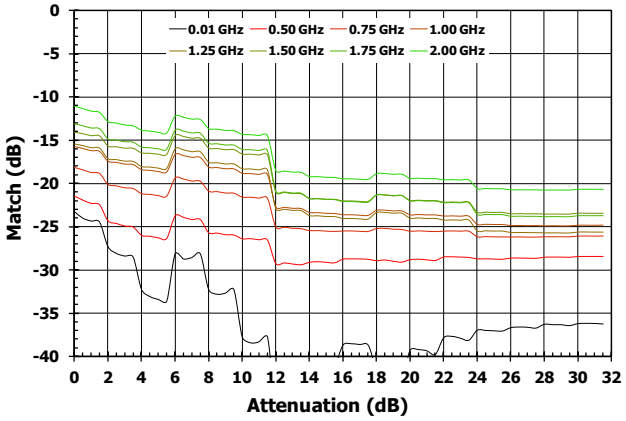


Figure 9. RF2 Return Loss vs. Attenuation State



Typical Performance Characteristics

Figure 10. Relative Insertion Phase vs. Frequency (All States)

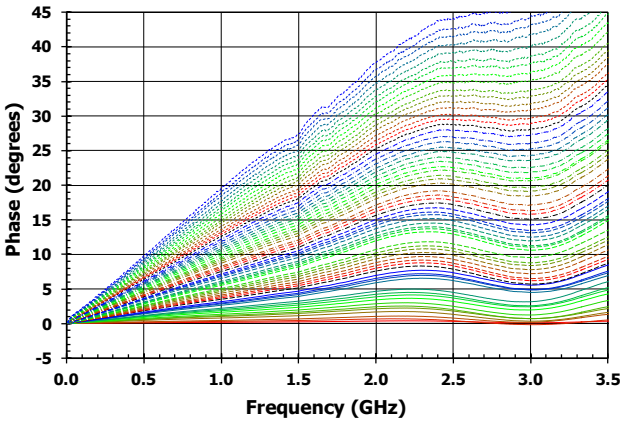


Figure 11. Relative Insertion Phase vs. Attenuation

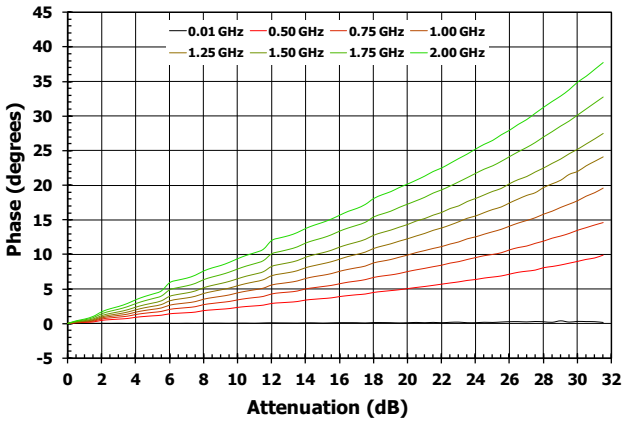


Figure 12. Worst-Case Absolute Accuracy Error

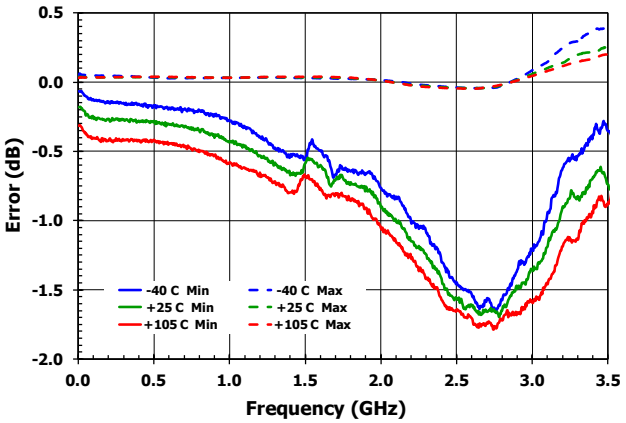


Figure 13. Accuracy Error vs. Attenuation

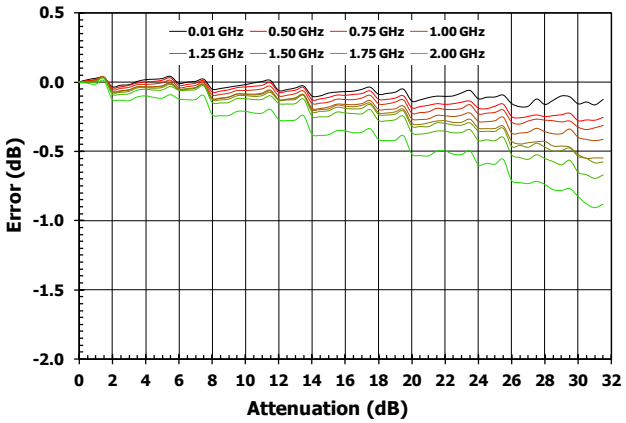


Figure 14. Worst-Case Step Accuracy

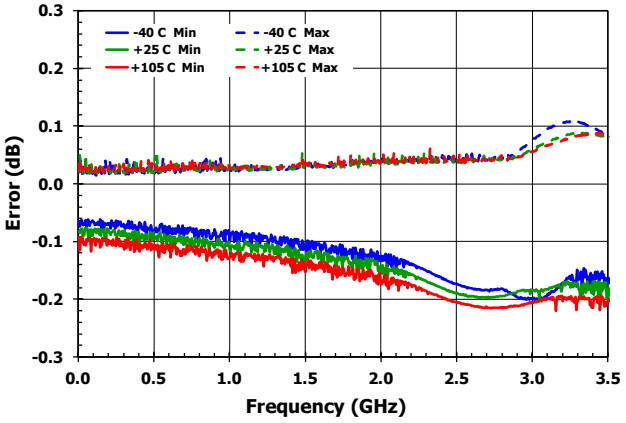
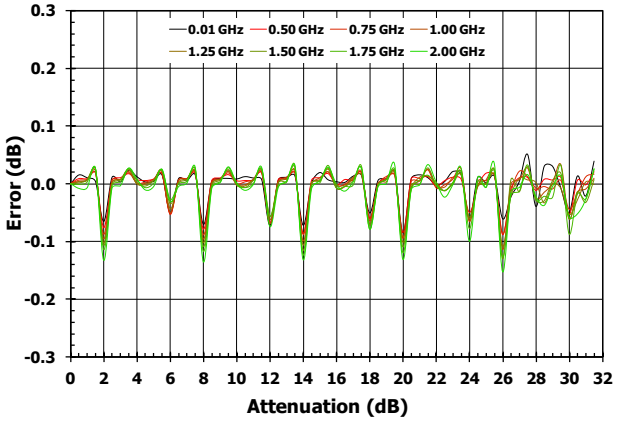


Figure 15. Step Error vs. Attenuation



Typical Performance Characteristics

Figure 16. Compression versus Input Power [Attenuation = 0.0dB]

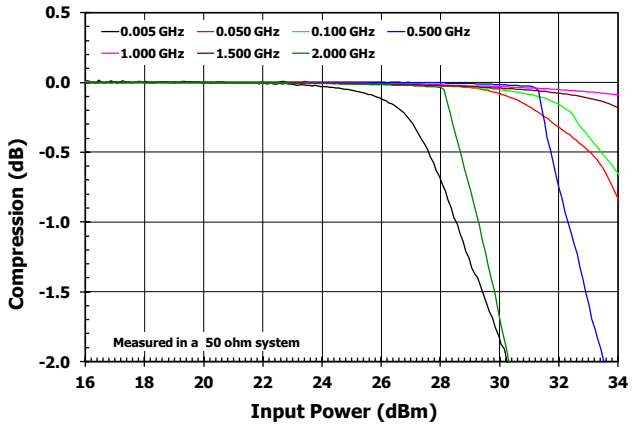
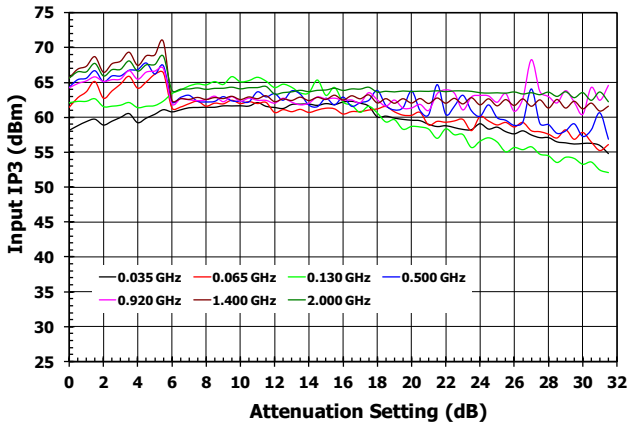


Figure 17. Input IP3 versus Attenuation Setting



Programming

The F1975 can be programmed using either the parallel or the serial interface, which is selectable via V_{MODE} (pin 13). Serial Mode is selected by floating V_{MODE} or pulling it to a logic HIGH, and Parallel Mode is selected by setting V_{MODE} to a logic LOW.

For a comparison of the F1975 and F1975 products, see the Application Note AN945 – Comparison of F1975 and F1975 Digital Step Attenuator Serial Programming Methods.

Serial Control Mode

The F1975 Serial Mode is selected by floating V_{MODE} (pin 13) or pulling it to a logic HIGH. The serial interface is a 6-bit shift register and shifts in the most significant bit (MSB) (D5 bit) first.

Table 7. 6 Bit SPI DATA Word Sequence

Bit	Definition
D5	Attenuation 16dB Control Bit
D4	Attenuator 8dB Control Bit
D3	Attenuator 4dB Control Bit
D2	Attenuator 2dB Control Bit
D1	Attenuator 1dB Control Bit
D0	Attenuator 0.5dB Control Bit

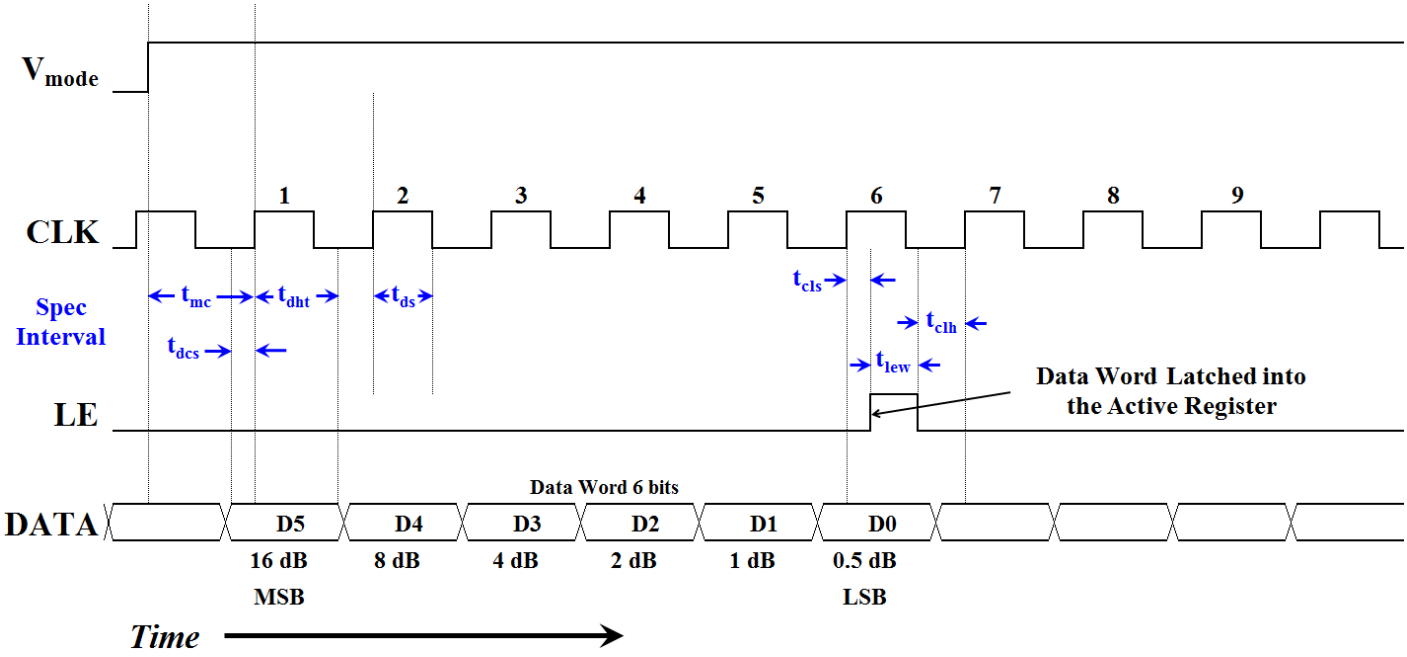
Table 8. Truth Table for Serial Control Word Bits

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

Serial Mode Programming

In the Serial Mode, the F1975 is programmed via the serial port on the rising edge of the Latch Enable (LE) signal. It is required that LE be kept at logic LOW until all data bits are clocked into the shift register. The F1975 will change its attenuation state after the data word is latched into the active register as illustrated in Figure 18. After the data word in the shift register has been latched into the active register, the LE signal must be dropped LOW. This allows shifting new data into the shift register without uploading it to the active register until the next time LE goes HIGH. The timing specification intervals are shown in blue font in Figure 18.

Figure 18. Serial Register Timing Diagram



Note: If the Serial Register programming method is used, the attenuator will change to the new attenuation state only after the data word is latched into the active register, a single programming event.

Table 9. Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{mc}	Parallel Mode to Serial Mode setup time: from the rising edge of V_{MODE} to the rising edge of CLK for the D5 bit	100		ns
t_{ds}	Clock HIGH pulse width	10		ns
t_{cls}	LE setup time: from the rising edge of the CLK pulse for D0 to LE rising edge minus half the clock period	10		ns
t_{clh}	LE hold time: from the falling edge of the LE pulse to the rising edge of CLK	10		ns
t_{lew}	LE pulse width	10		ns
t_{dcs}	Data setup time: from the starting edge of the data bit to the rising edge of CLK	10		ns
t_{dht}	Data hold time: from rising edge of CLK to falling edge of the data bit	10		ns

Serial Mode Default Startup Condition

When the device is first powered up, it will default to the maximum attenuation of 31.5dB independent of the parallel pin [D5:D0] conditions.

Table 10. Default Control Word for the Serial Mode

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
1	1	1	1	1	1	31.5

Parallel Control Mode

For the F1975, the user has the option of programming in one of two parallel modes: Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode

Direct Parallel Mode is selected when V_{MODE} (pin 13) is set to a logic LOW and LE (pin 5) is set to a logic HIGH. In this mode, the device will immediately react to any voltage changes in the parallel control pins (1, 15, 16, 17, 19, and 20). Use direct parallel mode for the fastest settling time.

Direct Parallel Default Startup Condition

In the Direct Parallel Mode, the attenuation value is determined by the logic condition of the parallel pins (1, 15, 16, 17, 19, and 20) at the time of start-up.

Latched Parallel Mode

The Latched Parallel Mode is selected when V_{MODE} is set to a logic LOW and LE (pin 5) is toggled from a logic LOW to a logic HIGH.

To utilize the Latched Parallel Mode, complete these steps:

- Set the LE pin to a logic LOW.
- Set pins 1, 15, 16, 17, 19, and 20 for the desired attenuation setting. (While LE is set to a logic LOW, the attenuation state will not change.)
- Toggle LE to a logic HIGH. The device will then transition to the attenuation settings reflected by pins D5 through D0.

Latched Parallel Default Startup Condition

The Latched Parallel Mode establishes a default attenuation state when the device is first powered up which is the maximum attenuation.

Table 11. Truth Table for the Parallel Pins

D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

Figure 19. Latched Parallel Mode Timing Diagram

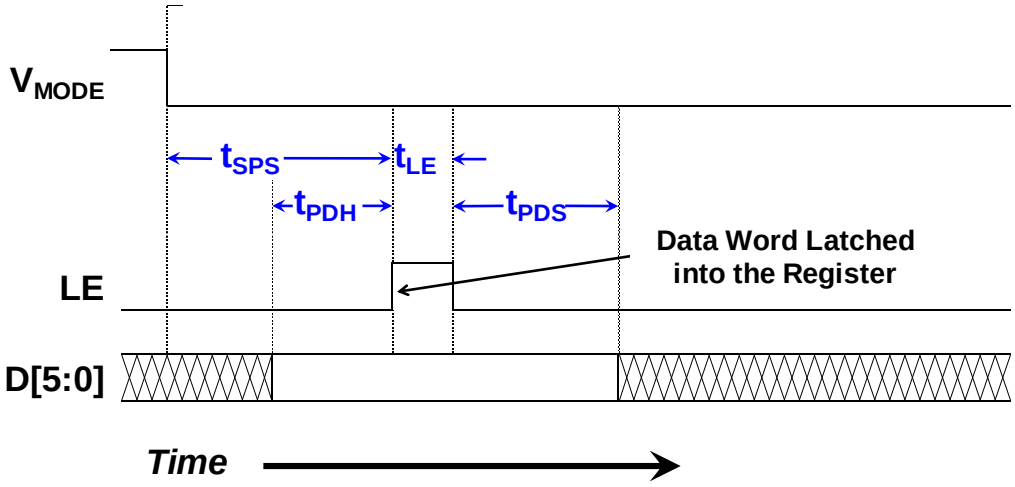


Table 12. Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Units
t_{SPS}	Serial Mode to Parallel Mode setup time	100		ns
t_{PDH}	Parallel data hold time	10		ns
t_{PDS}	LE minimum pulse width	10		ns
t_{LE}	Parallel data setup time	10		ns

Applications Information

F1975 Digital Pin Voltage and Resistance Values (Pins not Connected)

Table 13 lists the resistance between various pins and ground when no DC power is applied. When the device is powered up with +5V DC, these pins will exhibit a voltage to ground as indicated.

Table 13. Voltage and Resistance to Ground for the Logic Pins

Pin	Name	DC Voltage (Volts)	Resistance (Ohms)
13	V_{MODE}	2.5V	100kΩ pull-up resistor to internally regulated 2.5V.
3, 4, 5	DATA, CLK, LE	2.5V	100kΩ pull-up resistor to internally regulated 2.5V.
1, 15–17, 19, 20	D5, D4, D3, D2, D1, D0	2.5V	100kΩ pull-up resistor to internally regulated 2.5V.

Figure 20. F1975EVBI Evaluation Board – Top View

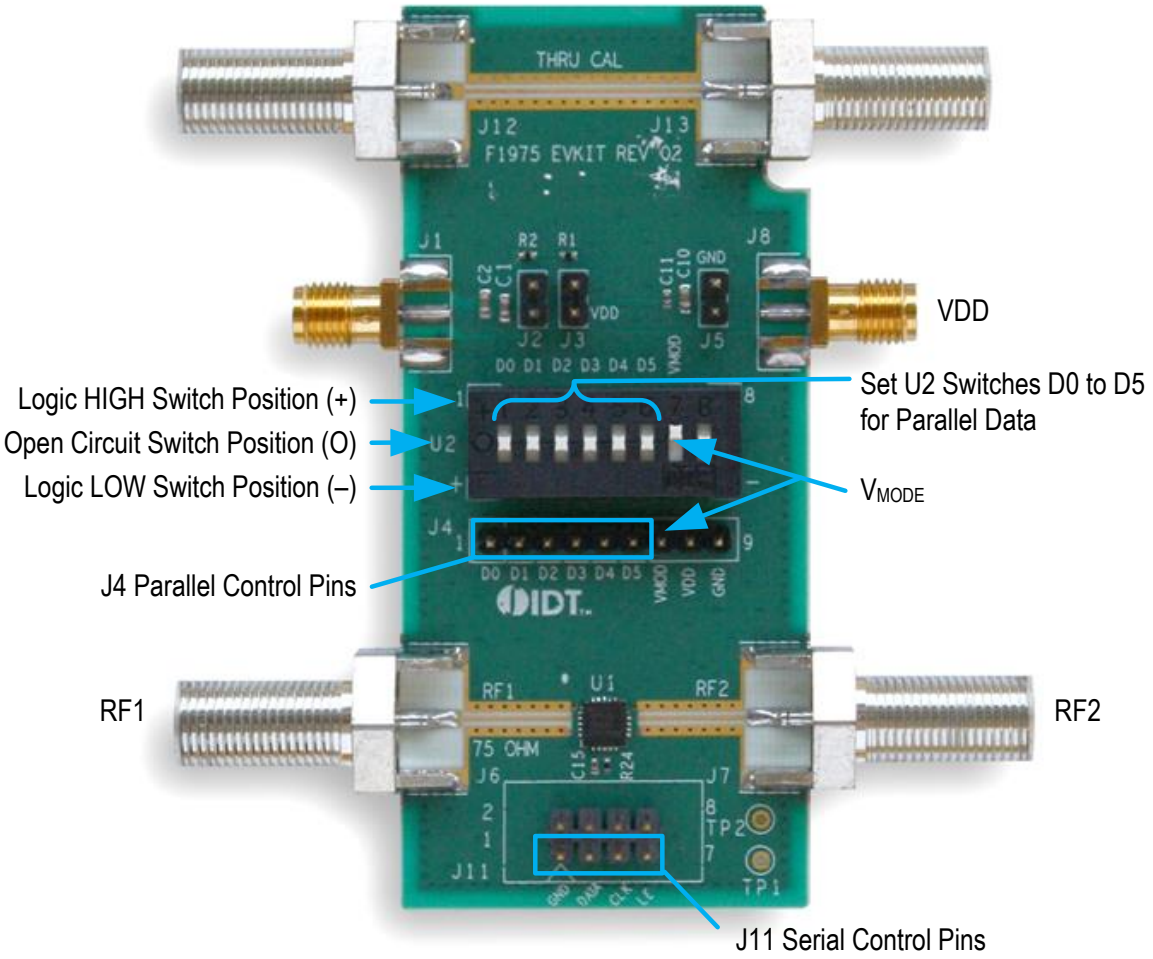
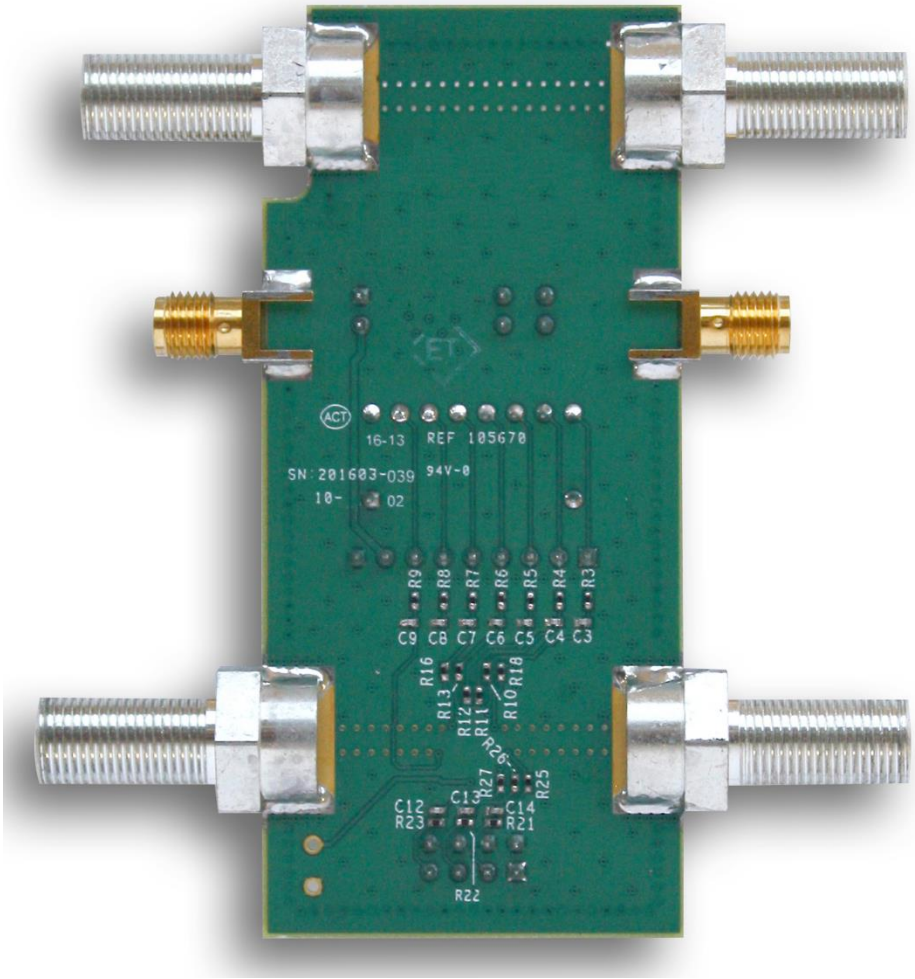
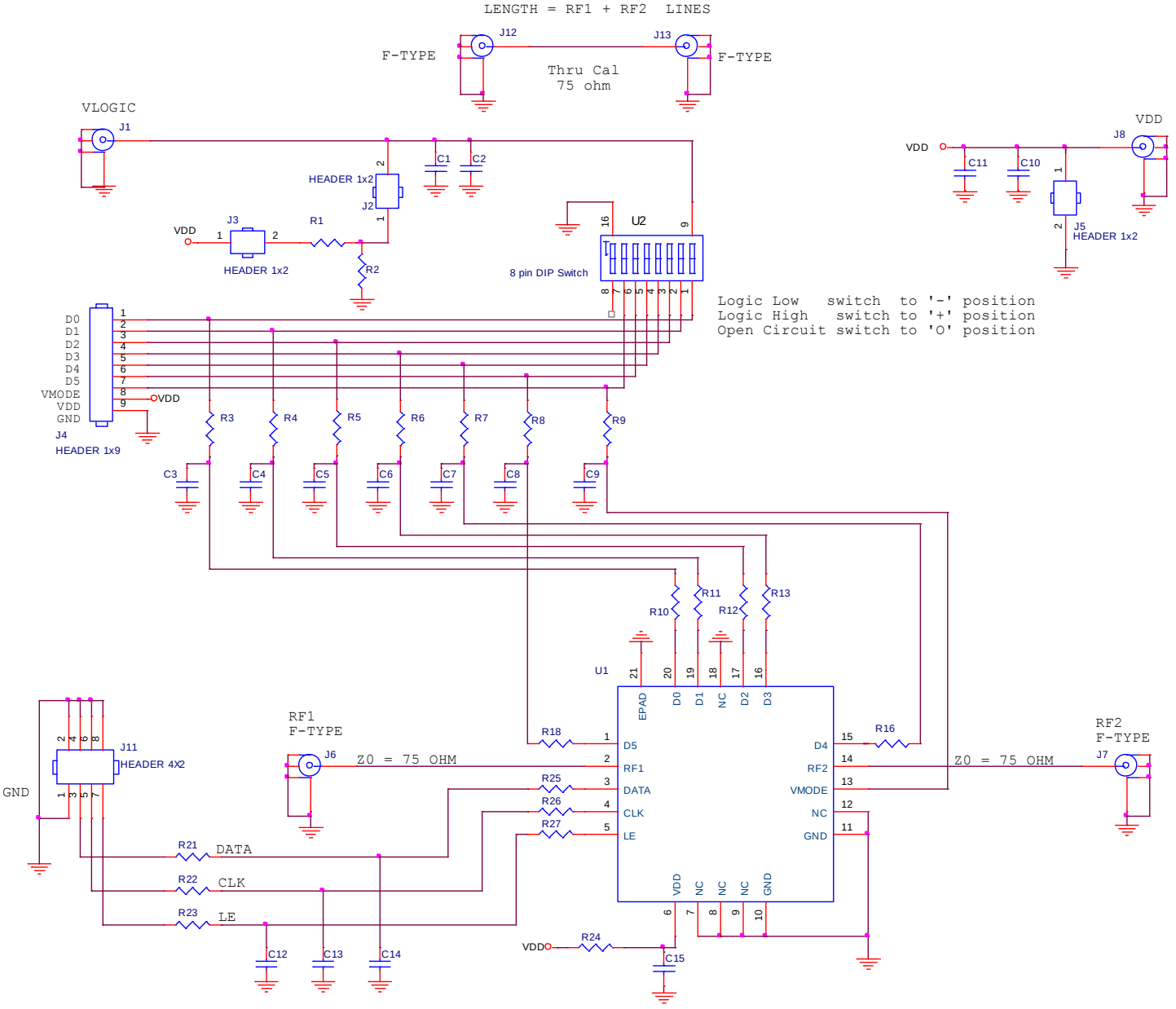


Figure 21. F1975EVBI Evaluation Board – Back View



Evaluation Kit / Applications Circuit

Figure 22. Electrical Schematic



Bill of Materials (BOM)

Table 14. Evaluation Kit Bill of Material

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1, C11, C15	3	100nF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	MURATA
C2, C10	2	10nF ±5%, 50V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	MURATA
C3 - C9, C12, C13, C14	10	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	MURATA
R3 - R9	7	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
R10-R13, R15-R18, R24-R27	12	0Ω Resistor (0402)	ERJ-2GE0R00X	PANASONIC
R21, R22, R23	3	3kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
R1	1	8.25kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF8251X	PANASONIC
R2	1	10kΩ ±5%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
J2, J3, J5	3	Conn Header Vert SGL 2 X 1 Pos Gold	961102-6404-AR	3M
J11	1	Conn Header Vert DBL 4 X 2 Pos Gold	67997-108HLF	FCI
J4	1	Conn Header Vert SGL 9 X 1 Pos Gold	961109-6404-AR	3M
J1, J8	2	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
J6, J7, J12, J13	4	Edge Launch F-type 75 Ohm	222181	Amphenol
U2	1	Switch 8-Position Dip Switch	KAT1108E	E-Switch
U1	1	DSA	F1975NCGI	IDT
	1	Printed Circuit Board	F1975 EVKit Rev 02	IDT

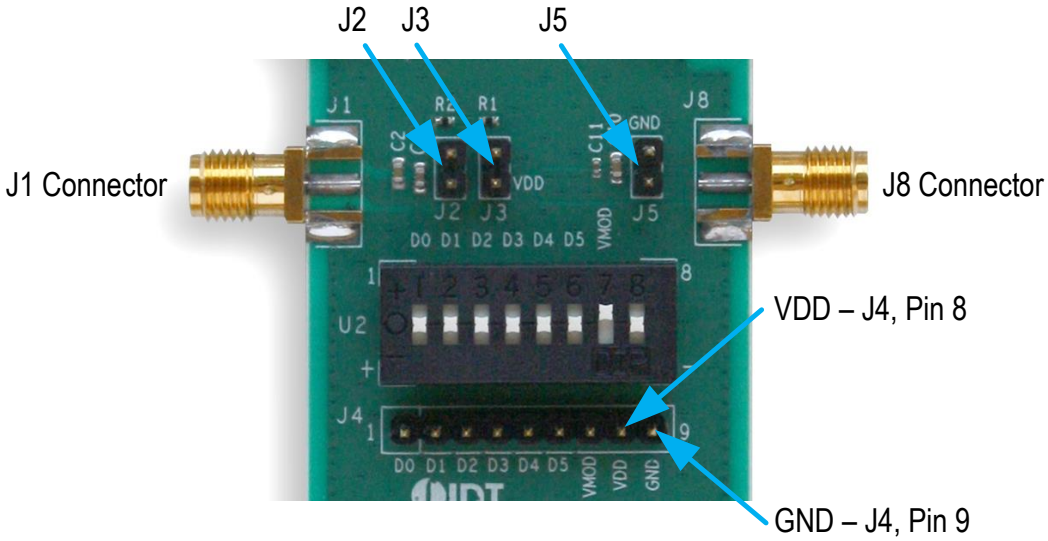
Evaluation Kit Operation

Power Supply Setup

Set up a power supply in the voltage range of 3.0V to 5.25V with the power supply output disabled. The voltage can be applied via one of the following connections (see Figure 23):

- J8 connector
- J5 header connection (note the polarity of the GND pin on this connector)
- Pin 8 (V_{DD}) and pin 9 (GND) on the J4 header connection

Figure 23. Power Supply and Logic Voltage Connections



Parallel Logic Control Setup

The Evaluation Board has the ability to control the F1975 in the Parallel Mode. For external control, apply logic voltages to the J4 header pins 1 through 6 (see Figure 20). For manual control, switches 1 through 6 on U2 can be set. The switch is a three-position switch. The bottom position "–" will ground the pin. The center position "O" will leave the pin open circuited. Setting the switch to the top position "+" will apply a voltage that is supplied to the switch.

The logic voltage can be applied in one of two ways (see Figure 23):

- Direct connection to connector J1.
- Leave J1 open circuit, and add jumpers to headers J2 and J3. This will apply a logic voltage that is $0.24 * V_{DD}$.

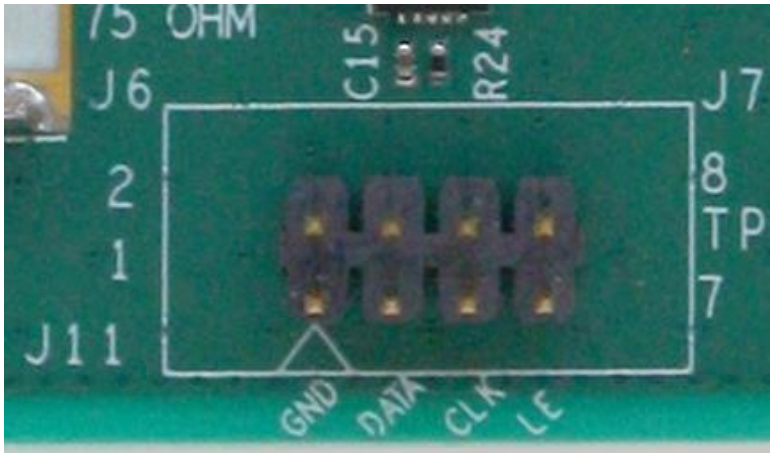
The F1975 has internal pull-up resistors for the D0 – D5 parallel pins and V_{MODE}. The switches can be used to apply a logic LOW (ground) for proper operation. To use the Parallel Mode, either apply a ground to the VMOD pin 7 on J4 or set U2 switch 7 (VMOD) to the "–" position (see Figure 20). The attenuation setting can be set via the U2 switches 1 through 6 (D0 through D5) according to Table 11.

Serial Logic Control Setup

The Evaluation Board has the ability to control the F1975 in the Serial Mode. Connect the serial controller to the J11 header connection as shown in Figure 24. To use the Serial Mode, set U2 switch 7 to the “+” or “O” position.

The attenuation setting can be programmed according to Table 8.

Figure 24. Serial Logic Connections



Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the “Power Supply Setup” section and either the “Parallel Logic Control Setup” or “Serial Logic Control Setup” sections above.

Enable the V_{DD} supply.

Enable the proper attenuation setting according to Figure 20 and Table 8 for Serial Mode or Table 11 for the Parallel Mode.

Power-Off Procedure

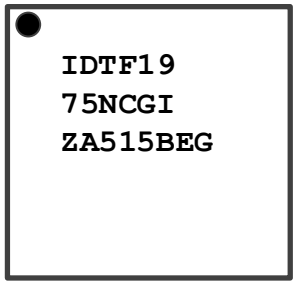
Set the logic control pins to a logic LOW.

Disable the V_{DD} supply.

Package Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Marking Diagram



1. Line 1 and 2 are the part number.
2. Line 3: “ZA” is for die version.
3. Line 3: “yww” = “515” = one digit year and two digit week that the part was assembled.
4. Line 3: “BEG” denotes assembly site.

Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
F1975NCGI	4mm x 4mm x 0.75mm QFN	1	Tray	-40°C to +105°C
F1975NCGI8	4mm x 4mm x 0.75mm QFN	1	Reel	-40°C to +105°C
F1975EVBI	Evaluation Board			
F1975EVSI	Evaluation Solution including the Evaluation Board, Controller Board, and cable. The Evaluation Software is available for download on the product page on the IDT website: www.IDT.com/F1975			

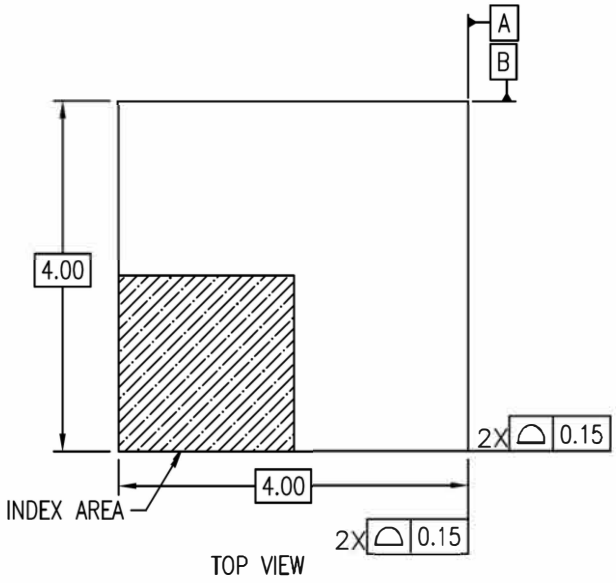
Revision History

Revision	Revision Date	Description of Change
1	September 21, 2017	Updated evaluation board images, top markings, and updated to the latest template.
O	July 31, 2017	Initial release of the datasheet.

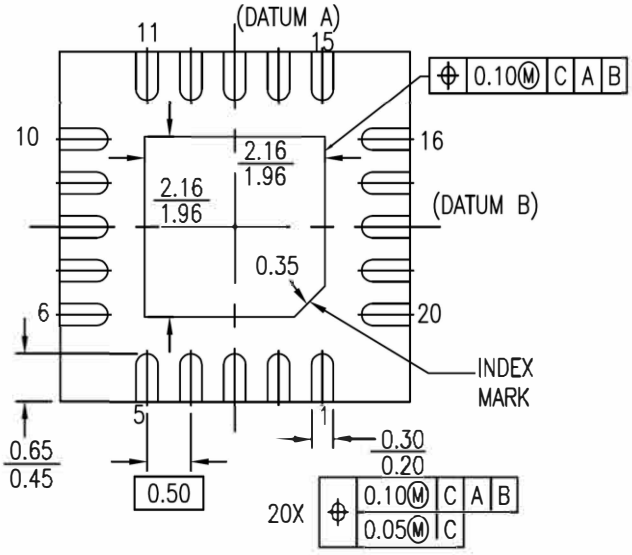
20-QFN, Package Outline Drawing

4.0 x 4.0 x 0.75 mm Body, 0.5mm Pitch, Epad 2.06 x 2.06 mm

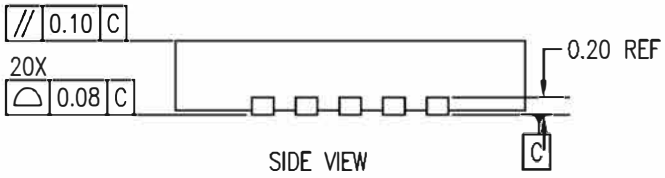
NCG20P1, PSC-4445-01, Rev 01, Page 1



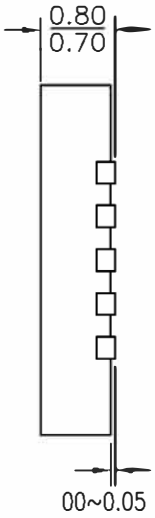
TOP VIEW



BOTTOM VIEW

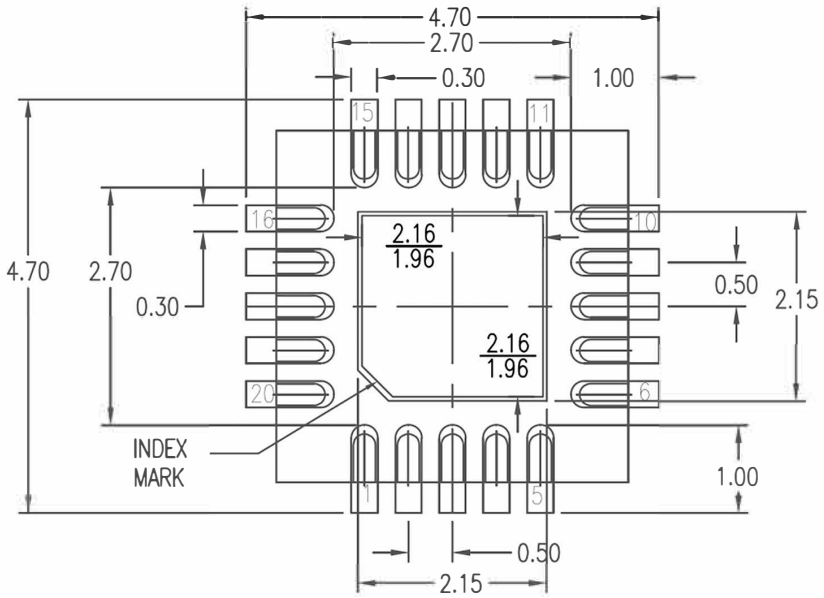


SIDE VIEW



NOTE:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS COPLANARITY SHALL NOT EXCEED 0.06 MM
3. WARPAGE SHALL NOT EXCEED 0.10
4. REFER JEDEC MO-220



RECOMMENDED LAND PATTERN DIMENSION

NOTE:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
2. TOP DOWN VIEW AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MPOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Sept 12, 2017	Rev 01	Correct Title
Sept 11, 2017	Rev 00	Initial Release

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