



June 2015

# FDMD8260L

## Dual N-Channel Power Trench<sup>®</sup> MOSFET

60 V, 5.8 mΩ

### Features

- Max  $r_{DS(on)}$  = 5.8 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 15\text{ A}$
- Max  $r_{DS(on)}$  = 8.7 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 12\text{ A}$
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- Termination is Lead-free and RoHS Compliant

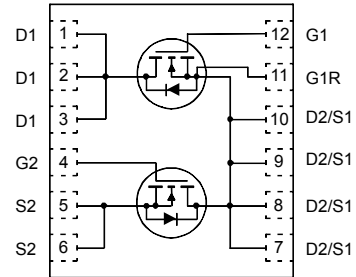
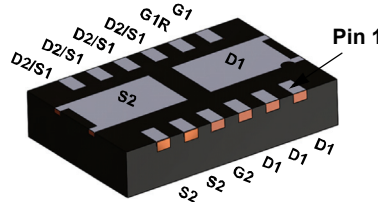
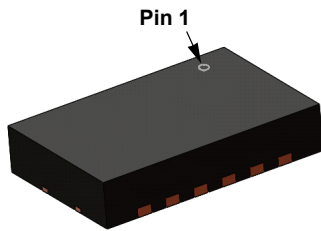


### General Description

This device includes two 60V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}$ /Qg FOM silicon.

### Applications

- Synchronous Buck : Primary Switch of Half / Full bridge Converter for Telecom
- Motor Bridge : Primary Switch of Half / Full bridge Converter for BLDC Motor
- MV POL : 48V Synchronous Buck Switch



Power 3.3 x 5

### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	60	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	64
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	40
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	15
	-Pulsed	(Note 4)	293
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	181
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	37
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.1
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1b)	1.0
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	130	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8260L	FDMD8260L	Power 3.3 x 5	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		33		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 15\ \text{A}$		4.5	5.8	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 12\ \text{A}$		6.6	8.7	
		$V_{GS} = 10\ \text{V}, I_D = 15\ \text{A}, T_J = 125^\circ\text{C}$		5.9	7.8	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 15\ \text{A}$		56		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}$ $f = 1\ \text{MHz}$		3745	5245	pF
$C_{oss}$	Output Capacitance			558	785	pF
$C_{rss}$	Reverse Transfer Capacitance			22	50	pF
$R_g$	Gate Resistance		0.1	3.0	6.0	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\ \text{V}, I_D = 15\ \text{A}$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		12	21	ns
$t_r$	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			47	74	ns
$t_f$	Fall Time			11	20	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\ \text{V to } 10\ \text{V}$	$V_{DD} = 30\ \text{V}$ $I_D = 15\ \text{A}$	49	68
	Total Gate Charge	$V_{GS} = 0\ \text{V to } 5\ \text{V}$	25		35	nC
$Q_{gs}$	Gate to Source Charge			8.6		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5.2		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 15\ \text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 1.6\ \text{A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 15\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		36	58	ns
$Q_{rr}$	Reverse Recovery Charge			17	30	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

a.  $60^\circ\text{C}/\text{W}$  when mounted on  
a 1 in<sup>2</sup> pad of 2 oz copper

b.  $130^\circ\text{C}/\text{W}$  when mounted on  
a minimum pad of 2 oz copper

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FDMD8260L

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3.  $E_{AS}$  of 181 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\ \text{mH}$ ,  $I_{AS} = 11\ \text{A}$ ,  $V_{DD} = 60\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ . 100% tested at  $L = 0.1\ \text{mH}$ ,  $I_{AS} = 36\ \text{A}$ .

4. Pulsed  $I_d$  please refer to Fig 11 SOA graph for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

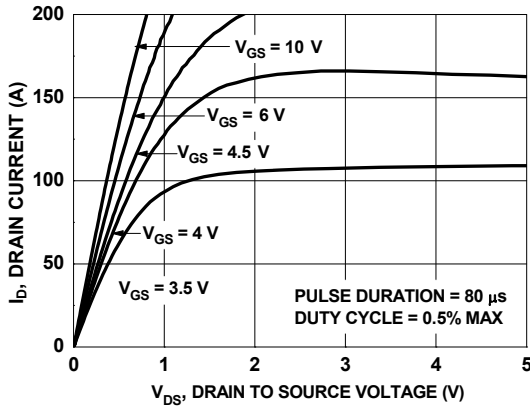


Figure 1. On-Region Characteristics

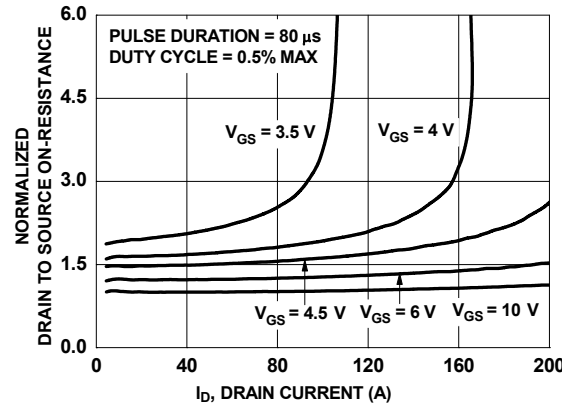


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

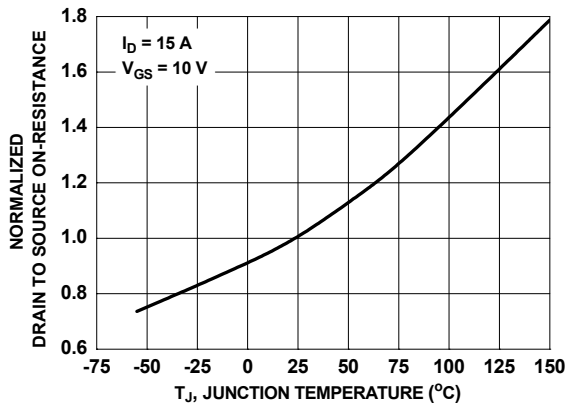


Figure 3. Normalized On Resistance vs. Junction Temperature

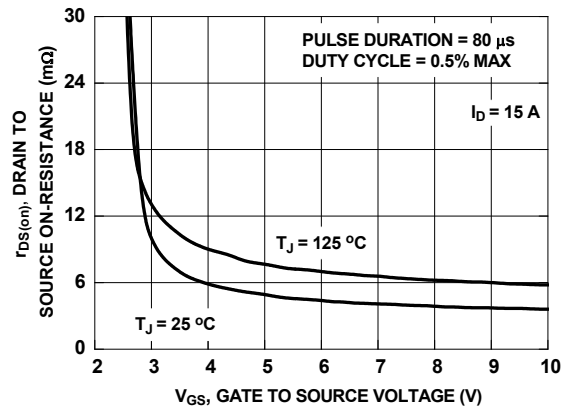


Figure 4. On Resistance vs. Gate to Source Voltage

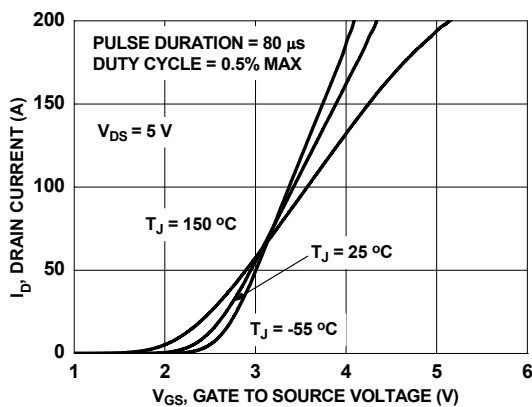


Figure 5. Transfer Characteristics

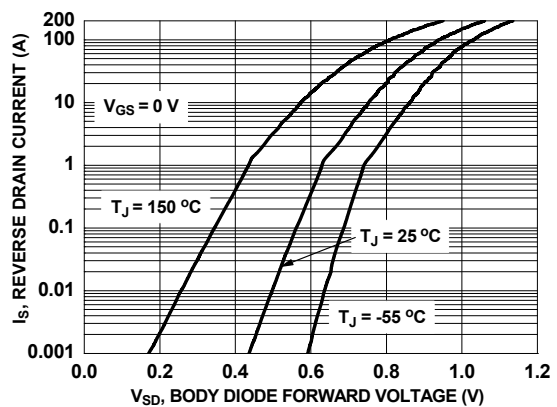
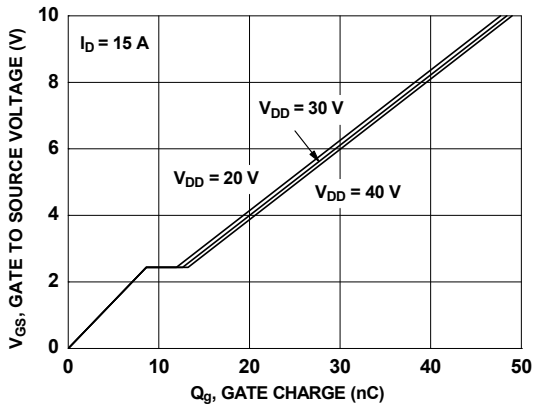
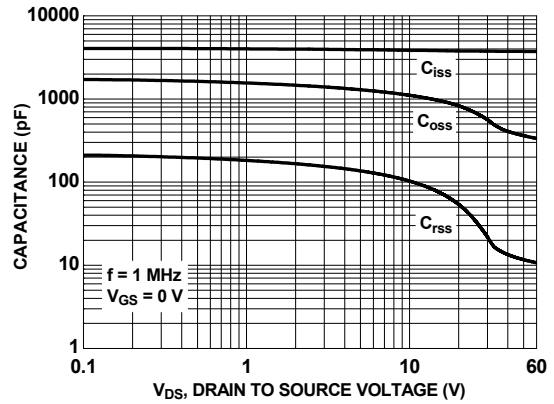


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

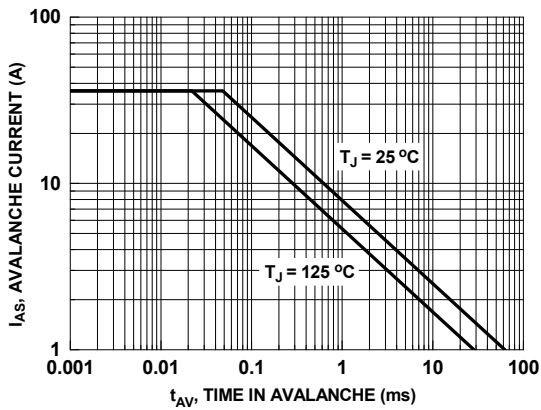
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



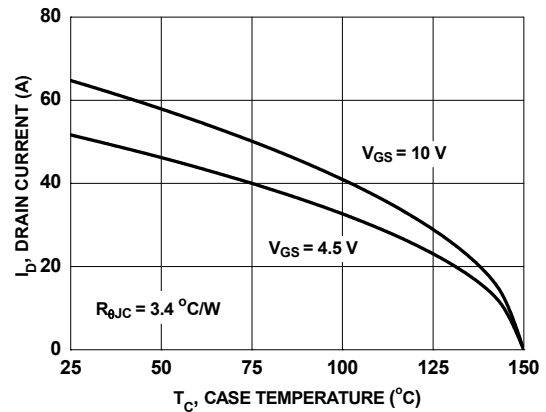
**Figure 7. Gate Charge Characteristics**



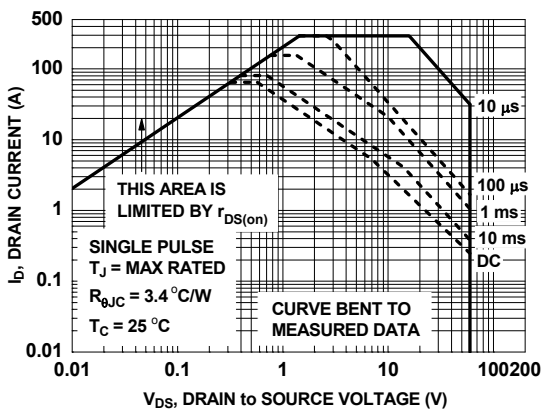
**Figure 8. Capacitance vs. Drain to Source Voltage**



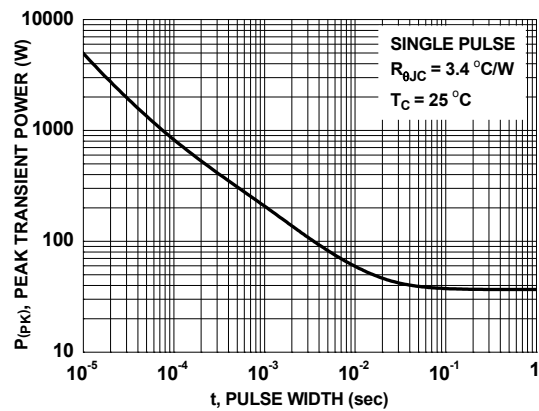
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

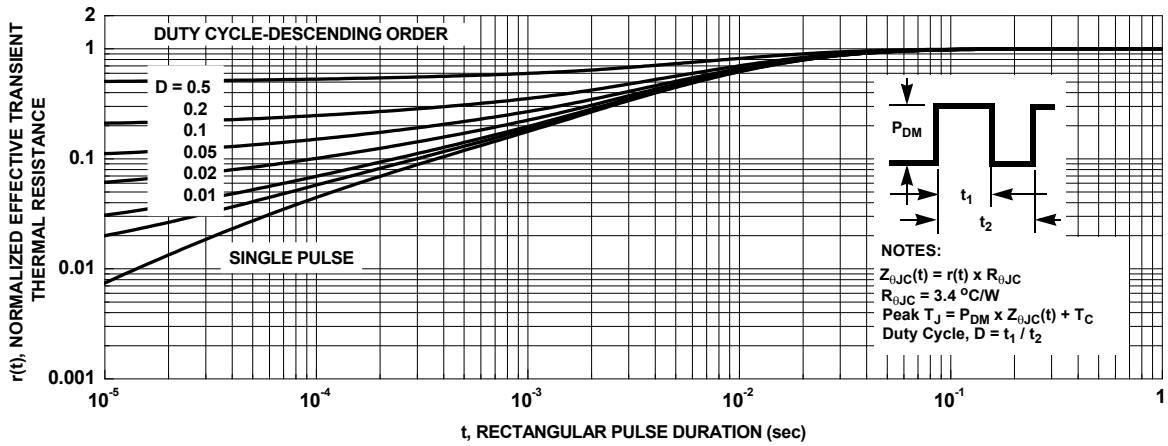


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**