



FDMD8280

Dual N-Channel Power Trench[®] MOSFET 80 V, 40 A, 8.2 mΩ

Features

- Max $r_{DS(on)}$ = 8.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$
- Max $r_{DS(on)}$ = 11 mΩ at $V_{GS} = 8\text{ V}$, $I_D = 9.5\text{ A}$
- Ideal for flexible layout in primary side of bridge topology
- Termination is Lead-free and RoHS Compliant
- 100% UIL tested
- Kelvin High Side MOSFET drive pin-out capability

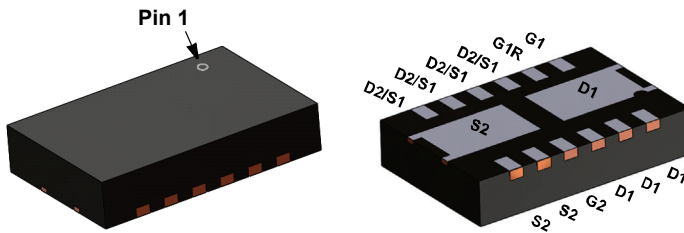


General Description

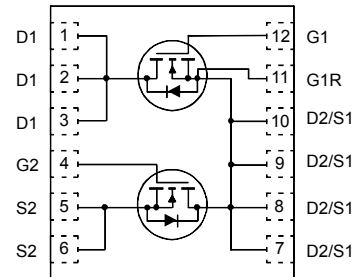
This device includes two 80V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$ /Qg FOM silicon.

Applications

- Synchronous Buck : Primary Switch of Half / Full bridge converter for telecom
- Motor Bridge : Primary Switch of Half / Full bridge converter for BLDC motor
- MV POL : 48V Synchronous Buck Switch



Power 3.3 x 5



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous	40	A
	Drain Current -Continuous	11	
	-Pulsed	160	
E_{AS}	Single Pulse Avalanche Energy	150	mJ
P_D	Power Dissipation	38	W
	Power Dissipation	2.1	
	Power Dissipation	1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8280	FDMD8280	Power 3.3 x 5	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		48		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	3.0	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$		6.6	8.2	m Ω
		$V_{GS} = 8\text{ V}$, $I_D = 9.5\text{ A}$		7.5	11	
		$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		10	12.4	
g_{FS}	Forward Transconductance	$V_{DD} = 10\text{ V}$, $I_D = 11\text{ A}$		29		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$		2179	3050	pF
C_{oss}	Output Capacitance			341	480	pF
C_{rss}	Reverse Transfer Capacitance			15	25	pF
R_g	Gate Resistance		0.1	2.7	5.4	Ω

Switching Characteristics

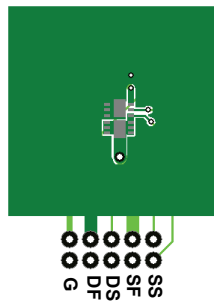
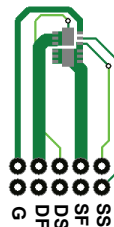
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$, $I_D = 11\text{ A}$ $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		15	27	ns	
t_r	Rise Time			12	22	ns	
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns	
t_f	Fall Time			8.9	18	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		31	44	nC
	Total Gate Charge		$V_{GS} = 0\text{ V to }8\text{ V}$		25	35	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 40\text{ V}$ $I_D = 11\text{ A}$		9.5		nC	
Q_{gd}	Gate to Drain "Miller" Charge			6.6		nC	

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 11\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = 1.8\text{ A}$ (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 11\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		27	43	ns
Q_{rr}	Reverse Recovery Charge			12	22	nC

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.


 a. $60\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper

 b. $130\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.

- E_{AS} of 150 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 10\text{ A}$, $V_{DD} = 72\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 32\text{ A}$.

- Pulse I_d measured at $t_d \leq 250\text{ }\mu\text{s}$, refer to Fig 11 SOA graph for more details.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

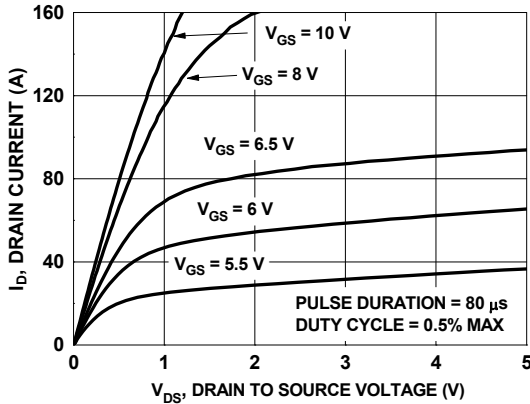


Figure 1. On-Region Characteristics

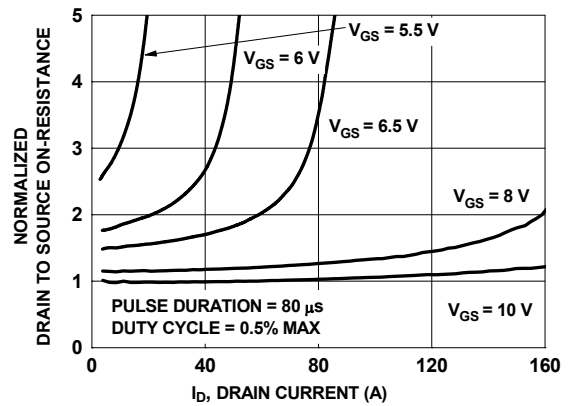


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

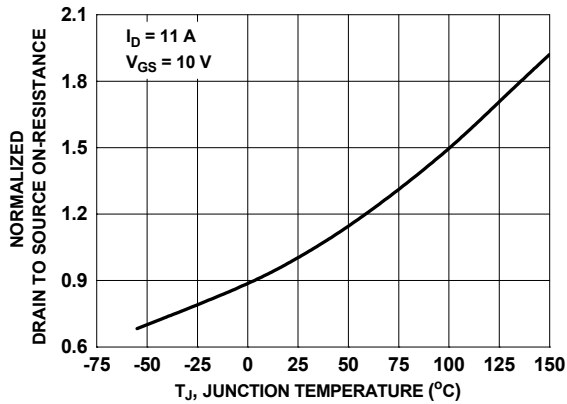


Figure 3. Normalized On Resistance vs Junction Temperature

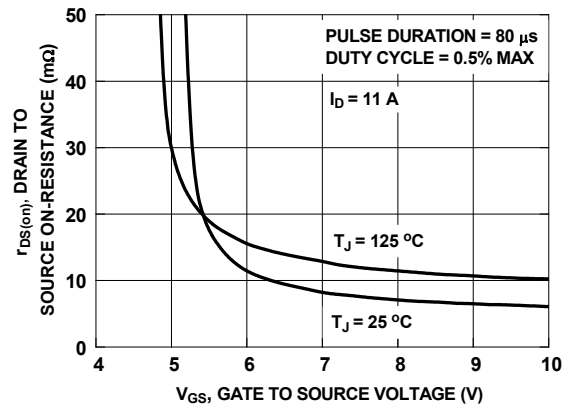


Figure 4. On Resistance vs Gate to Source Voltage

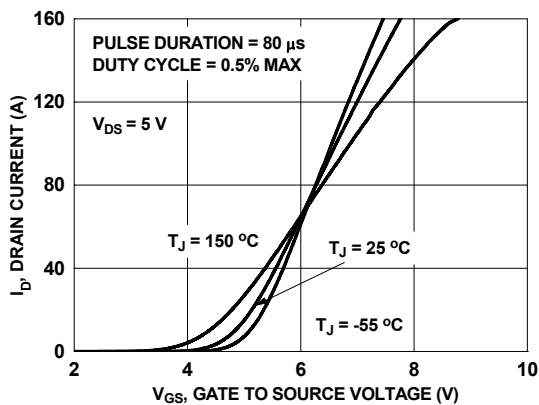


Figure 5. Transfer Characteristics

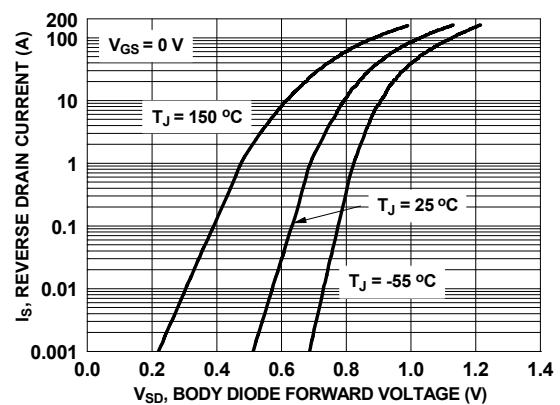


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

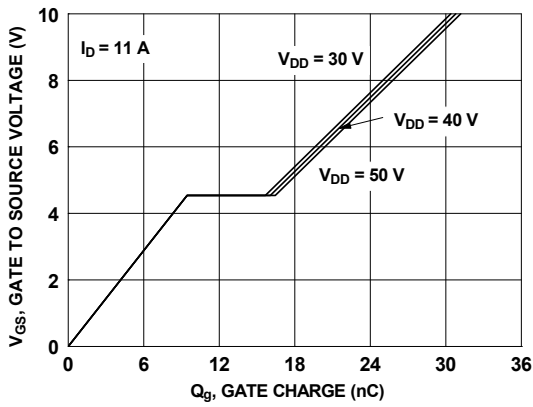


Figure 7. Gate Charge Characteristics

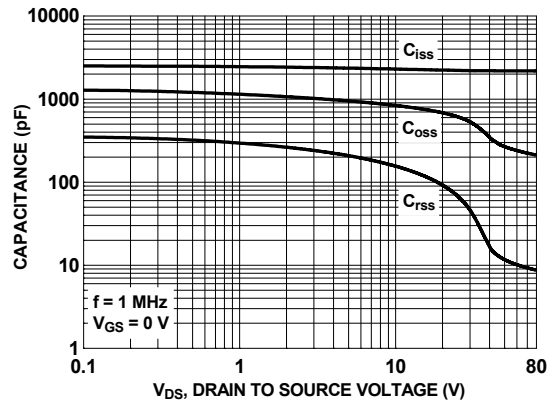


Figure 8. Capacitance vs Drain to Source Voltage

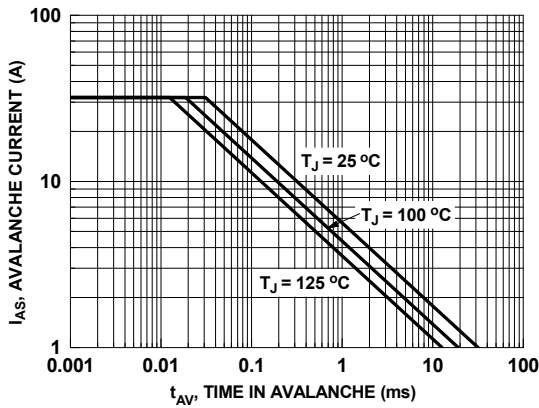


Figure 9. Gate Leakage Current vs Gate to Source Voltage

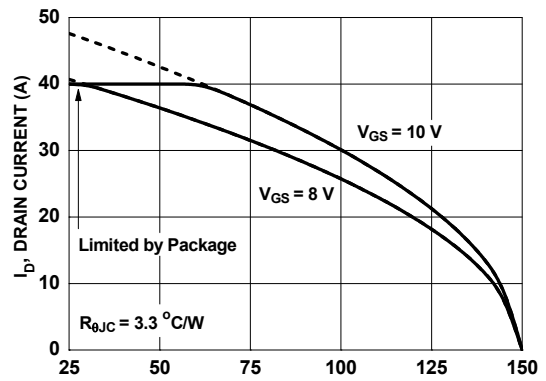


Figure 10. Maximum Continuous Drain Current vs Case Temperature

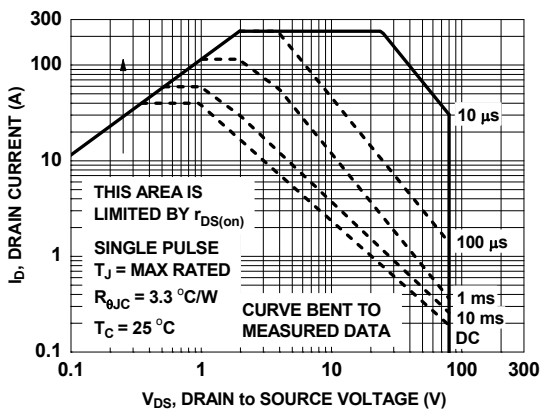


Figure 11. Forward Bias Safe Operating Area

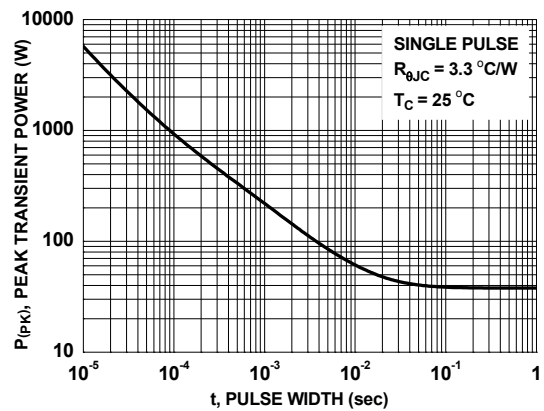


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

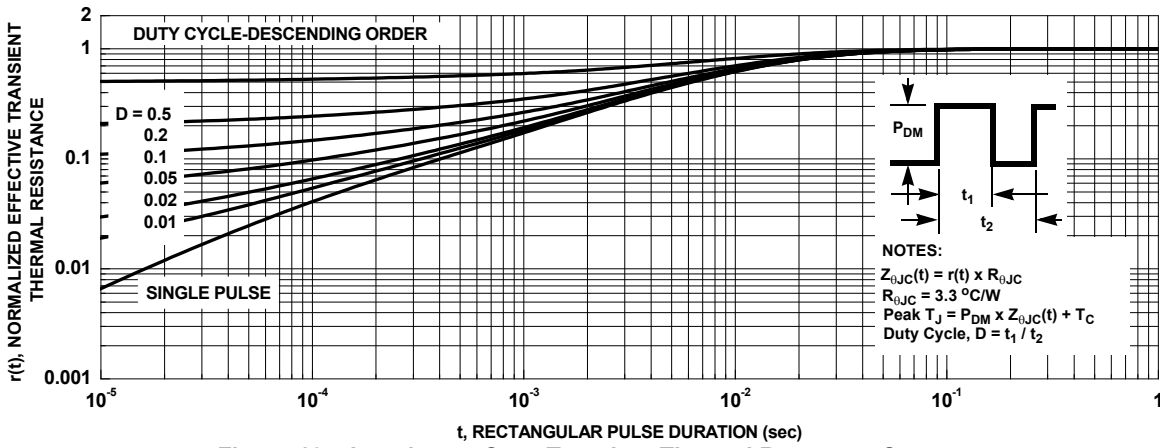
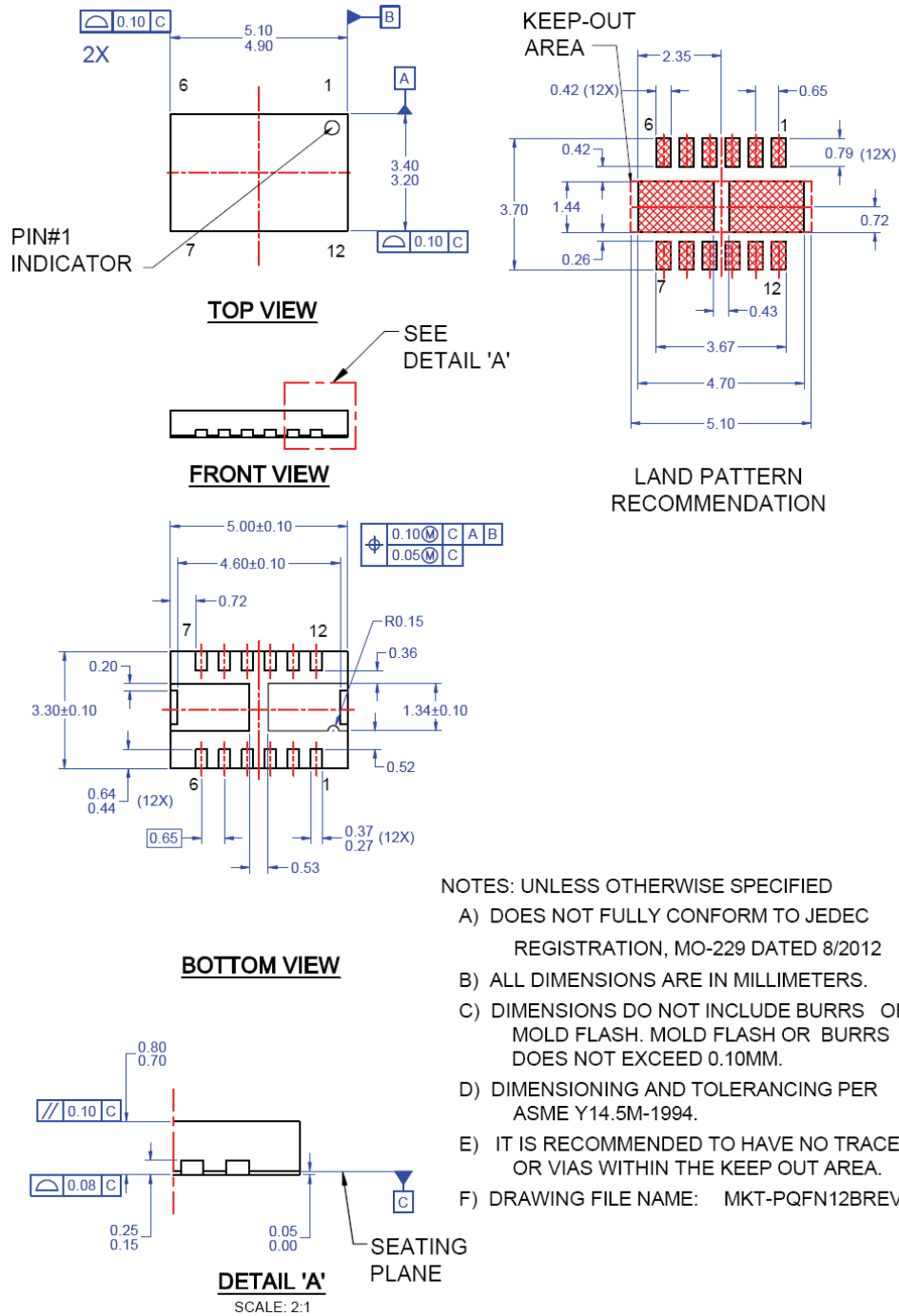


Figure 13. Junction-to-Case Transient Thermal Response Curve

Dimensional Outline and Pad Layout




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