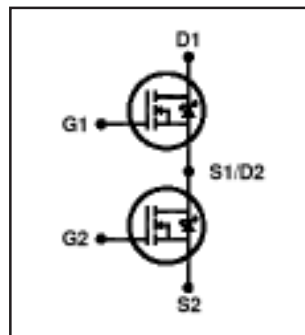


# IRFI4212H-117P

## Features

- Integrated half-bridge package
- Reduces the part count by half
- Facilitates better PCB layout
- Key parameters optimized for Class-D audio amplifier applications
- Low  $R_{DS(ON)}$  for improved efficiency
- Low  $Q_g$  and  $Q_{sw}$  for better THD and improved efficiency
- Low  $Q_{rr}$  for better THD and lower EMI
- Can delivery up to 150W per channel into 4Ω load in half-bridge configuration amplifier
- Lead-free package

Key Parameters ⑤		
$V_{DS}$	100	V
$R_{DS(ON)}$ typ. @ 10V	58	mΩ
$Q_g$ typ.	12	nC
$Q_{sw}$ typ.	6.9	nC
$R_{G(int)}$ typ.	3.4	Ω
$T_J$ max	150	°C



G1, G2	D1, D2	S1, S2
Gate	Drain	Source

## Description

This Digital Audio MosFET Half-Bridge is specifically designed for Class D audio amplifier applications. It consists of two power MosFET switches connected in half-bridge configuration. The latest process is used to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery, and internal Gate resistance are optimized to improve key Class D audio amplifier performance factors such as efficiency, THD and EMI. These combine to make this Half-Bridge a highly efficient, robust and reliable device for Class D audio amplifier applications.

## Absolute Maximum Ratings ⑤

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	11	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	6.8	
$I_{DM}$	Pulsed Drain Current ①	44	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation ④	18	W
$P_D$ @ $T_C = 100^\circ\text{C}$	Power Dissipation ④	7.0	
	Linear Derating Factor	0.14	W/°C
$E_{AS}$	Single Pulse Avalanche Energy②	41	mJ
$T_J$	Operating Junction and	-55 to + 150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

## Thermal Resistance ⑤

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	7.1	°C/W
$R_{\theta JA}$	Junction-to-Ambient (free air)	—	65	

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified) ⑤

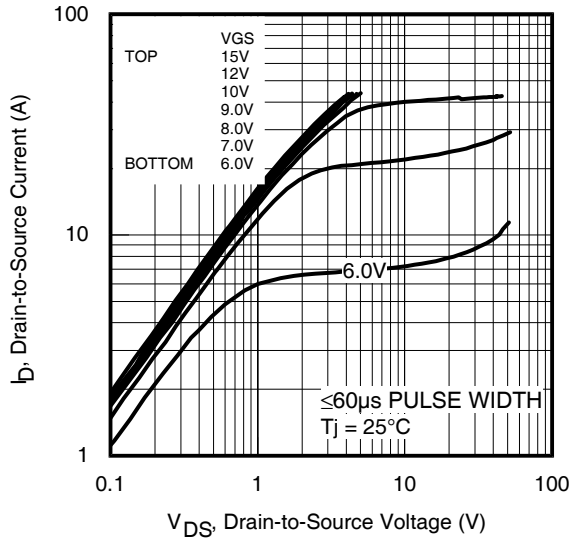
	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	58	72.5	mΩ	$V_{GS} = 10V, I_D = 6.6A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-11	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$g_{fs}$	Forward Transconductance	11	—	—	S	$V_{DS} = 50V, I_D = 6.6A$
$Q_g$	Total Gate Charge	—	12	18	nC	$V_{DS} = 80V$ $V_{GS} = 10V$ $I_D = 6.6A$ See Fig. 6 and 15
$Q_{gs1}$	Pre-Vth Gate-to-Source Charge	—	1.6	—		
$Q_{gs2}$	Post-Vth Gate-to-Source Charge	—	0.71	—		
$Q_{gd}$	Gate-to-Drain Charge	—	6.2	—		
$Q_{godr}$	Gate Charge Overdrive	—	3.5	—		
$Q_{sw}$	Switch Charge ( $Q_{gs2} + Q_{gd}$ )	—	6.9	—		
$R_{G(int)}$	Internal Gate Resistance	—	3.4	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	4.7	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ ③ $I_D = 6.6A$ $R_G = 2.5\Omega$
$t_r$	Rise Time	—	8.3	—		
$t_{d(off)}$	Turn-Off Delay Time	—	9.5	—		
$t_f$	Fall Time	—	4.3	—		
$C_{iss}$	Input Capacitance	—	490	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0MHz,$ See Fig.5 $V_{GS} = 0V, V_{DS} = 0V$ to $80V$
$C_{oss}$	Output Capacitance	—	64	—		
$C_{riss}$	Reverse Transfer Capacitance	—	34	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	110	—		
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		

## Diode Characteristics ⑤

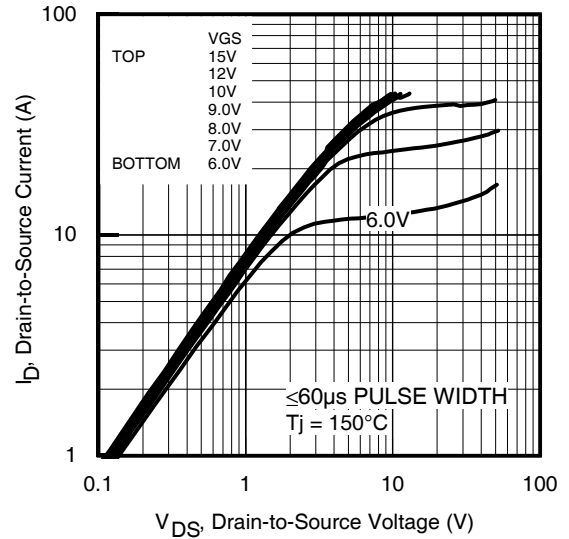
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	11	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	44		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 6.6A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	36	54	ns	$T_J = 25^\circ\text{C}, I_F = 6.6A$
$Q_{rr}$	Reverse Recovery Charge	—	56	84	nC	$di/dt = 100A/\mu s$ ③

### Notes:

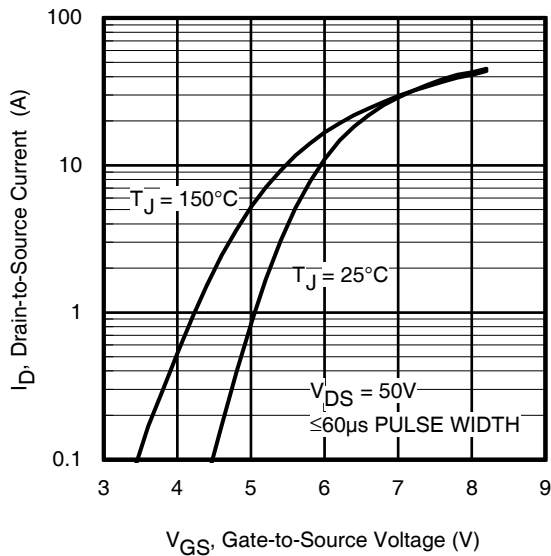
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}, L = 1.9mH, R_G = 25\Omega, I_{AS} = 6.6A$ .
- ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ④  $R_{\theta}$  is measured at  $T_J$  of approximately  $90^\circ\text{C}$ .
- ⑤ Specifications refer to single MosFET.



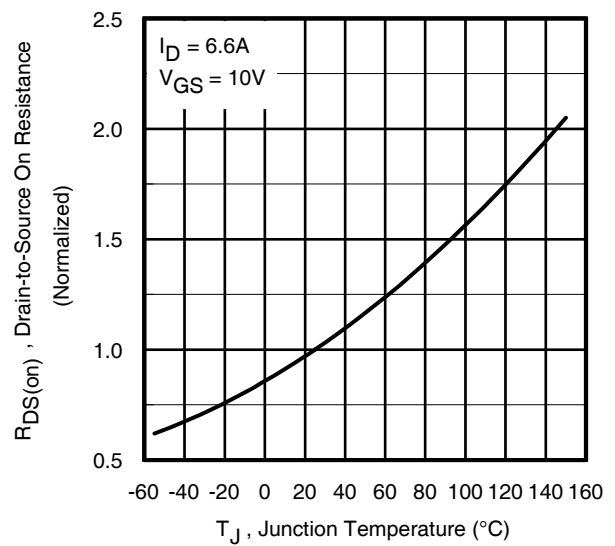
**Fig 1.** Typical Output Characteristics



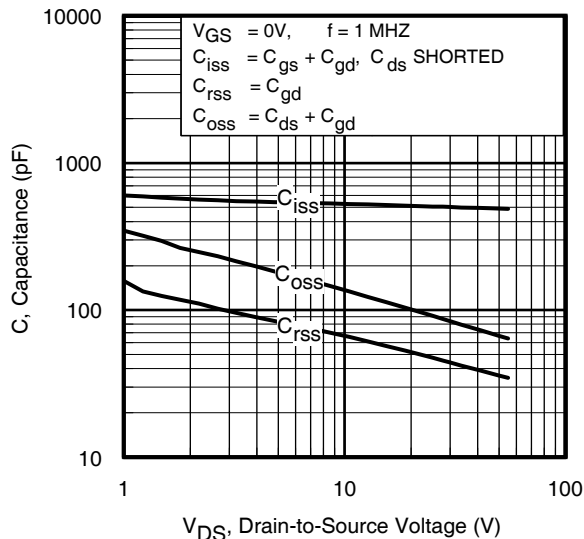
**Fig 2.** Typical Output Characteristics



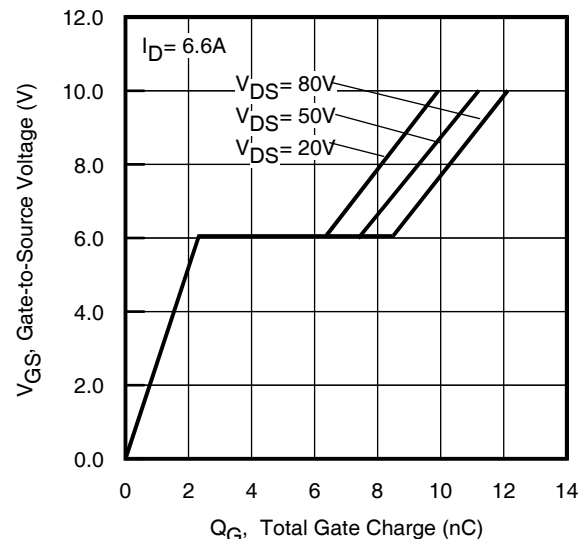
**Fig 3.** Typical Transfer Characteristics



**Fig 4.** Normalized On-Resistance vs. Temperature



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
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**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

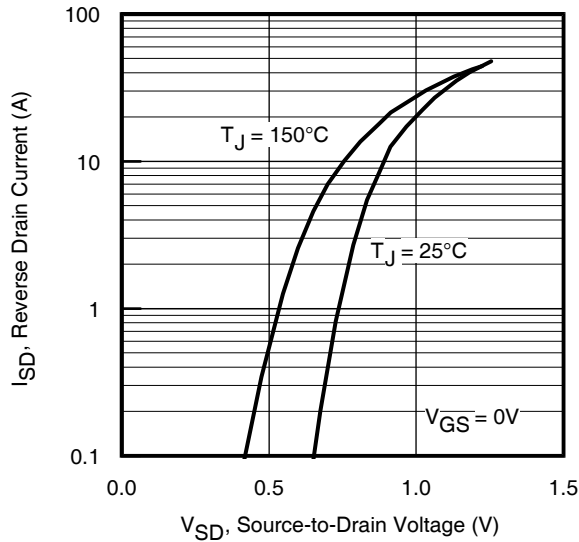


Fig 7. Typical Source-Drain Diode Forward Voltage

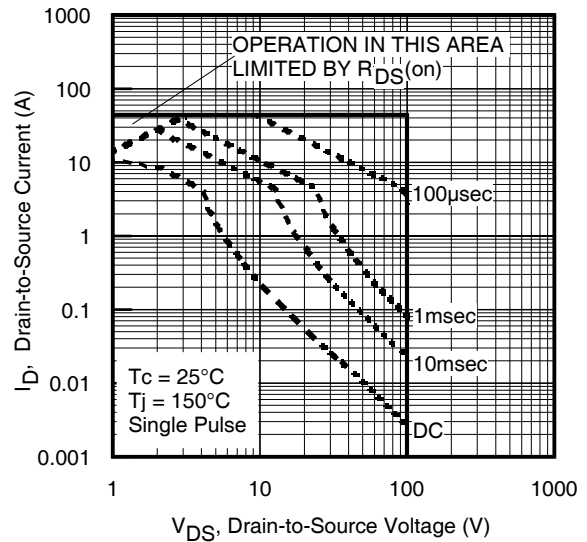


Fig 8. Maximum Safe Operating Area

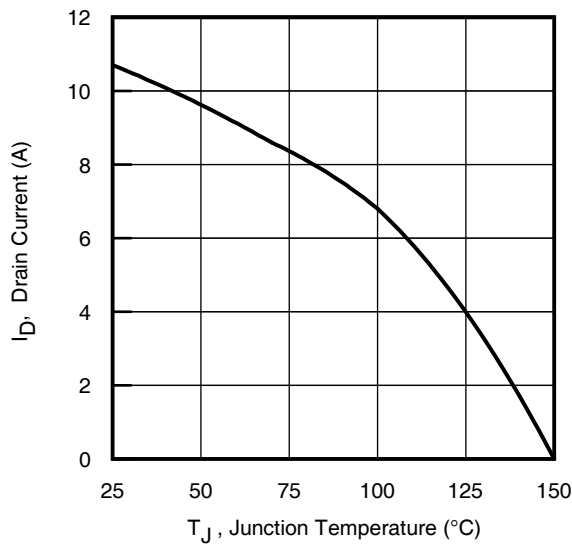


Fig 9. Maximum Drain Current vs. Junction Temperature

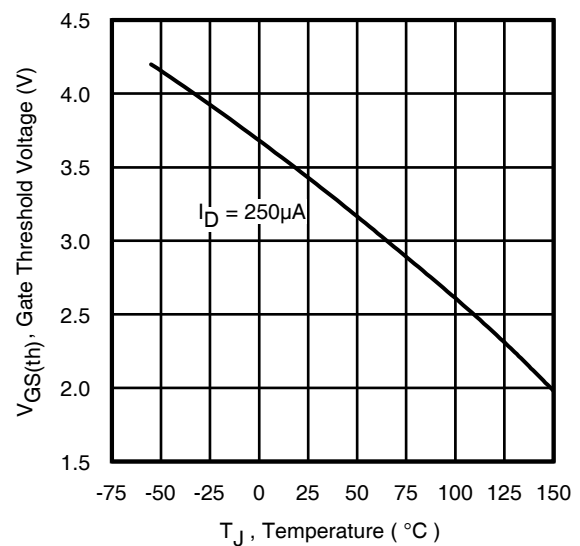


Fig 10. Threshold Voltage vs. Temperature

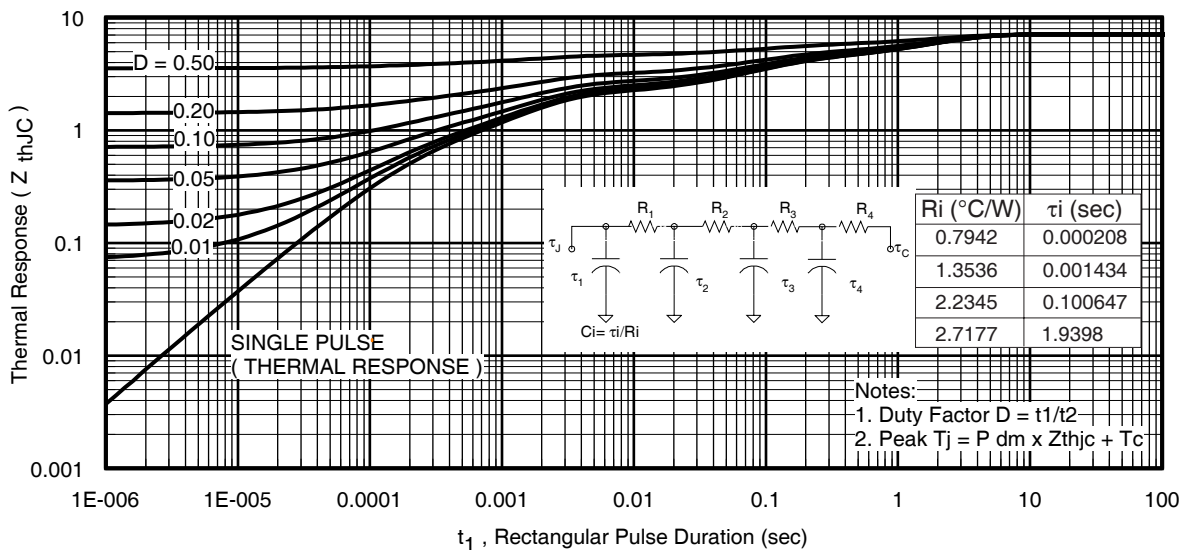
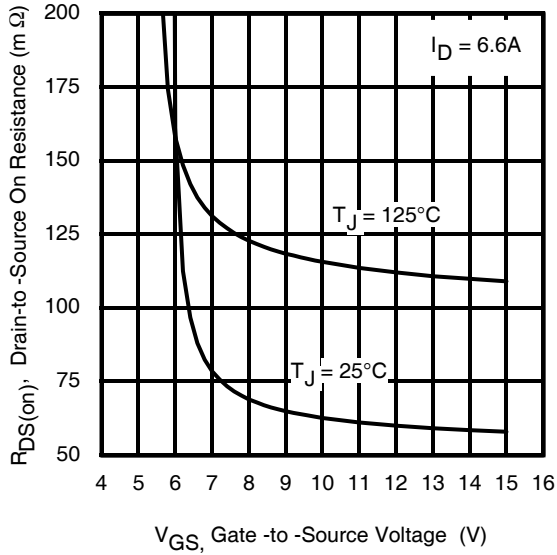
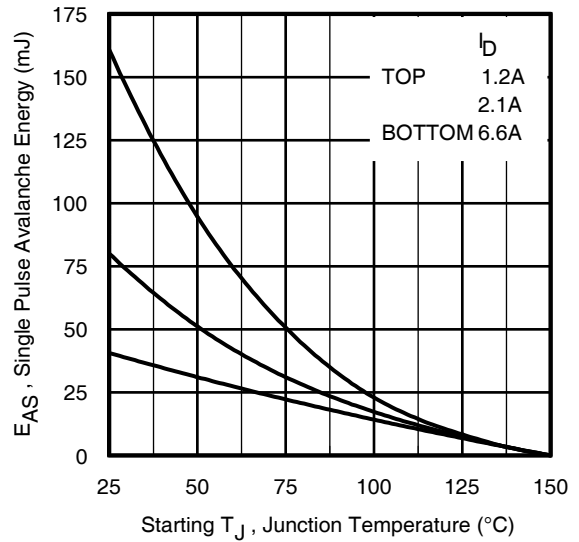


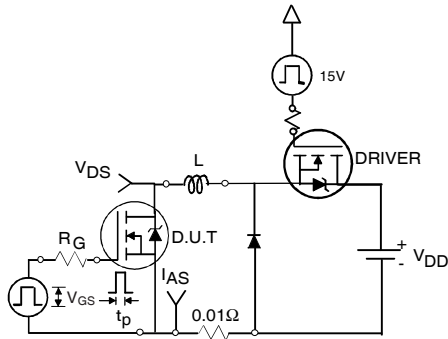
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



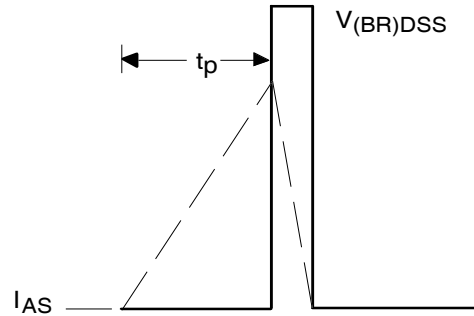
**Fig 12.** On-Resistance vs. Gate Voltage



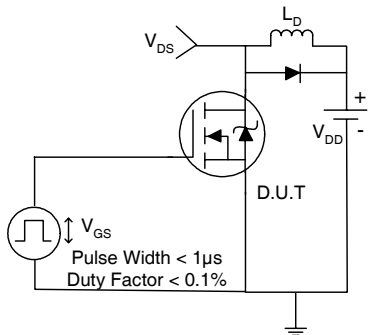
**Fig 13a.** Maximum Avalanche Energy vs. Drain Current



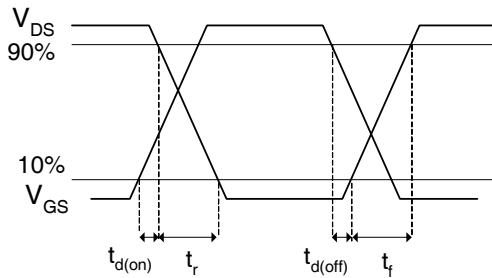
**Fig 13b.** Unclamped Inductive Test Circuit



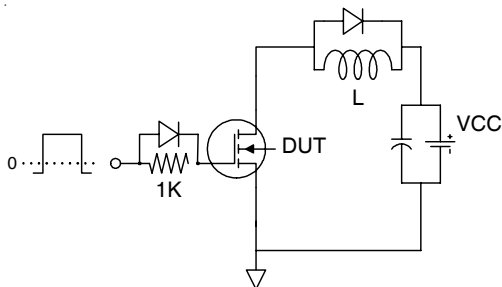
**Fig 13c.** Unclamped Inductive Waveforms



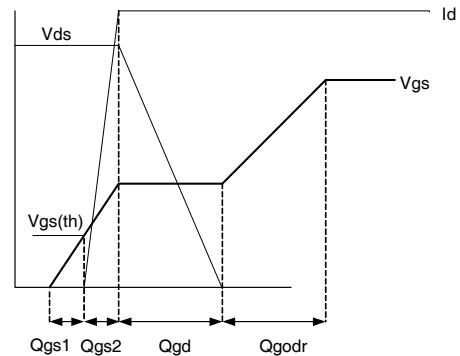
**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms



**Fig 15a.** Gate Charge Test Circuit



**Fig 15b** Gate Charge Waveform



Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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