OptiMOS™- 6 Power-Transistor

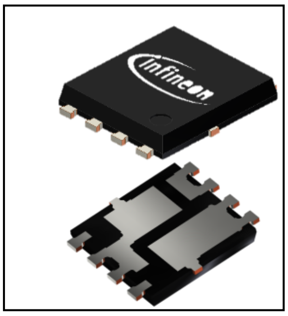
Product Summary

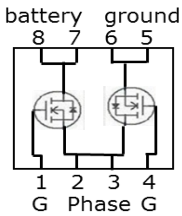
V_{DS}	40	V
$R_{DS(on),max}$	3.0	mΩ
I_D	60	A

Features

- OptiMOS™ - power MOSFET for automotive applications
- Half-Bridge - N-channel - Enhancement mode - Logic Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TDSON-8-56





Type	Package	Marking
IAUC60N04S6L030H	PG-TDSON-8-56	6N04L030

Maximum ratings per channel, at T_j=25 °C, unless otherwise specified

Parameter	**Symbol**	**Conditions**	**Value**	**Unit**
Drain current	I_D	V_{GS}=10V, Chip Limitation[1,2]	119	A
		V_{GS}=10V, DC current[3]	60	
		T_a=85°C, V_{GS}=10V, R_{thJA} on 2s2p[2,4]	22	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25°C, t_p=100µs	311	
Avalanche energy, single pulse[2]	E_{AS}	I_D=20A, $R_{g,min}$=25Ω	100	mJ
Avalanche current, single pulse	I_{AS}	$R_{g,min}$=25Ω	20	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation	P_{tot}	T_C=25°C	75	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.0	K/W
Thermal resistance, junction - ambient[4]	R_{thJA}	-	-	34	-	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=25µA	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V, T_j=25°C	-	-	1	µA
		V_{DS}=40V, V_{GS}=0V, T_j=125°C[2]	-	-	10	
Gate-source leakage current	I_{GSS}	V_{GS}=16V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5V, I_D=30A	-	3.1	4.2	mΩ
		V_{GS}=10V, I_D=30A	-	2.3	3.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1637	2128	pF
Output capacitance	C_{oss}		-	458	596	
Reverse transfer capacitance	C_{rss}		-	29	44	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, I_D=60A, R_G=3.5Ω	-	3	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	16	-	
Fall time	t_f		-	8	-	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=32V, I_D=60A, V_{GS}=0 to 10V	-	5.0	6.6	nC
Gate to drain charge	Q_{gd}		-	5.2	7.9	
Gate charge total	Q_g		-	27	35	
Gate plateau voltage	$V_{plateau}$		-	3.0	-	V
Reverse Diode						
Diode continous forward current[2)]	I_S	T_C=25°C	-	-	75	A
Diode pulse current[2)]	$I_{S,pulse}$	T_C=25°C, t_p=100µs	-	-	341	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=30A, T_j=25°C	-	0.8	1.1	V
Reverse recovery time[2)]	t_{rr}	V_R=20V, I_F=50A, di_F/dt=100A/µs	-	30	-	ns
Reverse recovery charge[2)]	Q_{rr}		-	18	-	nC

[1)] Practically the current is limited by overall system design including customer specific PCB.

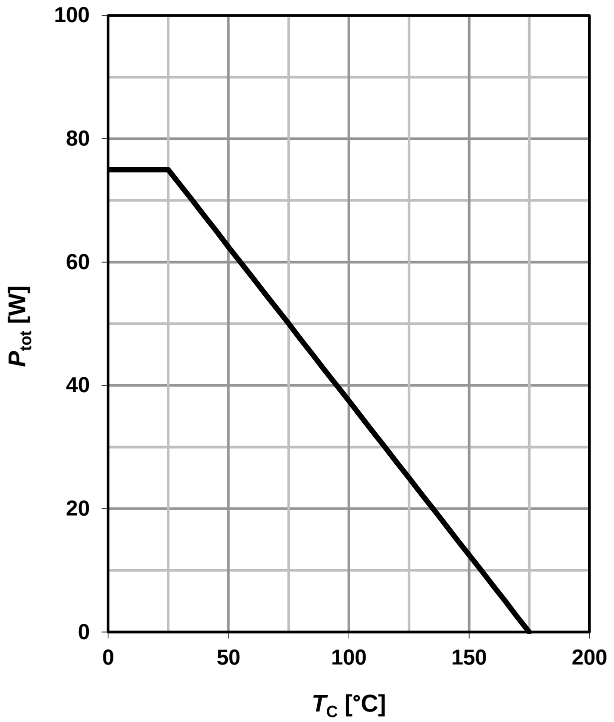
[2)] The parameter is not subject to production test - specified by design.

[3)] The product can operate at specified current based on best practice to minimize electromigration at the solder joint. For rare events and inrush currents the value may be exceeded.

[4)] Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

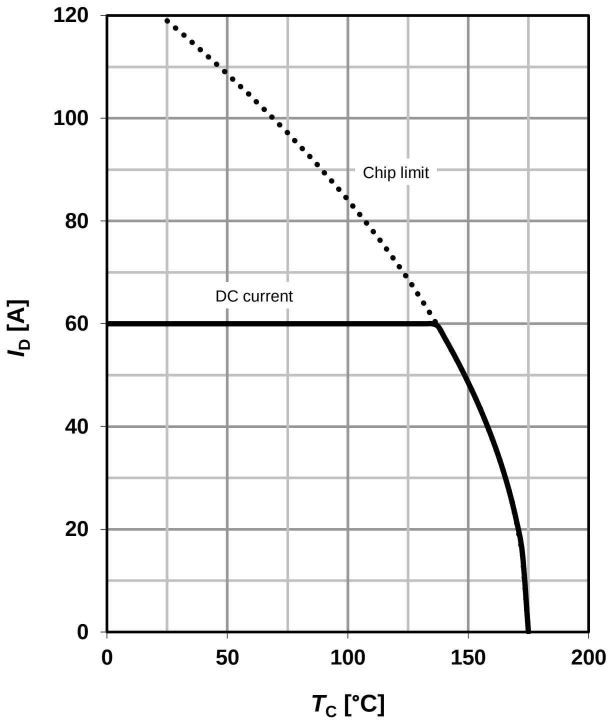
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} = 10$ V



2 Drain current

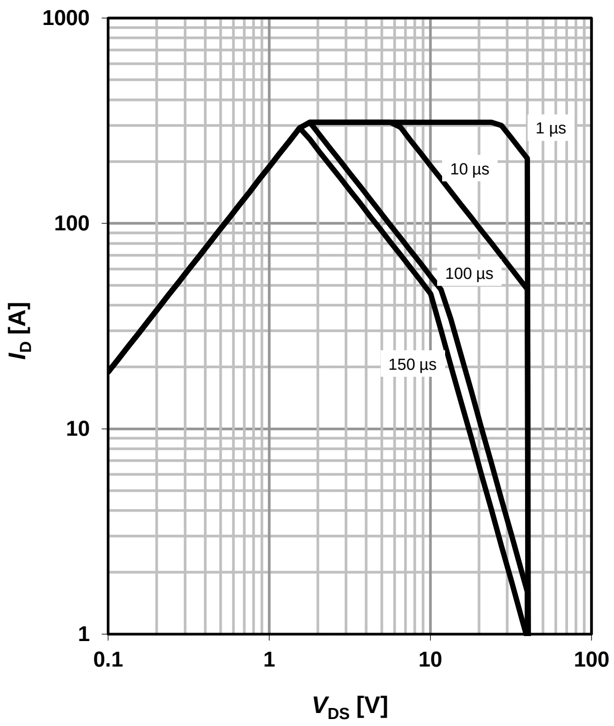
$I_D = f(T_C)$; $V_{GS} = 10$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

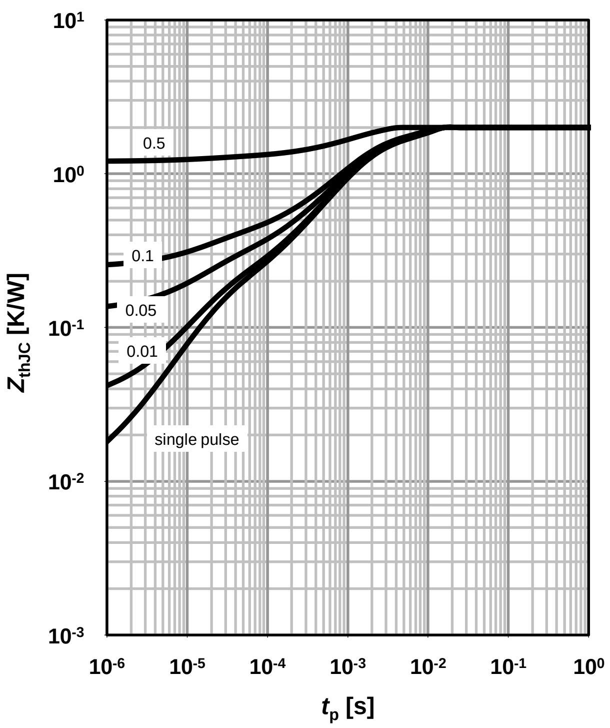
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

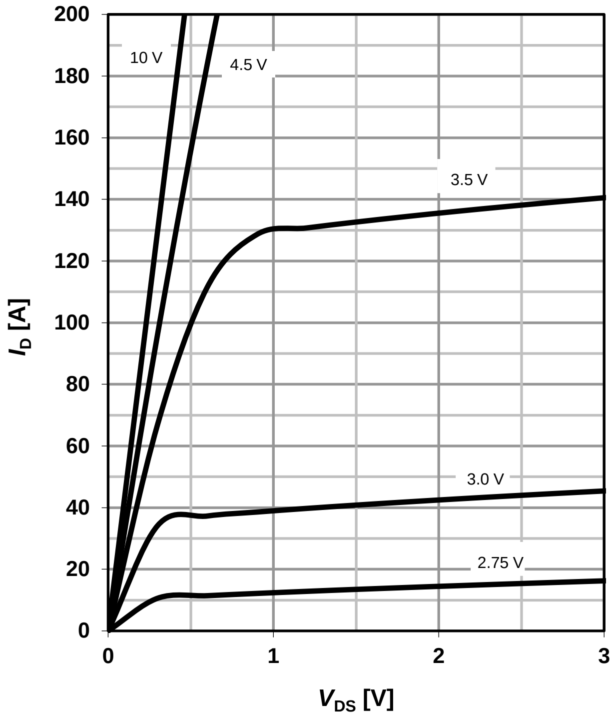
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25\ °C$

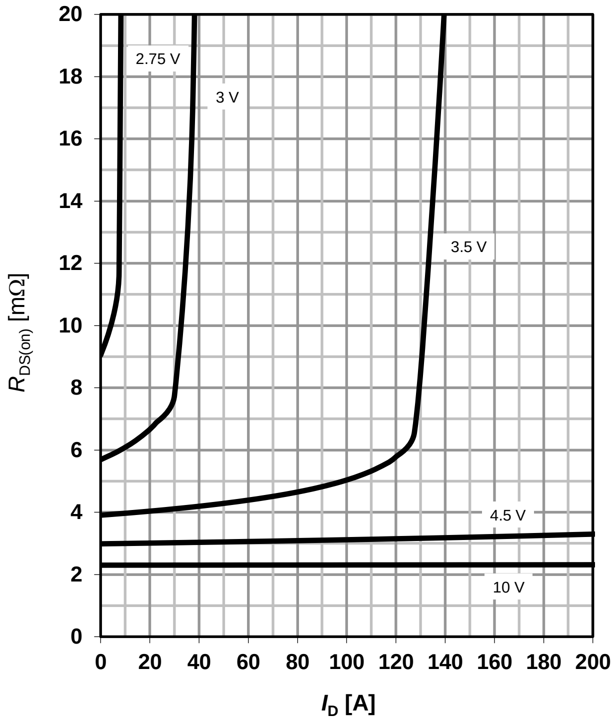
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25\ °C$

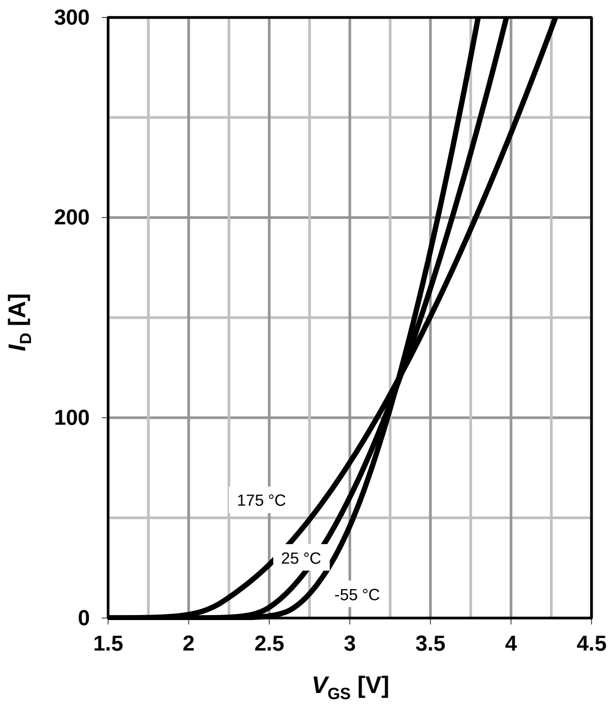
parameter: V_{GS}



7 Typ. transfer characteristics

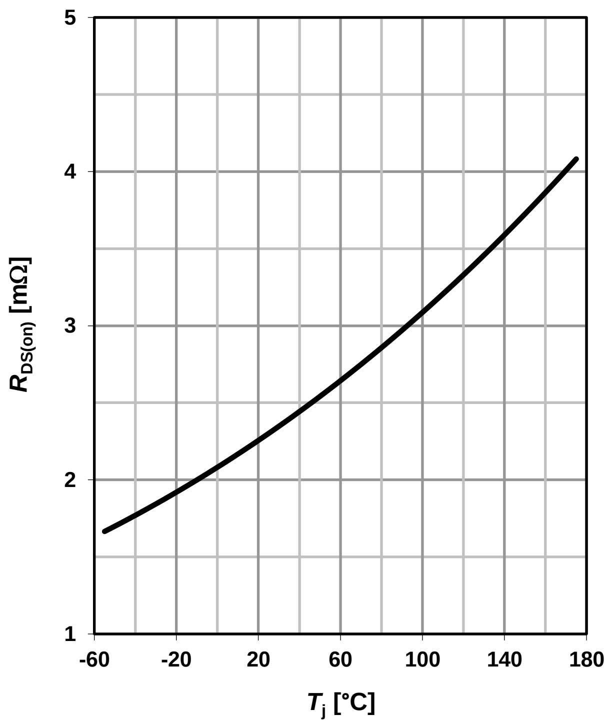
$I_D = f(V_{GS})$; $V_{DS} = 6V$

parameter: T_j



8 Typ. drain-source on-state resistance

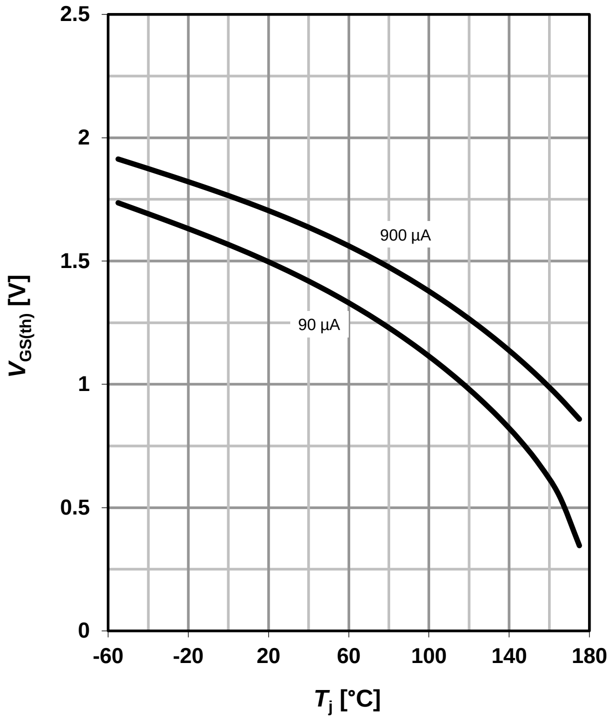
$R_{DS(on)} = f(T_j)$; $I_D = 30\ A$; $V_{GS} = 10\ V$



9 Typ. gate threshold voltage

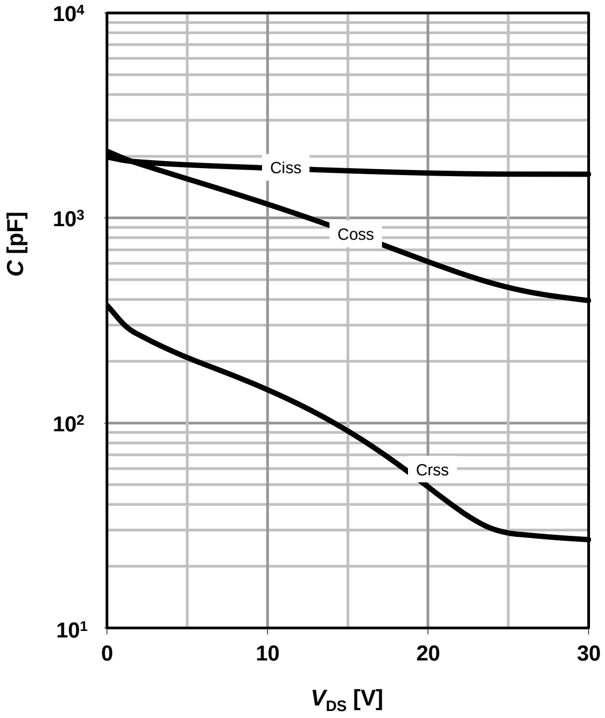
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

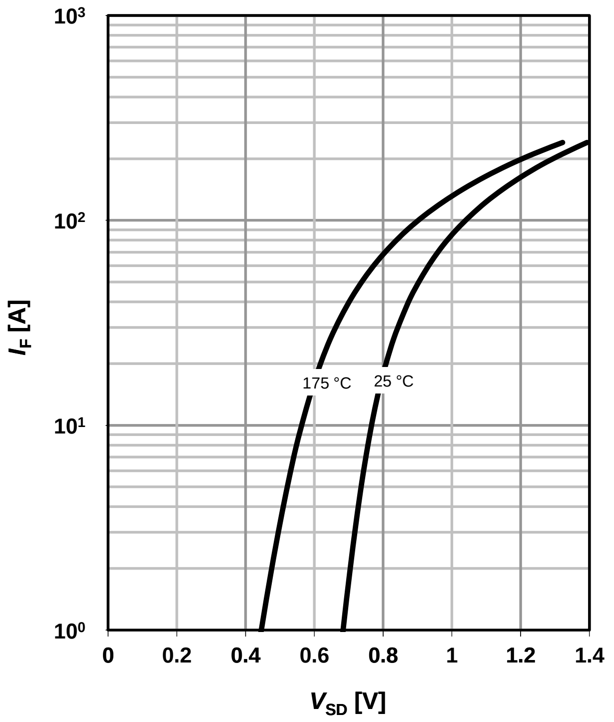
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

$IF = f(V_{SD})$

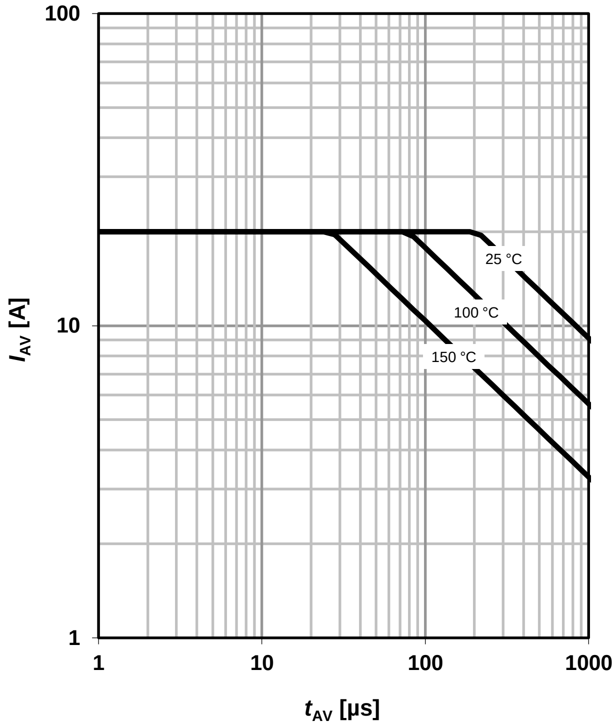
parameter: T_j



12 Avalanche characteristics

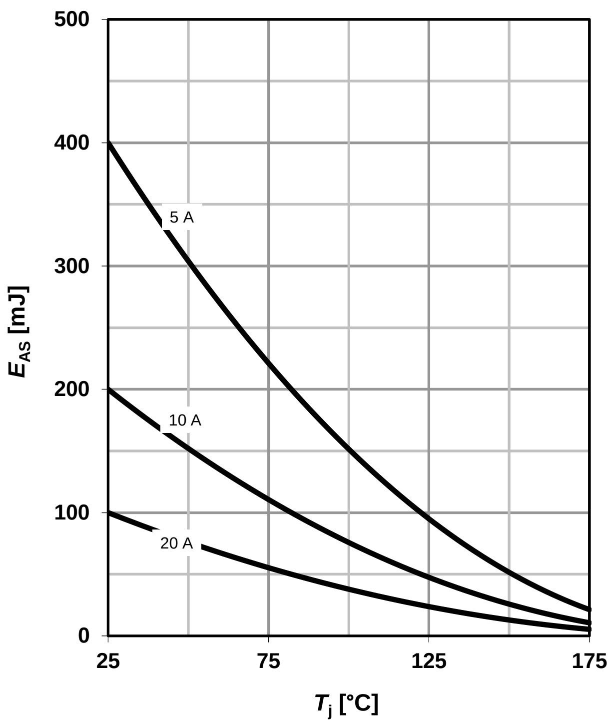
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



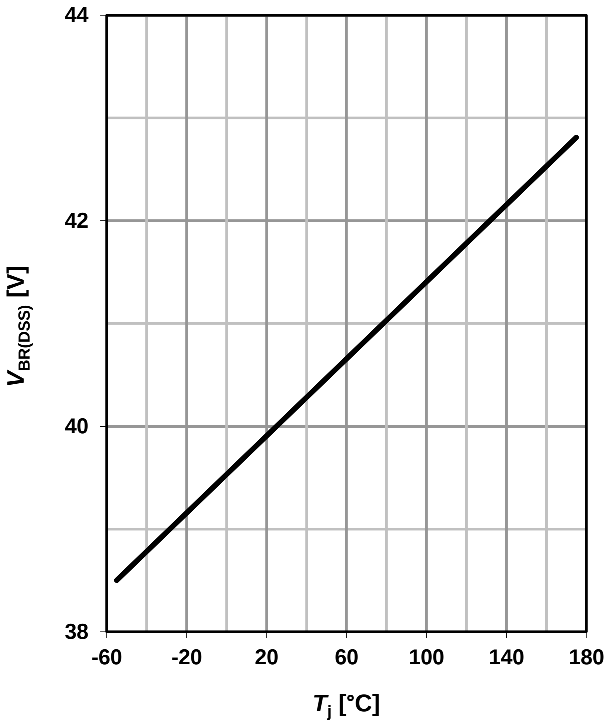
13 Avalanche energy

$E_{AS} = f(T_j)$



14 Drain-source breakdown voltage

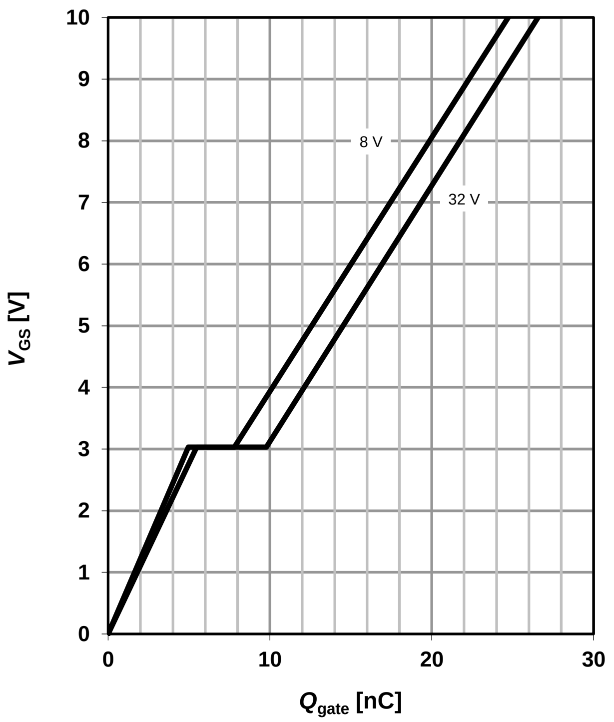
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



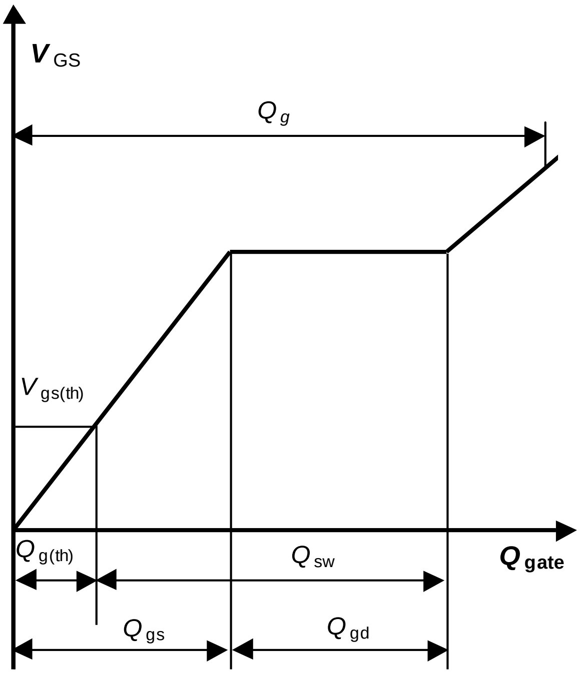
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 40$ A pulsed

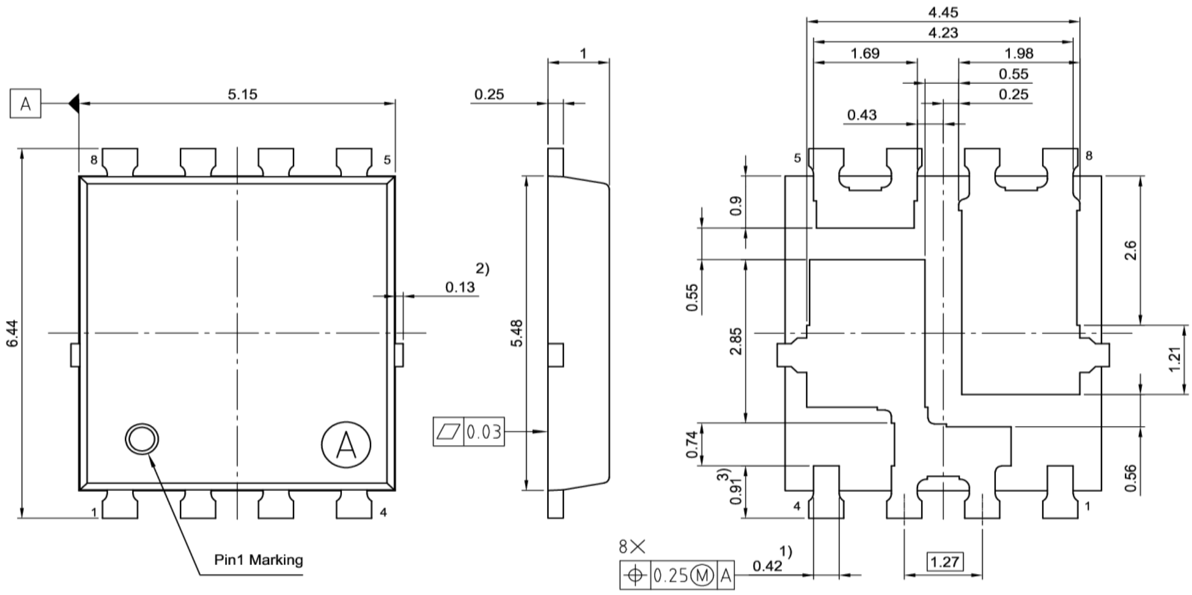
parameter: V_{DD}



16 Gate charge waveforms

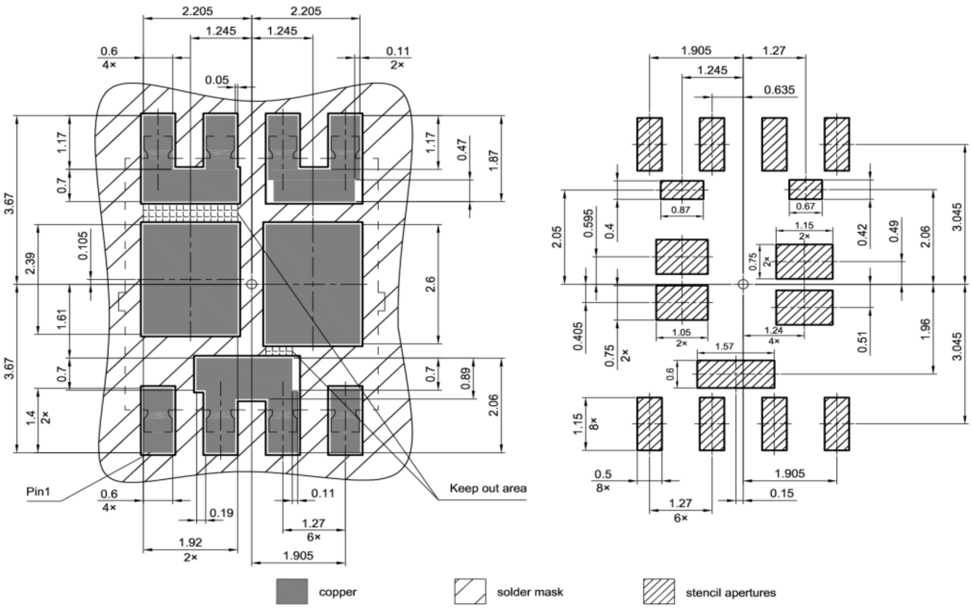


PG-TDSON-8: Outline



1) Excluded mold flash
2) Removal on mold gate: Intrusion 0.1mm, Protrusion 0.1mm
3) Lead length up to anti flash line
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊖⊕]

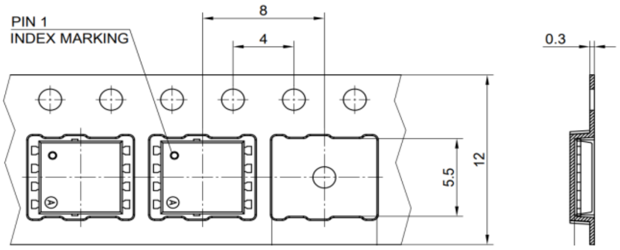
Footprint



Based on stencil thickness 0.15 mm
All dimensions are in units mm

Dimensions in mm

Packaging



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	18.09.2020	Final datasheet