# FDMC007N30D

# MOSFET, Dual N-Channel, POWERTRENCH®

## Q1: 30 V, 11.6 mΩ; Q2: 30 V, 6.4 mΩ

### General Description

This device includes two specialized N−Channel MOSFETs in a dual Power33 (3mm × 3mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

### Features

Q1: N−Channel

- Max $r_{DS(on)}$ = 11.6 mΩ at $V_{GS}$ = 10 V, $I_D$ = 10 A
- Max $r_{DS(on)}$ = 13.3 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 9 A

Q1: N−Channel

- Max $r_{DS(on)}$ = 6.4 mΩ at $V_{GS}$ = 10 V, $I_D$ = 16 A
- Max $r_{DS(on)}$ = 7.0 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 15 A
- RoHS Compliant

### Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

**MOSFET MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Parameter | Q1 | Q2 | Unit |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 30 | 30 | V |
| $V_{GS}$ | Gate to Source Voltage (Note 4) | ±12 | ±12 | V |
| $I_D$ | Drain Current:<br>– Continuous, $T_C$ = 25°C (Note 6)<br>– Continuous, $T_C$ = 100°C (Note 6)<br>– Continuous, $T_A$ = 25°C (Note 1a)<br>– Pulsed (Note 5) | <br>29<br>18<br>10 (Note 1a)<br>113 | <br>46<br>29<br>16 (Note 1b)<br>302 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 24 | 54 | mJ |
| $P_D$ | Power Dissipation for Single Operation:<br>$T_A$ = 25°C<br>$T_A$ = 25°C | <br>1.9 (Note 1a)<br>0.7 (Note 1c) | <br>2.5 (Note 1b)<br>1.0 (Note 1d) | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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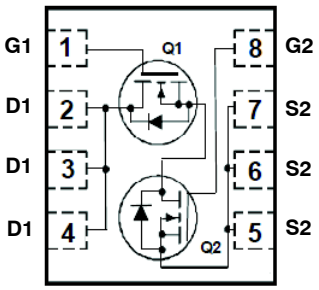
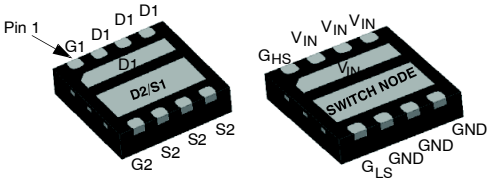



**Dual N-Channel MOSFET**

**Bottom**




**WDFN8 3x3**
**CASE 511DE**

### MARKING DIAGRAM


| | |
|---|---|
| $Y | = ON Semiconductor Logo |
| &Z | = Assembly Plant Code |
| &2 | = Data Code (Year & Week) |
| &K | = Lot |
| FDMC7N30D | = Specific Device Code |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## PACKAGE MARKING AND ORDERING INFORMATION

| Device Marking | Device | Package | Quantity |
|---|---|---|---|
| FDMC7N30D | FDMC007N30D | WDFN−8<br>(Power 33) | 3000/Tape&Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Q1 | Q2 | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 8.2 | 6.1 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | 65 (Note 1a) | 50 (Note 1b) | |
| | | 180 (Note 1c) | 125 (Note 1d) | |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

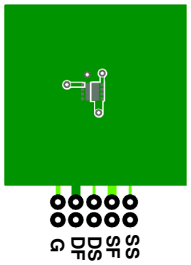
| Symbol | Parameter | Test Condition | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V<br>$I_D$ = 250 μA, $V_{GS}$ = 0 V | Q1<br>Q2 | 30<br>30 | | | V |
| $\Delta BV_{DSS}$ /$\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C<br>$I_D$ = 250 μA, referenced to 25°C | Q1<br>Q2 | | 15<br>16 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 V | Q1<br>Q2 | | | ±100<br>±100 | nA |
| **ON CHARACTERISTICS** | | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA<br>$V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | Q1<br>Q2 | 1.0<br>1.0 | 1.3<br>1.8 | 3.0<br>3.0 | V |
| $\Delta V_{GS(th)}$ /$\Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C<br>$I_D$ = 250 μA, referenced to 25°C | Q1<br>Q2 | | −4<br>−4 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 10 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 9 A<br>$V_{GS}$ = 10 V, $I_D$ = 10 A, $T_J$ = 125°C | Q1 | | 7.7<br>8.9<br>10.8 | 11.6<br>13.3<br>16.3 | mΩ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 16 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 15 A<br>$V_{GS}$ = 10 V, $I_D$ = 16 A, $T_J$ = 125°C | Q2 | | 4.4<br>5.4<br>6.2 | 6.4<br>7.0<br>9.0 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 10 A<br>$V_{DD}$ = 5 V, $I_D$ = 16 A | Q1<br>Q2 | | 46<br>70 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | Q1<br>Q2 | | 792<br>1685 | 1110<br>2360 | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | | 230<br>467 | 325<br>655 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 20<br>36 | 30<br>50 | pF |
| $R_g$ | Gate Resistance | | Q1<br>Q2 | 0.1<br>0.1 | 2.0<br>1.2 | 4.0<br>2.4 | Ω |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued)

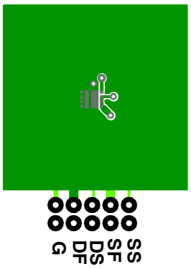
| Symbol | Parameter | Test Condition | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | Q1<br>$V_{DD}$ = 15 V, $I_D$ = 10 A,<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω<br><br>Q2<br>$V_{DD}$ = 15 V, $I_D$ = 16 A,<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 7<br>10 | 14<br>20 | ns |
| $t_r$ | Rise Time | | Q1<br>Q2 | | 2<br>3 | 10<br>10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1<br>Q2 | | 19<br>24 | 33<br>39 | ns |
| $t_f$ | Fall Time | | Q1<br>Q2 | | 2<br>3 | 10<br>10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, Q1 $V_{DD}$ = 15 V, $I_D$ = 10 A | Q1<br>Q2 | | 12<br>24 | 17<br>34 | nC |
| | | $V_{GS}$ = 0 V to 4.5 V, Q1 $V_{DD}$ = 15 V, $I_D$ = 10 A | Q1<br>Q2 | | 5.5<br>11 | 7.7<br>16 | nC |
| $Q_{gs}$ | Gate to Source Charge | Q2 $V_{DD}$ = 15 V, $I_D$ = 16 A | Q1<br>Q2 | | 1.7<br>4.4 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | Q1<br>Q2 | | 1.3<br>2.7 | | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| $V_{SD}$ | Source−Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 10 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 1.5 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 16 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 2 A (Note 2) | Q1<br>Q1<br>Q2<br>Q2 | | 0.85<br>0.75<br>0.83<br>0.73 | 1.2<br>1.2<br>1.2<br>1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | Q1<br>$I_F$ = 10 A, di/dt = 100 A/μs | Q1<br>Q2 | | 17<br>27 | 31<br>42 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | Q2<br>$I_F$ = 16 A, di/dt = 100 A/μs | Q1<br>Q2 | | 5<br>10 | 10<br>20 | nC |

NOTES:

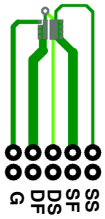
1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user’s board design.




a. 65 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.




b. 50 °C/W when mounted on a1 $in^2$ pad of 2 oz copper.




c. 180 °C/W when mounted on a minimum pad of 2 oz copper.


d. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 uS, Duty cycle < 2.0%.
3. Q1: $E_{AS}$ of 24 mJ is based on starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = 4 A, $V_{DD}$ = 30 V, $V_{GS}$ = 10 V. 100% tested at L = 0.1 mH, $I_{AS}$ = 13 A.
   Q2: $E_{AS}$ of 54 mJ is based on starting $T_J$ = 25°C, L = 3 mH, $I_{AS}$ = 6 A, $V_{DD}$ = 30 V, $V_{GS}$ = 10 V. 100% tested at L = 0.1 mH, $I_{AS}$ = 22 A.
4. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
5. Pulsed Id please refer to Figure 11 and Figure. 24 SOA graph for more details.
6. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

## TYPICAL CHARACTERISTICS (Q1 N−CHANNEL)

($T_J$ = 25°C unless otherwise noted)

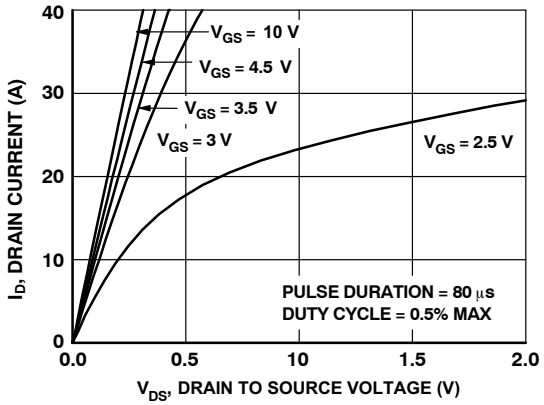



**Figure 1. On Region Characteristics**

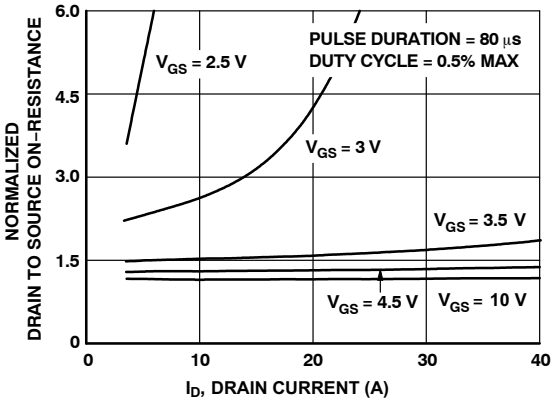



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

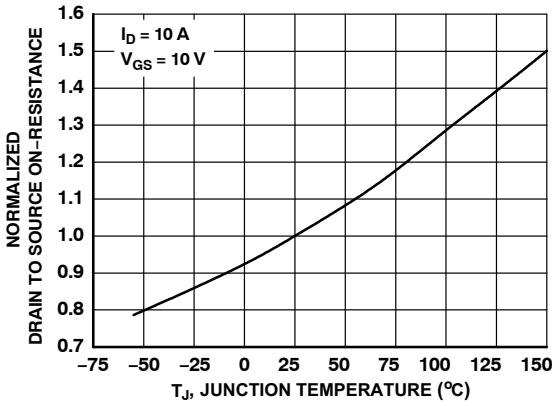



**Figure 3. Normalized On Resistance vs. Junction Temperature**

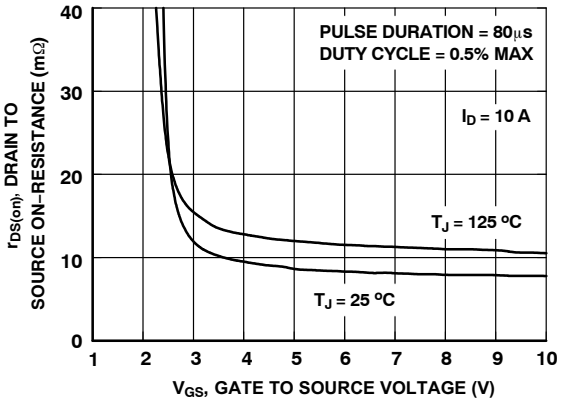



**Figure 4. On−Resistance vs. Gate to Source Voltage**

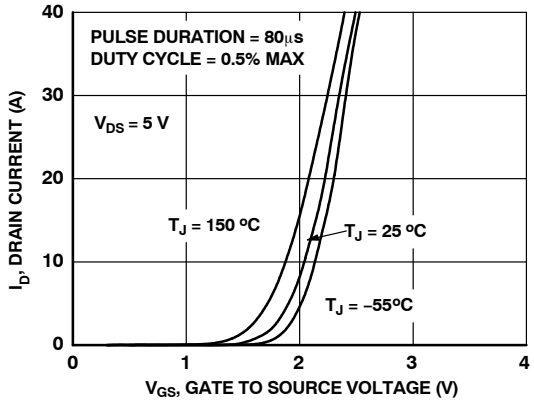



**Figure 5. Transfer Characteristics**

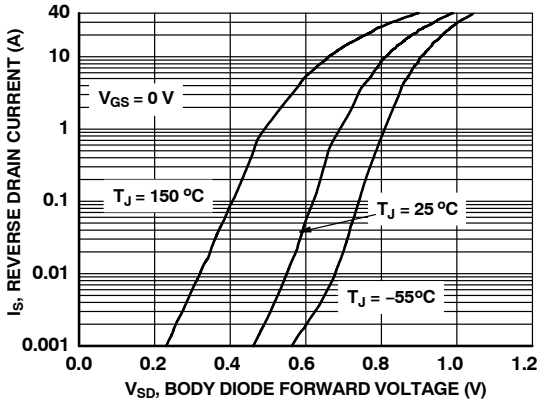



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (continued)

($T_J$ = 25°C unless otherwise noted)

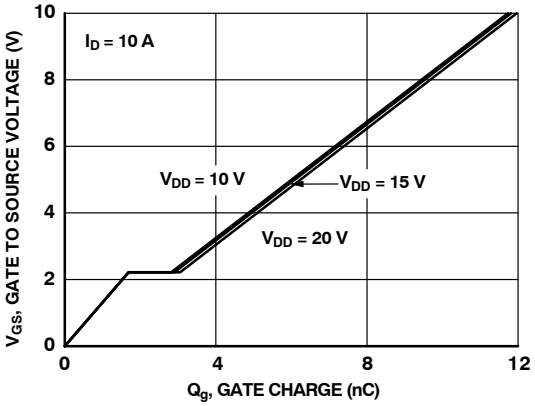



**Figure 7. Gate Charge Characteristics**

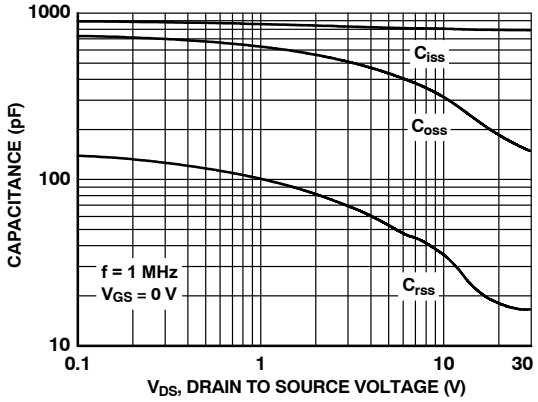



**Figure 8. Capacitance vs. Drain to Source Voltage**

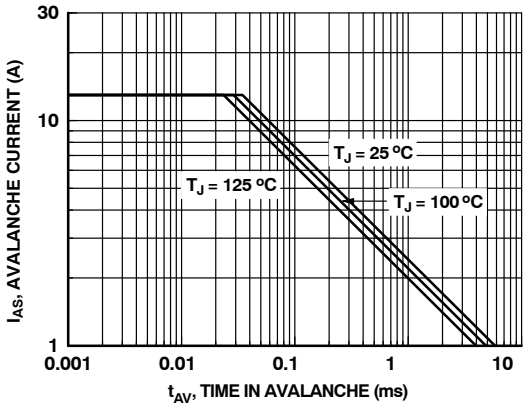



**Figure 9. Unclamped Inductive Switching Capability**

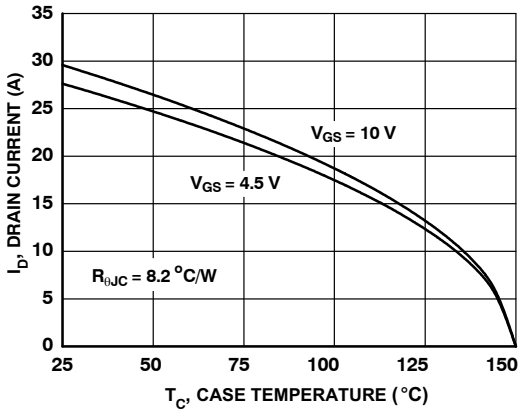



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

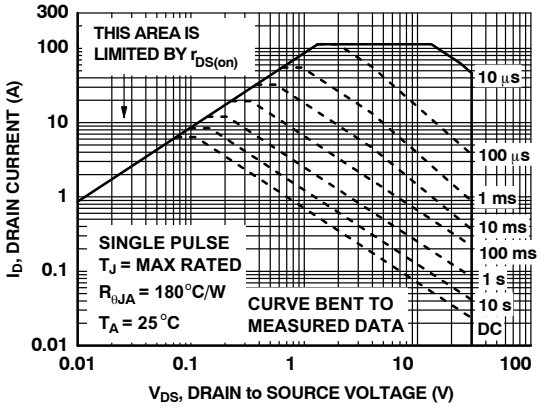



**Figure 11. Forward Bias Safe Operating Area**

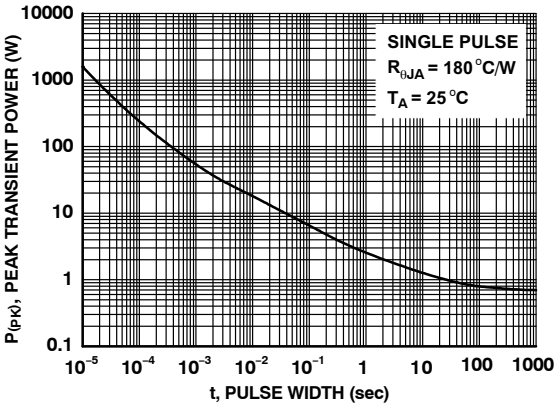



**Figure 12. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (continued)

($T_J$ = 25°C unless otherwise noted)

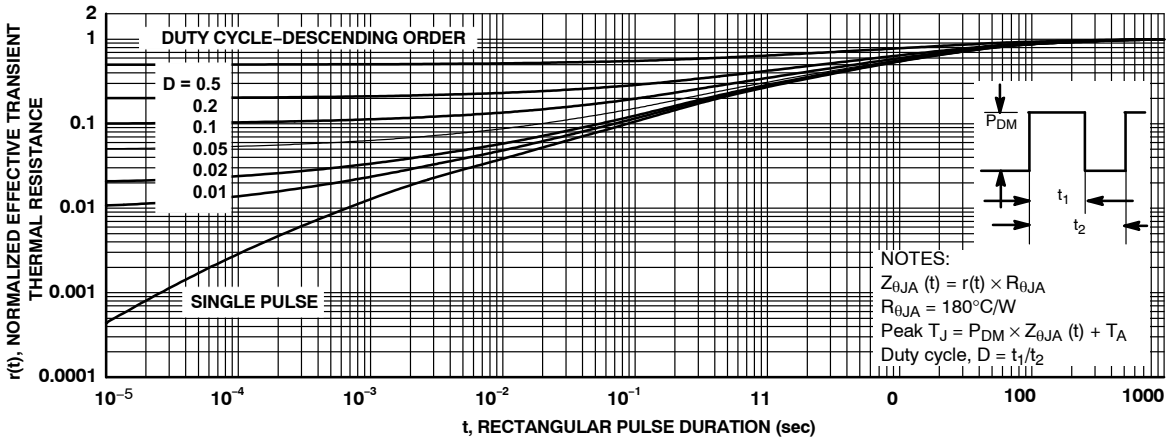



**Figure 13. Junction−to−Ambient Transient Thermal Response Curve**

## TYPICAL CHARACTERISTICS (Q2 N−CHANNEL)

($T_J$ = 25°C unless otherwise noted)

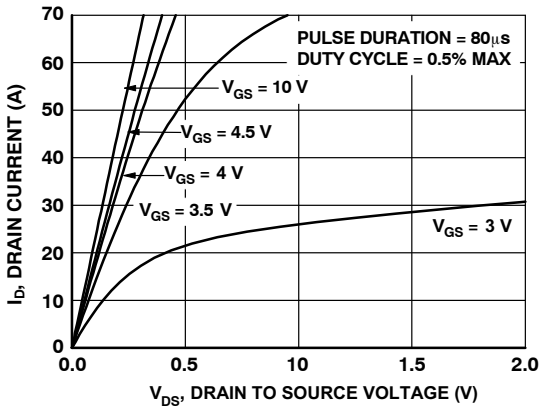



Figure 14. On Region Characteristics

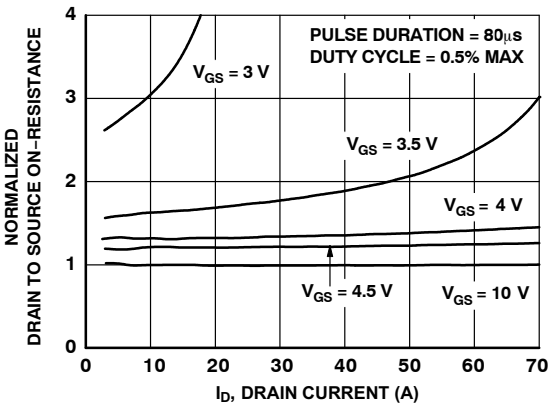



Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage

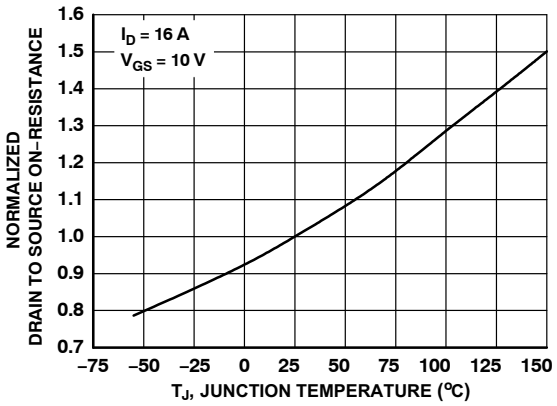



Figure 16. Normalized On Resistance vs. Junction Temperature

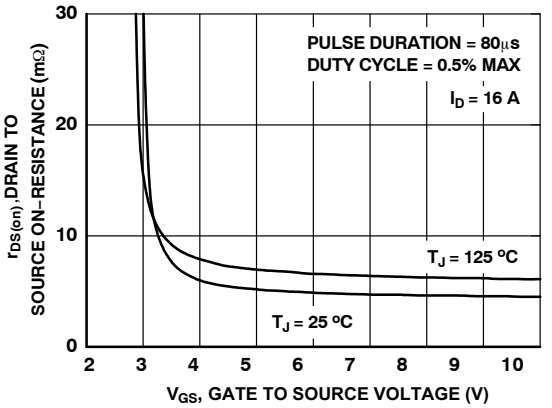



Figure 17. On−Resistance vs. Gate to Source Voltage

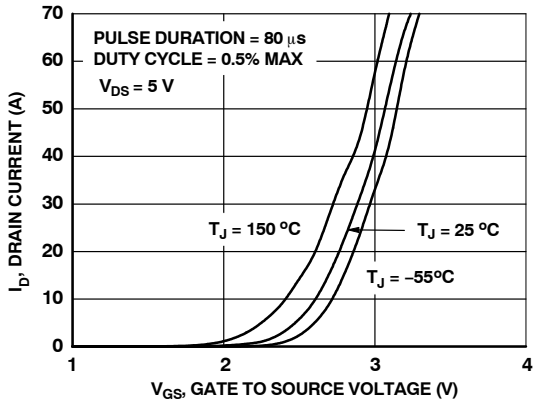



Figure 18. Transfer Characteristics

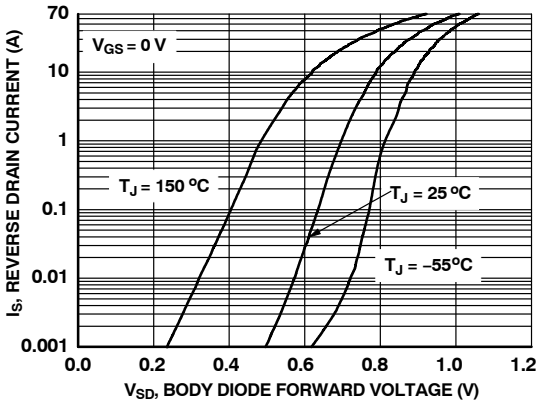



Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

## TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (continued)

($T_J$ = 25°C unless otherwise noted)

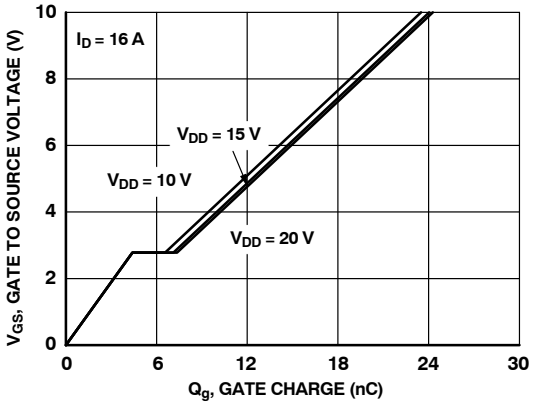



**Figure 20. Gate Charge Characteristics**

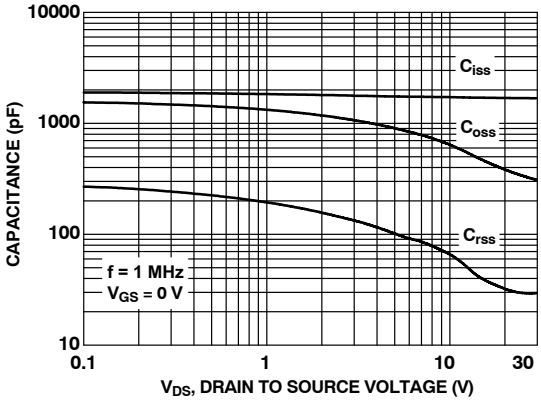



**Figure 21. Capacitance vs. Drain to Source Voltage**

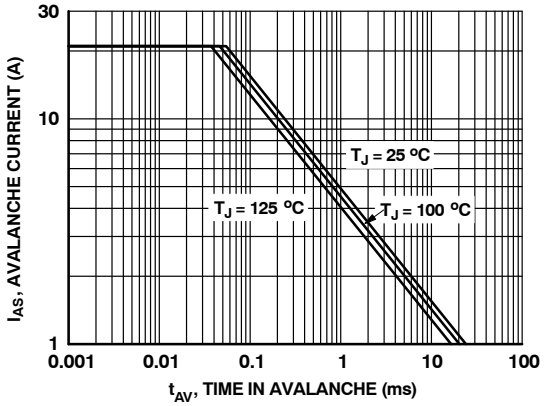



**Figure 22. Unclamped Inductive Switching Capability**

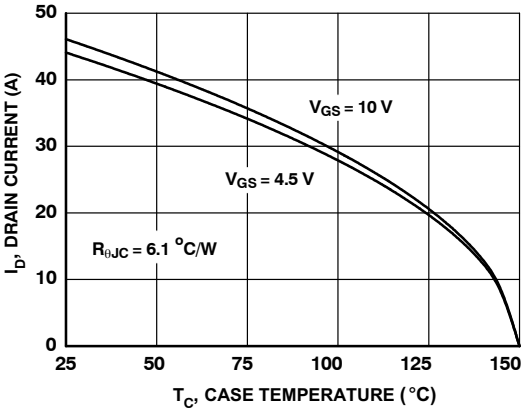



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

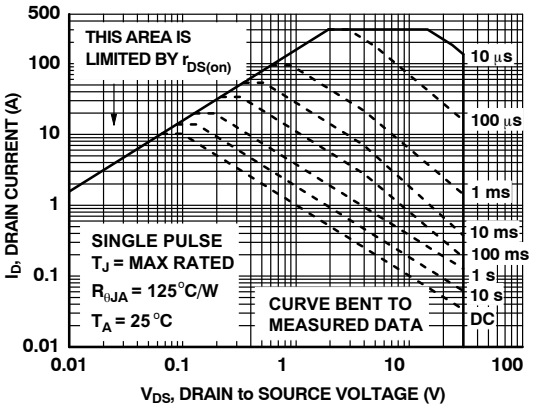



**Figure 24. Forward Bias Safe Operating Area**

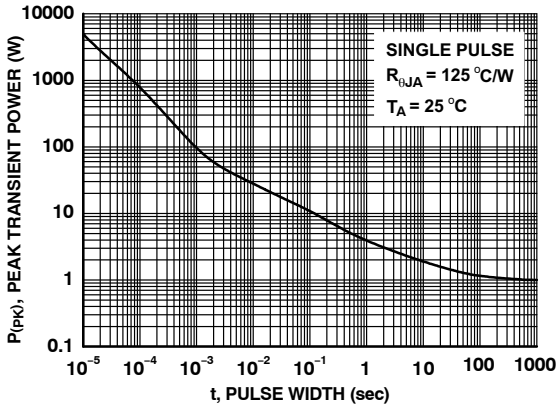



**Figure 25. Single Pulse Maximum Power Dissipation**

## TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (continued)

($T_J$ = 25°C unless otherwise noted)

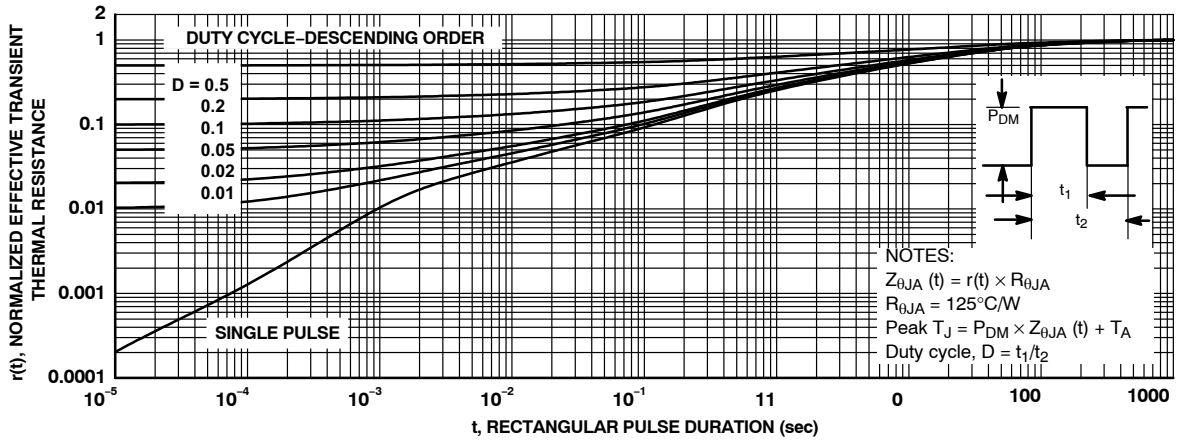
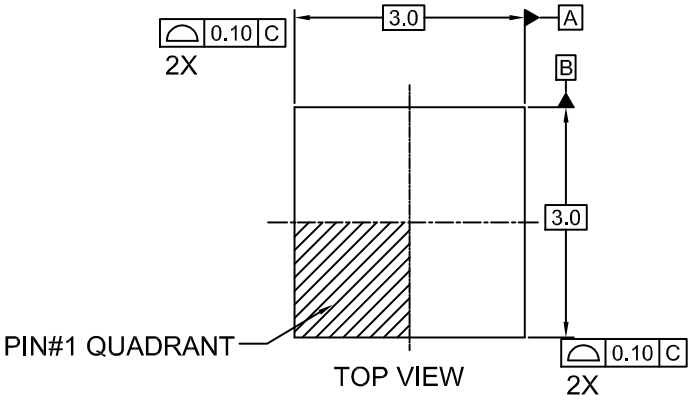
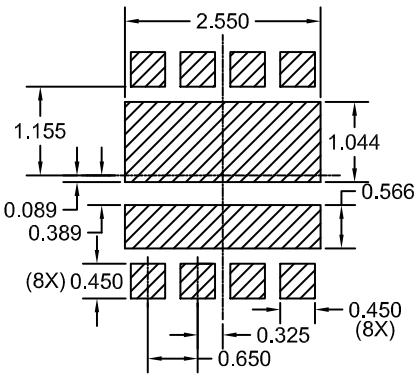



**Figure 26. Junction−to−Ambient Transient Thermal Response Curve**

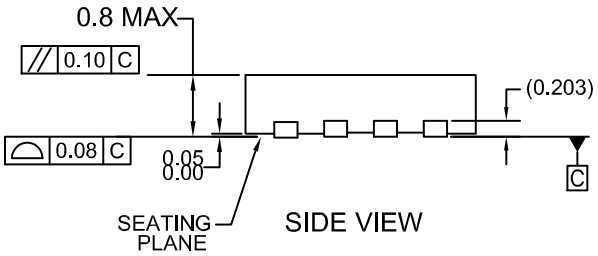
**WDFN8 3x3, 0.65P**
CASE 511DE
ISSUE O

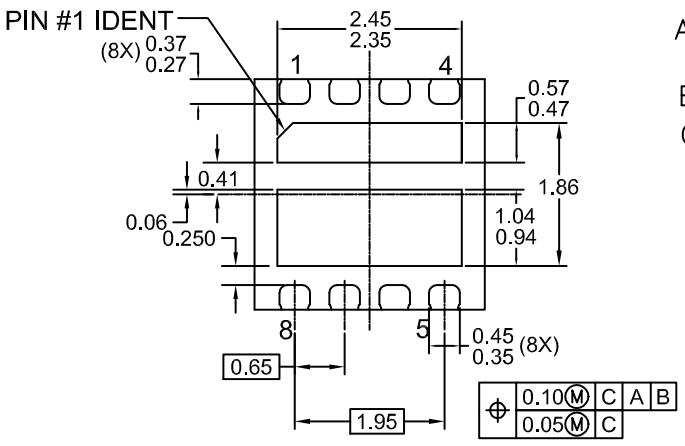
DATE 31 AUG 2016




RECOMMENDED LAND PATTERN




BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

| | | |
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