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ON Semiconductor®

FDMQ8203

GreenBridge™ Series of High-Efficiency Bridge Rectifiers
Dual N-Channel and Dual P-Channel PowerTrench® MOSFET
N-Channel: 100 V, 6 A, 110 mΩ P-Channel: -80 V, -6 A, 190 mΩ

Features

Q1/Q4: N-Channel

- Max $r_{DS(on)}$ = 110 mΩ at V_{GS} = 10 V, I_D = 3 A
- Max $r_{DS(on)}$ = 175 mΩ at V_{GS} = 6 V, I_D = 2.4 A

Q2/Q3: P-Channel

- Max $r_{DS(on)}$ = 190 mΩ at V_{GS} = -10 V, I_D = -2.3 A
- Max $r_{DS(on)}$ = 235 mΩ at V_{GS} = -4.5 V, I_D = -2.1 A
- Substantial efficiency benefit in PD solutions
- RoHS Compliant

General Description

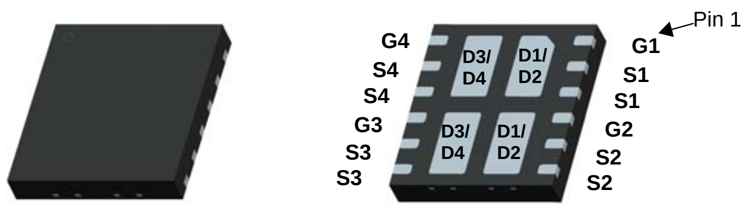
This quad mosfet solution provides ten-fold improvement in power dissipation over diode bridge.

Application

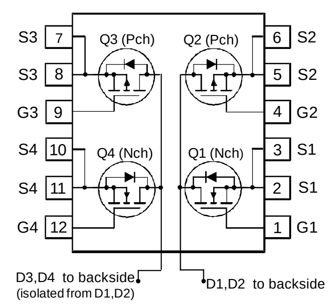
- High-Efficiency Bridge Rectifiers

Top

Bottom



MLP 4.5x5



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter				Q1/Q4	Q2/Q3	Units
V_{DS}	Drain to Source Voltage				100	-80	V
V_{GS}	Gate to Source Voltage				±20	±20	V
I_D	Drain Current	-Continuous (Package limited)	T_C = 25 °C		6	-6	A
		-Continuous (Silicon limited)	T_C = 25 °C		10	-10	
		-Continuous	T_A = 25 °C	(Note 1a)	3.4	-2.6	
		-Pulsed			12	-10	
P_D	Power Dissipation for Single Operation		T_C = 25 °C		22	37	W
	Power Dissipation for Dual Operation		T_A = 25 °C	(Note 1a)	2.5		
T_J, T_{STG}	Operating and Storage Junction Temperature Range				-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	160	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMQ8203	FDMQ8203	MLP4.5x5	13 ”	12 mm	3000 units

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Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = -250 μA, V_{GS} = 0 V	Q1/Q4 Q2/Q3	100 -80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = -250 μA, referenced to 25 °C	Q1/Q4 Q2/Q3		72 -79		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V V_{DS} = -64 V, V_{GS} = 0 V	Q1/Q4 Q2/Q3			1 -1	μA μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS}= 0 V	Q1/Q4 Q2/Q3			±100 ±100	nA nA

On Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = -250 μA	Q1/Q4 Q2/Q3	2 -1	3 -1.6	4 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C I_D = -250 μA, referenced to 25 °C	Q1/Q4 Q2/Q3		-8 5		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3 A V_{GS} = 6 V, I_D = 2.4 A V_{GS} = 10 V, I_D = 3 A , T_J = 125 °C	Q1/Q4		85 118 147	110 175 191	mΩ
		V_{GS} = -10 V, I_D = -2.3 A V_{GS} = -4.5 V, I_D = -2.1 A V_{GS} = -10 V, I_D = -2.3 A, T_J = 125 °C	Q2/Q3		161 188 273	190 235 323	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3 A V_{DS} = -10 V, I_D = -2.3 A	Q1/Q4 Q2/Q3		6 6		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
C_{iss}	Input Capacitance	Q1/Q4: V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHZ Q2/Q3: V_{DS} = -40 V, V_{GS} = 0 V, f = 1 MHZ	Q1/Q4 Q2/Q3		158 639	210 850	pF
C_{oss}	Output Capacitance		Q1/Q4 Q2/Q3		41 46	55 65	pF
C_{rss}	Reverse Transfer Capacitance		Q1/Q4 Q2/Q3		2.6 24	5 40	pF

Switching Characteristics

Symbol	Parameter	Test Conditions		Type	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	Q1/Q4: V_{DD} = 50 V, I_D = 3 A, V_{GS} = 10 V, R_{GEN} = 6 Ω Q2/Q3: V_{DD} = -40 V, I_D = -2.3 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		Q1/Q4 Q2/Q3		3.8 4.7	10 10	ns
t_r	Rise Time			Q1/Q4 Q2/Q3		1.3 2.8	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time			Q1/Q4 Q2/Q3		7.5 22	15 35	ns
t_f	Fall Time			Q1/Q4 Q2/Q3		1.9 2.7	10 10	ns
Q_g	Total Gate Charge	VGS = 0 V to 10 V VGS = 0 V to -10 V	Q1/Q4: V_{DD} = 50 V, I_D = 3 A Q2/Q3: V_{DD} = -40 V, I_D = -2.3A	Q1/Q4 Q2/Q3		2.9 13	5 19	nC
Q_g	Total Gate Charge	VGS = 0 V to 5 V VGS = 0 V to -4.5 V		Q1/Q4 Q2/Q3		1.6 6.4	3 10	nC
Q_{gs}	Gate to Source Gate Charge			Q1/Q4 Q2/Q3		0.8 1.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			Q1/Q4 Q2/Q3		0.8 2.6		nC

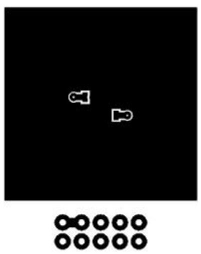
Electrical Characteristics T_J = 25 °C unless otherwise noted

Drain-Source Diode Characteristics

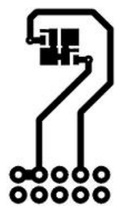
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 3 A (Note 2) V_{GS} = 0 V, I_S = -2.3 A (Note 2)	Q1/Q4 Q2/Q3		0.86 -0.82	1.3 -1.3	V
t_{rr}	Reverse Recovery Time	Q1/Q4: I_F = 3 A, di/dt = 100 A/μs	Q1/Q4 Q2/Q3		32 26	52 42	ns
Q_{rr}	Reverse Recovery Charge	Q2/Q3: I_F = -2.3 A, di/dt = 100 A/μs	Q1/Q4 Q2/Q3		21 26	34 42	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.



b. 160 °C/W when mounted on a minimum pad of 2 oz copper, the board designed Q1+Q3 or Q2+Q4.

2: Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

Typical Characteristics (N-Channel) T_J = 25 °C unless otherwise noted

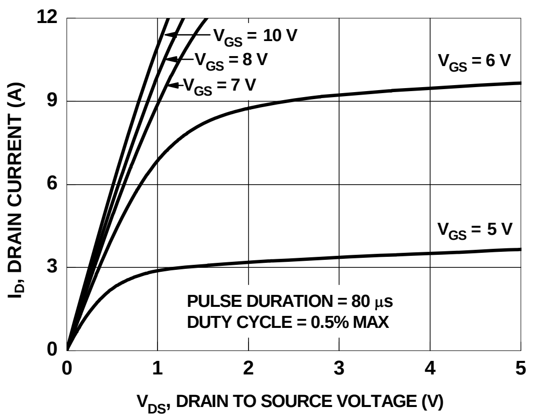


Figure 1. On Region Characteristics

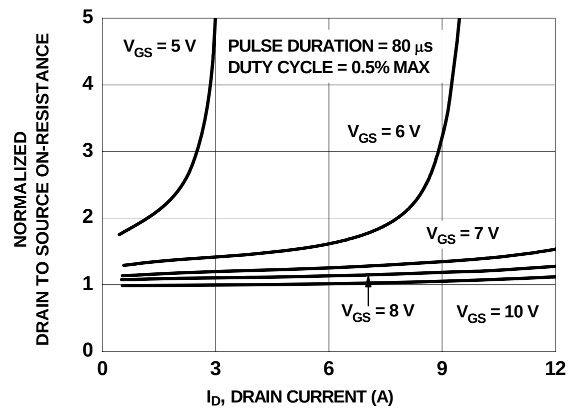


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

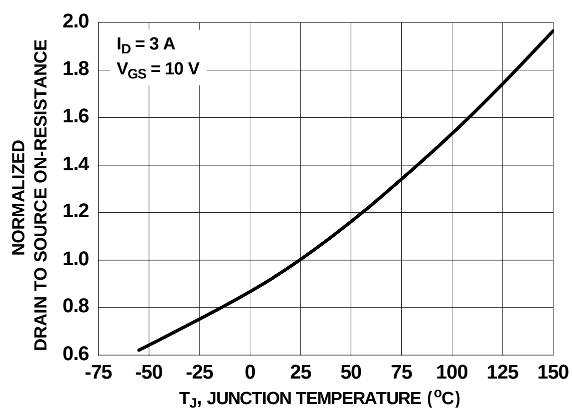


Figure 3. Normalized On Resistance vs Junction Temperature

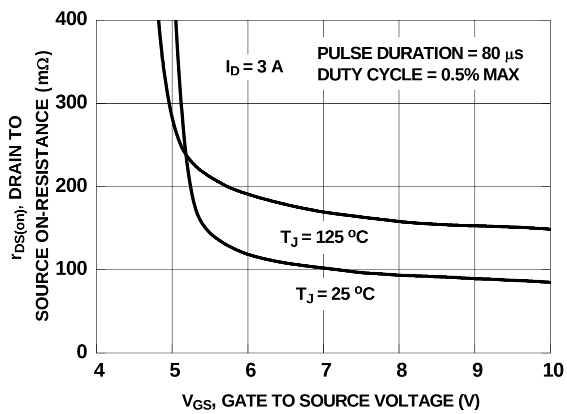


Figure 4. On-Resistance vs Gate to Source Voltage

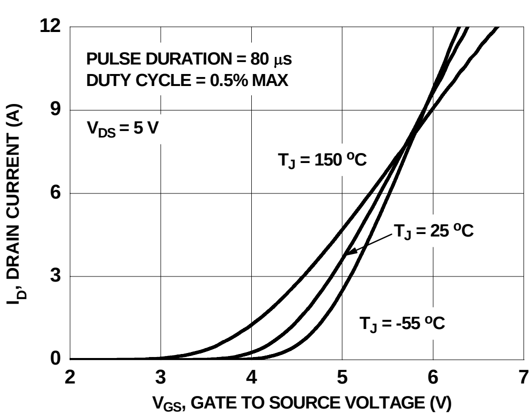


Figure 5. Transfer Characteristics

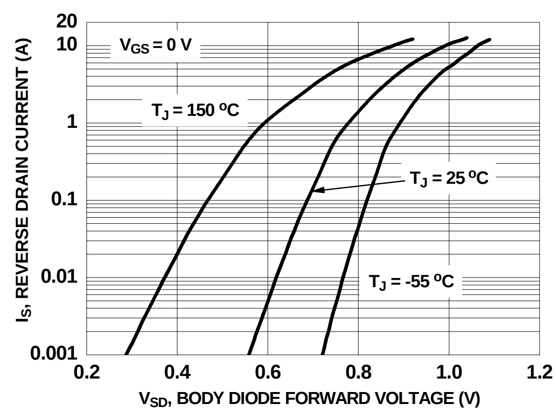


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (N-Channel) T_J = 25 °C unless otherwise noted

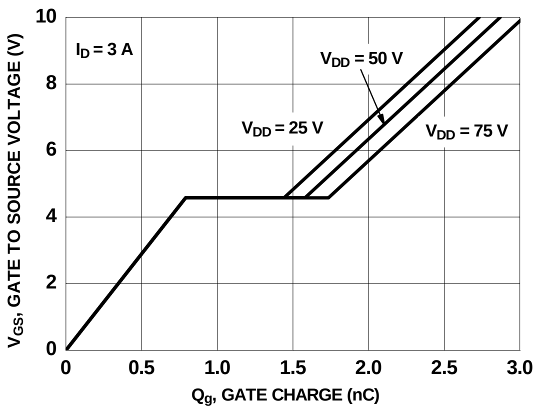


Figure 7. Gate Charge Characteristics

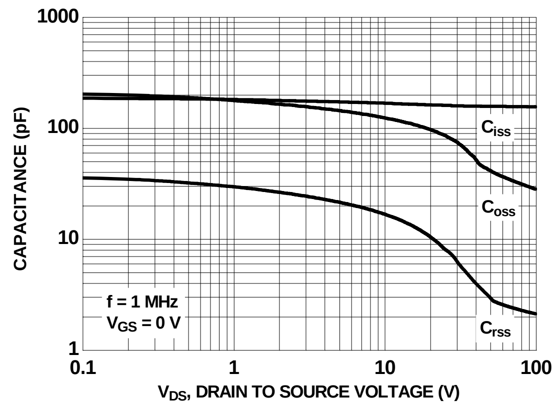


Figure 8. Capacitance vs Drain to Source Voltage

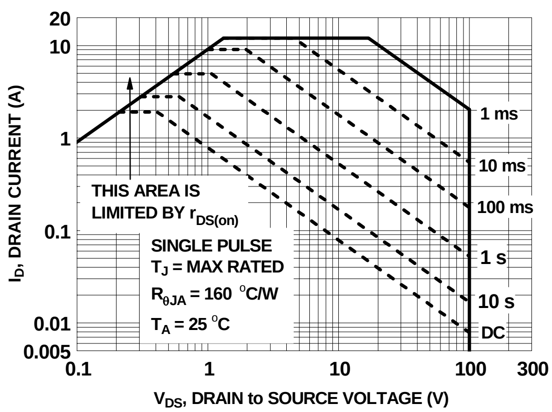


Figure 9. Forward Bias Safe Operating Area

Typical Characteristics (P-Channel) T_J = 25 °C unlenss otherwise noted

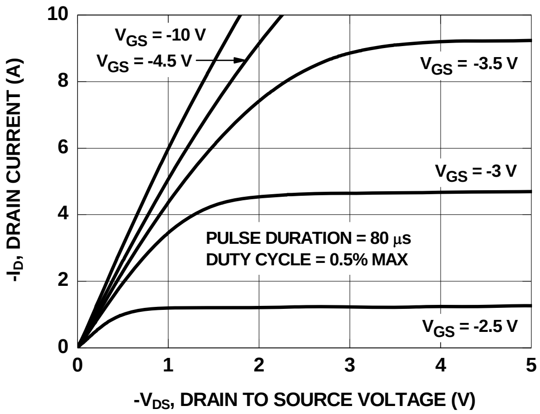


Figure 10. On-Region Characteristics

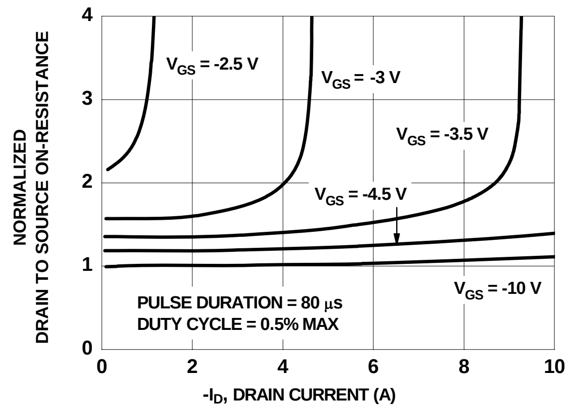


Figure 11. Normalized on-Resistance vs Drain Current and Gate Voltage

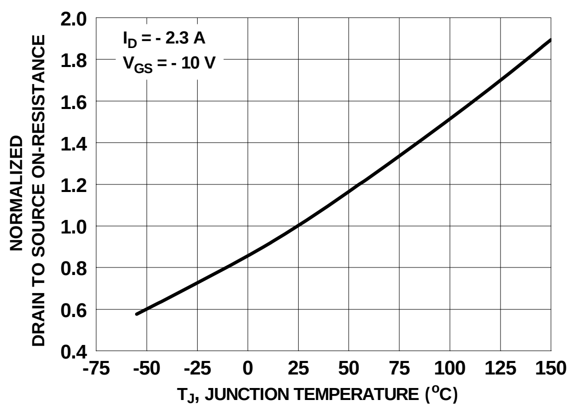


Figure 12. Normalized On-Resistance vs Junction Temperature

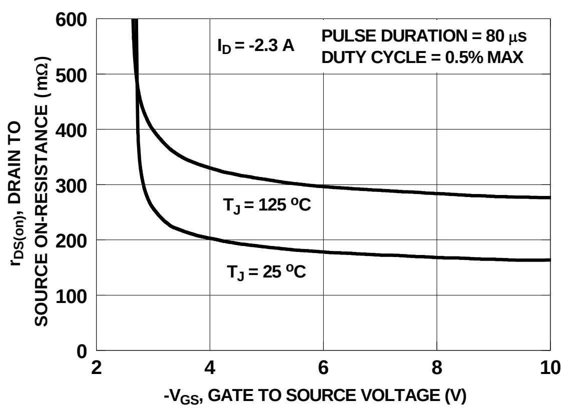


Figure 13. On-Resistance vs Gate to Source Voltage

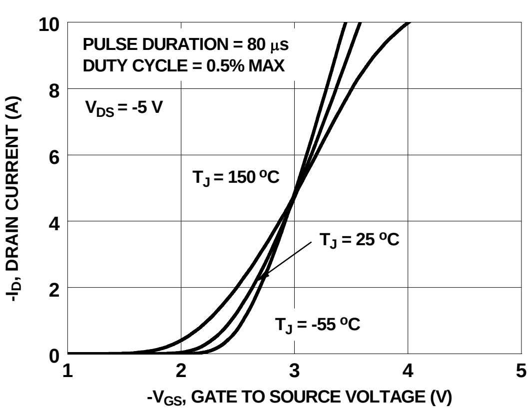


Figure 14. Transfer Characteristics

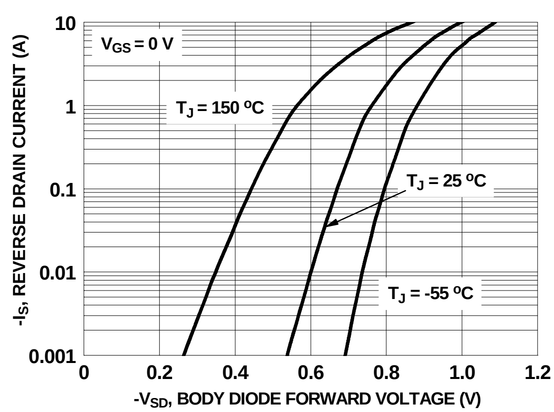


Figure 15. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (P-Channel) T_J = 25 ^oC unlenss otherwise noted

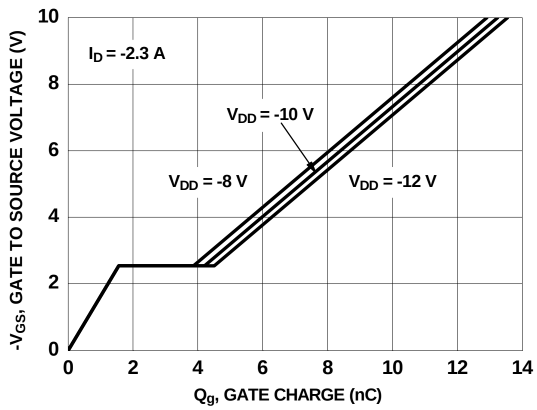


Figure 16. Gate Charge Characteristics

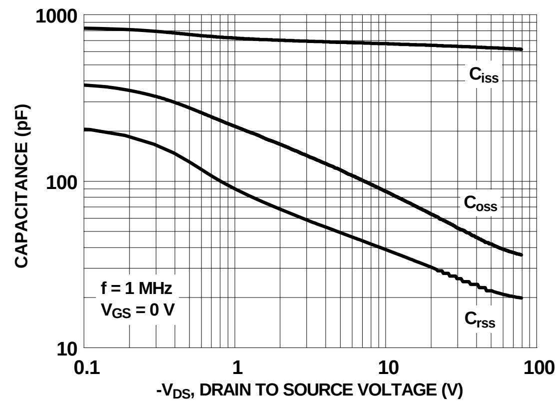


Figure 17. Capacitance vs Drain to Source Voltage

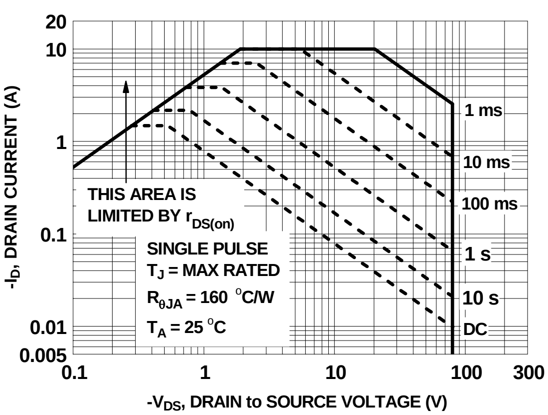


Figure 18. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unlenss otherwise noted

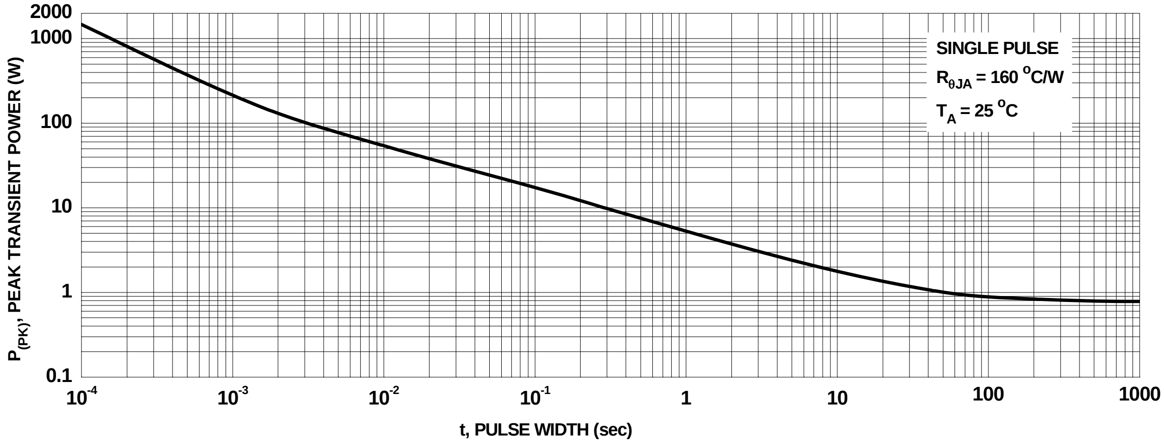


Figure 19. Single Pulse Maximum Power Dissipation

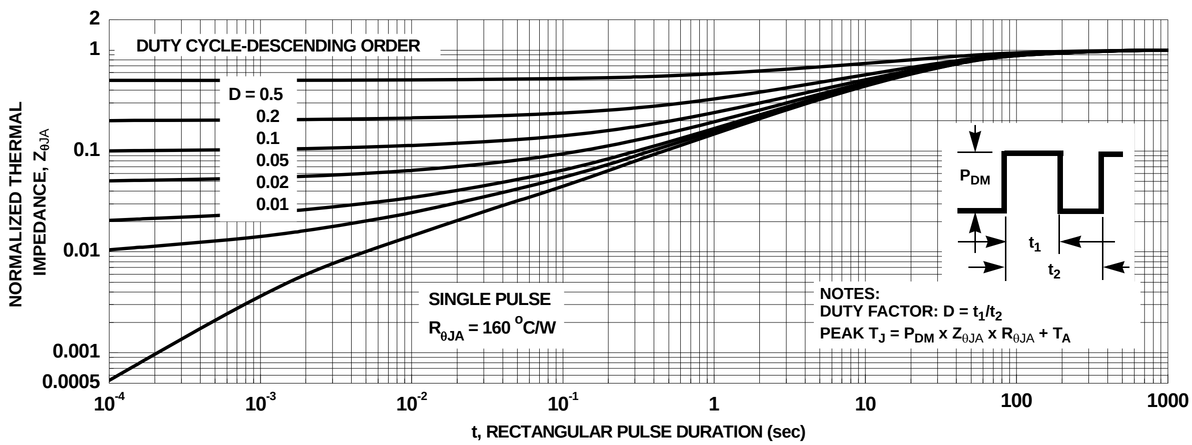
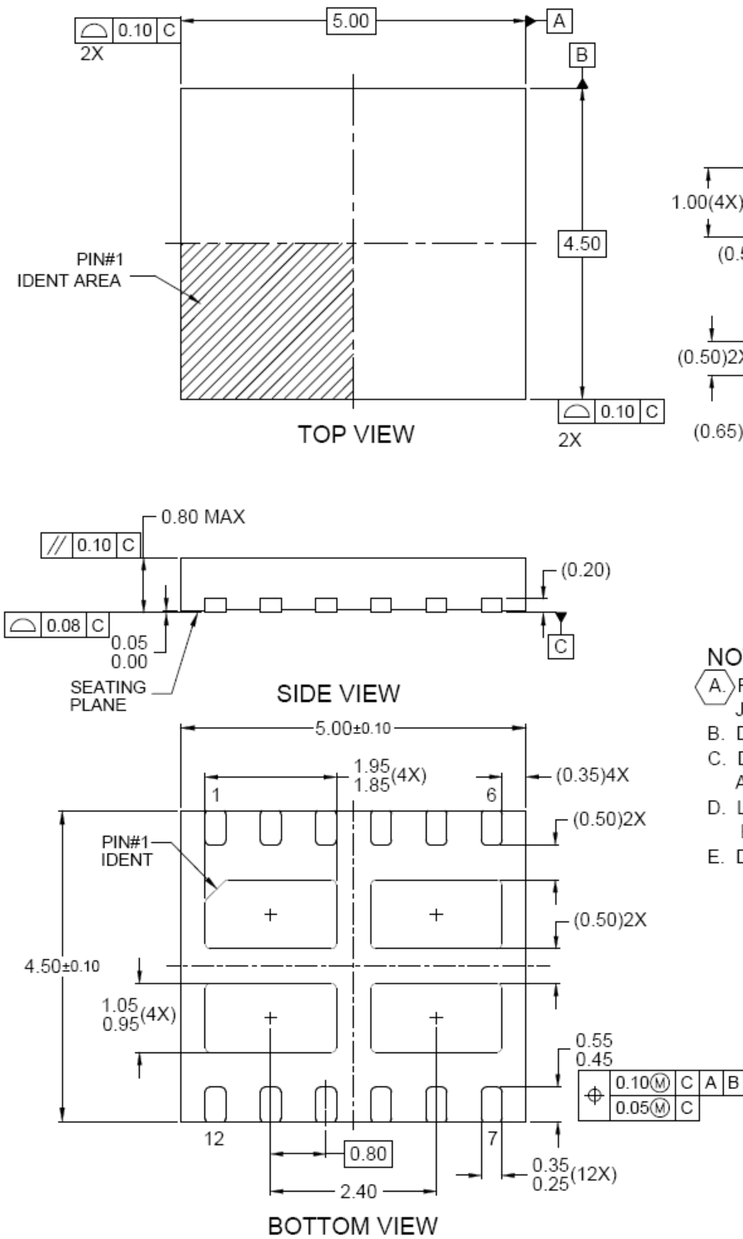
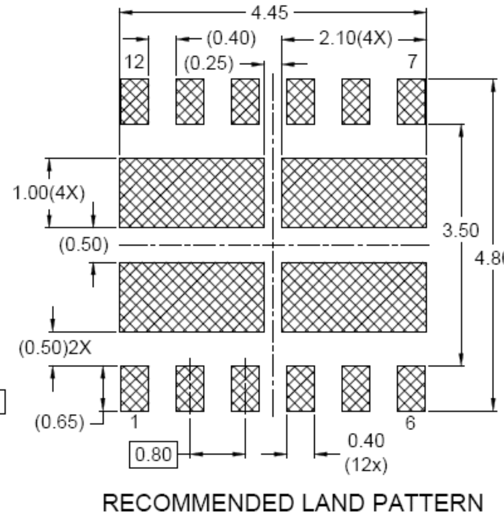


Figure 20. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout





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