

NTJD4158C, NVJD4158C

MOSFET – Small Signal, Complementary, SC-88 30 V/-20 V, +0.25/-0.88 A

Features

- Leading 20 V Trench for Low $R_{DS(on)}$ Performance
- ESD Protected Gate
- SC-88 Package for Small Footprint (2 x 2 mm)
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Conversion
- Load/Power Management
- Load Switch
- Cell Phones, MP3s, Digital Cameras, PDAs

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage	N-Ch	V_{DS}	30	V
	P-Ch		-20	
Gate-to-Source Voltage	N-Ch	V_{GS}	± 20	V
	P-Ch		± 12	
N-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D 0.25	A
		$T_A = 85^\circ\text{C}$	0.18	
P-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-0.88	
		$T_A = 85^\circ\text{C}$	-0.63	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D 0.27	W
Pulsed Drain Current	N-Ch	$t_p = 10 \mu\text{s}$	I_{DM} 0.5	A
	P-Ch		-3.0	
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	N-Ch	I_S	0.25	A
	P-Ch		-0.48	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	460	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

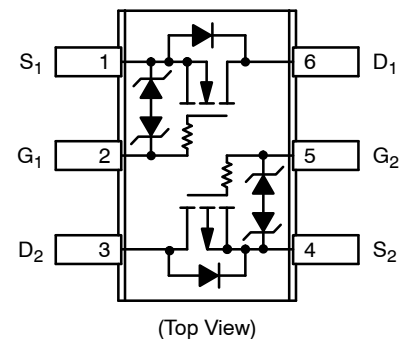


ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
N-Ch 30 V	1.0 Ω @ 4.5 V	0.25 A
	1.5 Ω @ 2.5 V	
P-Ch -20 V	215 m Ω @ -4.5 V	-0.88 A
	345 m Ω @ -2.5 V	

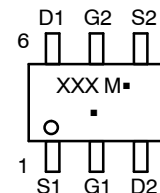
SC-88 (SOT-363)
(6-Leads)



MARKING DIAGRAM & PIN ASSIGNMENT



SC-88 (SOT-363)
CASE 419B
STYLE 26



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NTJD4158C, NVJD4158C

1. Surface mounted on FR4 board using 1 in sq pad size
(Cu area = 1.127 in sq [1 oz] including traces).

NTJD4158C, NVJD4158C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 3)							
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	N	V _{GS} = 0 V	I _D = 250 μA	30		V
		P		I _D = -250 μA	-20		
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J	N			33		mV/°C
		P			-9.0		
Zero Gate Voltage Drain Current	I _{DSS}	N	V _{GS} = 0 V, V _{DS} = 30 V	T _J = 25°C		1.0	μA
		P	V _{GS} = 0 V, V _{DS} = -16 V			1.0	
		N	V _{GS} = 0 V, V _{DS} = 30 V	T _J = 125°C	0.5		
		P	V _{GS} = 0 V, V _{DS} = -16 V		0.5		
Gate-to-Source Leakage Current	I _{GSS}	N	V _{DS} = 0 V, V _{GS} = 10 V			1.0	μA
		P	V _{DS} = 0 V, V _{GS} = -4.5 V			1.0	

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	N	V _{GS} = V _{DS}	I _D = 100 μA	0.8	1.2	1.5	V
		P		I _D = -250 μA	-0.45	-0.61	-1.5	
Negative Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J	N				3.2		mV/°C
		P				-2.7		
Drain-to-Source On Resistance	R _{DS(on)}	N	V _{GS} = 4.5 V, I _D = 10 mA			1.0	1.5	Ω
		P	V _{GS} = -4.5 V, I _D = -0.88 A			0.215	0.260	
		N	V _{GS} = 2.5 V, I _D = 10 mA			1.5	2.5	
		P	V _{GS} = -2.5 V, I _D = -0.71 A			0.345	0.500	
Forward Transconductance	g _{FS}	N	V _{DS} = 3.0 V, I _D = 10 mA			0.08		S
		P	V _{DS} = -10 V, I _D = -0.88 A			3.0		

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	N	f = 1 MHz, V _{GS} = 0 V	V _{DS} = 5.0 V		20	33	pF
		P		V _{DS} = -20 V		155	225	
Output Capacitance	C _{OSS}	N		V _{DS} = 5.0 V		19	32	
		P		V _{DS} = -20 V		25	40	
Reverse Transfer Capacitance	C _{RSS}	N		V _{DS} = 5.0 V		7.25	12	
		P		V _{DS} = -20 V		18	30	
Total Gate Charge	Q _{G(TOT)}	N		V _{GS} = 5.0 V, V _{DS} = 24 V, I _D = 0.1 A		0.9	1.5	nC
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -0.88 A		2.2	3.5	
Threshold Gate Charge	Q _{G(TH)}	N		V _{GS} = 5.0 V, V _{DS} = 24 V, I _D = 0.1 A		0.2		
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -0.88 A		0.2		
Gate-to-Source Charge	Q _{GS}	N		V _{GS} = 5.0 V, V _{DS} = 24 V, I _D = 0.1 A		0.3		
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -0.88 A		0.5		
Gate-to-Drain Charge	Q _{GD}	N		V _{GS} = 5.0 V, V _{DS} = 24 V, I _D = 0.1 A		0.2		
		P		V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -0.88 A		0.65		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(ON)}	N	V _{GS} = 4.5 V, V _{DD} = 5.0 V, I _D = 250 mA, R _G = 50 Ω		15		ns
Rise Time	t _r				66		
Turn-Off Delay Time	t _{d(OFF)}				56		
Fall Time	t _f				78		
Turn-On Delay Time	t _{d(ON)}	P	V _{GS} = -4.5 V, V _{DD} = -10 V, I _D = -0.5 A, R _G = 20 Ω		5.8		
Rise Time	t _r				6.5		
Turn-Off Delay Time	t _{d(OFF)}				13.5		
Fall Time	t _f				3.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	N	V _{GS} = 0 V, T _J = 25°C	I _S = 10 mA		0.65	0.7	V
		P		I _S = -0.48 A		-0.8	-1.2	
		N	V _{GS} = 0 V, T _J = 125°C	I _S = 10 mA		0.45		
		P		I _S = -0.48 A		-0.66		
Reverse Recovery Time	t _{RR}	N	V _{GS} = 0 V, dI _S /dt = 8.0 A/μs	I _S = 10 mA		12.4		ns
		P	V _{GS} = 0 V, dI _S /dt = 100 A/μs	I _S = -0.48 mA		10.6		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL N-CHANNEL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

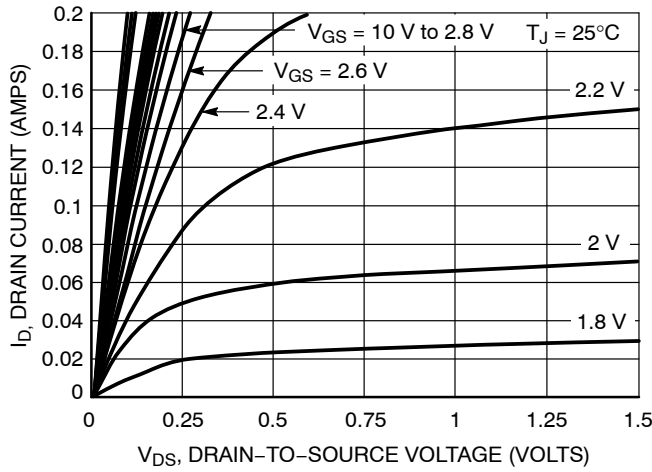


Figure 1. On-Region Characteristics

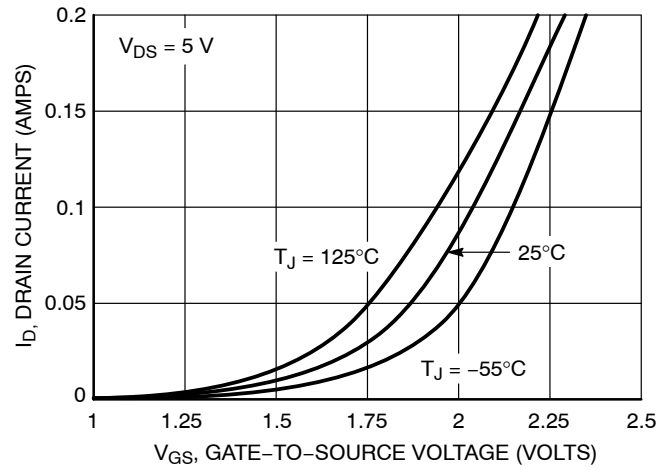


Figure 2. Transfer Characteristics

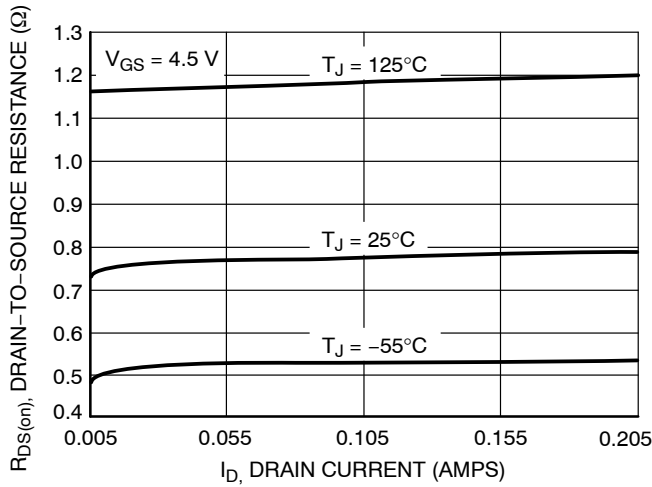


Figure 3. On-Resistance vs. Drain Current and Temperature

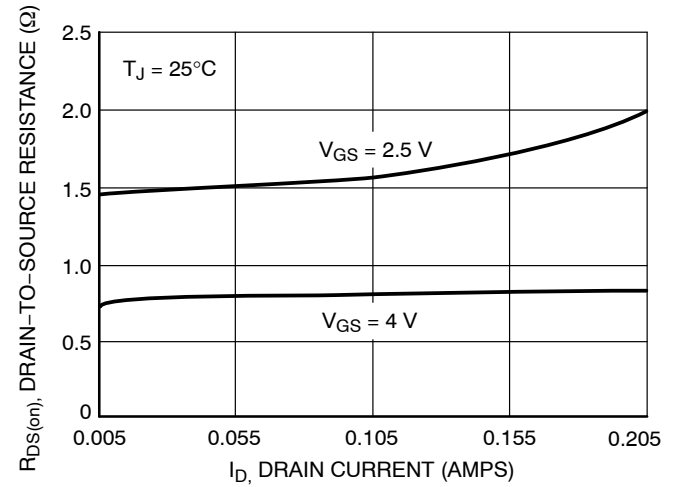


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

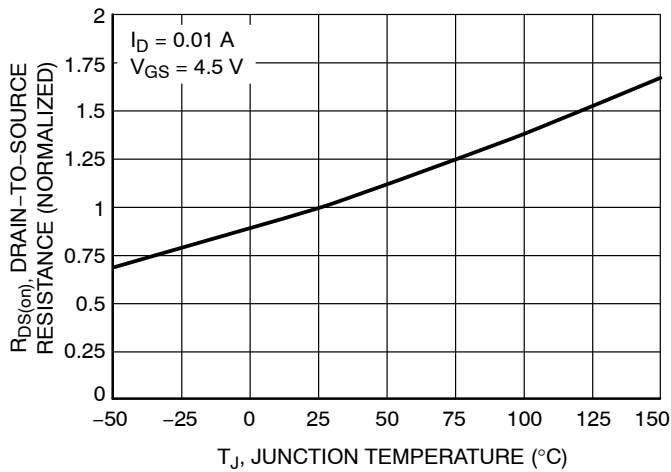


Figure 5. On-Resistance Variation with Temperature

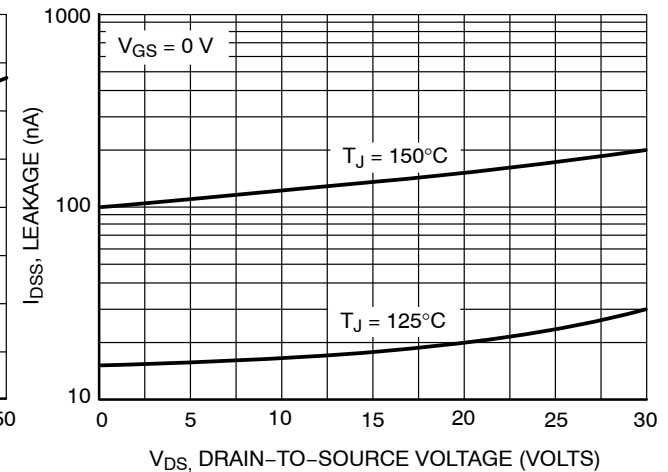


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

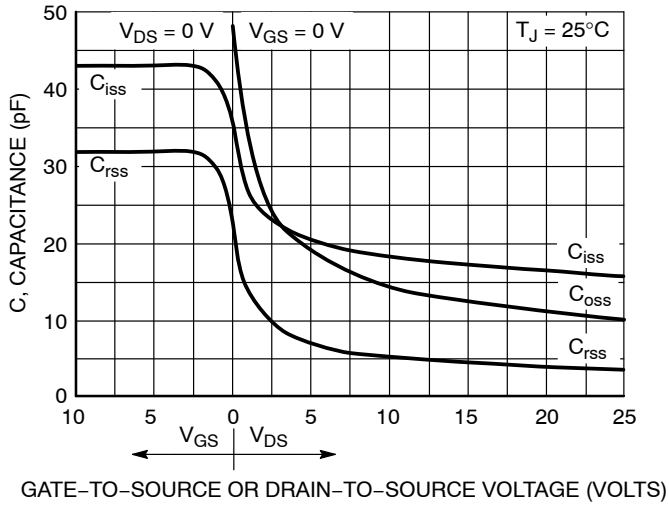


Figure 7. Capacitance Variation

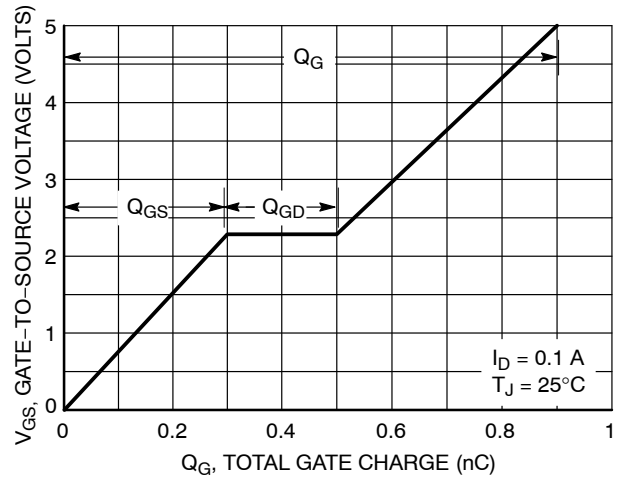


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

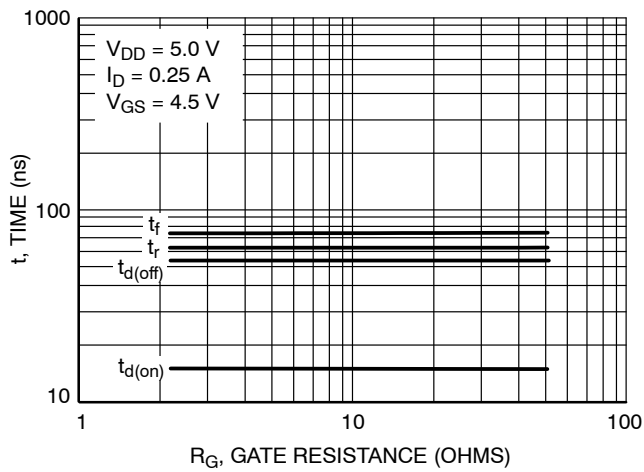


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

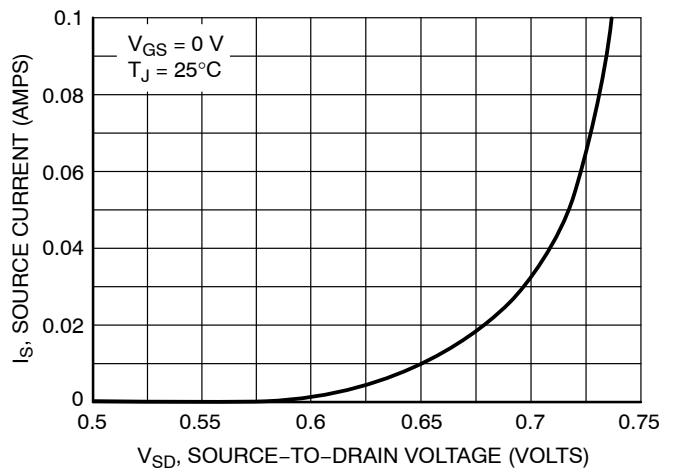


Figure 10. Diode Forward Voltage vs. Current

TYPICAL P-CHANNEL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

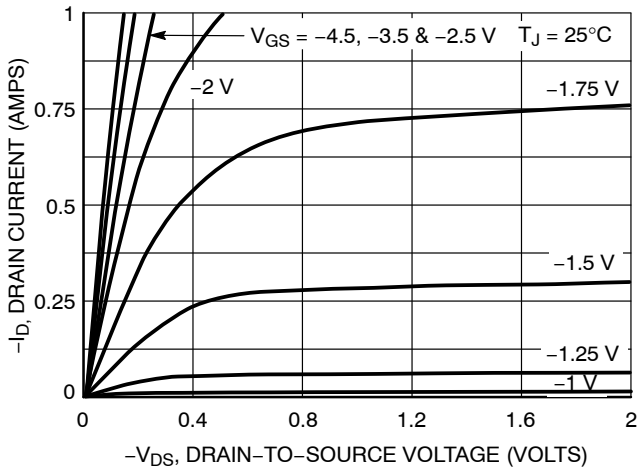


Figure 1. On-Region Characteristics

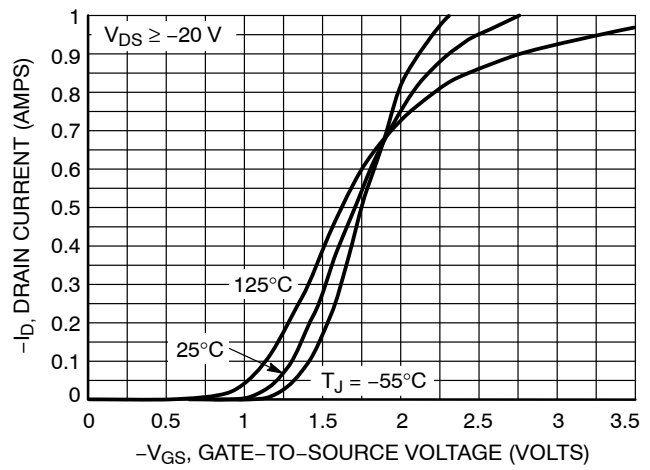


Figure 2. Transfer Characteristics

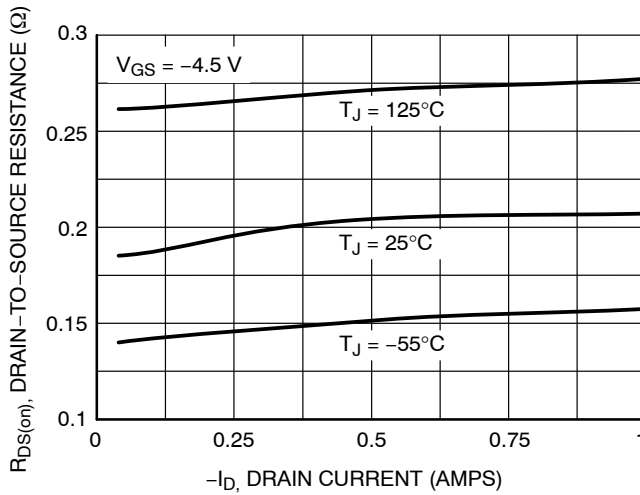


Figure 3. On-Resistance vs. Drain Current and Temperature

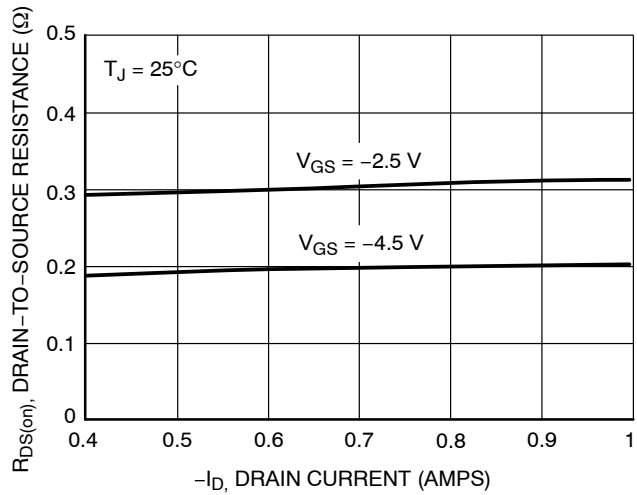


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

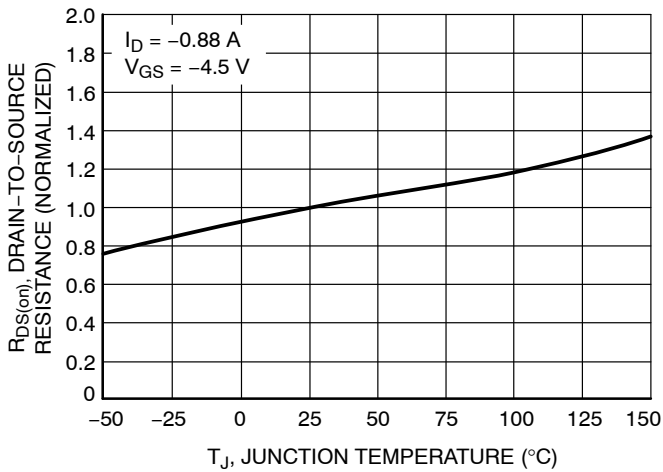


Figure 5. On-Resistance Variation with Temperature

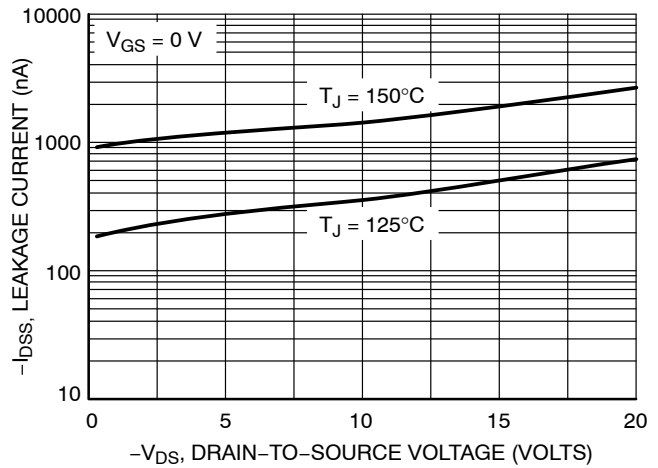


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTJD4158C, NVJD4158C

TYPICAL P-CHANNEL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

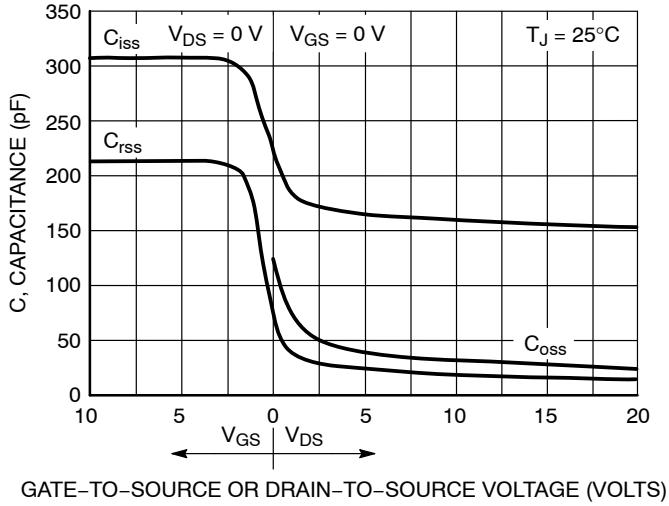


Figure 7. Capacitance Variation

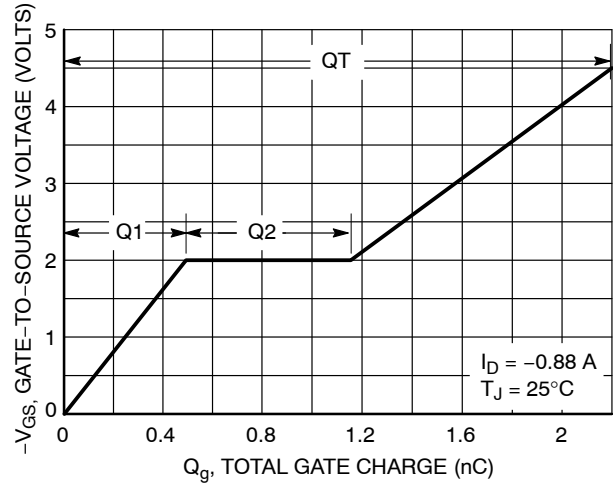


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

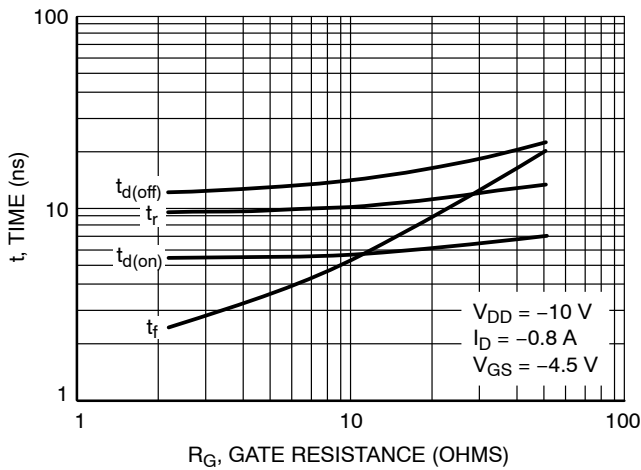


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

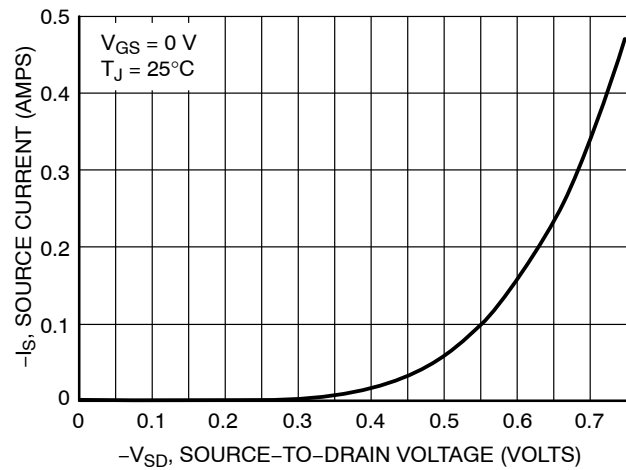


Figure 10. Diode Forward Voltage vs. Current

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTJD4158CT1G	TCD	SC-88 (Pb-Free)	3000 / Tape & Reel
NTJD4158CT2G	TCD		
NVJD4158CT1G*	VCD		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 2:1

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

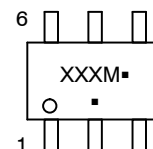


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

GENERIC MARKING DIAGRAM*



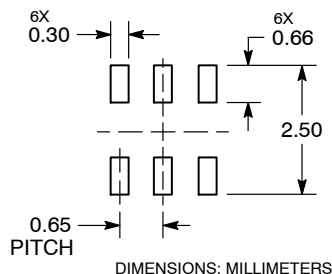
XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	SC-88/SC70-6/SOT-363	PAGE 1 OF 2

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SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 2: CANCELLED	STYLE 3: CANCELLED	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	STYLE 8: CANCELLED	STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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