

Digital FET, Dual N & P Channel

FDG6321C

General Description

These dual N & P-Channel logic level enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially on low voltage replacement for bipolar digital transistors and small signal MOSFETS. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

Features

- N-Ch 0.50 A, 25 V
 - ◆ $R_{DS(ON)} = 0.45 \Omega @ V_{GS} = 4.5 V$
 - ◆ $R_{DS(ON)} = 0.60 \Omega @ V_{GS} = 2.7 V$
- P-Ch -0.41 A, -25 V
 - ◆ $R_{DS(ON)} = 1.1 \Omega @ V_{GS} = -4.5 V$
 - ◆ $R_{DS(ON)} = 1.5 \Omega @ V_{GS} = -2.7 V$
- Very Small Package Outline SC70-6
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits ($V_{GS(th)} < 1.5 V$)
- Gate-Source Zener for ESD Ruggedness (>6 kV Human Body Model)
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

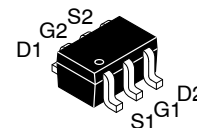
Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	25	-25	V
V_{GSS}	Gate-Source Voltage	8	-8	V
I_D	Drain Current	Continuous	0.5	-0.41
		Pulsed	1.5	-1.2
P_D	Maximum Power Dissipation (Note 1)	0.3		W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		$^\circ C$
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6		kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



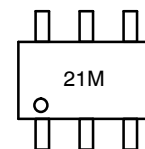
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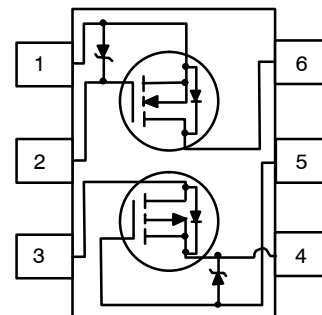
SC-88/SC70-6/SOT-363
CASE 419B-02

MARKING DIAGRAM



21 = Specific Device Code
M = Assembly Operation Month

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	$^{\circ}\text{C}/\text{W}$

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA} = 415^{\circ}\text{C}/\text{W}$ on minimum pad mounting on FR-4 board in still air.

ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	25	-	-	V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-25	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	N-Ch	-	26	-	$\text{mV}/^{\circ}\text{C}$
		$I_D = -250\ \mu\text{A}$, Referenced to 25°C	P-Ch	-	-22	-	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$	N-Ch	-	-	1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^{\circ}\text{C}$		-	-	10	
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	P-Ch	-	-	-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^{\circ}\text{C}$		-	-	-10	
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$	N-Ch	-	-	100	nA
		$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$	P-Ch	-	-	-100	

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	0.65	0.8	1.5	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-0.65	-0.82	-1.5	
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	N-Ch	-	-2.6	-	$\text{mV}/^{\circ}\text{C}$
		$I_D = -250\ \mu\text{A}$, Referenced to 25°C	P-Ch	-	2.1	-	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$	N-Ch	-	0.34	0.45	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}, T_J = 125^{\circ}\text{C}$		-	0.55	0.72	
		$V_{GS} = 2.7\text{ V}, I_D = 0.2\text{ A}$		-	0.44	0.6	
		$V_{GS} = -4.5\text{ V}, I_D = -0.41\text{ A}$	P-Ch	-	0.85	1.1	
		$V_{GS} = -4.5\text{ V}, I_D = -0.41\text{ A}, T_J = 125^{\circ}\text{C}$		-	1.2	1.8	
		$V_{GS} = -2.7\text{ V}, I_D = -0.05\text{ A}$		-	1.15	1.5	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	0.5	-	-	A
		$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-0.41	-	-	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 0.5\text{ A}$	N-Ch	-	1.45	-	S
		$V_{DS} = -5\text{ V}, I_D = -0.41\text{ A}$	P-Ch	-	0.9	-	

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$ P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	N-Ch	-	50	-	pF
			P-Ch	-	62	-	
C_{oss}	Output Capacitance		N-Ch	-	28	-	
			P-Ch	-	34	-	
C_{rss}	Reverse Transfer Capacitance		N-Ch	-	9	-	
			P-Ch	-	10	-	

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 2)

$t_{D(on)}$	Turn-On Delay Time	N-Channel $V_{DD} = 5\text{ V}$, $I_D = 0.5\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 50\ \Omega$	N-Ch	-	3	6	ns
			P-Ch	-	7	15	
t_r	Turn-On Rise Time	P-Channel $V_{DD} = -5\text{ V}$, $I_D = -0.5\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 50\ \Omega$	N-Ch	-	8.5	18	ns
			P-Ch	-	8	16	
$t_{D(off)}$	Turn-Off Delay Time		N-Ch	-	17	30	ns
			P-Ch	-	55	80	
t_f	Turn-Off Fall Time		N-Ch	-	13	25	ns
			P-Ch	-	35	60	
Q_g	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}$, $I_D = 0.5\text{ A}$, $V_{GS} = 4.5\text{ V}$	N-Ch	-	1.64	2.3	nC
			P-Ch	-	1.1	1.5	
Q_{gs}	Gate-Source Charge	P-Channel $V_{DS} = -5\text{ V}$, $I_D = -0.41\text{ A}$, $V_{GS} = -4.5\text{ V}$	N-Ch	-	0.38	-	nC
			P-Ch	-	0.31	-	
Q_{gd}	Gate-Drain Charge		N-Ch	-	0.45	-	nC
			P-Ch	-	0.29	-	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	-	-	0.25	A
			P-Ch	-	-	-0.25	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 0.5\text{ A}$ (Note 2)	N-Ch	-	0.8	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = -0.5\text{ A}$ (Note 2)	P-Ch	-	-0.8	-1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL

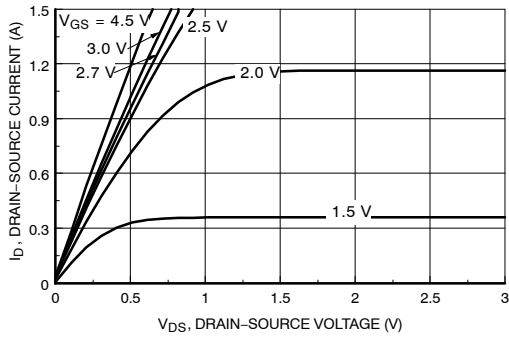


Figure 1. On-Region Characteristics

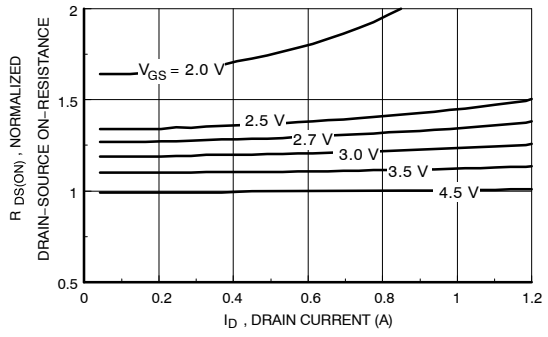


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

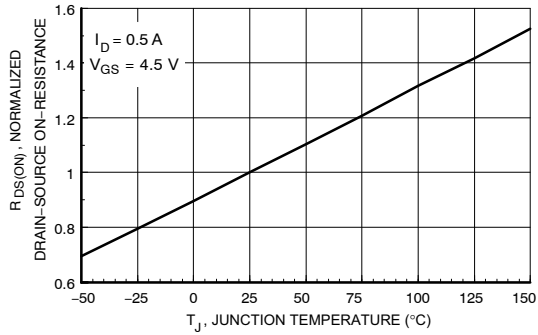


Figure 3. On-Resistance Variation with Temperature

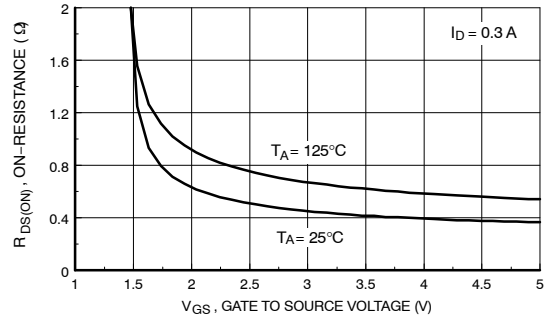


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

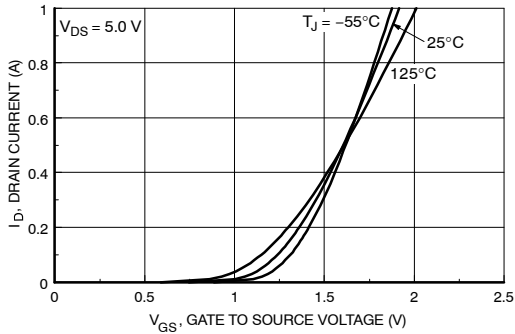


Figure 5. Transfer Characteristics

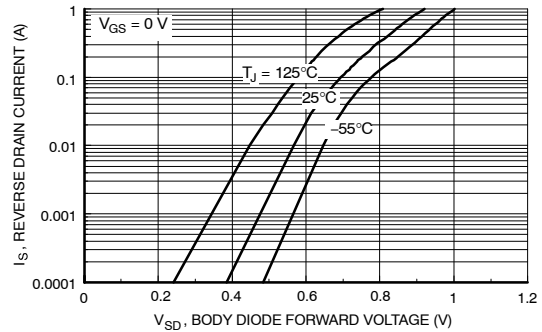


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: N-CHANNEL (continued)

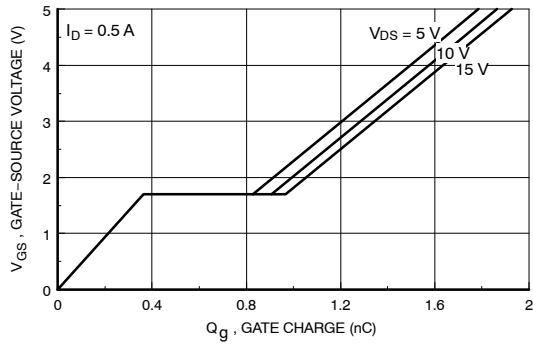


Figure 7. Gate Charge Characteristics

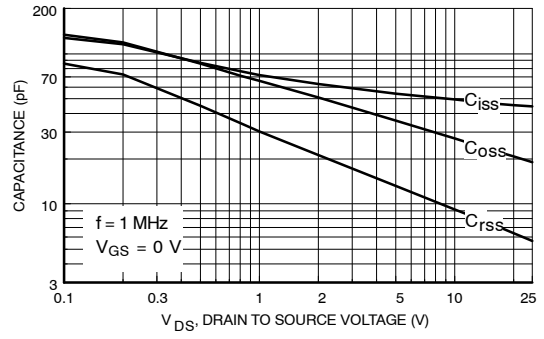


Figure 8. Capacitance Characteristics

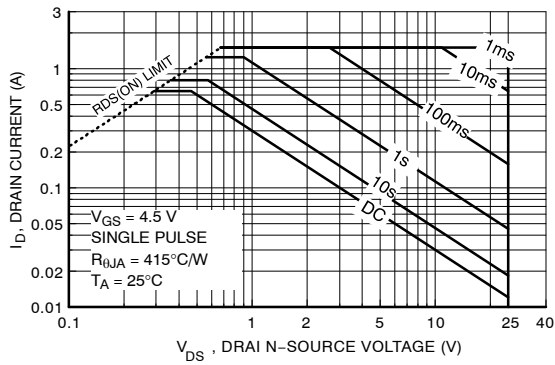


Figure 9. Maximum Safe Operating Area

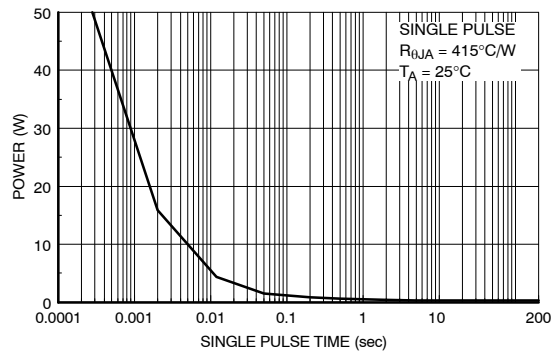


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL

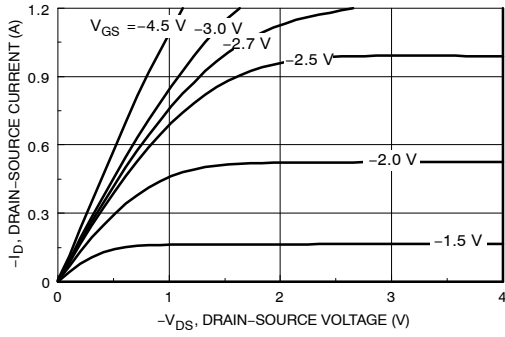


Figure 11. On-Region Characteristics

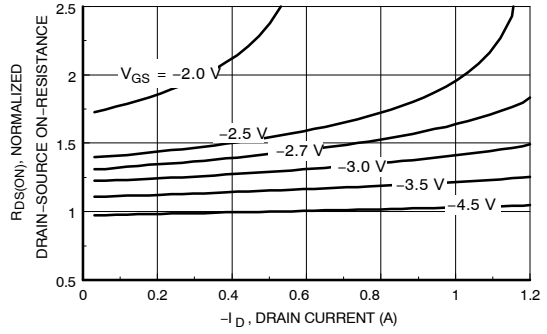


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

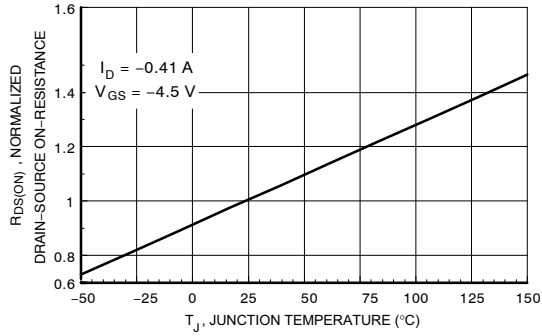


Figure 13. On-Resistance Variation with Temperature

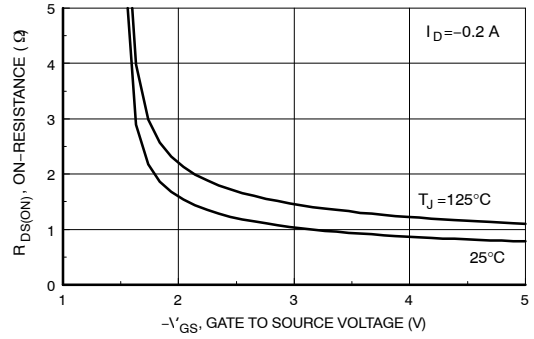


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

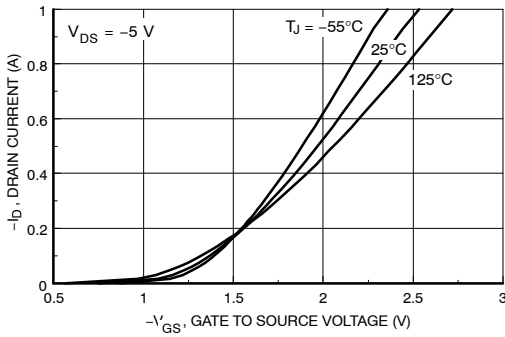


Figure 15. Transfer Characteristics

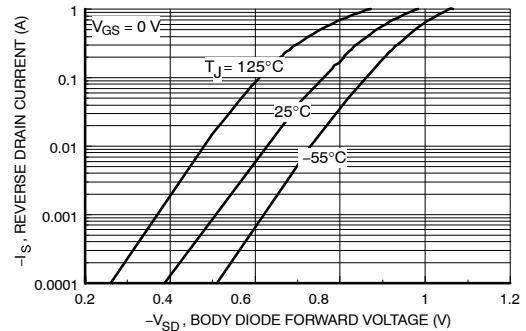


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS: P-CHANNEL (continued)

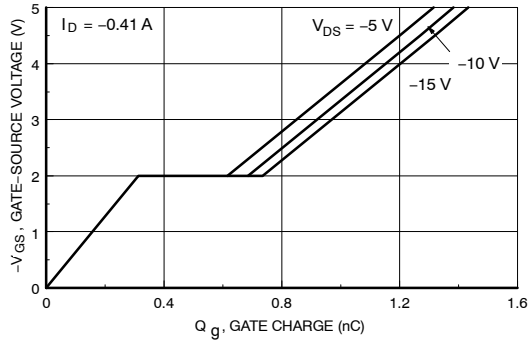


Figure 17. Gate Charge Characteristics

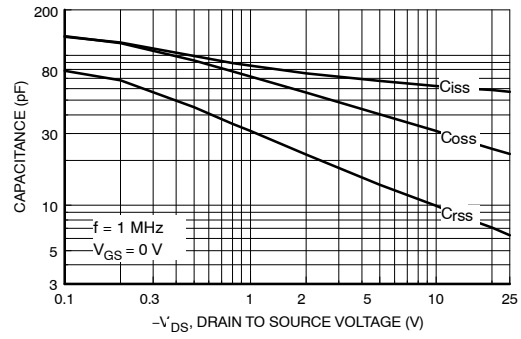


Figure 18. Capacitance Characteristics

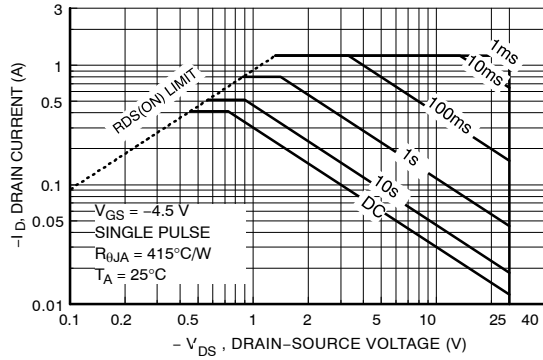


Figure 19. Maximum Safe Operating Area

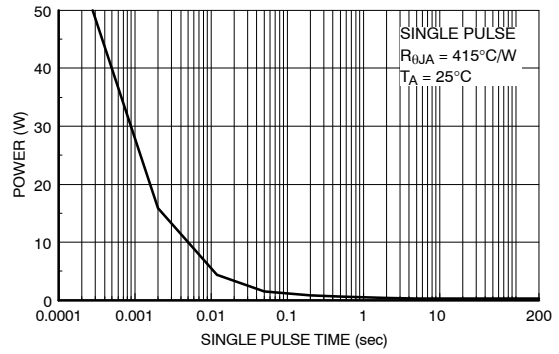
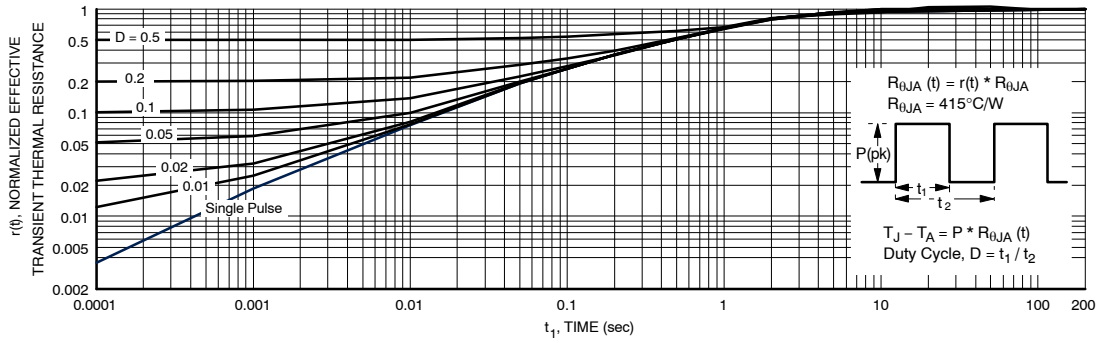


Figure 20. Single Pulse Maximum Power Dissipation

FDG6321C

TYPICAL PERFORMANCE CHARACTERISTICS: N & P-CHANNEL



Thermal characterization performed using the conditions described in Note 1.
 Transient thermal response will change depending on the circuit board design.

Figure 21. Transient Thermal Response Curve

ORDERING INFORMATION

Device Order Number	Device Marking	Package Type	Shipping†
FDG6321C	21	SC-88/SC70-6/SOT-363 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

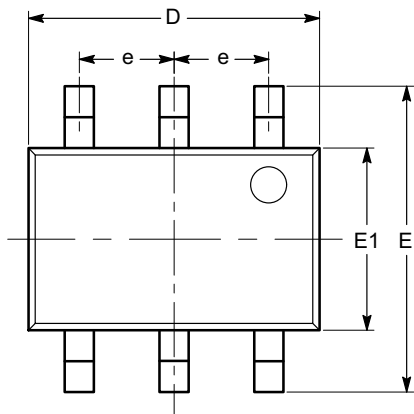
PACKAGE DIMENSIONS

ON Semiconductor®



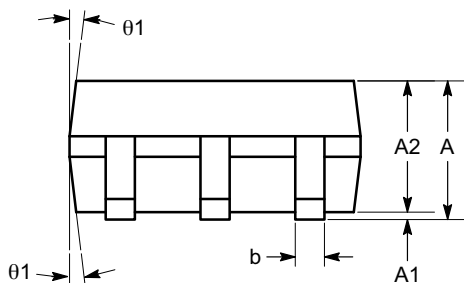
SC-88 (SC-70 6 Lead), 1.25x2
CASE 419AD-01
ISSUE A

DATE 07 JUL 2010

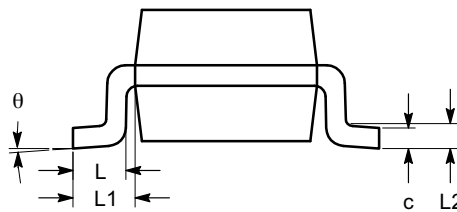


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
θ	0°		8°
θ_1	4°		10°



SIDE VIEW



END VIEW

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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DESCRIPTION:	SC-88 (SC-70 6 LEAD), 1.25X2	PAGE 1 OF 1

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