

NP16N06QLK

60 V – 16 A – Dual N-channel Power MOS FET Application: Automotive

R07DS1290EJ0200 Rev. 2.00 May 24, 2018

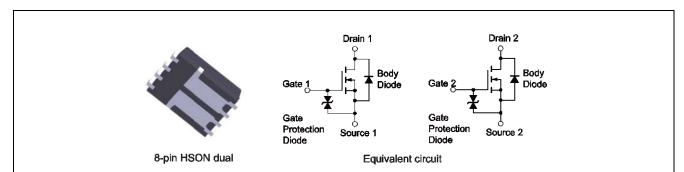
Description

NP16N06QLK is a dual N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance
 - $R_{DS(on)1} = 39$ mΩ MAX. ($V_{GS} = 10$ V, $I_D = 8$ A)
 - --- $R_{DS(on)2} = 60$ mΩ MAX. ($V_{GS} = 4.5$ V, $I_D = 4$ A)
- Low C_{iss} : $C_{iss} = 500 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON dual

Outline



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP16N06QLK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON dual
NP16N06QLK-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	60	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C) *4	I _{D(DC)}	±16	А
Drain Current (pulse) *1, 4, 5	I _{D(pulse)}	±32	А
Total Power Dissipation (T _C = 25°C) *4	P _{T1}	25	W
Total Power Dissipation (T _A = 25°C) *2, 4	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3, 5	I _{AR}	7	А
Repetitive Avalanche Energy *3, 5	E _{AR}	5	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)^*5}$ 5.95 °C/W Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)^*5}$ 150 °C/W

Notes: *1. T_C = 25°C, PW \leq 10 μ s, Duty Cycle \leq 1%

^{*2.} Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mmt with 4% copper area (35 μ m)

^{*3.} Rg = 25 Ω , Vgs = 20 V ightarrow 0 V

^{*4.} One channel operation

^{*5.} Not subject of production test. Verified by design/characterization.

Electrical Characteristics (T_A = 25°C)

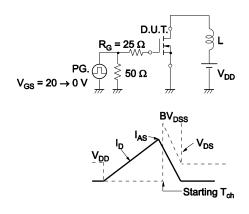
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μА	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±10	μА	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	2.1	2.5	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
Forward Transfer Admittance *1	y _{fs}	5	13		S	$V_{DS} = 5 \text{ V}, I_{D} = 8 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		30	39	mΩ	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$
Resistance *1	R _{DS(on)2}		38	60	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$
Input Capacitance *2	C _{iss}		500	750	pF	$V_{DS} = 25 V$,
Output Capacitance *2	Coss		50	75	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance *2	C _{rss}		30	54	pF	f = 1 MHz
Turn-on Delay Time *2	t _{d(on)}		15	30	ns	$V_{DD} = 30 \text{ V}, I_D = 8 \text{ A},$
Rise Time *2	t _r		5	13	ns	$V_{GS} = 10 V$,
Turn-off Delay Time *2	$t_{d(off)}$		30	60	ns	$R_G = 0 \Omega$
Fall Time *2	t _f		3	8	ns	
Total Gate Charge *2	Q_{G}		11	17	nC	$V_{DD} = 48 \text{ V},$
Gate to Source Charge	Q _{GS}		3		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		3		nC	I _D = 16 A
Body Diode Forward Voltage *1	V _{F(S-D)}		0.9	1.5	V	I _F = 16 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		20		ns	$I_F = 16 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Qrr		16		nC	di/dt = 100 A/μs

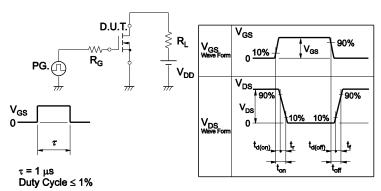
Note: *1. Pulsed test

Note: *2. Not subject of production test. Verified by design/characterization.

TEST CIRCUIT 1 AVALANCHE CAPABILITY

TEST CIRCUIT 2 SWITCHING TIME



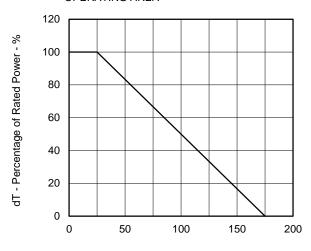


TEST CIRCUIT 3 GATE CHARGE

$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \underbrace{mA}_{W} \\ \hline PG. \\ \hline \end{array} \begin{array}{c} S \\ S \\ DU \\ \hline \end{array} \begin{array}{c} V_{DD} \\ \hline \end{array}$$

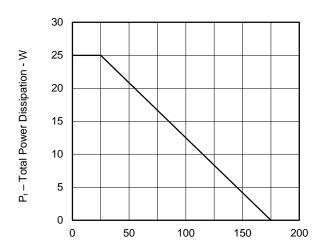
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



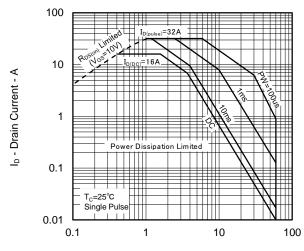
T_C - Case Temperature - °C

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



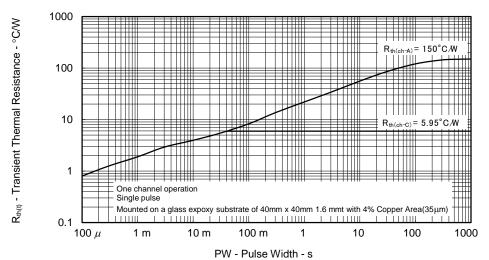
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 V_{DS} - Drain to Source Voltage $-\,V$

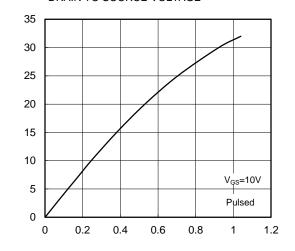
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



RENESAS

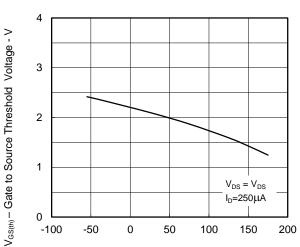
I_D - Drain Current - A

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



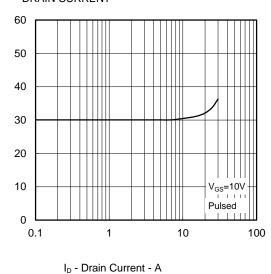
V_{DS} - Drain to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

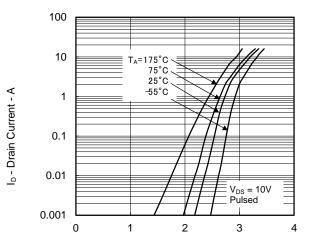


 T_{ch} - Channel Temperature - $^{\circ}C$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

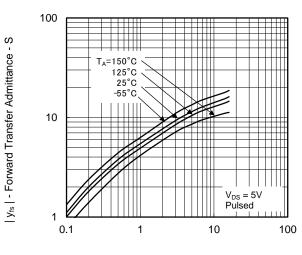


FORWARD TRANSFER CHARACTERISTICS



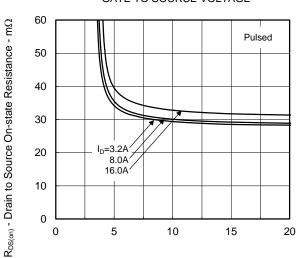
V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



ID - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

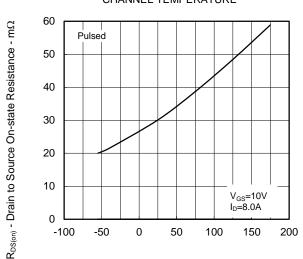


 V_{GS} - Gate to Source Voltage - V

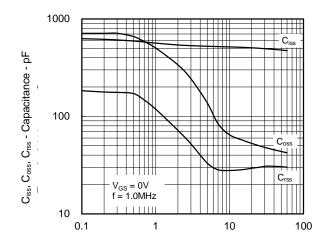
 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

td(on),tr,td(off),tr - Switching Time - ns

IF - Diode Forward Current - A

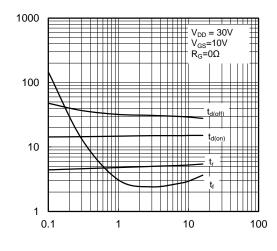


T_{ch} - Channel Temperature - °C



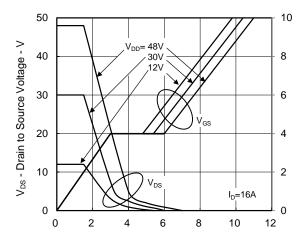
V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



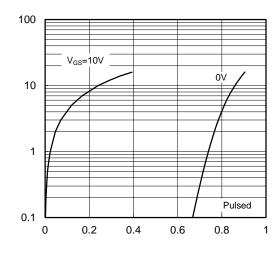
I_D - Drain Current - A

DYNAMIC INPUT CHARACTERISTICS



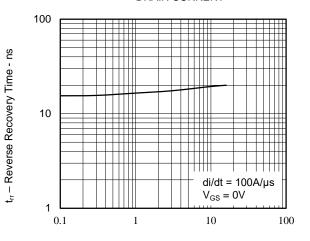
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{F(S\text{-}D)}$ - Source to Drain Voltage - V

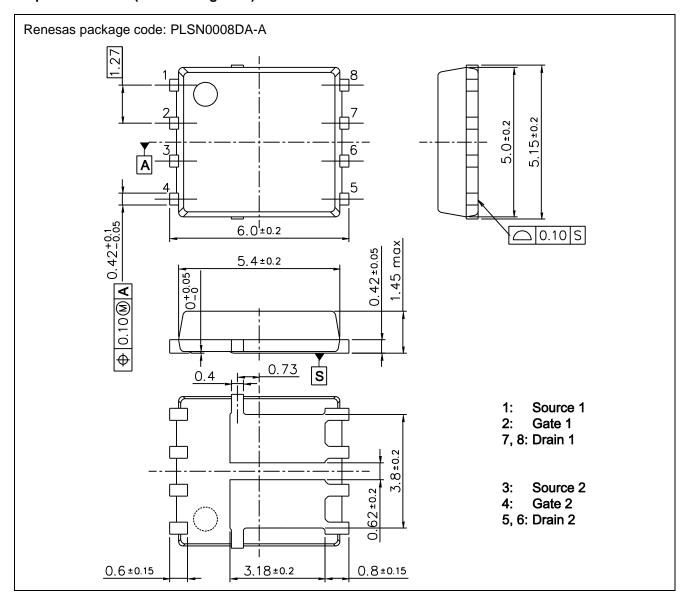
REVERSE RECOVERY TIME vs. DRAIN CURRENT



I_F - Drain Current - A

Package Drawings (Unit: mm)

8-pin HSON Dual (Mass: 0.12 g TYP.)



Revision History

NP16N06QLK Data Sheet

		Description			
Rev.	Date	Page	Summary		
1.00	Aug 18, 2015	_	First Edition Issued		
1.01	Oct 27, 2015	4	Modification of the characters on the Rth(t) graph		
		5	Modification of the characters on the VGS(th)-Tch graph		
2.00	May 24, 2018	2	Note 5 was added		
		3	Note 2 was added		

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