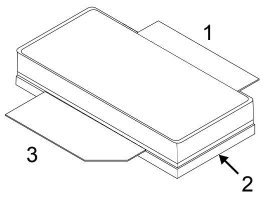
RF2L36075CF2

Datasheet

75 W, 28 V, 3.1 to 3.6 GHz RF power LDMOS transistor



B2

Pin connection	
Pin	**Connection**
1	Gate
2	Source (bottom side)
3	Drain

Product status link
RF2L36075CF2

Product summary	
Order code	RF2L36075CF2
Marking	2L36075
Package	B2
Packing	Tape and reel 13"
Base / Bulk qty	120/120

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF2L36075CF2	3500 MHz	28 V	75 W	12.5 dB	45%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internal input matching for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- Telecom
- S-Band radar

Description

The RF2L36075CF2 is a 75 W internally matched LDMOS transistor designed for multicarrier WCDMA/PCS/DCS/LTE base stations and S-Band radar applications in the frequency range from 3.1 to 3.6 GHz. It can be used in class AB, B or C for all typical cellular base station modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC} (1)	Thermal resistance, junction-to-case	0.35	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	60			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 28 V			1	µA
		V_{GS} = 0 V, V_{DS} = 50 V				
I_{GSS}	Gate-body leakage current	V_{GS} = -6/10 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 1 V, I_{DS} = 600 µA	1.75		2.50	V
		V_{DS} = 28 V, I_{DS} = 600 µA				
$V_{GS(Q)}$	Gata quiescent voltage	V_{DS} = 1 V, I_{DS} = 600 mA		3		V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 800 mA	30		170	mV
		V_{GS} = 10 V, I_{DS} = 3.5 A	150		750	
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_{DS} = 800 mA			1	Ω
		V_{GS} = 10 V, I_{DS} = 3.5 A				

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		3100		3500	MHz
P_{OUT}	Output power	f = 3500 MHz, 1 dB compression point		75		W
G_{PS}	Power gain			12.5		dB
η_D	Drain efficiency			45		%
VSWR	Load mismatch	at 10 W WCDMA Output Power			10:1	

Note: *V_{DD} = 28 V, I_{DQ} = 600 mA, pulsed CW, PW = 10 µs, duty cycle = 10%.*

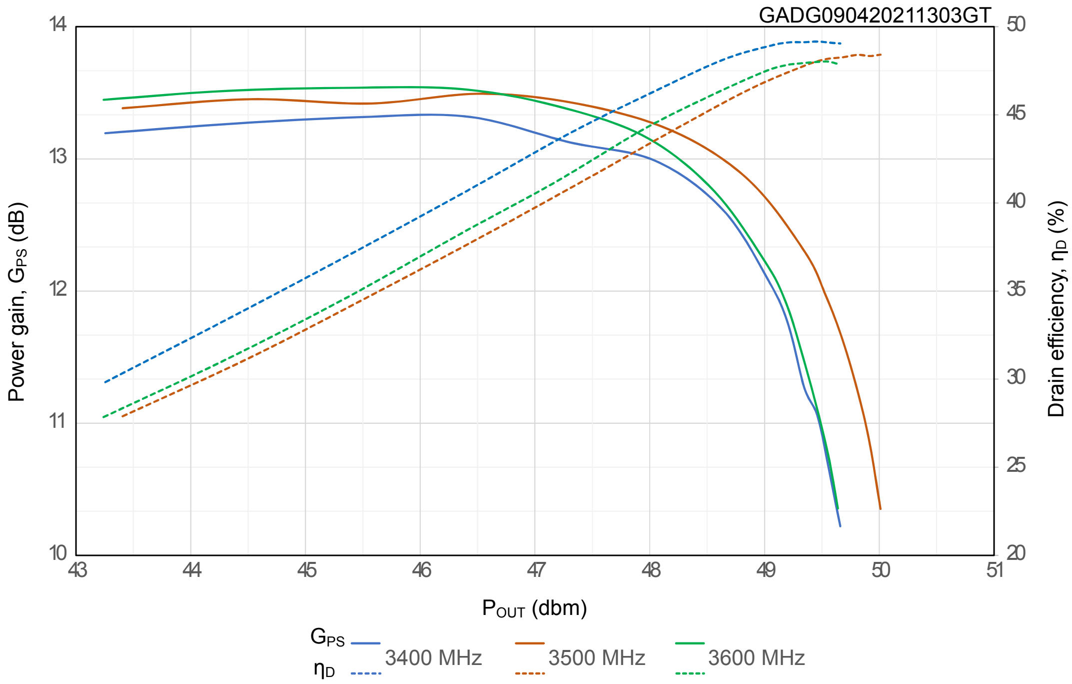
3 Typical performance

3.1 Pulsed CW performance

Table 6. **Typical performance vs frequency**

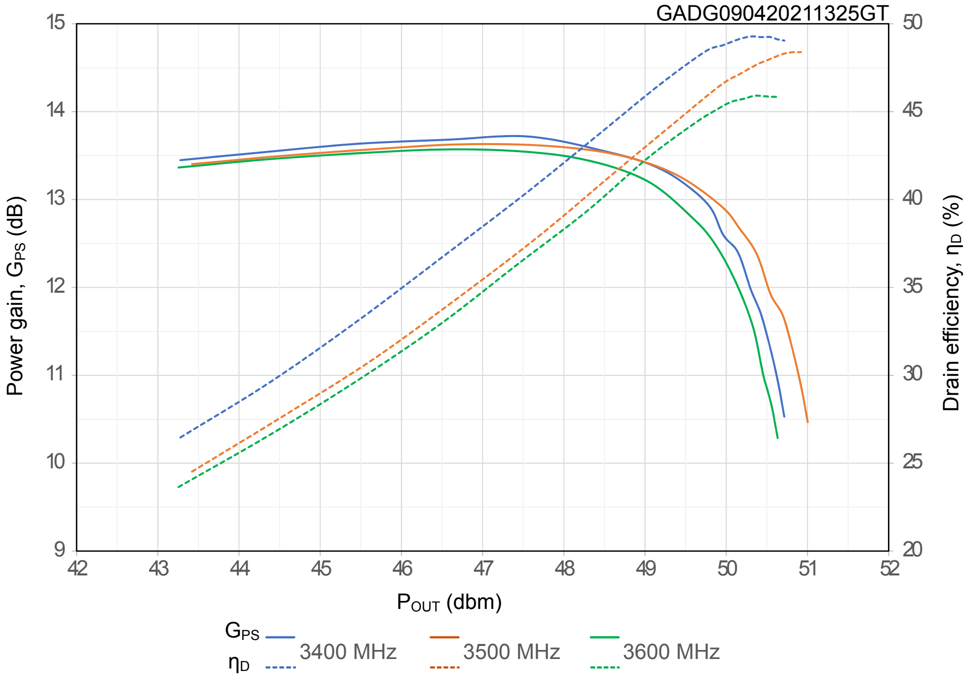
f (MHz)	G_{PS}@P_{1dB}(dB)	P_{1dB} (dBm)	η_D @P_{1dB} (%)	P_{3dB} (dBm)	η_D @P_{3dB} (%)
3400	12.3	48.3	46.3	50	49
3500	12.5	48.8	44.7	49.6	47
3600	12.5	48.2	42.8	49.3	48

Figure 1. **Power gain and drain efficiency vs output power over 3400-3600 MHz band (V_{DD} = 28 V)**



Note: *I_{DQ} = 600 mA, pulse width = 10 µs, duty cycle = 10%.*

Figure 2. **Power gain and drain efficiency vs output power over 3400-3600 MHz band (V_{DD} = 32 V)**



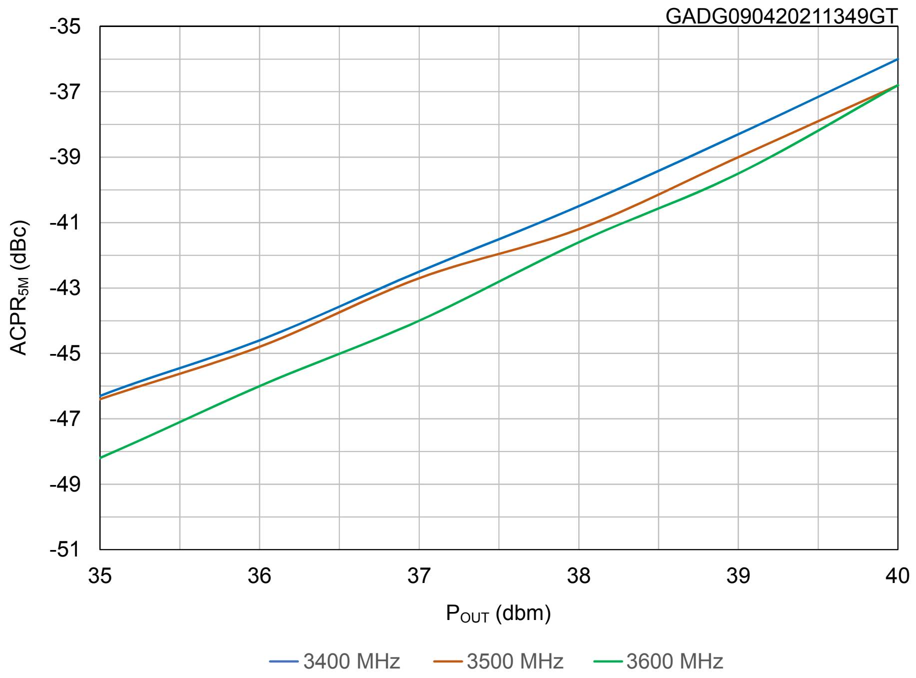
Note: *I_{DQ} = 600 mA, pulse width = 10 µs, duty cycle = 10%.*

3.2 WCDMA performance

Table 7. Typical Single-Carrier W-CDMA performance

$P_{OUT, avg}$(dBm)	$ACPR_{5M}$ (dBc)		
	3400 MHz	3500 MHz	3600 MHz
33	-50.4	-50.2	-52.0
34	-48.4	-48.1	-50.2
35	-46.3	-46.4	-48.2
36	-44.6	-44.8	-46.0
37	-42.5	-42.7	-44.0
38	-40.5	-41.2	-41.6
39	-38.3	-39.0	-39.5
40	-36.0	-36.8	-36.8

Figure 3. $ACPR_{5M}$ vs output power over 3400-3600 MHz band



Note: *V_{DD} = 28 V, I_{DQ} = 600 mA, WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; channel bandwidth = 3.84 MHz, PAR = 10.5 dB at 0.01% probability on CCDF.*

4 Test circuits

Figure 4. Test circuit layout (over 3400 – 3600 MHz band)

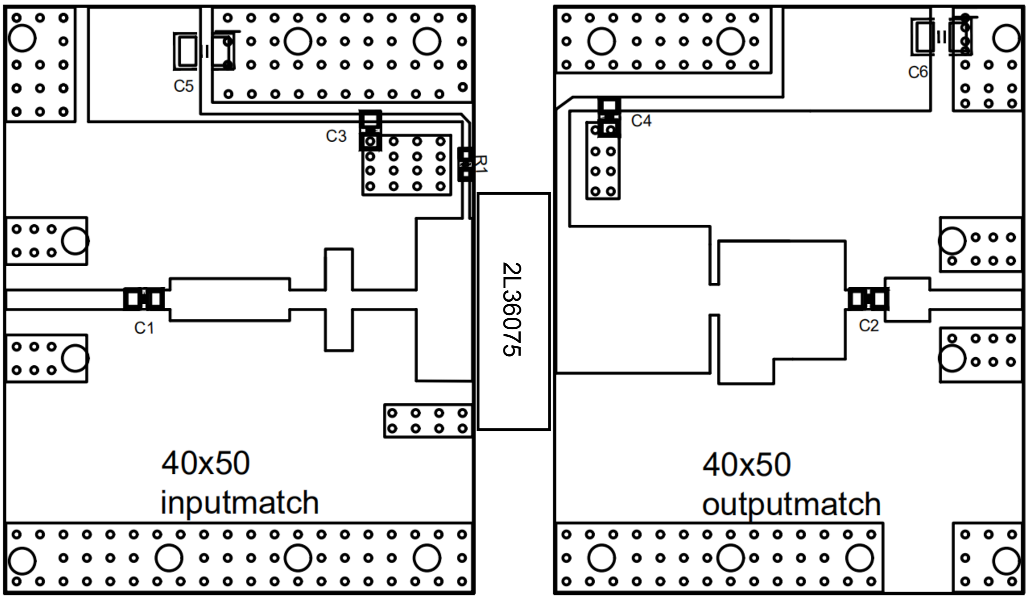


Figure 5. Test circuit photo (over 3400 - 3600 MHz band)

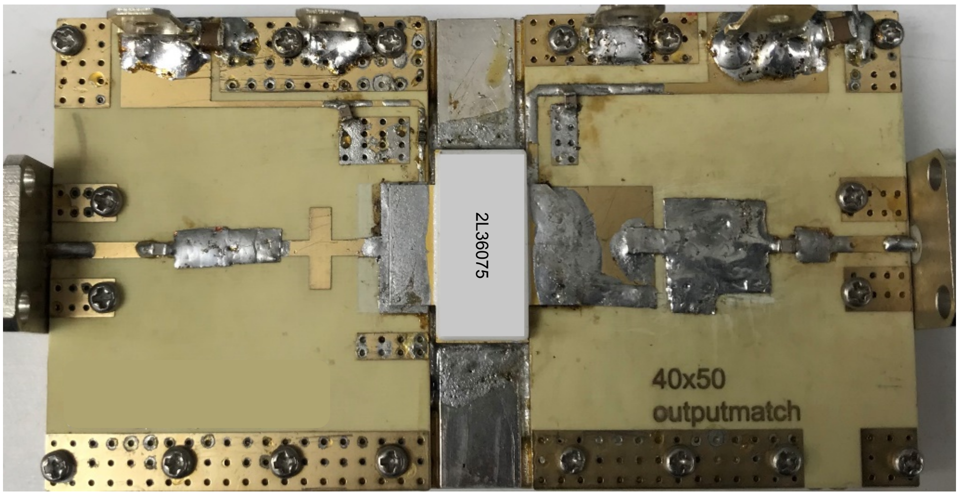


Table 8. Components list

Component	Value	Size	Reference
C1, C2, C3, C4	6.8 pF	0805	ATC600F
C5, C6	10 µF	1210	ceramic multilayer capacitor
R1	10 Ω	0603	chip resistor
PCB	0.508 mm (0.020") thick, εr = 3.48, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 B2 package information

Figure 6. B2 package outline

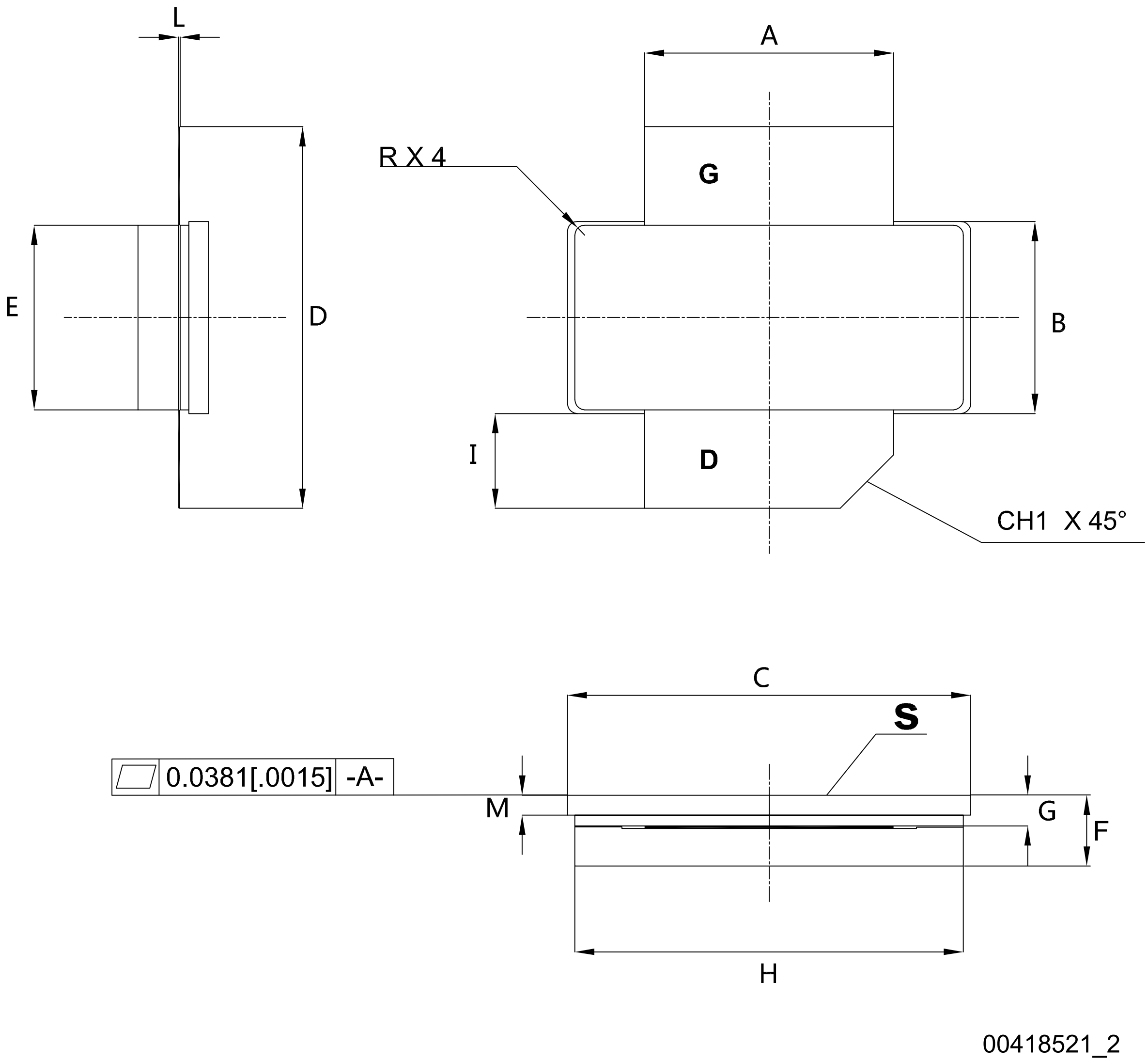
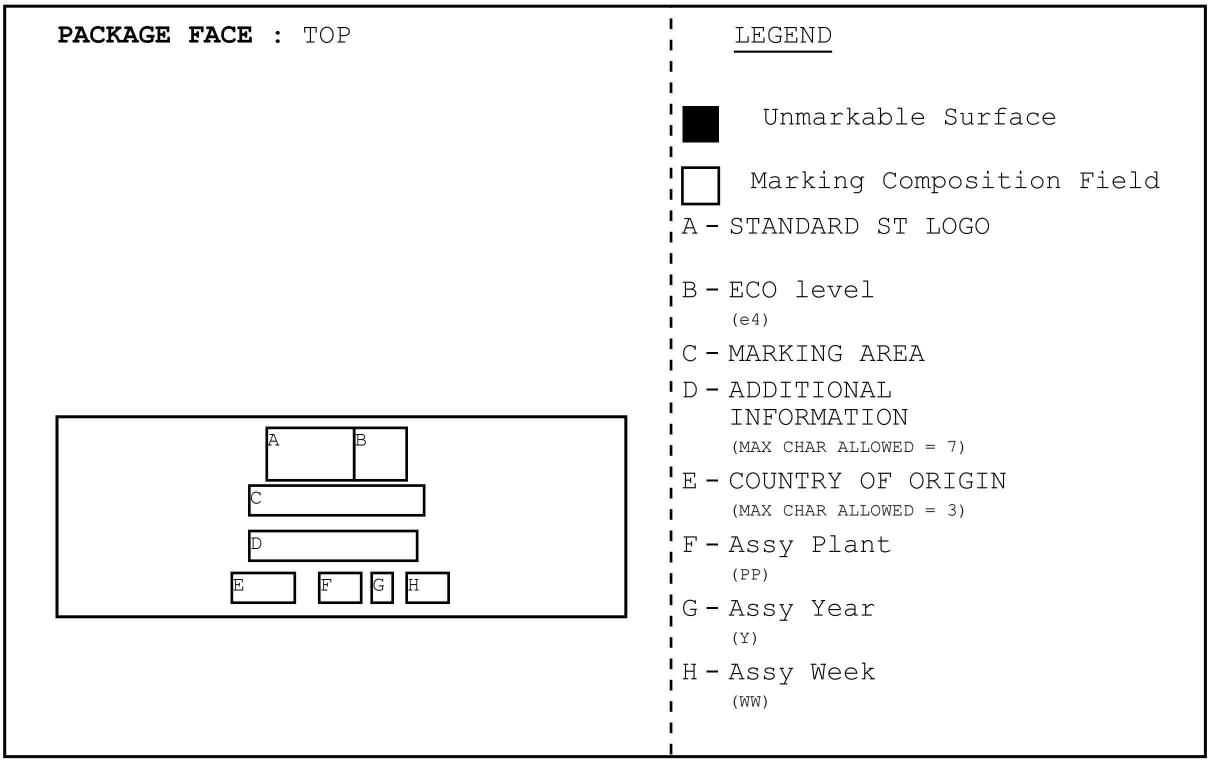


Table 9. B2 mechanical data

Symbol	Millimetres		
	Min	Typ	Max
A	12.57	12.7	12.83
B	9.65	9.78	9.91
C	20.44	20.57	20.70
D	19.31	19.44	19.57
E	9.27	9.40	9.53
F	3.23	3.61	3.99
G	1.44	1.57	1.70
H	19.68	19.81	19.94
I	4.70	4.83	4.96
L	0.07	0.10	0.15
M	0.89	1.02	1.15
CH1		2.72	
R		0.51	

5.2 Marking information

Figure 7. Marking composition



GADG040220211644GT

Revision history

Table 10. Document revision history

Date	Version	Changes
09-Jun-2020	1	Initial release
14-Apr-2021	2	Updated Features and Device summary in cover page. Updated Section 1 Electrical ratings. Updated Section 2 Electrical characteristics. Updated Figure 1. Power gain and drain efficiency vs output power over 3400-3600 MHz band (V_{DD} = 28 V). Added Figure 2. Power gain and drain efficiency vs output power over 3400-3600 MHz band (V_{DD} = 32 V). Updated Figure 3. $ACPR_{5M}$ vs output power over 3400-3600 MHz band. Updated Section 4 Test circuits. Added Section 5.2 Marking information. Minor text changes.

Contents