

BLF6G10LS-135R

Power LDMOS transistor

Rev. 01 — 17 November 2008

Product data sheet

1. Product profile

1.1 General description

135 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$ in a class-AB production test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η_D (%)	ACPR (dBc)
2-carrier W-CDMA	869 to 894	28	26.5	21.0	28.0	-39 ^[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

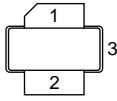
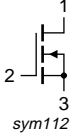
- Typical 2-carrier W-CDMA performance at frequencies of 869 MHz and 894 MHz, a supply voltage of 28 V and an I_{DQ} of 950 mA:
 - ◆ Average output power = 26.5 W
 - ◆ Power gain = 21.0 dB
 - ◆ Efficiency = 28.0 %
 - ◆ ACPR = -39 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE, W-CDMA and CDMA base stations and multi carrier applications in the 800 MHz to 1000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		 sym112
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G10LS-135R	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	32	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 25\text{ W}$	0.56	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.8\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 180\text{ mA}$	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 950\text{ mA}$	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	3	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	24	32	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 9\text{ A}$	7	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 6.3\text{ A}$	-	0.1	-	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}; f = 1\text{ MHz}$	-	2.0	-	pF

7. Application information

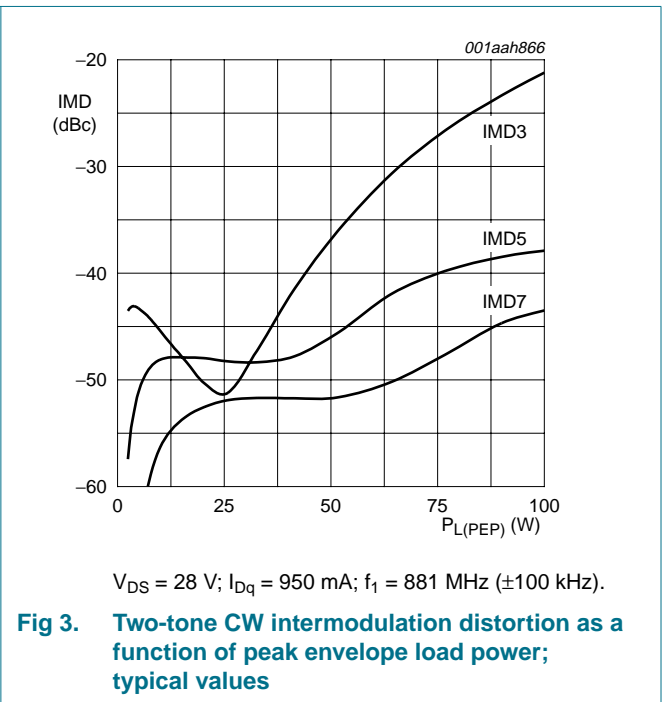
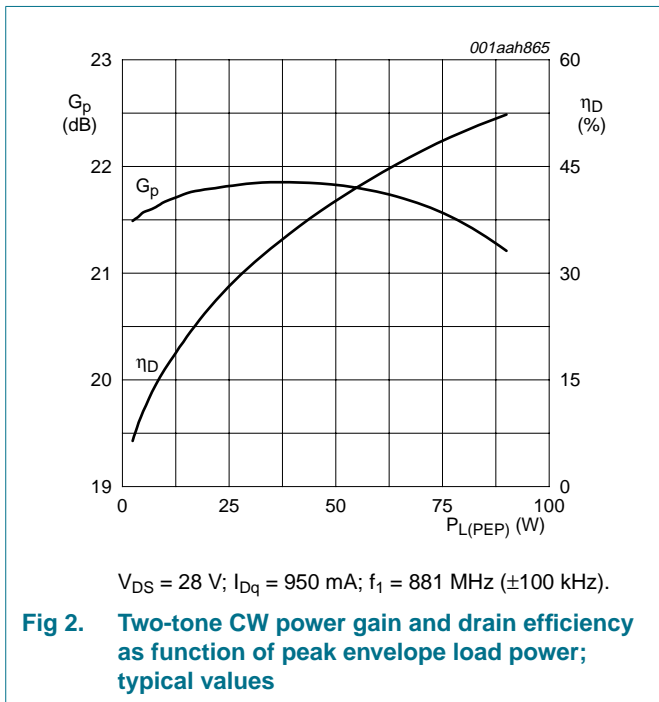
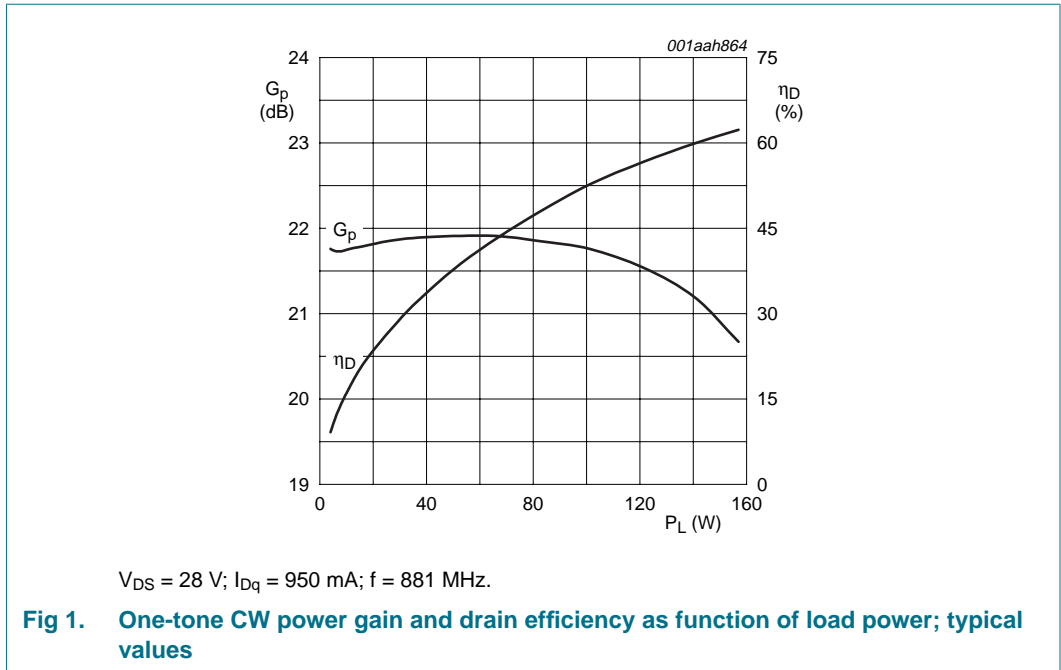
Table 7. Application information

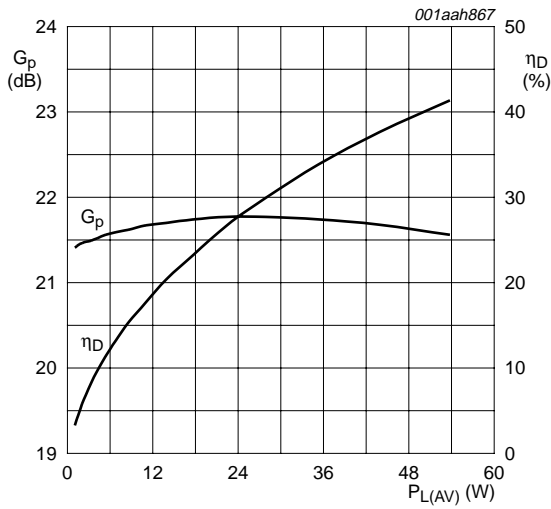
Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 PDPCH; $f_1 = 871.5\text{ MHz}; f_2 = 876.5\text{ MHz}; f_3 = 886.5\text{ MHz}; f_4 = 891.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 950\text{ mA}; T_{case} = 25\text{ }^\circ\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	26.5	-	W
G_p	power gain	$P_{L(AV)} = 26.5\text{ W}$	20.0	21.0	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 26.5\text{ W}$	-	-11.0	-8.0	dB
η_D	drain efficiency	$P_{L(AV)} = 26.5\text{ W}$	26.0	28.0	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 26.5\text{ W}$	-	-39	-36.5	dBc

7.1 Ruggedness in class-AB operation

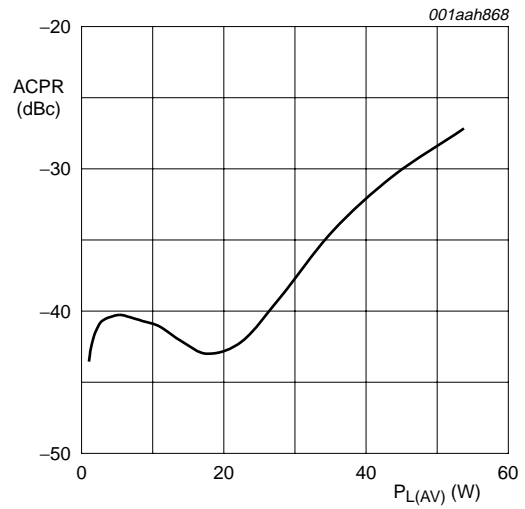
The BLF6G10LS-135R is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}; I_{Dq} = 950\text{ mA}; P_L = 135\text{ W}; f = 894\text{ MHz}$.





$V_{DS} = 28\text{ V}$; $I_{DQ} = 950\text{ mA}$; $f_1 = 881\text{ MHz}$; $f_2 = 886\text{ MHz}$; carrier spacing 5 MHz.

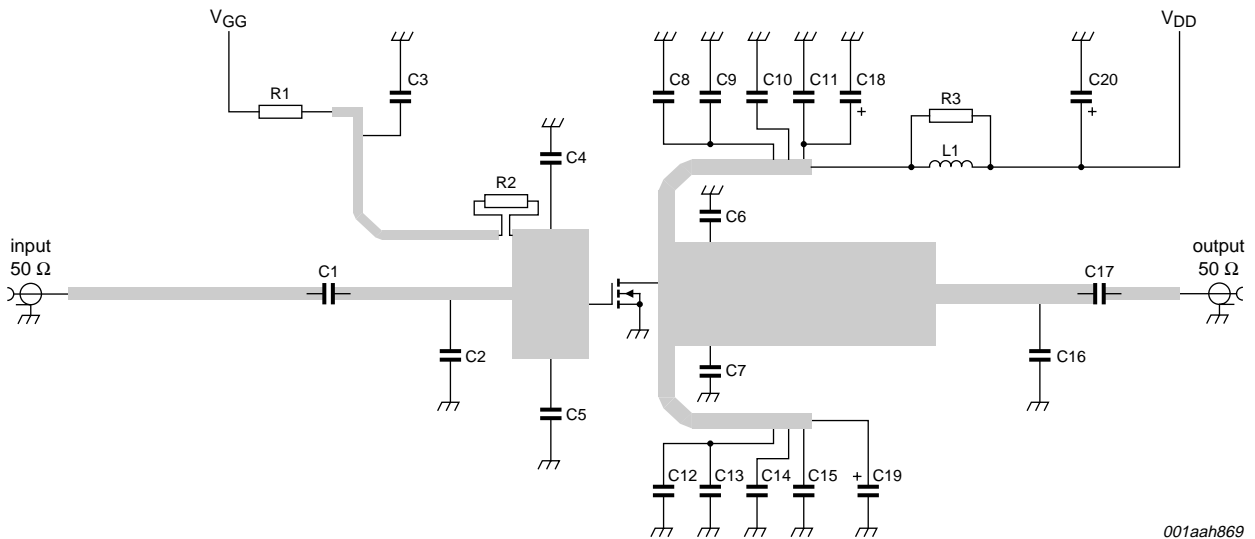
Fig 4. 2-carrier W-CDMA power gain and drain efficiency as function of average load power; typical values



$V_{DS} = 28\text{ V}$; $I_{DQ} = 950\text{ mA}$; $f_1 = 881\text{ MHz}$; $f_2 = 886\text{ MHz}$; carrier spacing 5 MHz.

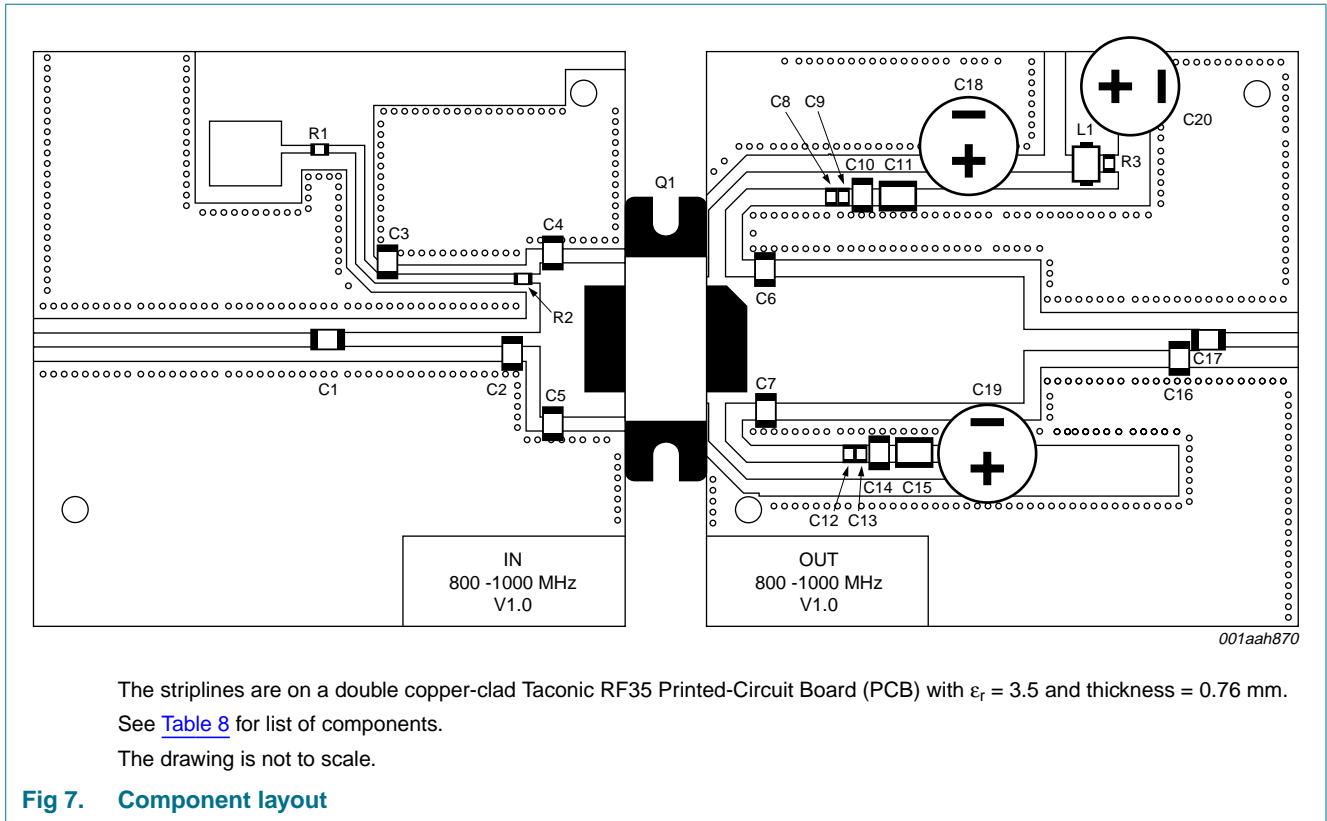
Fig 5. 2-carrier W-CDMA adjacent power channel ratio as a function of average load power; typical values

8. Test information



The drawing is not to scale.

Fig 6. Test circuit for operation at 800 MHz



The striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) with $\epsilon_r = 3.5$ and thickness = 0.76 mm.
See Table 8 for list of components.

Fig 7. Component layout

Table 8. List of components (see Figure 6 and 7).

Component	Description	Value	Remarks
C1, C3, C10, C14, C17	multilayer ceramic chip capacitor	68 pF	[1] solder vertically
C2, C4, C5	multilayer ceramic chip capacitor	8.2 pF	[1] solder vertically
C6, C7	multilayer ceramic chip capacitor	10 pF	[1] solder vertically
C8, C9, C12, C13	electrolytic capacitor	100 nF	Vishay or capacitor of same quality.
C11, C15	multilayer ceramic chip capacitor	4.7 μ F; 50 V	[2]
C16	multilayer ceramic chip capacitor	3.0 pF	[1] solder vertically
C18, C19, C20	electrolytic capacitor	220 μ F; 63 V	
L1	ferrite SMD bead		Ferroxcube BDS 3/3/4.6-4S2 or equivalent
Q1	BLF6G10LS-135R		
R1, R2, R3	SMD resistor	9.1 Ω ; 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] TDK or capacitor of same quality.

9. Package outline

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

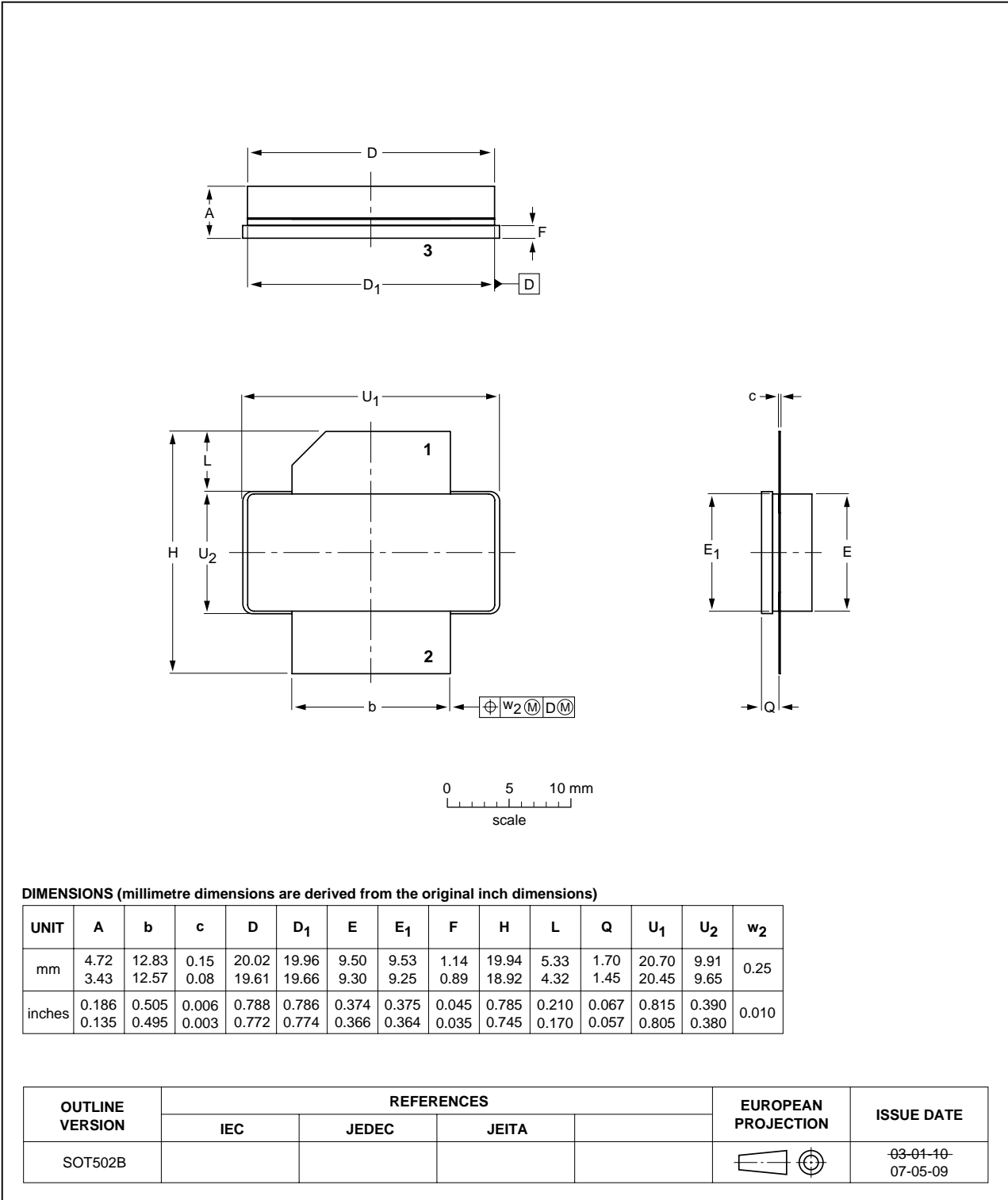


Fig 8. Package outline SOT502B

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G10LS-135R_1	20081117	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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