

## MOSFET

### OptiMOS™ Power-Transistor, 60 V

#### Features

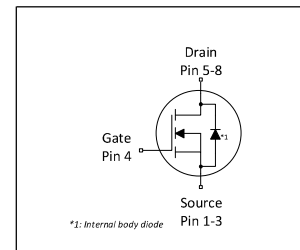
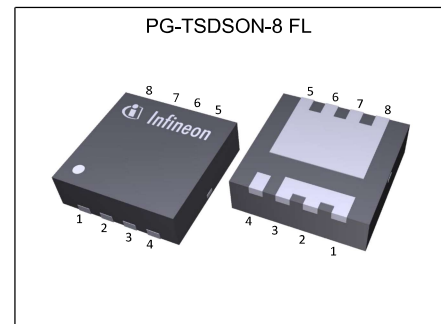
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, Logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching

#### Product validation

Qualified according to JEDEC Standard

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	6.5	m $\Omega$
$I_D$	65	A
$Q_{oss}$	19	nC
$Q_G(0V..4.5V)$	10	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSZ0703LS	PG-TSDSON-8 FL	0703LS	-

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	65 41 14	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=60\text{K/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	260	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	38	mJ	$I_D=20\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	46 2.1	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=60\text{ K/W}^2)$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	1.6	2.7	K/W	-
Device on PCB, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	60	K/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	$V_{DS}=V_{GS}$ , $I_D=20\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.4 7.3	6.5 9.4	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ $V_{GS}=4.5\text{ V}$ , $I_D=10\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.2	1.8	$\Omega$	-
Transconductance	$g_{fs}$	25	50	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=20\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance <sup>1)</sup>	$C_{iss}$	-	1400	1800	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance <sup>1)</sup>	$C_{oss}$	-	300	390	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance <sup>1)</sup>	$C_{rss}$	-	16	28	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	5.0	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	2.9	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	2.6	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=20\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	4.1	-	nC	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.3	-	nC	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	3.3	4.9	nC	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	$Q_{sw}$	-	5.1	-	nC	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	10	13	nC	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	$V_{DD}=30\text{ V}$ , $I_D=20\text{ A}$ , $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	18	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	19	26	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test

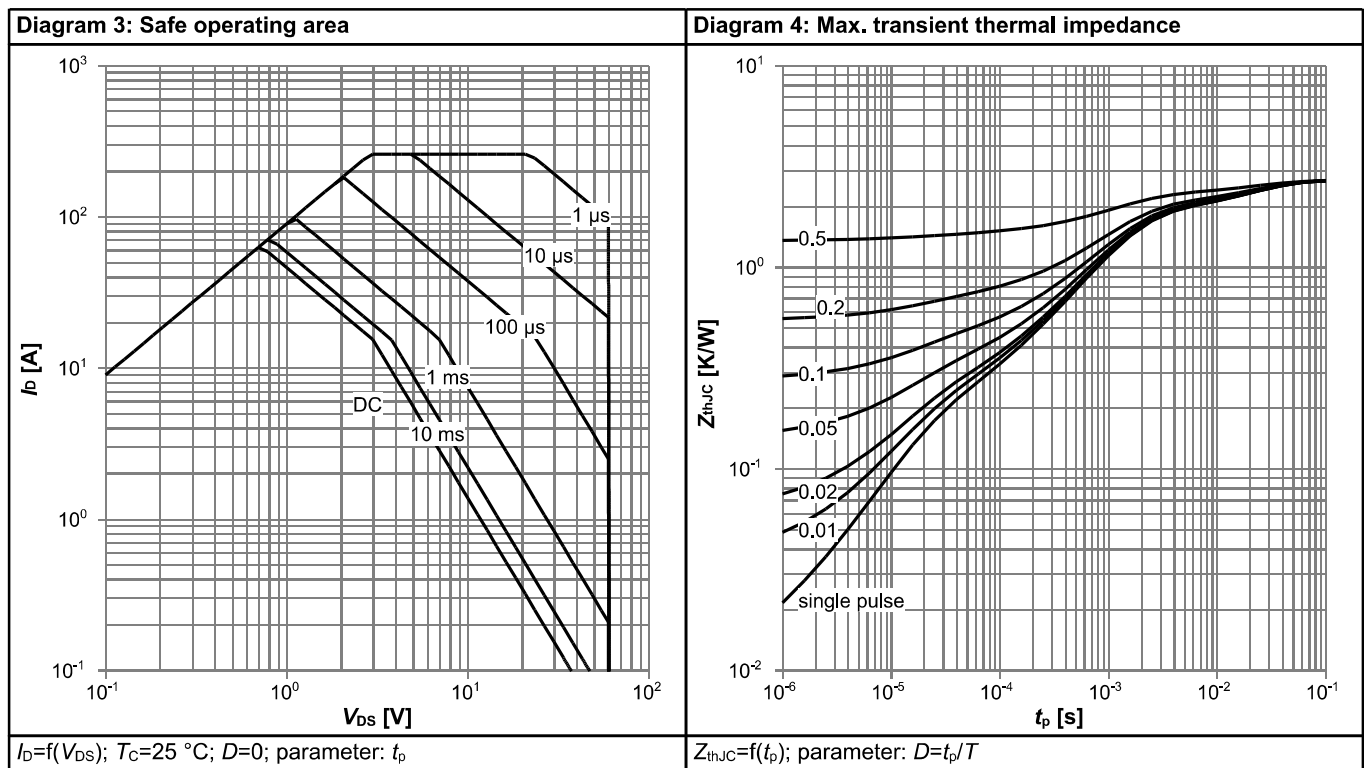
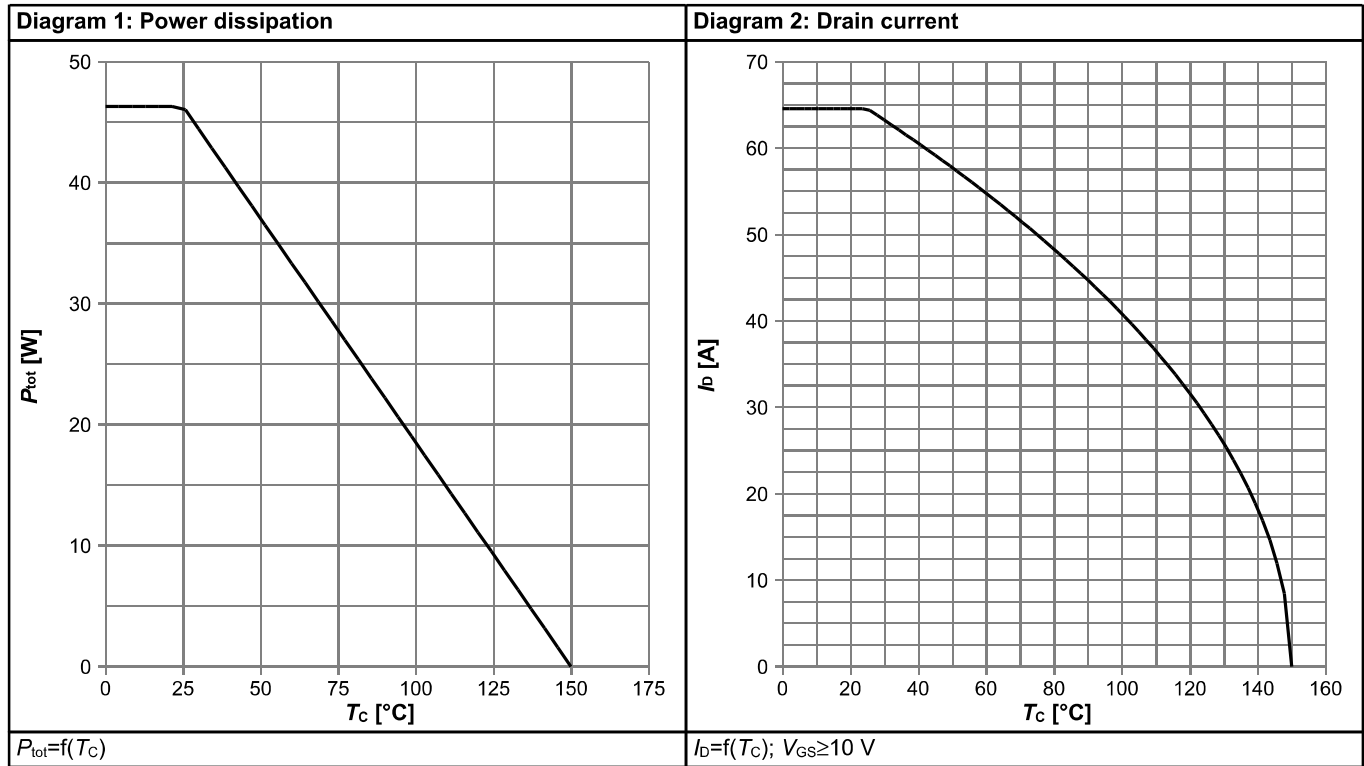
<sup>2)</sup> See "Gate charge waveforms" for parameter definition

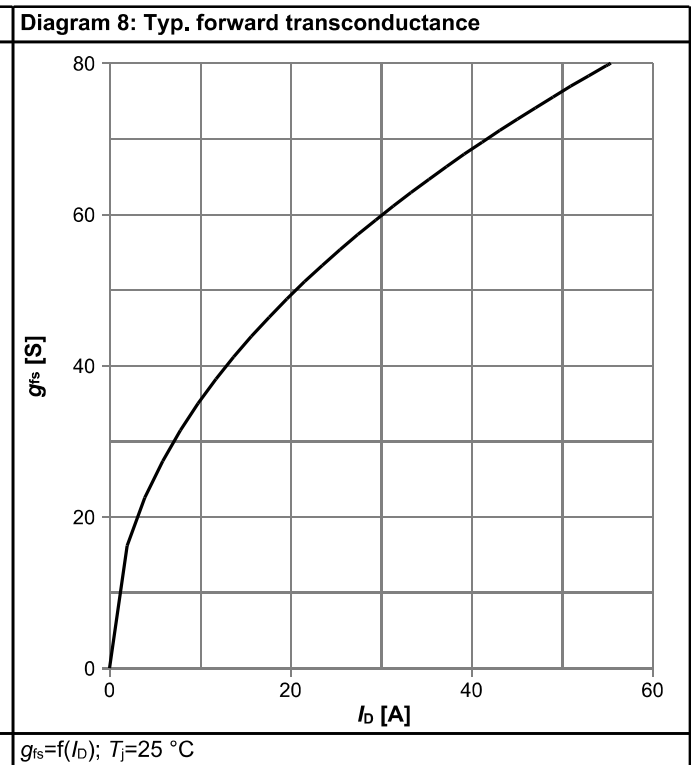
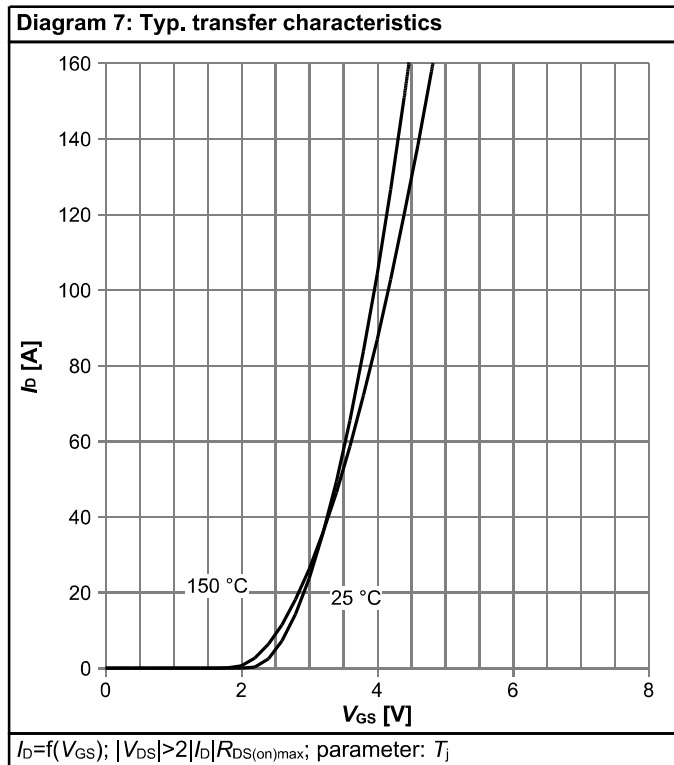
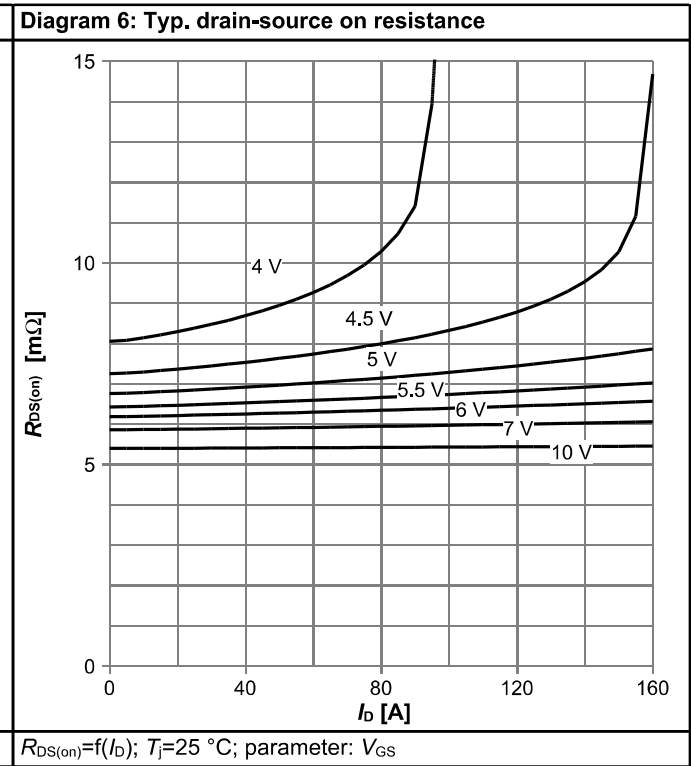
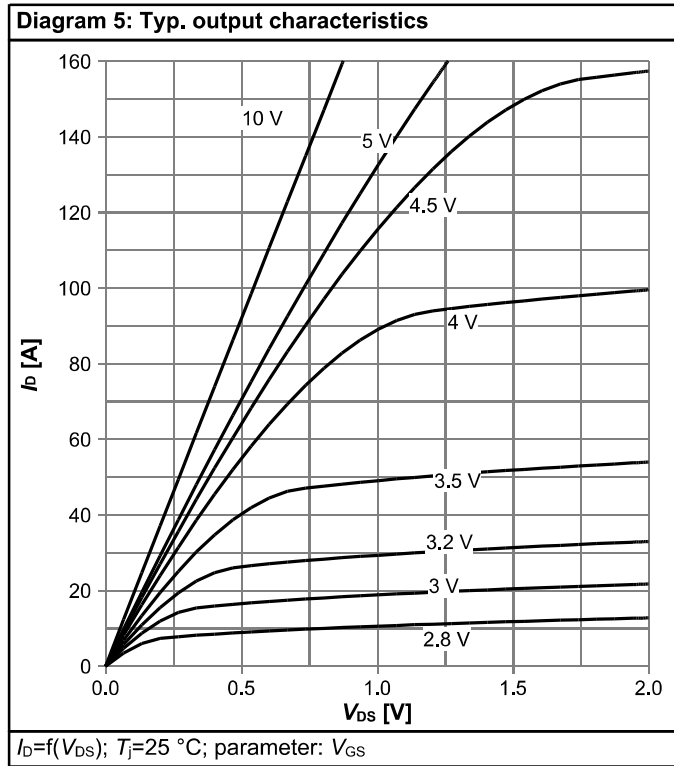
**Table 7 Reverse diode**

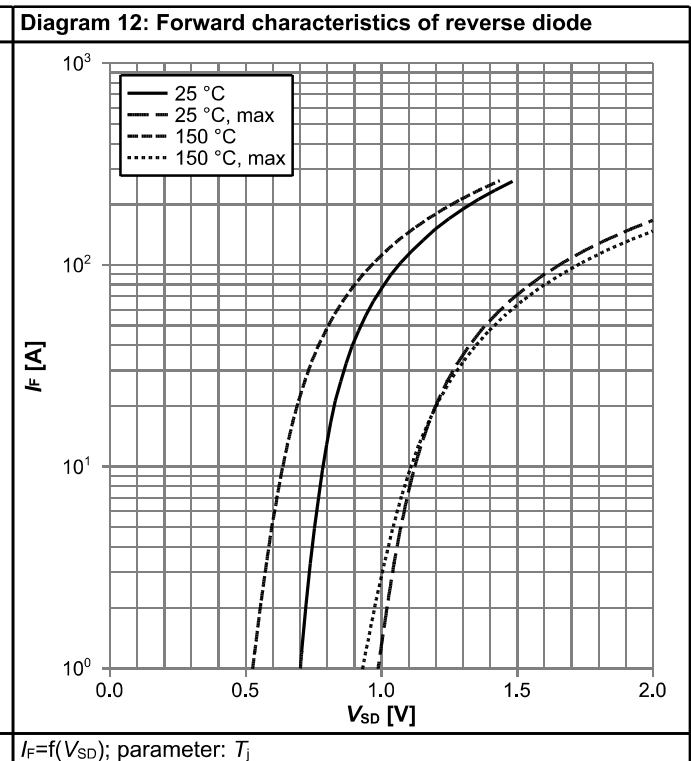
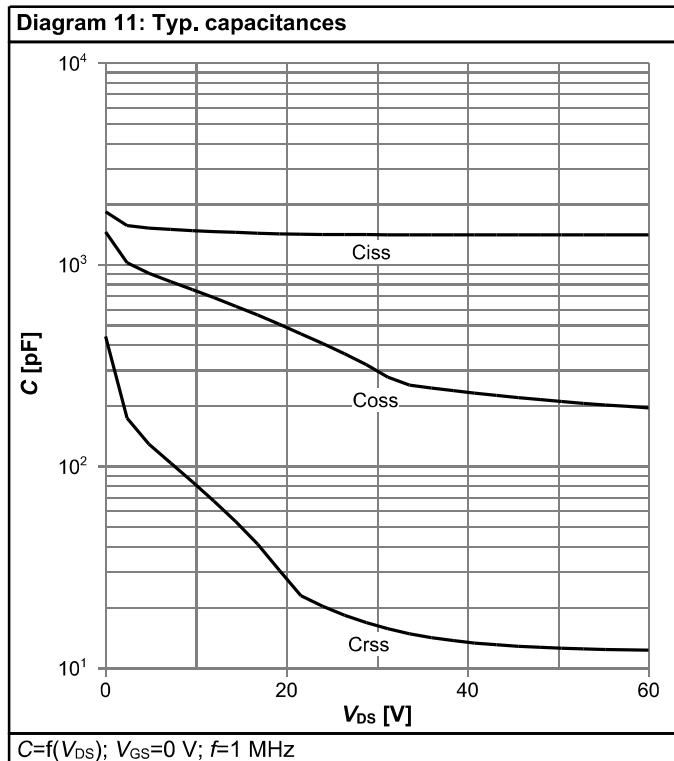
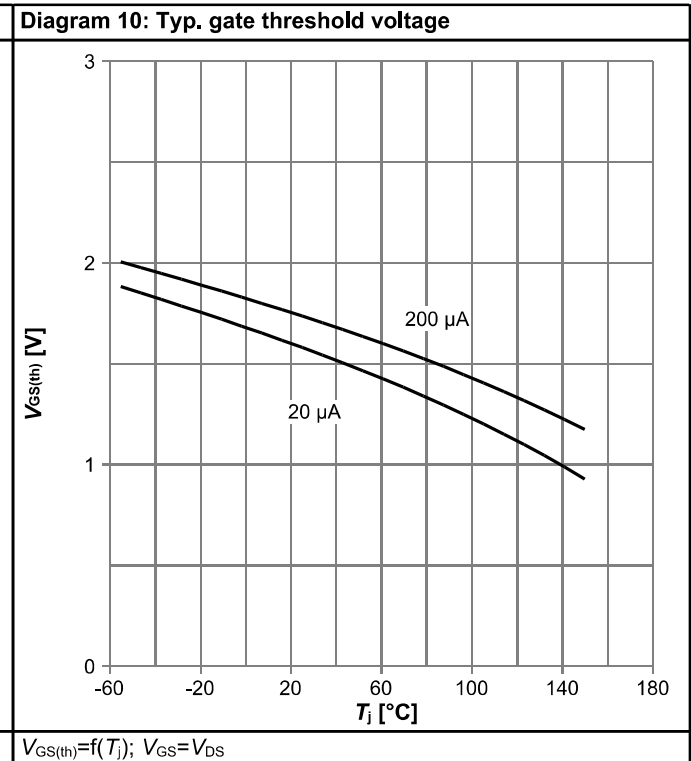
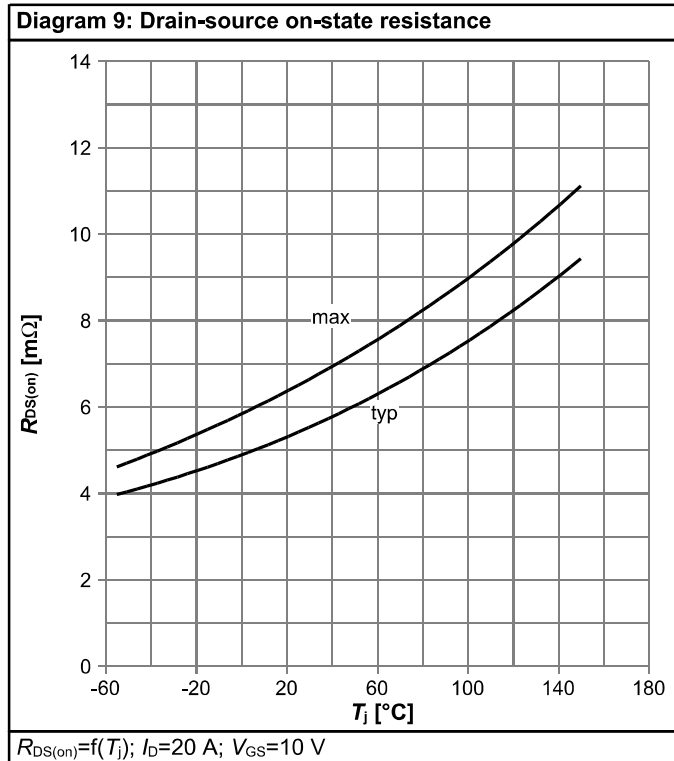
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	39	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	260	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.83	1.2	V	$V_{GS}=0\text{ V}, I_F=20\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	18	36	ns	$V_R=30\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	7	14	nC	$V_R=30\text{ V}, I_F=20\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

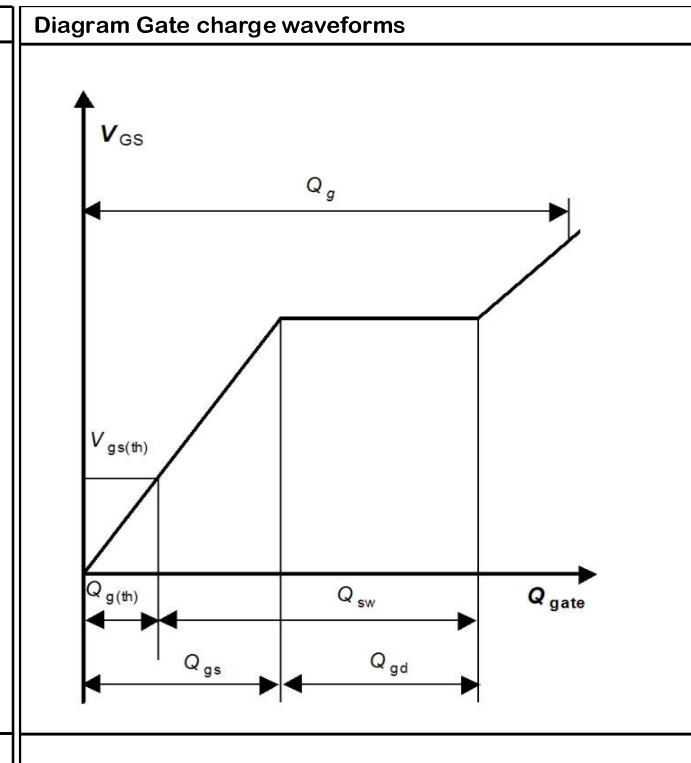
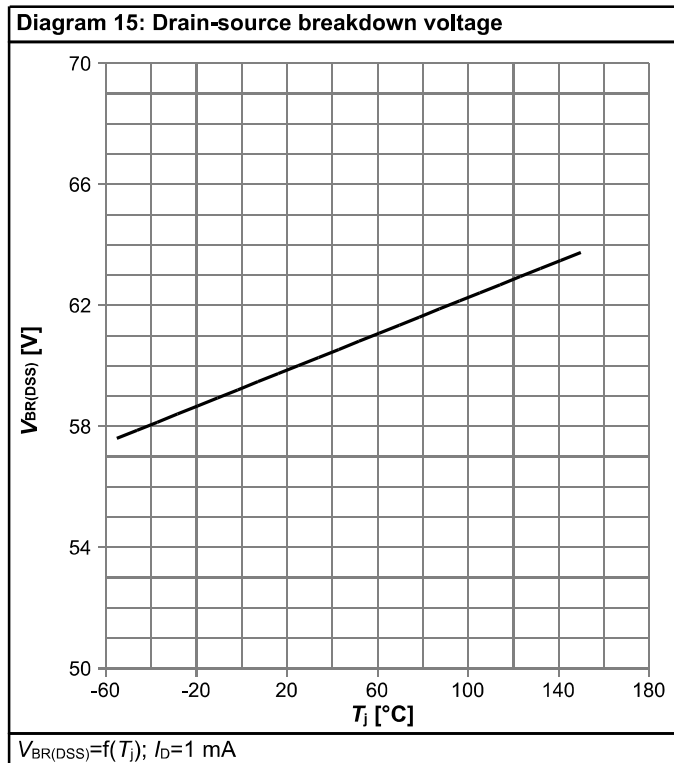
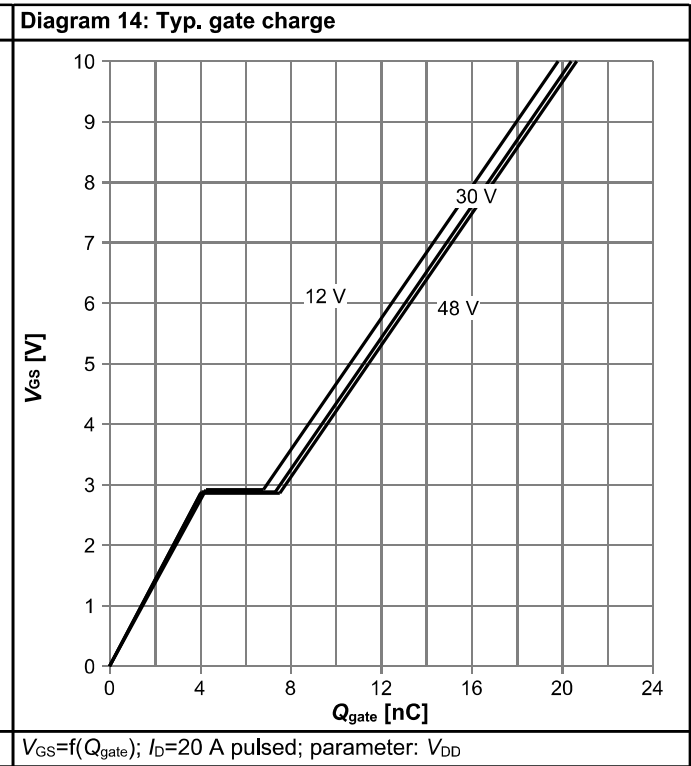
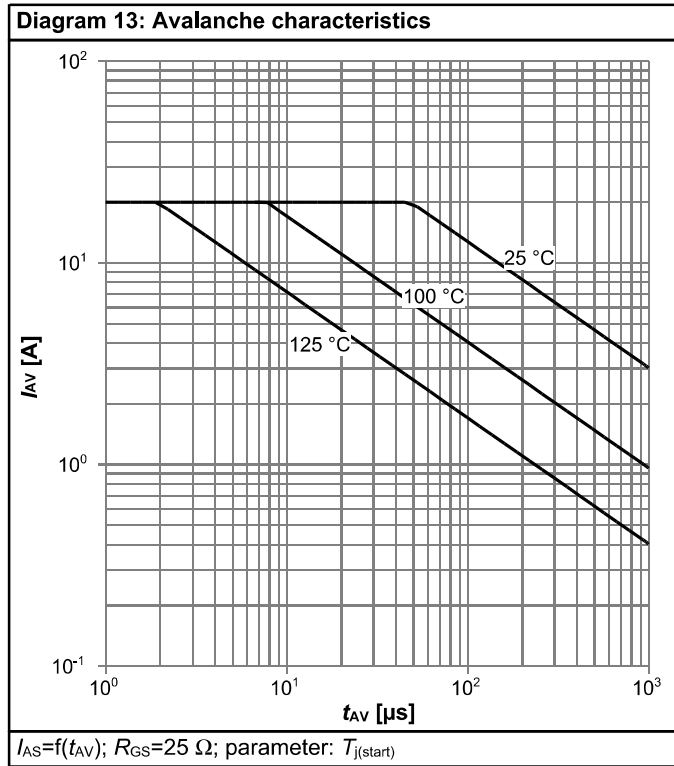
## 4 Electrical characteristics diagrams



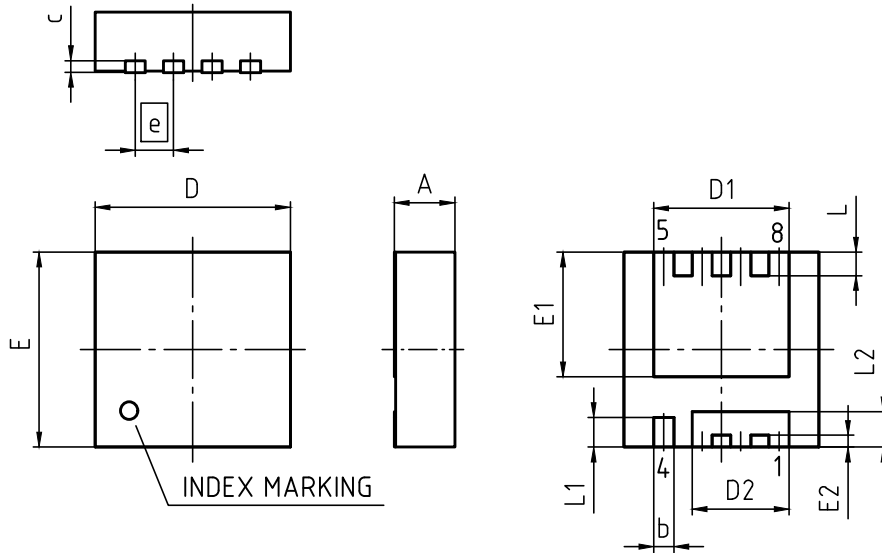








## 5 Package Outlines



PACKAGE - GROUP NUMBER: <b>PG-TSDSON-8-U03</b>		
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

Figure 1 Outline PG-TSDSON-8 FL, dimensions in mm

## Revision History

BSZ0703LS

**Revision: 2021-03-17, Rev. 2.3**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-08-10	Release of final version
2.1	2016-10-20	Update " Features "
2.2	2020-11-09	Update package drawing
2.3	2021-03-17	Update current rating

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