

NVMYS025N06CL

MOSFET – Power, Single N-Channel

60 V, 27.5 mΩ, 21 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current R _{θJC} (Notes 1, 2, 3)	Steady State	T _C = 25°C	I _D	21	A
		T _C = 100°C		12	
Power Dissipation R _{θJC} (Notes 1, 2)		T _C = 25°C	P _D	24	W
		T _C = 100°C		7.6	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _A = 25°C	I _D	8.5	A
		T _A = 100°C		6.0	
Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	P _D	3.8	W
		T _A = 100°C		1.9	
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		I _{DM}	103	A
Operating Junction and Storage Temperature Range			T _J , T _{stg}	−55 to +175	°C
Source Current (Body Diode)			I _S	20	A
Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 1.5 A)			E _{AS}	44.6	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	6.0	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	39.5	

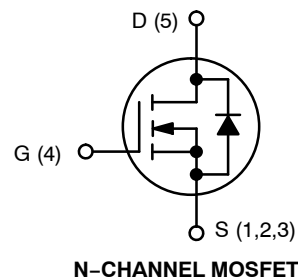
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	27.5 mΩ @ 10 V	21 A
	43 mΩ @ 4.5 V	

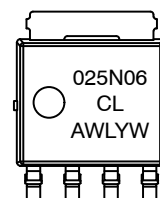


N-CHANNEL MOSFET



LFPK4
CASE 760AB

MARKING DIAGRAM



025N06CL = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

NVMYS025N06CL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25 °C		10	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 13 μA	1.2		2.0	V
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.5 A		22.9	mΩ
		V _{GS} = 4.5 V	I _D = 7.5 A		35.8	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 10 A		20		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		330		pF
Output Capacitance	C _{OSS}			172		
Reverse Transfer Capacitance	C _{RSS}			5		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 7.5 A		5.8		nC
Threshold Gate Charge	Q _{G(TH)}			0.8		
Gate-to-Source Charge	Q _{GS}			1.3		
Gate-to-Drain Charge	Q _{GD}			0.6		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 7.5 A		2.7		nC

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 7.5 A, R _G = 1.0 Ω		5		ns
Rise Time	t _r			12.5		
Turn-Off Delay Time	t _{d(OFF)}			14		
Fall Time	t _f			2.5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 7.5 A	T _J = 25°C		0.87	1.2	V
			T _J = 125°C		0.76		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 20 A/μs, I _S = 7.5 A			18		ns
Charge Time	t _a				8.3		
Discharge Time	t _b				9.7		
Reverse Recovery Charge	Q _{RR}				7.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

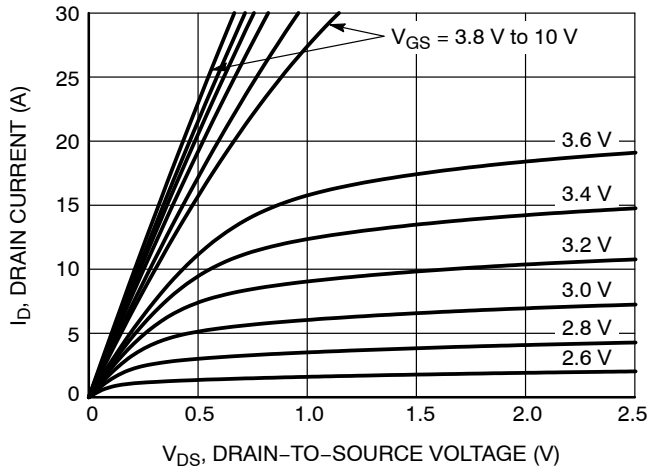


Figure 1. On-Region Characteristics

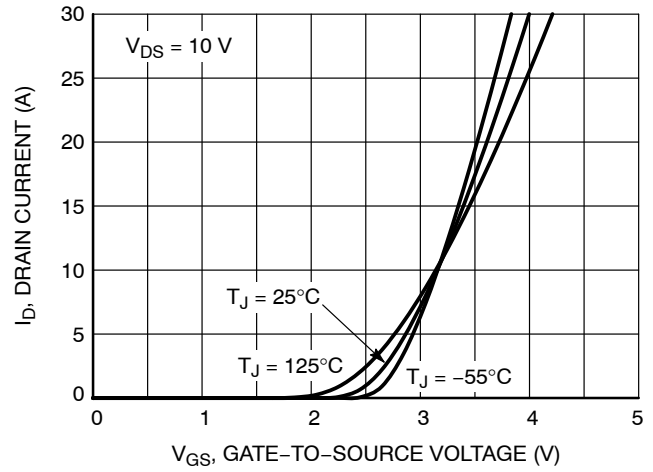


Figure 2. Transfer Characteristics

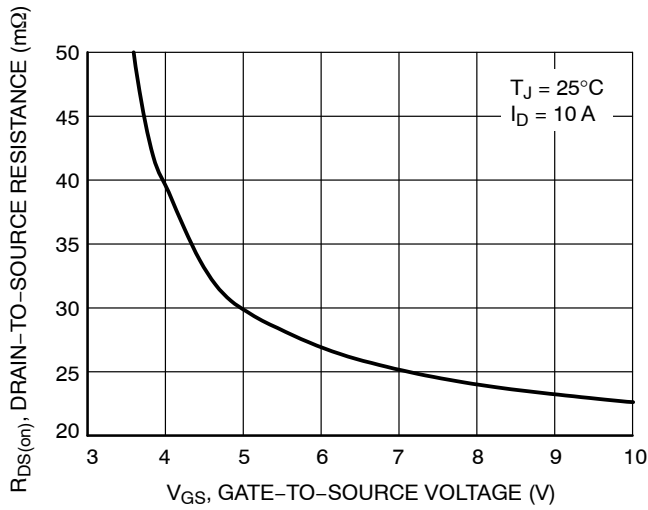


Figure 3. On-Resistance vs. Gate-to-Source Voltage

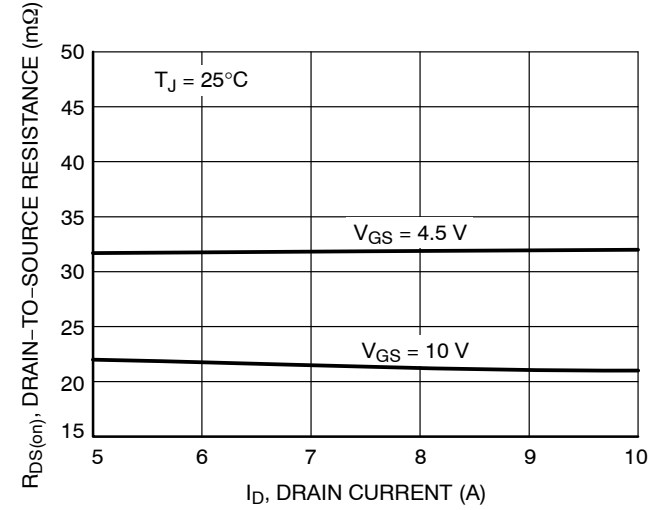


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

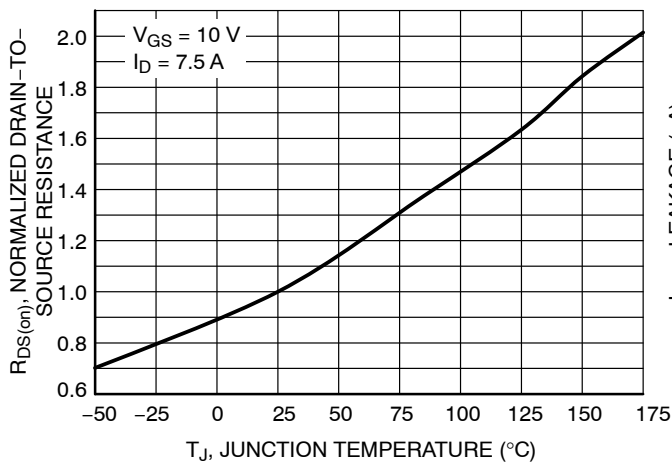


Figure 5. On-Resistance Variation with Temperature

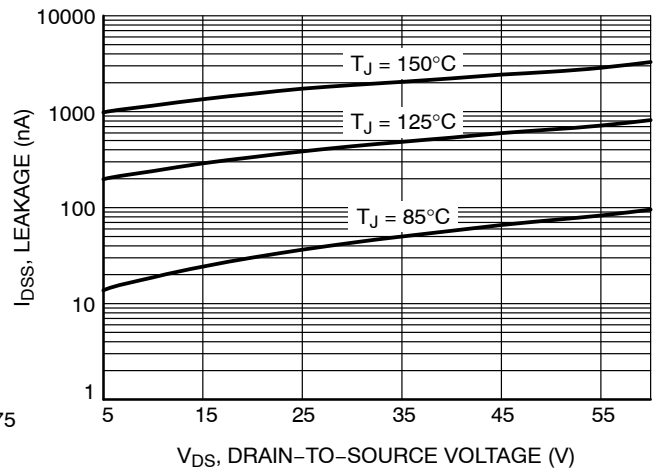


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

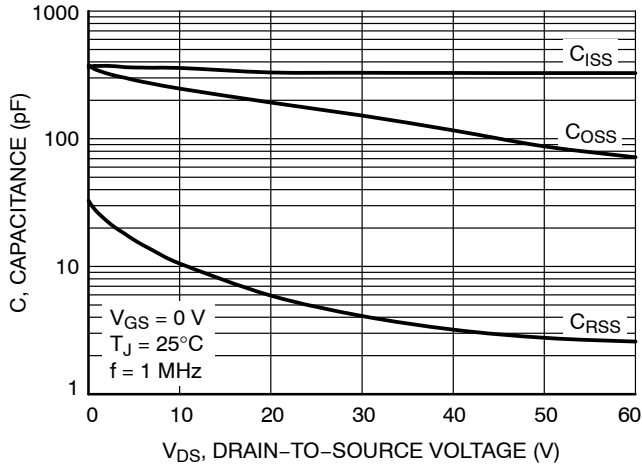


Figure 7. Capacitance Variation

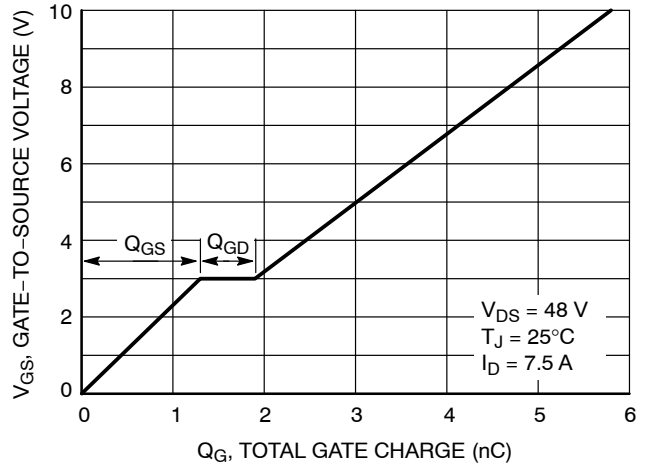


Figure 8. Gate-to-Source vs. Total Charge

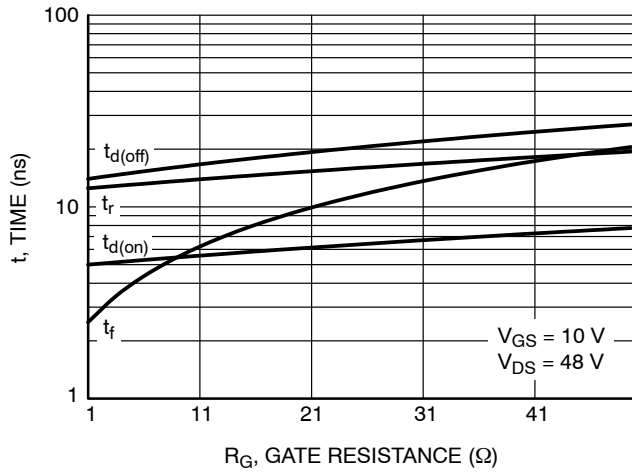


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

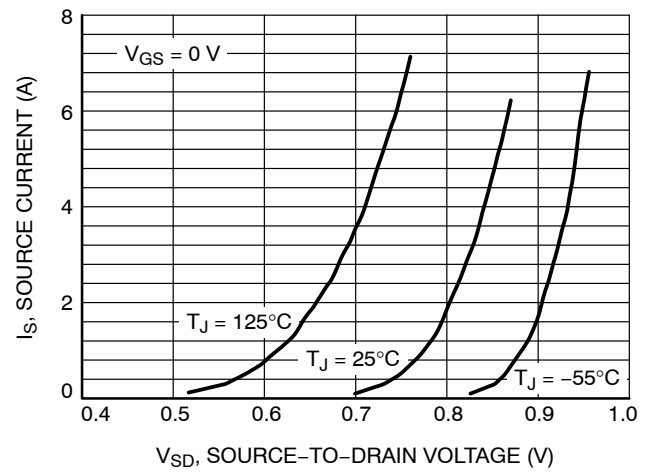


Figure 10. Diode Forward Voltage vs. Current

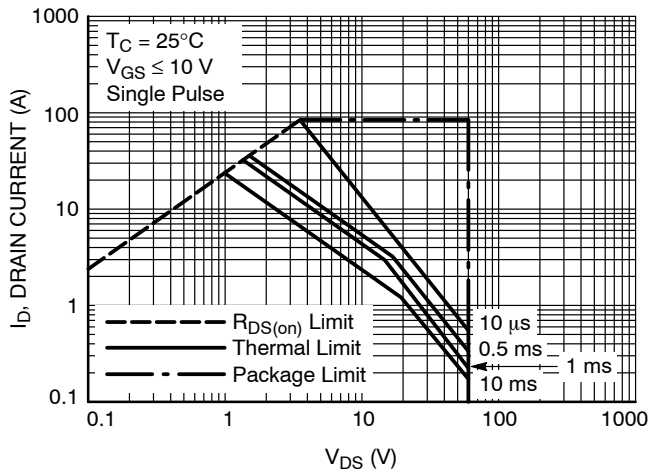


Figure 11. Maximum Rated Forward Biased Safe Operating Area

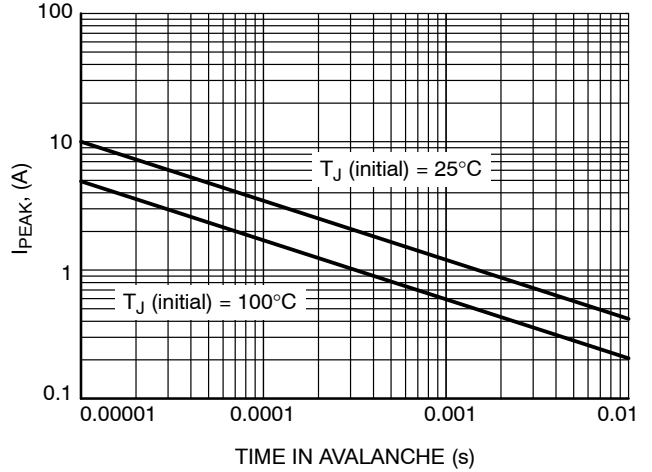


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMYS025N06CL

TYPICAL CHARACTERISTICS

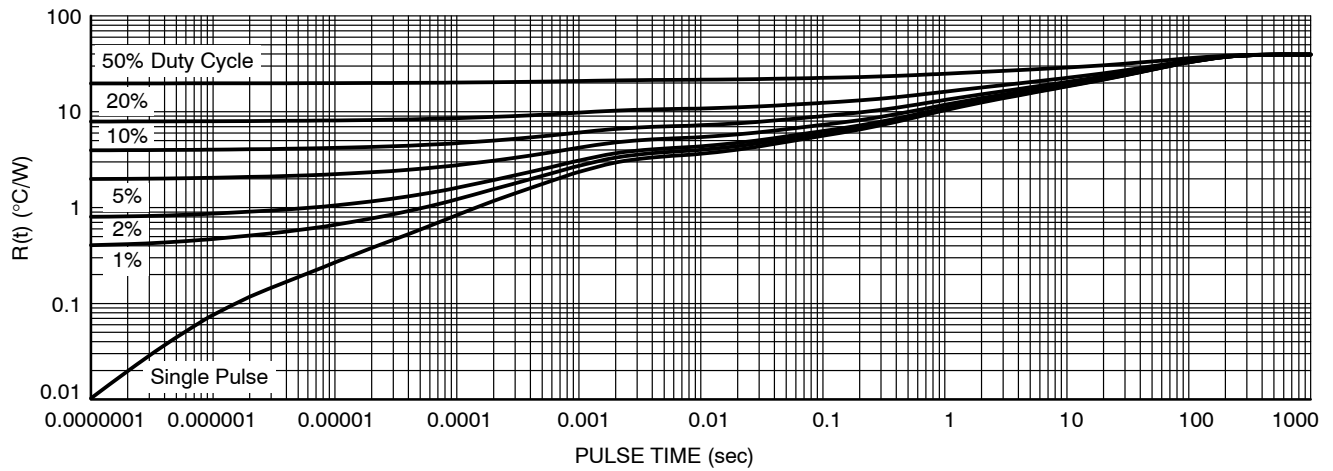


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMYS025N06CLTWG	025N06CL	LFP4K4 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

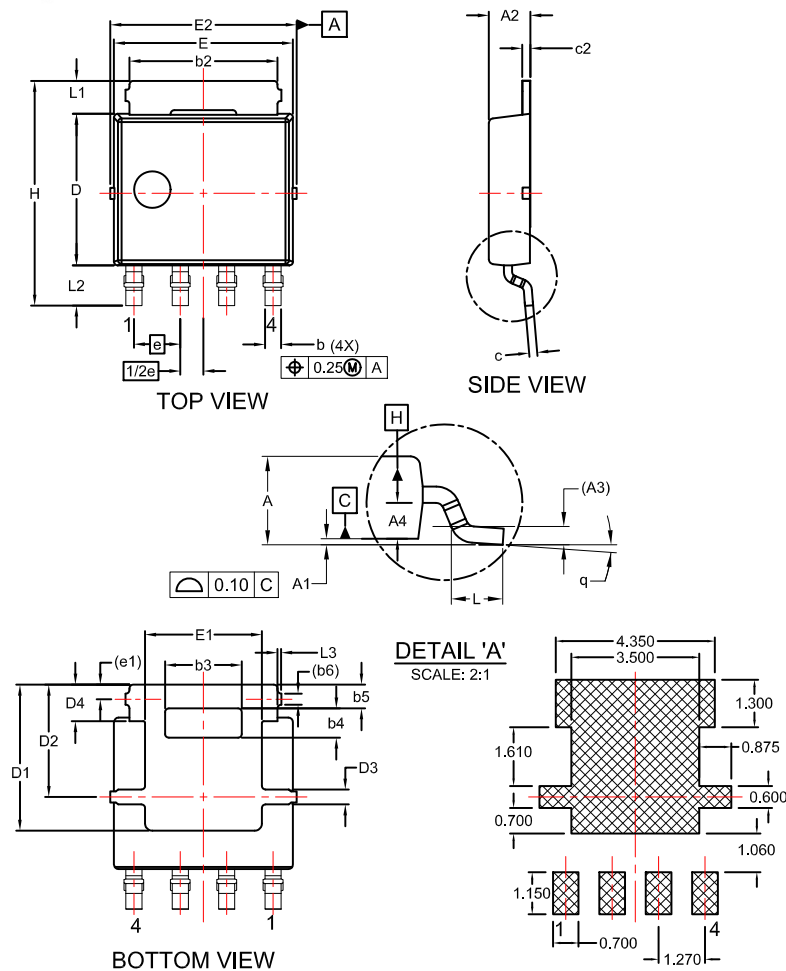


LFPAK4 5x6
CASE 760AB
ISSUE C

DATE 19 NOV 2019

NOTES:

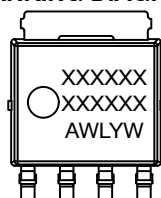
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

UNIT IN MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 REF		
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b3	2.00	2.10	2.20
b4	0.70	0.80	0.90
b5	0.55	0.65	0.75
b6	0.31 REF		
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.05	4.15	4.25
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
E	4.80	4.90	5.00
E1	3.10	3.20	3.30
E2	5.00	5.15	5.30
e	1.27 BSC		
1/2e	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.40	0.65	0.85
L1	0.80	0.90	1.00
L2	0.90	1.10	1.30
L3	0.00	0.10	0.20
q	0°	4°	8°

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DESCRIPTION: LFPAK4 5x6

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