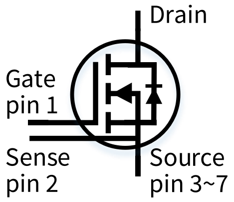
IMBF170R1K0M1

CoolSiC™ 1700V SiC Trench MOSFET
Silicon Carbide MOSFET

Features

- Revolutionary semiconductor material - Silicon Carbide
- Optimized for fly-back topologies
- 12V/0V gate-source voltage compatible with most fly-back controllers
- Very low switching losses
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.5V
- Fully controllable dV/dt for EMI optimization



Benefits

- Reduction of system complexity
- Directly drive from fly-back controller
- Efficiency improvement and cooling effort reduction
- Enabling higher frequency

Potential applications

- Energy generation
    - Solar string inverter
    - Solar Central inverter
- Industrial power supplies
    - Industrial UPS
    - Industrial SMPS
- Infrastructure – Charger
    - Charger

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC 47/20/22

Note: *the source and sense pins are not exchangeable, their exchange might lead to malfunction recommended for forward operation mode only*

Table 1 Key Performance and Package Parameters

Type	V_{DS}	I_D T_C = 25°C, $R_{th(j\text{-}c,max)}$	$R_{DS(on)}$ T_{vj} = 25°C, I_D = 1A, V_{GS} = 12V	$T_{vj,max}$	Marking	Package
IMBF170R1K0M1	1700V	5.2A	1000mΩ	175°C	170M11K0	PG-TO263-7

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1 Maximum ratings

For optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Value	Unit
Drain-source voltage, $T_{vj} \geq 25°C$	V_{DSS}	1700	V
DC drain current for $R_{th(j-c,max)}$, limited by T_{vjmax}, $V_{GS} = 12V$, $T_C = 25°C$ $T_C = 100°C$	I_D	 5.2 3.7	A
Pulsed drain current, t_p limited by T_{vjmax}, $V_{GS} = 12V$	$I_{D,pulse}$[1]	13.3	A
Gate-source voltage[2] Max transient voltage, < 1% duty cycle Recommended turn-on gate voltage Recommended turn-off gate voltage	 V_{GS} $V_{GS,on}$ $V_{GS,off}$	 -10… 20 12… 15 0	V
Power dissipation, limited by T_{vjmax} $T_C = 25°C$ $T_C = 100°C$	P_{tot}	 68 34	W
Virtual junction temperature	T_{vj}	-55… 175	°C
Storage temperature	T_{stg}	-55… 150	°C
Soldering temperature Reflow soldering (MSL1 according to JEDEC J-STD-020)	T_{sold}	260	°C

[1] verified by design
[2] **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note *AN2018-09* must be considered to ensure sound operation of the device over the planned lifetime.

2 Thermal resistances

Table 3

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
MOSFET thermal resistance, junction – case	$R_{th(j-c)}$		-	1.7	2.2	K/W
Thermal resistance, junction – ambient	$R_{th(j-a)}$	leaded	-	-	62	K/W

3 Electrical Characteristics

3.1 Static characteristics

Table 4 Static characteristics (at T_{vj} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 12V, I_D = 1A,				mΩ
		T_{vj} = 25°C	-	1000	-	
		T_{vj} = 100°C	-	1416	-	
		T_{vj} = 175°C	-	2037	-	
		V_{GS} = 15V, I_D = 1A,				
		T_{vj} = 25°C	-	809	880	
Gate-source threshold voltage	$V_{GS(th)}$	*(tested after 1 ms pulse at* V_{GS} = 20V*)*				V
		I_D = 1.1mA, V_{DS} = V_{GS}				
		T_{vj} = 25°C	3.5	4.5	5.7	
		T_{vj} =175°C	-	3.6	-	
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0V, V_{DS} = 1700V				µA
		T_{vj} = 25°C	-	0.4	11	
		T_{vj} = 175°C	-	6	-	
Gate-source leakage current	I_{GSS}	V_{GS} = 20V, V_{DS} = 0V	-	-	100	nA
		V_{GS} = -10V, V_{DS} = 0V	-	-	-100	nA
Transconductance	g_{fs}	V_{DS} = 20V, I_D = 1A	-	0.42	-	S
Internal gate resistance	$R_{G,int}$	f = 1MHz, V_{AC} = 25mV	-	35	-	Ω

3.2 Dynamic characteristics

Table 5 Dynamic characteristics (at T_{vj} = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{DD} = 1000V, V_{GS} = 0V, f = 1MHz, V_{AC} = 25mV	-	275	-	pF
Output capacitance	C_{oss}		-	7.2	-	
Reverse capacitance	C_{rss}		-	0.7	-	
C_{oss} stored energy	E_{oss}		-	1.3	-	µJ
Total gate charge	Q_G	V_{DD} = 1000V, I_D = 1A, V_{GS} = 0/12V, turn-on pulse	-	5	-	nC
Gate to source charge	$Q_{GS,pl}$		-	1.5	-	
Gate to drain charge	Q_{GD}		-	1.6	-	

3.3 Switching characteristics

Table 6 Switching characteristics, Inductive load [3]

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
MOSFET Characteristics, T_{vj} = 25°C						
Turn-on delay time	$t_{d(on)}$	V_{DD} = 1000V, I_D = 1A, V_{GS} = 0/12V, $R_{G,ext}$ = 22Ω, L_σ = 40nH, diode: body diode at V_{GS} = 0V see Fig. E	-	19	-	ns
Rise time	t_r		-	14	-	ns
Turn-off delay time	$t_{d(off)}$		-	20	-	ns
Fall time	t_f		-	22	-	ns
Turn-on energy	E_{on}		-	31	-	µJ
Turn-off energy	E_{off}		-	7	-	µJ
Total switching energy	E_{tot}		-	37	-	µJ
MOSFET Characteristics, T_{vj} = 175°C						
Turn-on delay time	$t_{d(on)}$	V_{DD} = 1000V, I_D = 1A, V_{GS} = 0/12V, $R_{G,ext}$ = 22Ω, L_σ = 40nH, diode: body diode at V_{GS} = 0V see Fig. E	-	16	-	ns
Rise time	t_r		-	11	-	ns
Turn-off delay time	$t_{d(off)}$		-	23	-	ns
Fall time	t_f		-	23	-	ns
Turn-on energy	E_{on}		-	33	-	µJ
Turn-off energy	E_{off}		-	8	-	µJ
Total switching energy	E_{tot}		-	41	-	µJ

[3] The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package. In applications, e.g. fly-back topology, the switching behavior highly depends on the circuitry (transformer, snubber…), the switching loss in the application will be different from the datasheet value.

4 Electrical characteristic diagrams

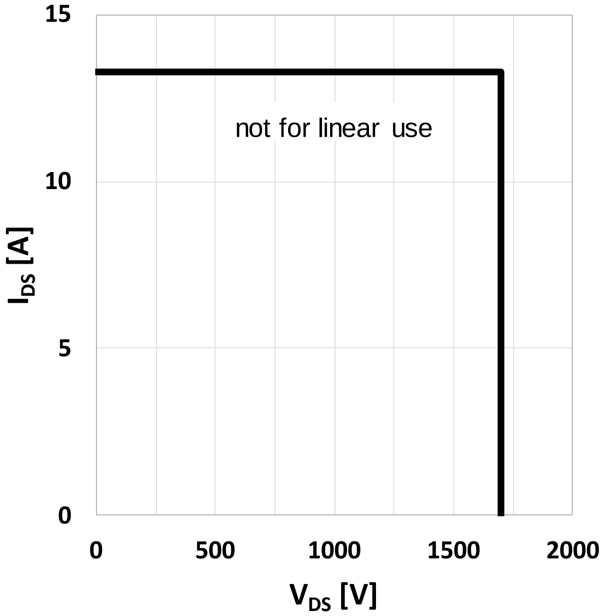


Figure 1 Safe operating area (SOA)
(V_{GS} = 0/12V, T_c = 25°C, T_j ≤ 175°C)

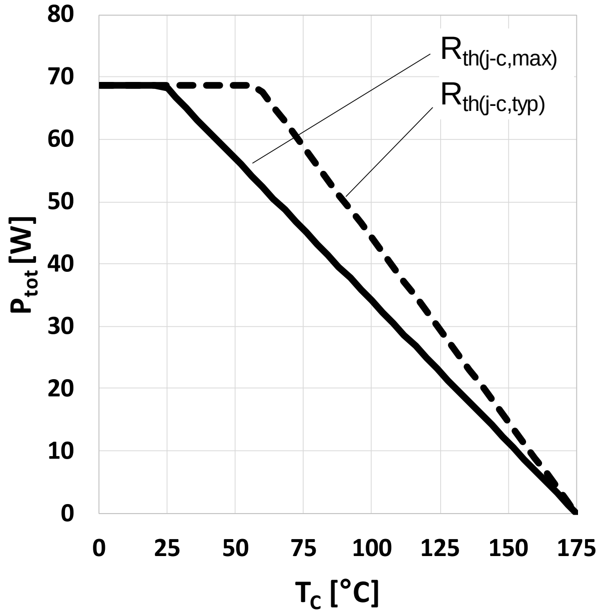


Figure 2 Power dissipation as a function of case temperature limited by bond wire
(P_{tot} = f(T_C))

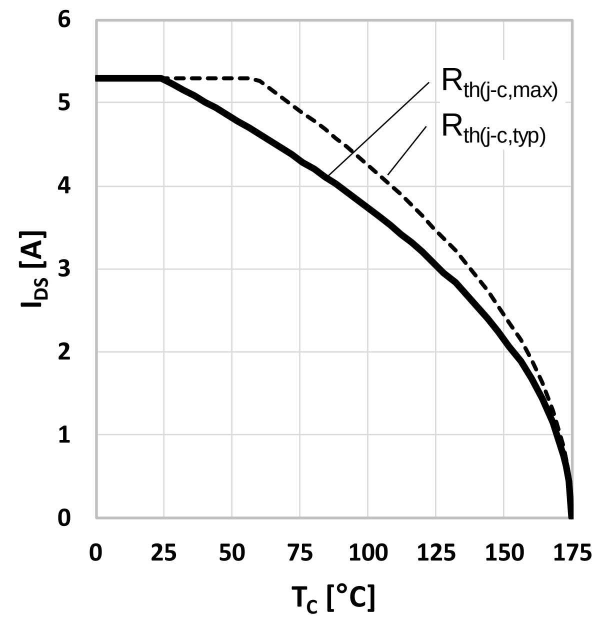


Figure 3 Maximum DC drain to source current as a function of case temperature limited by bond wire (I_{DS} = f(T_C))

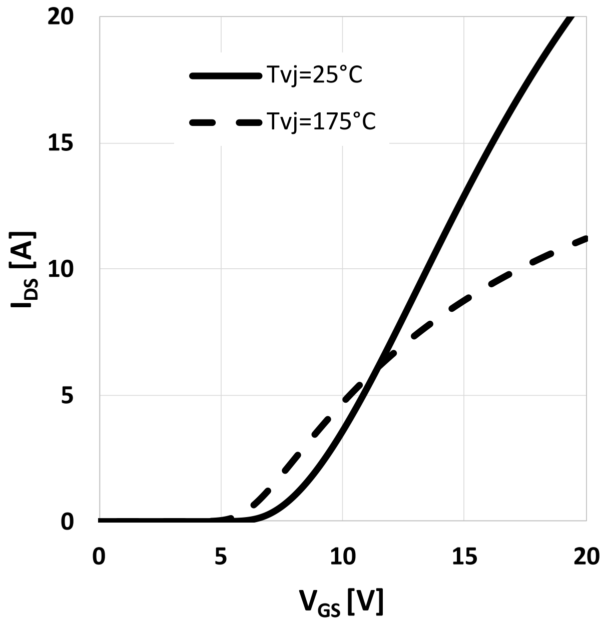


Figure 4 Typical transfer characteristic
(I_{DS} = f(V_{GS}), V_{DS} = 20V, t_P = 20µs)

Electrical characteristic diagrams

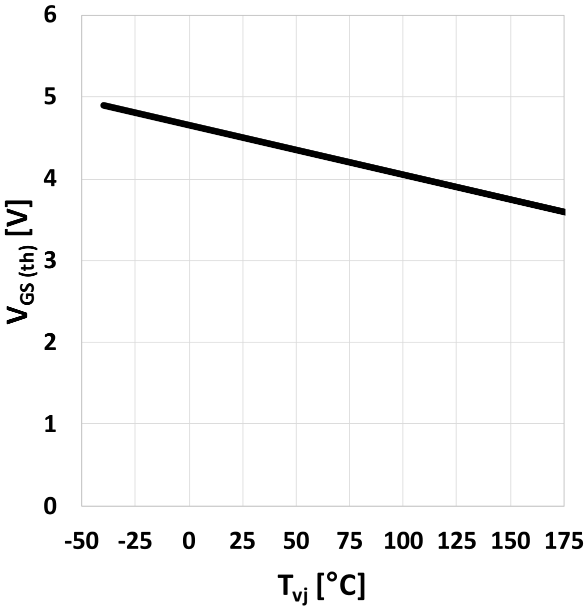


Figure 5 Typical gate-source threshold voltage as a function of junction temperature
($V_{GS(th)}$ = f(T_{vj}), I_{DS} = 1.1mA, V_{GS} = V_{DS})

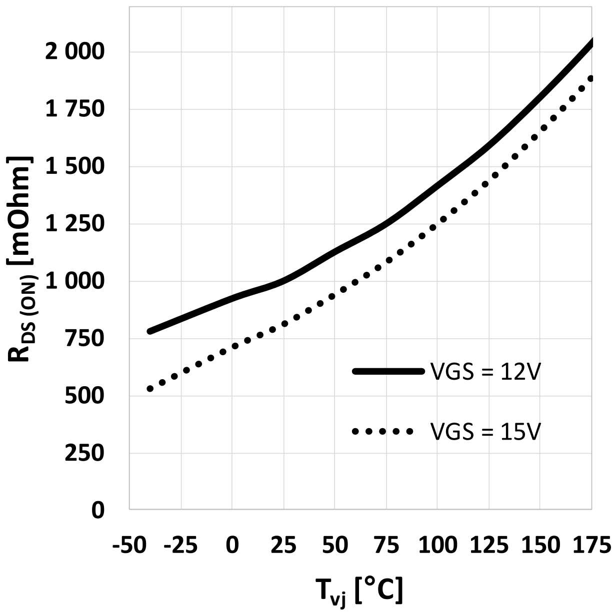


Figure 6 Typical on-resistance as a function of junction temperature
($R_{DS(on)}$ = f(T_{vj}), I_{DS} = 1A)

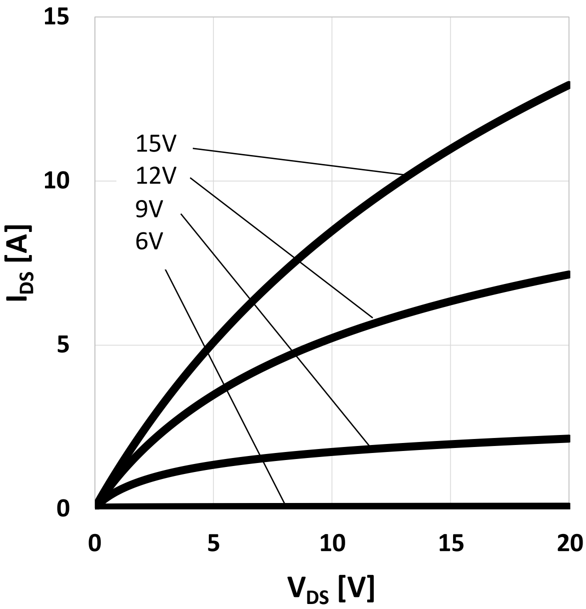


Figure 7 Typical output characteristic, V_{GS} as parameter
(I_{DS} = f(V_{DS}), T_{vj}=25°C, t_P = 20µs)

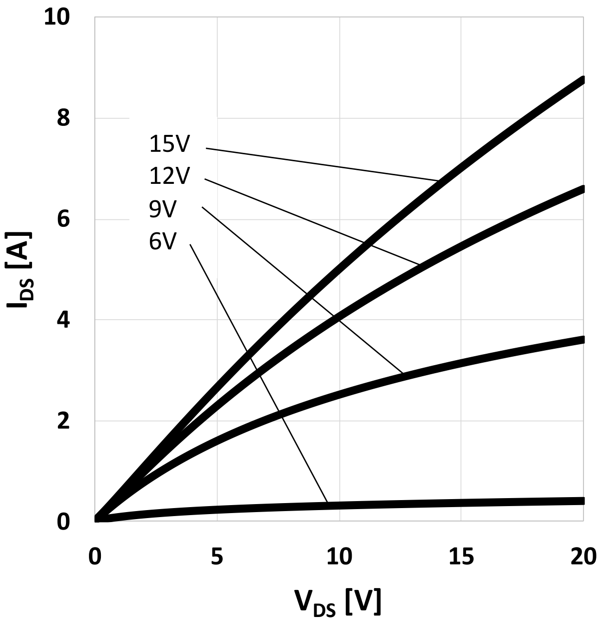


Figure 8 Typical output characteristic, V_{GS} as parameter
(I_{DS} = f(V_{DS}), T_{vj}=175°C, t_P = 20µs)

Electrical characteristic diagrams

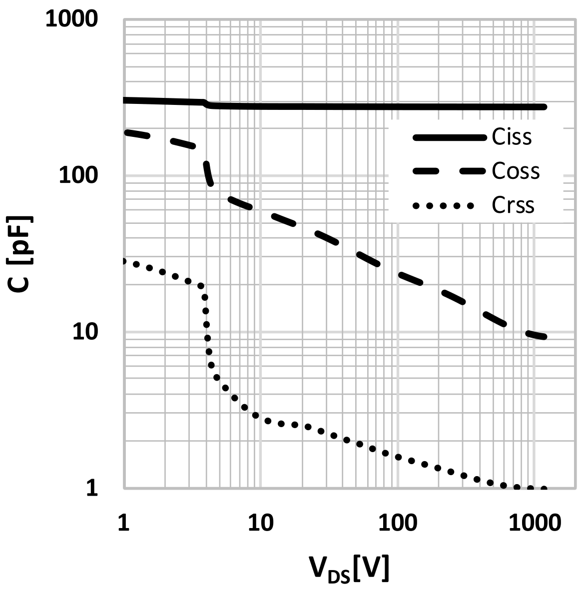


Figure 9 **Typical capacitance as a function of drain-source voltage**
(C = f(V_{DS}), V_{GS} = 0V, f = 1MHz)

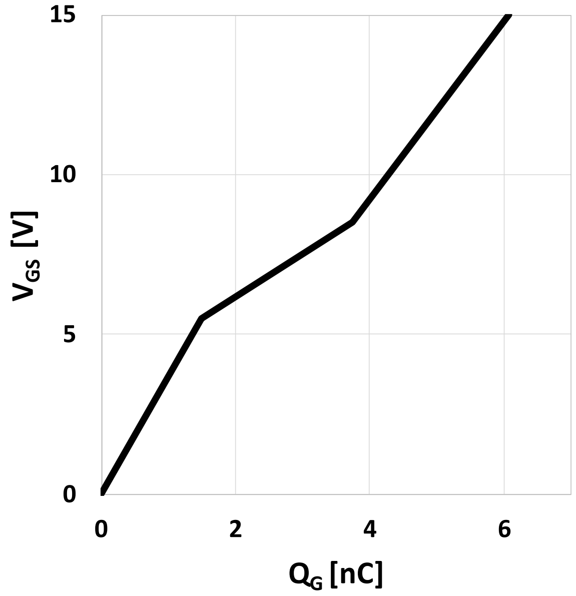


Figure 10 **Typical gate charge**
(V_{GS} = f(Q_G), I_{DS} = 1A, V_{DS} = 1000V, turn-on pulse)

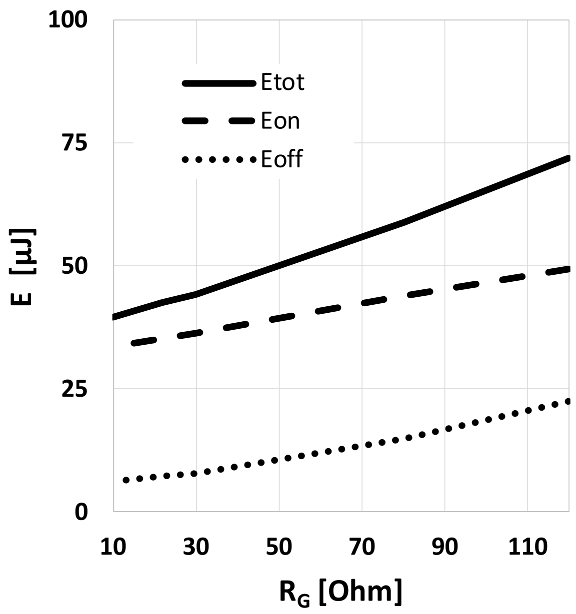


Figure 11 **Typical switching energy losses as a function of gate resistance**
(E = f($R_{G,ext}$), V_{DD} = 1000V, V_{GS} = 0V/12V, I_D = 1A, T_{vj} = 175°C, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

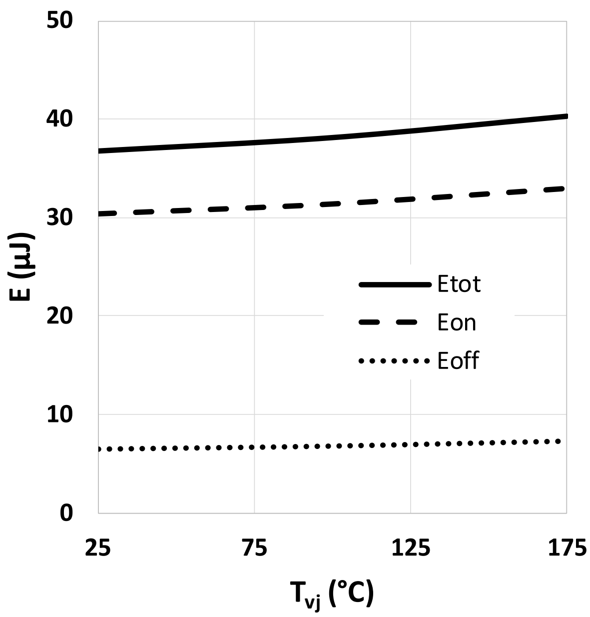


Figure 12 **Typical switching energy losses as a function of junction temperature**
(E = f(T_{vj}), V_{DD} = 1000V, V_{GS} = 0V/12V, $R_{G,ext}$ = 22Ω, I_D = 1A, ind. load, test circuit in Fig. E, diode: body diode at V_{GS} = 0V)

Electrical characteristic diagrams

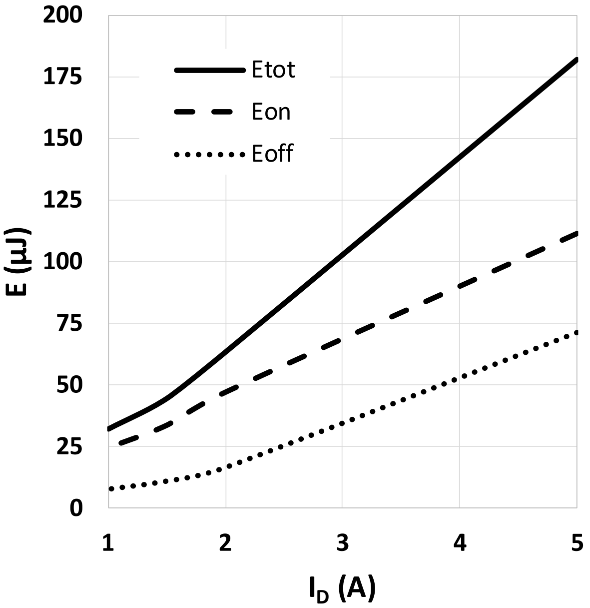


Figure 13 Typical switching energy losses as a function of drain-source current
($E = f(I_{DS})$, $V_{DD} = 1000V$, $V_{GS} = 0V/12V$, $R_{G,ext} = 22\Omega$, $T_{vj} = 175°C$, ind. load, test circuit in Fig. E, diode: body diode at $V_{GS} = 0V$)

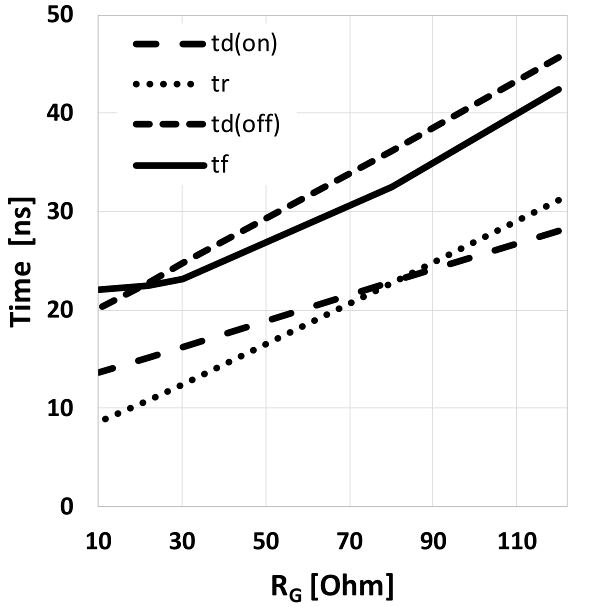
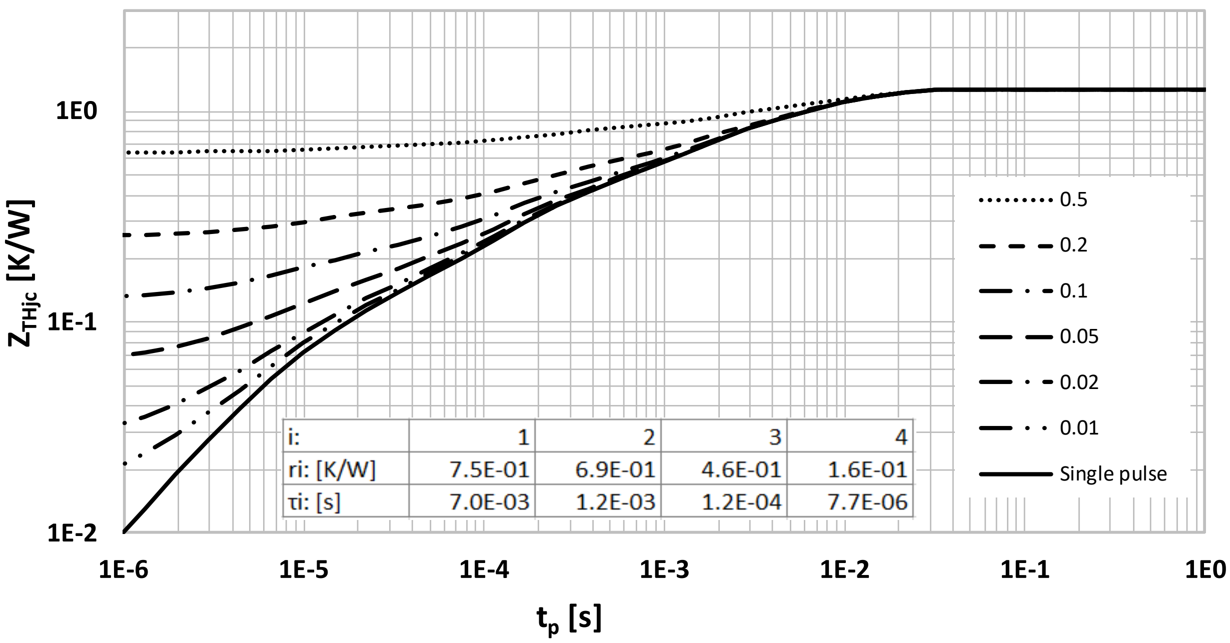


Figure 14 Typical switching times as a function of gate resistor
($t = f(R_{G,ext})$, $V_{DD} = 1000V$, $V_{GS} = 0V/12V$, $I_D = 1A$, $T_{vj} = 175°C$, ind. load, test circuit in Fig. E, diode: body diode at $V_{GS} = 0V$)



i:	1	2	3	4
ri: [K/W]	7.5E-01	6.9E-01	4.6E-01	1.6E-01
τi: [s]	7.0E-03	1.2E-03	1.2E-04	7.7E-06

Figure 15 Max. transient thermal resistance (MOSFET)
($Z_{th(j-c,max)} = f(t_P)$, parameter $D = t_p/T$, thermal equivalent circuit in Fig. D)

5 Package drawing

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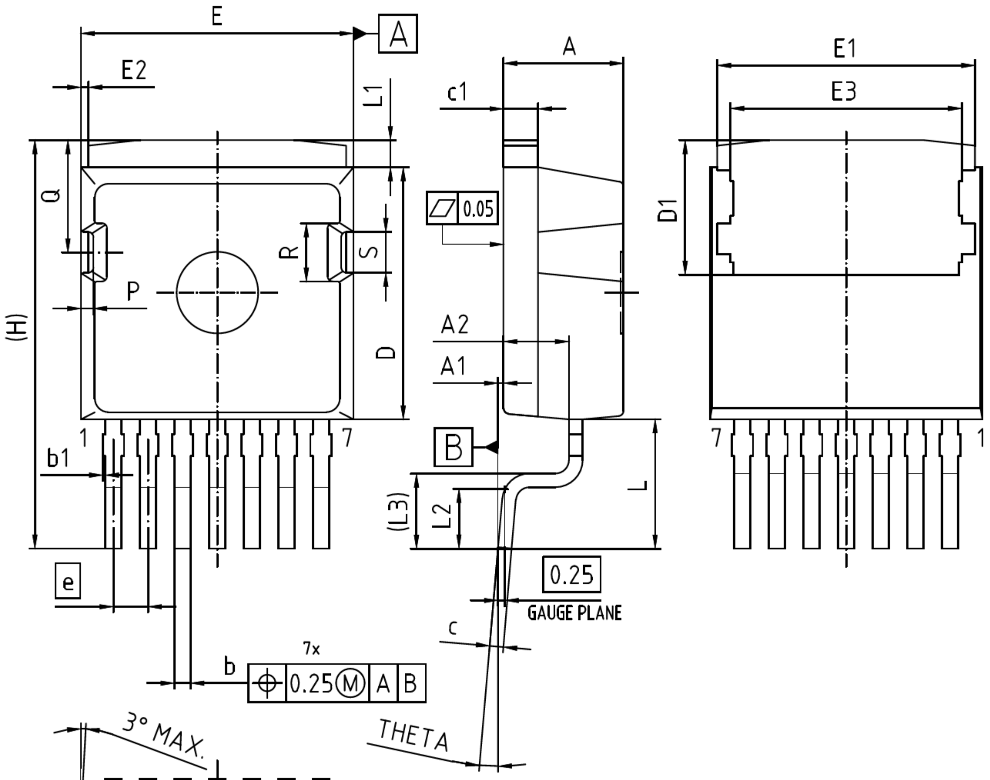

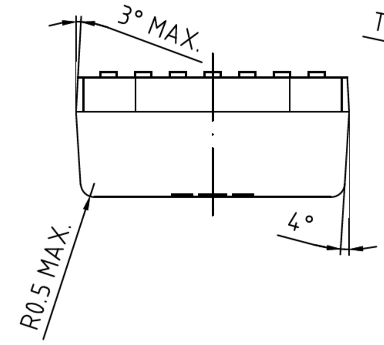

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.20
A2	2.30	2.50
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	4.85	5.05
E	9.80	10.20
E1	9.36	9.56
E2	0.00	0.30
E3	8.40	8.60
e	1.27	
H	15.00	
L	4.20	5.20
L1	0.70	1.30
L2	1.70	2.70
L3	2.70	
P	0.35	0.55
Q	4.02	4.22
R	2.03	2.23
S	1.40	1.60
THETA	0.00°	8.00°

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Figure 16 Package drawing

6 Test conditions

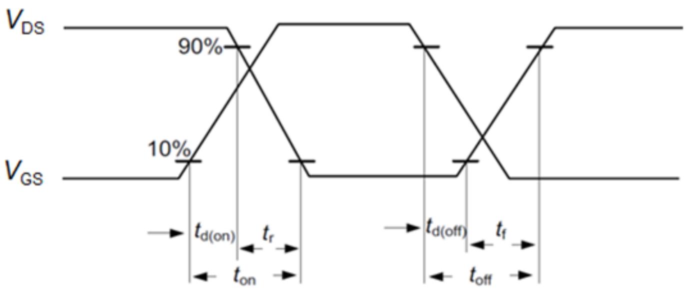

Figure A. **Definition of switching times**

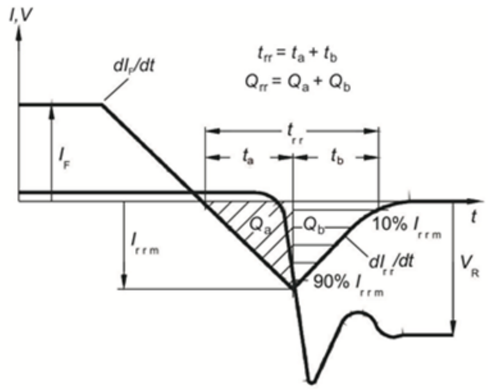

Figure C. **Definition of diode switching characteristics**

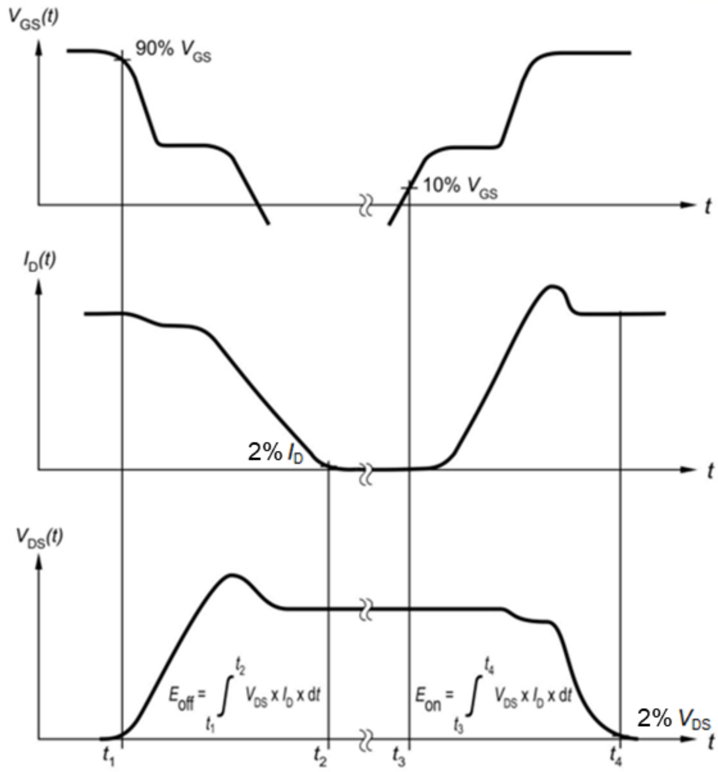

Figure B. **Definition of switching losses**

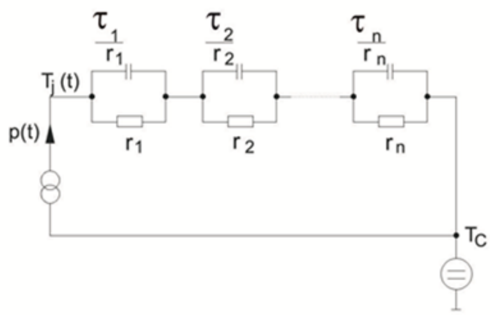

Figure D. **Thermal equivalent circuit**

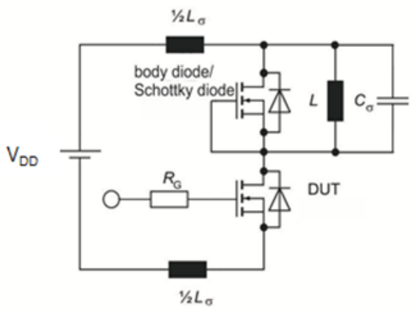

Figure E. **Dynamic test circuit**
Parasitic inductance L_{σ},
parasitic capacitor C_{σ},

Figure 17 Test conditions

Revision history

Document version	Date of release	Description of changes
2.1	2020-04-27	Final Datasheet
2.2	2020-12-11	Correction of circuit symbol on page 1
2.3	2021-04-12	Editorial changes

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