SIEMENS

ICs for Communications

ISDN Echocancellation Circuit
IEC-Q

PEB 2091 Version 5.3

PEF 2091 Version 5.3

Delta Sheet 09.98

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1 Overview

The PEB/F 2091, IEC-Q Version 5.3 is an optimized version of the IEC-Q which offers

- new features to support applications gaining increasing importance in the marketplace,
- improved electrical behavior and functions, as well as
- full compatibility to previous IEC-Q versions.

New Features

New features are introduced to support applications such as Wireless Local Loop, U interface repeaters, Dual Mode S and U Terminals and PC cards.

Improved Characteristics

Electrical Characteristics, such as power consumption, ESD immunity, and dynamic characteristics of the Microprocessor interface have been significantly improved.

Some functions were improved to achieve more flexibility and comply with various customers needs.

All errata with significance to function or service have been cleared.

Compatibility

Version 5.3 is compatible to all previous versions of PEB/F 2091 and PSB/F 21910 up to Version 5.2. This Delta Sheet refers to Version 5.1 of PEB/F 2091[1)]. It can also serve as Delta Sheet compared with versions 5.2 if points 3.6, page 50, 3.7, page 50 and 5.1, page 54 are ignored. These points have been implemented in Version 5.2. For differences in default settings between Version 5.3 and versions 5.1 and 5.2 see Footnote 2, page 29 and Note, page 38.

1 Related documents: User's Manual 02.95 of the PEB 2091 Version 4.3, Delta Sheet of the PEB/F 2091 Version 4.4 and Delta Sheet of the PEB/F 2091 Version 5.1.

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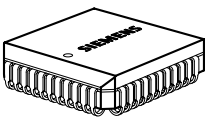
ISDN Echocancellation Circuit IEC-Q

PEB 2091
PEF 2091

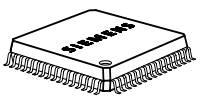
Version 5.3

CMOS

1.1 Features



P-LCC-44



M-QFP-64

T-QFP-64

- All functions of PEB/F 2091 and PSB/F 21910
- Compatible with all PEB/F 2091 and PSB/F 21910 versions up to Version 5.2
- Significant reduction in power consumption compared with all versions up to Version 5.1
- Significant improvement in ESD immunity
- Accelerated microprocessor interface in parallel mode
- Reduced Jitter of the IOM®-2 interface in all NT and TE modes
- Internal undervoltage detection control
- User defined control of Single Bits indication and filtering
- A Schmitt Trigger has been introduced in the Hardware Reset path
- Available in three packages: P-LCC-44, M-QFP-64 and T-QFP-64

In µP mode:

- User defined enable or disable of the superframe marker function
- Wake-up function in NT Mode without IOM®-2 interface
- Selectable polarity of the S/G bit
- Indication of S/G bit status on pin SG (available only in M-QFP-64 and TQFP-64 packages)

In repeater applications:

- Upstream wake-up indication in LT Repeater mode
- 15.36 MHz master clock available on pin CLS in NT Repeater mode

1.2 Pin Configuration

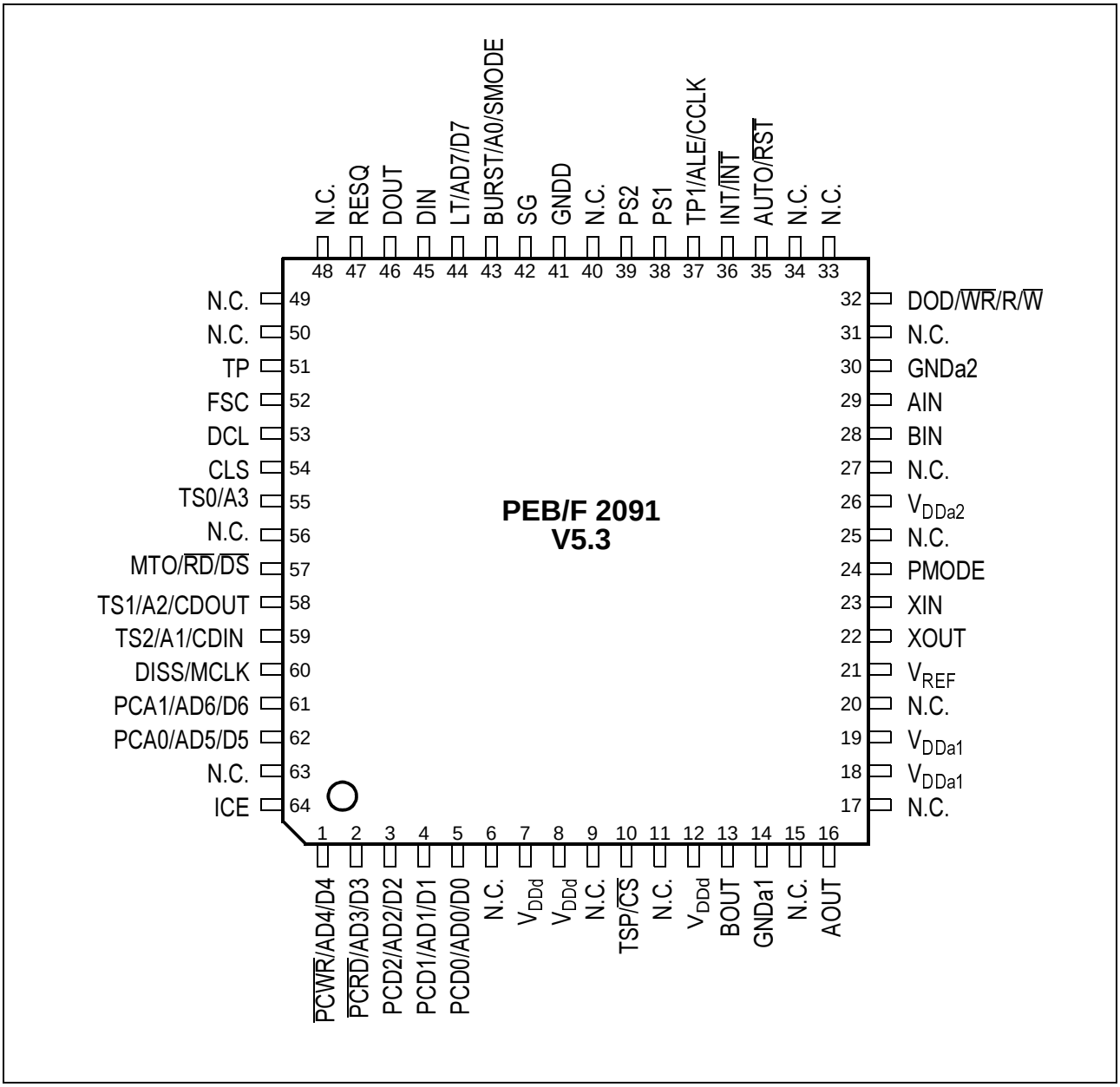


Figure 1 Pin Configuration for M-QFP-64 and T-QFP-64 Packages (top view)

1.3 Pin Definitions and Functions

The following tables group the pins according to their functions. They include pin name, pin number, type and a brief description of the function. Changes compared with versions 5.1 and 5.2 will be written in bold type style.

1.3.1 Pin Definition in Stand Alone Mode

(i.e. PMODE=”0” or unconnected)

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

1.3.1.1 Mode Selection Pins

12	24	PMODE	I	Processor Interface Enable: Setting PMODE to “1“ enables the Processor Interface (Multiplexed, demultiplexed and serial modes). Tie to GND or do not connect to select stand alone mode. Internal pull down.
28	47	$\overline{\text{RESQ}}$	I	**Reset:** Low active, must be (0) at least for **30** ns. The reset in the LT and NT-PBX mode will be carried out only after the on IOM®-2 clock have been applied to the IEC-Q. Tie to VDD if not used.
3	10	TSP	I	Single pulse test mode: For activation refer to table 2 on page 48 in the User’s Manual 02.95 of the PEB 2091 Version 4.3. When active, alternating 2.5 V pulses are issued in 1.5 ms intervals. Tie to GND if not used.
25	44	LT	I/O	LT-modes: Selects LT, COT 512/1536, LT-RP (1) and non LT modes NT, TE, NT-PBX, NT-RP (0).
24	43	BURST	I	Selection of burst modes (LT, NT-PBX) with (1) and non-burst modes (NT, TE, COT-512/1536, LT/NT-RP) with (0).

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
33	55	TS0	I	Time-slot: IOM®-2 channel selection for burst mode. LSB, active high.
35	58	TS1	I/O	Time-slot: IOM®-2 channel selection for burst mode. Active high.
36	59	TS2	I	Time-slot: IOM®-2 channel selection for burst mode. MSB, active high.
18	35	AUTO	I/O	Auto mode: Selection between auto- and transparent mode for EOC channel processing. (Automode = (1))

1.3.1.2 Power Supply Pins

1, 2	7, 8, 12	V_{DDD}	I	5 V ± 5% digital supply voltage
5	14	GNDA1	I	0 V analog
7, 8	18, 19	V_{DDA1}	I	5 V ± 5% analog supply voltage
9	21	V_{REF}	O	VREF pin to buffer internally generated voltage with capacitor 100 nF vs GND
13	26	V_{DDA2}	I	5 V ± 5% analog supply voltage
16	30	GNDA2	I	0 V analog
23	41	GNDD	I	0 V digital

1.3.1.3 IOM®-2 Pins

31	53	DCL	I/O	Data clock: Clock range 512 kHz to 4096 kHz, depending on mode.
30	52	FSC	I/O	Frame synchronization clock: The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
26	45	DIN	I	Data in: Input of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in LT and DU (data upstream) in NT-applications.
27	46	DOUT	O	Data out: Output of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in NT and DU (data upstream) in LT-applications.

1.3.1.4 IOM®-2 Control Pins

17	32	DOD	I	DOUT open drain: Select open drain with DOD = (1) (external pull-up resistor required) and tristate with DOD = (0).
34	57	MTO	I	Monitor procedure time-out: Disables the internal 6 ms monitor time-out when set to (1). Internal pull-down resistor.

1.3.1.5 U-Interface Pins

15	29	AIN	I	Differential U-Interface input: Connect to hybrid.
14	28	BIN	I	Differential U-Interface input: Connect to hybrid.
6	16	AOUT	O	Differential U-Interface output: Connect to hybrid.
4	13	BOUT	O	Differential U-Interface output: Connect to hybrid.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

1.3.1.6 Power Controller Pins

44	5	PCD0	I/O	Data bus of power controller interface: LSB. Do not connect if not used. Internal pull-up.
43	4	PCD1	I/O	Data bus of power controller interface: Do not connect if not used. Internal pull-up.
42	3	PCD2	I/O	Data bus of power controller interface: MSB. Do not connect if not used. Internal pull-up.
39	62	PCA0	I/O	Address bus of power controller interface.
38	61	PCA1	I/O	Address bus of power controller interface.
41	2	$\overline{\text{PCRD}}$	I/O	Power controller interface read request: Low active.
40	1	$\overline{\text{PCWR}}$	I/O	Power controller interface write request: Low active.
19	36	INT	I/O	Interrupt: Change-sensitive. After a change of level has been detected the C/I code “INT” will be issued on IOM®-2. Tie to GND during operation.
37	60	DISS	O	Disable power supply: Different function in LT and NT modes. LT: the DISS pin is set to (1) with the C/I command “LTD”. NT: the DISS pin is set to (1) after receipt of MON-0 LBBD in auto-mode.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
21	38	PS1	I	Power status (primary): Different function in LT- and NT-mode. LT: (1) indicates that the remote power is switched off. (1) on PS1 results in C/I message “HI”. Clamp to low if not used. NT: (1) indicates that prim. Power supply is OK. The pin value is identical to the overhead bit “PS1” value.
22	39	PS2	I	Power status (secondary): Different function in LT- and NT-mode. LT: the current feed value is transmitted (8 bit serially) from a power controller. Read the value with MON-8 “RPFC”. NT: (1) indicates that secondary power supply is OK. The pin value is identical to the overhead bit “PS2” value.

1.3.1.7 Clocks

10	22	XOUT	O	Crystal OUT: 15.36-MHz crystal is connected. Suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. Leave open if not used.
11	23	XIN	I	Crystal IN: External 15.36-MHz clock signal or 15.36-MHz crystal is connected. In case a crystal is connected, suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
32	**54**	**CLS**	**O**	Clock Signal: In the NT-Modes this clock is synchronized to U-Interface. Used to synchronize external PLL or to clock S-Interface devices. In the NT-, NT-Auto, COT- and TE-, modes a 7.68 MHz clock is provided on this pin. In the PBX- and in the LT-RP modes a 512 kHz is provided. **In the NT-RP mode a 15.36 MHz clock is provided (not synchronized to U-Interface).** In the LT- mode the clock on CLS is not defined.

1.3.1.8 Miscellaneous Pins

Not available	**64**	**ICE**	**I**	**IOM®-2 Clocks Enable** **0: no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. Pin DOUT is 'floating'.** **1: Behavior as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins.** **Due to the 100kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected.** **This pin can be overridden by the bit ADF2:ICEC. For more information see "IOM®-2 Clock Disable", page 37.** **Internal pull up.**

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
Not available	**42**	**SG**	**O**	**Stop/Go Bit Status Pin** **Gives the status of the S/G bit in TE mode if the S/G bit control function is being used, see "Indication of S/G Bit Status on Pin SG", page 47 for details.**

1.3.1.9 Test Pins

29	51	TP	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.
20	37	TP1	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.

1.3.2 Pin Definition in Microprocessor Mode

(i.e. PMODE="1")

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

1.3.2.1 Mode Selection Pins

12	24	PMODE	I	Processor Interface Enable: Setting PMODE to "1" enables the Processor Interface (Multiplexed, demultiplexed and serial modes). Tie to GND or do not connect to select stand alone mode. Internal pull down.
28	47	$\overline{\text{RESQ}}$	I	**Reset:** Low active, must be (0) at least for **30 ns**. The reset in the LT and NT-PBX mode will be carried out only after the on IOM®-2 clock have been applied to the IEC-Q. Tie to VDD if not used.

1.3.2.2 Data, Address and µP Selection Pins

24	43	SMODE A0	I	Serial mode pin: SMODE = 1 selects serial mode, SMODE = 0 enables the multiplexed mode. Address bus pin (Demultiplexed mode)
36	59	CDIN A1 not used	I	Controller Data In (Serial mode): CCLK determines the data rate. Address bus pin (Demultiplexed mode). (Multiplexed mode) tie to GND.
35	58	CDOUT	I/O	Controller Data Out (Serial mode): CCLK determines the data rate. CDOUT is "high Z" if no data is transmitted.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
35	58	A2 not used	I/O	Address bus pin (Demultiplexed mode). (Multiplexed mode) tie to GND.
33	55	not used A3 not used	I	(Serial mode) tie to GND. Address bus pin (Demultiplexed mode). (Multiplexed mode) tie to GND.
44	5	not used D0 AD0	I/O	(Serial mode) tie to GND. Data bus pin (Demultiplexed mode) Address/Data bus pin (Multiplexed mode)
43	4	not used D1 AD1	I/O	(Serial mode) tie to GND. Data bus pin (Demultiplexed mode) Address/Data bus pin (Multiplexed mode)
42	3	not used D2 AD2	I/O	(Serial mode) tie to GND. Data bus pin (Demultiplexed mode) Address/Data bus pin (Multiplexed mode)
41	2	not used D3 AD3	I/O	(Serial mode) tie to GND. Data bus pin (Demultiplexed mode) Address/Data bus pin (Multiplexed mode)
40	1	not used D4 AD4	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
39	62	not used D5 AD5	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)
38	61	not used D6 AD6	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)
25	44	not used D7 AD7	I/O	(Serial mode) tie to GND. Data bus pin (demultiplexed modes) Address/Data bus pin (Multiplexed mode)

1.3.2.3 µP Control Pins

19	36	$\overline{INT}$	I/O	Interrupt line (Multiplexed, demultiplexed and serial modes): Low active.
3	10	$\overline{CS}$	I	Chip select (Multiplexed, demultiplexed and serial modes): Low active.
17	32	not used WR R/$\overline{W}$	I	(Serial mode) tie to GND. Write (Siemens/Intel multiplexed and demultiplexed modes): indicates a write operation, active low. Read/Write (Motorola demultiplexed mode): indicates a read (high) or write (low) operation.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
34	57	not used	I	(Serial mode) tie to GND.
		RD		Read (Siemens/Intel multiplexed and demultiplexed modes): indicates a read operation, active low.
		DS		Data Strobe (Motorola demultiplexed mode): indicates a data transfer, active low.
20	37	CCLK	I	Controller data clock (Serial mode): Shifts data from or to the device.
		ALE		Address Latch Enable (Demultiplexed mode): ALE tied to GND selects the Siemens/Intel type. ALE tied to VDD selects the Motorola type.
		ALE	I	Address Latch Enable (Multiplexed mode): In the Siemens/Intel µP interface modes a high indicates an address on the AD0..3 pins which is latched with the falling edge of ALE.

1.3.2.4 Power Supply Pins

1, 2	7, 8, 12	V_{DDD}	I	5 V ± 5% digital supply voltage
5	14	GNDA1	I	0 V analog
7, 8	18, 19	V_{DDA1}	I	5 V ± 5% analog supply voltage
9	21	V_{REF}	O	VREF pin to buffer internally generated voltage with capacitor 100 nF vs GND
13	26	V_{DDA2}	I	5 V ± 5% analog supply voltage
16	30	GNDA2	I	0 V analog
23	41	GNDD	I	0 V digital

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

1.3.2.5 IOM®-2 Pins

31	53	DCL	I/O	Data clock: Clock range 512 kHz to 4096 kHz, depending on mode.
30	52	FSC	I/O	Frame synchronization clock: The start of the B1-channel in time-slot 0 is marked. FSC = (1) for one DCL-period indicates a superframe marker. FSC = (1) for at least two DCL-periods marks a standard frame.
26	45	DIN	I	Data in: Input of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in LT and DU (data upstream) in NT-applications.
27	46	DOUT	O	Data out: Output of IOM®-2 data synchronous to DCL-clock. Corresponds to DD (data downstream) in NT and DU (data upstream) in LT-applications.

1.3.2.6 U-Interface Pins

15	29	AIN	I	Differential U-Interface input: Connect to hybrid.
14	28	BIN	I	Differential U-Interface input: Connect to hybrid.
6	16	AOUT	O	Differential U-Interface output: Connect to hybrid.
4	13	BOUT	O	Differential U-Interface output: Connect to hybrid.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function

1.3.2.7 Power Controller Pins

21	38	PS1	I	Power status (primary): Different function in LT- and NT-mode. LT: (1) indicates that the remote power is switched off. (1) on PS1 results in C/I message “HI”. Clamp to low if not used. NT: (1) indicates that primary power supply is OK. The pin value is identical to the overhead bit “PS1” value.
22	39	PS2	I	Power status (secondary): Different function in LT- and NT-mode. LT: the current feed value is transmitted (8 bit serially) from a power controller. Read the value with MON-8 “RPFC”. NT: (1) indicates that secondary power supply is OK. The pin value is identical to the overhead bit “PS2” value.

1.3.2.8 Clocks

10	22	XOUT	O	Crystal OUT: 15.36-MHz crystal is connected. Suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout. Leave open if not used.
11	23	XIN	I	Crystal IN: External 15.36-MHz clock signal or 15.36-MHz crystal is connected. In case a crystal is connected, suitable load capacitances should be connected in parallel. Their value depends on the crystal chosen and board Layout.

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
32	**54**	**CLS**	**O**	Clock Signal: In the NT-Modes this clock is synchronized to U-Interface. Used to synchronize external PLL or to clock S-Interface devices. In the NT-, NT-Auto, COT- and TE-, modes a 7.68 MHz clock is provided on this pin. In the PBX- and in the LT-RP modes a 512 kHz is provided. **In the NT-RP mode a 15.36 MHz clock is provided (not synchronized to U-Interface).** In the LT- mode the clock on CLS is not defined.
37	60	MCLK	O	Microprocessor clock output (Multiplexed, demultiplexed and serial modes): provided with four programmable clock rates: 7.68 MHz, 3.84 MHz, 1.92 MHz and 0.96 MHz.

1.3.2.9 Miscellaneous Pins

18	35	$\overline{\text{RST}}$	O	Reset output (Multiplexed, demultiplexed and serial modes): Low active.
Not available	**42**	**SG**	**O**	**Stop/Go Bit Status Pin** **Gives the status of the S/G bit in TE mode if the S/G bit control function is being used, see "Indication of S/G Bit Status on Pin SG", page 47 for details.** **In all other modes the SG pin in set to “1”.**

Pin No. P-LCC-44	Pin No. T-QFP64 M-QFP64	Symbol	Input (I) Output (O)	Function
Not available	**64**	**ICE**	**I**	**IOM®-2 Clocks Enable** **0: no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. Pin DOUT is 'floating'.** **1: Behavior as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins.** **Due to the 100kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected.** **This pin can be overridden by the bit ADF2:ICEC. For more information see "IOM®-2 Clock Disable", page 37.** **Internal pull up.**

1.3.2.10 Test Pin

29	51	TP	I	Test pin: Not available to user. Do not connect. Internal pull-down resistor.

1.4 Microprocessor Bus Interface (Overview)

The table below gives an overview of the different microprocessor bus modes.

Table 1 Microprocessor Bus Interface

Pin Number		Stand Alone Mode	Symbol in Processor Mode			
P-LCC-44	T-QFP-64 and M-QFP-64		Siemens/ Intel multiplexed	Siemens/ Intel demultiplex.	Motorola demultiplex.	Serial
12	24	PMODE = 0	PMODE = 1			
44	5	PCD0	AD0	D0	D0	n.c.
43	4	PCD1	AD1	D1	D1	n.c.
42	3	PCD2	AD2	D2	D2	n.c.
41	2	$\overline{\text{PCRD}}$	AD3	D3	D3	n.c.
40	1	$\overline{\text{PCWR}}$	AD4	D4	D4	n.c.
39	62	PCA0	AD5	D5	D5	n.c.
38	61	PCA1	AD6	D6	D6	n.c.
25	44	LT	AD7	D7	D7	n.c.
19	36	INT	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$	$\overline{\text{INT}}$
24	43	BURST	SMODE=0	A0	A0	SMODE=1
36	59	TS2	n.c.	A1	A1	CDIN
35	58	TS1	n.c.	A2	A2	CDOUT
33	55	TS0	n.c.	A3	A3	n.c.
20	37	TP1	ALE	ALE=0	ALE=1	CCLK
34	57	MTO	$\overline{\text{RD}}$	$\overline{\text{RD}}$	$\overline{\text{DS}}$	n.c.
17	32	$\overline{\text{DOD}}$	$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{W}}$	n.c.
3	10	$\overline{\text{TSP}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$	$\overline{\text{CS}}$
37	60	$\overline{\text{DISS}}$	$\overline{\text{MCLK}}$			
18	35	$\overline{\text{AUTO}}$	$\overline{\text{RST}}$			

1.5 System Integration

The PEB/F 2091 can be combined with a variety of other devices to fit in numerous applications. Some of them are described in the User's Manual 02.95 of the PEB 2091 Version 4.3, page 35 ff. Version 5.3, with its new features, offers various possibilities to achieve significant cost and power reduction in some applications, as well as introducing new applications. Some of these possibilities are sketched briefly below.

1.5.1 Repeater

New repeater features have been implemented in this version:

- A wake-up tone from downstream is indicated directly on DOUT. No special circuit for wake tone detection is needed any more. See "Upstream Wake-Up Indication in the LT Repeater Mode", page 35.
- A master clock is delivered on pin CLS in the NT Repeater mode. This clock will be available in both power-up and power-down states. This allows reducing power consumption to a minimum in power down. Furthermore, PLL architecture can be simplified. See "Master Clock on Pin CLS in NT Repeater Mode", page 36.
- The undervoltage detection function can be used to detect power supply level drops on the board and reduce external reset circuitry. See "Undervoltage Detection", page 33.

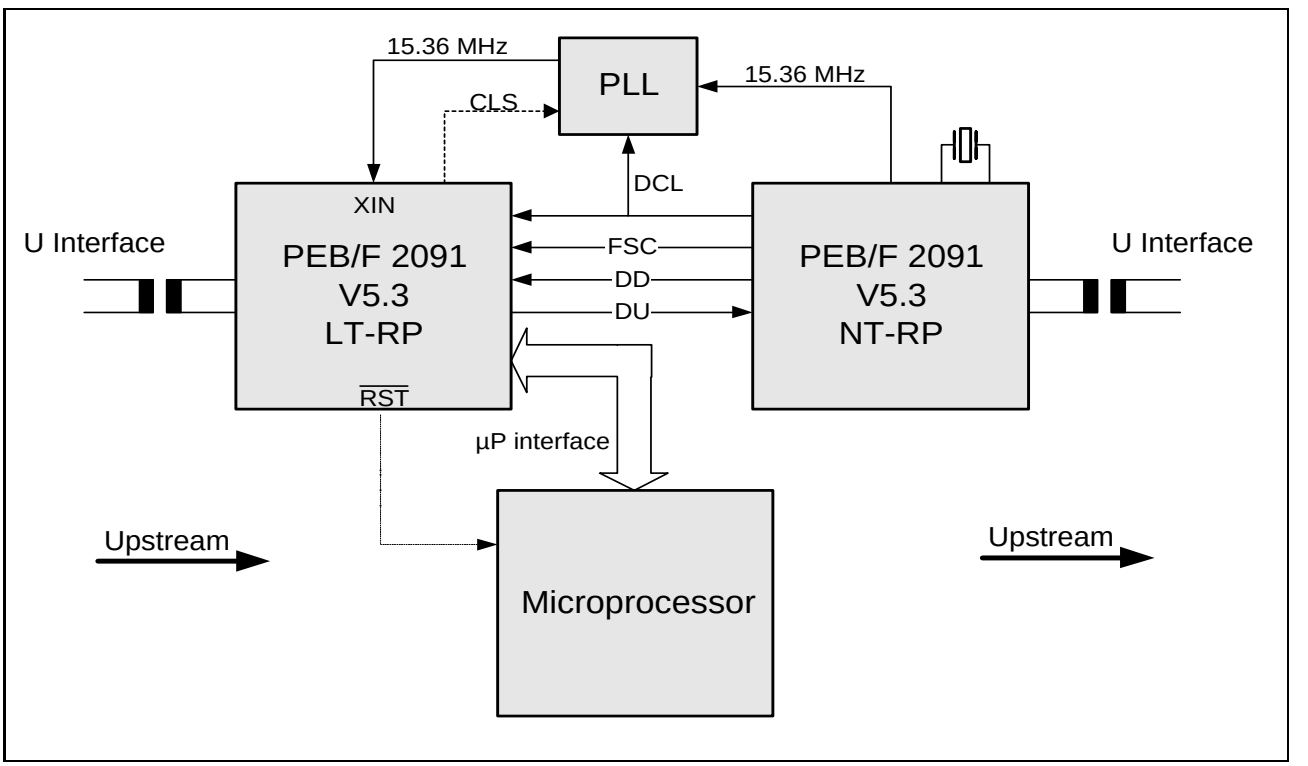


Figure 2 Architecture of Repeater Application

1.5.2 Wireless Local Loop

In Figure 3 a possible Base Station configuration is sketched. The PEB/F 2091 Version 5.3 is designed to suit to PEB 24911/PEB 24902 (DFE-Q/AFE) in the linecard, and to the PMB 2727 (Multichannel Burst Mode Controller) in the base station. The two new features of Version 5.3 concerning the Stop/Go function (see "Selectable Polarity of S/G Bit", page 40, and "Indication of S/G Bit Status on Pin SG", page 47) allow flexible and cost effective construction of Base Station boards without the need for external circuitry for S/G bit evaluation. Like the S/G bit, the S/G pin can be used for transmitting a common synchronization pulse to the burst mode controller. Moreover the undervoltage detection feature (see "Undervoltage Detection", page 33) can be used to simplify control of power supply level on the board.

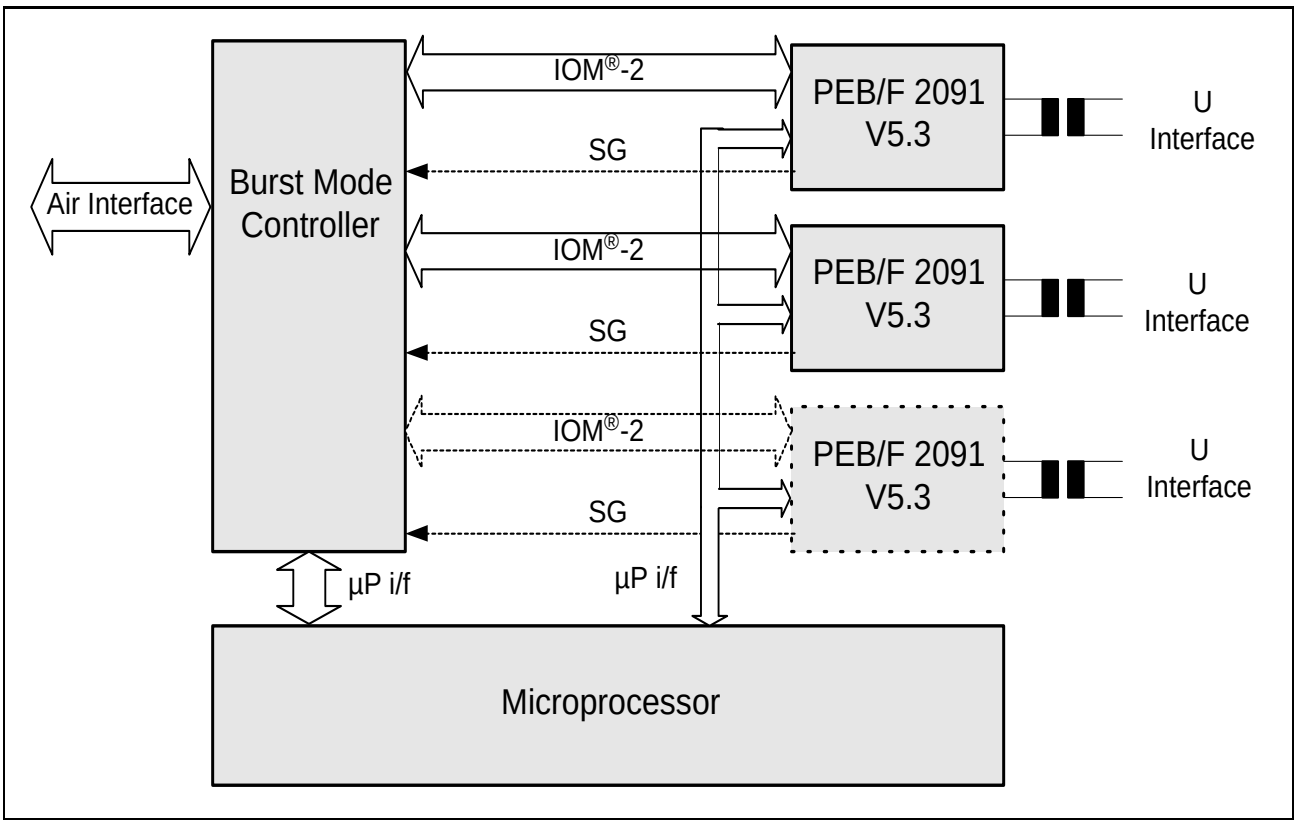


Figure 3 Architecture of the Wireless Local Loop Base Station

1.5.3 Dual Mode U and S Terminals and PC Cards

In this version of PEB/F 2091 the IOM®-2 interface can be set to tristate when the IOM®-2 master mode is used. This allows introduction of Dual Mode terminals and PC adapter cards using e.g. IPAC without external gluelogic. See 2.6, page 37 for details.

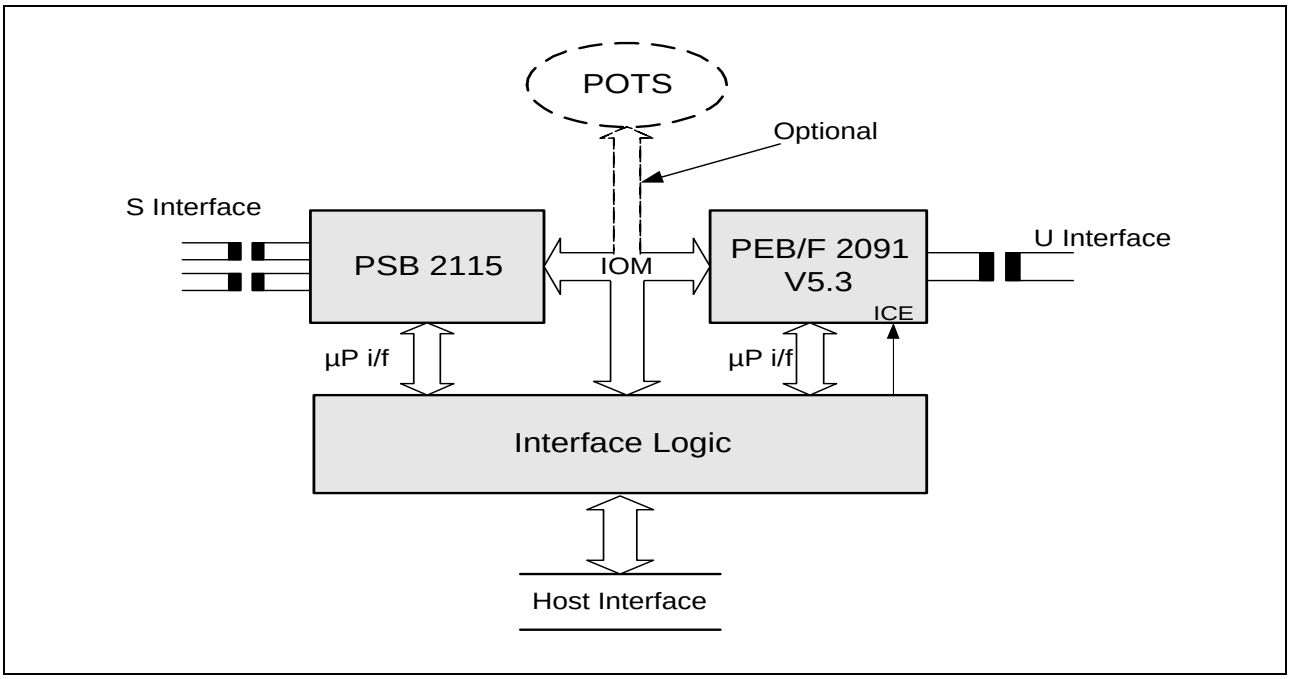


Figure 4 Dual Mode PC Adapter Card

2 Functional Description

2.1 Control of Single Bits Indications

The received Single Bits of the U Interface (see page 30 for definition) have to be forwarded via MON-2 messages to the controller unit[1)] to allow higher layer evaluation of this data. In all PEB/F 2091 versions up to Version 5.2 this Single Bits will be forwarded in the following way:

- In Repeater modes a MON-2 message containing all 12 Single Bits will be issued every 12 ms (see User's Manual 02.95 of the PEB 2091 Version 4.3, page 129).
- In all other modes the conditions for issuing the MON-2 message, containing all 12 Single Bits, depend on the version used:
  In Version 5.1: A MON-2 is issued if the polarity of at least one of the Single Bits, other than FEBE, has been changed (see corresponding point of Errata Sheet of the PEB/F 2091 V5.1).
  In all other versions: The MON-2 message will be issued only if in addition no CRC violations have been detected in the completed last two superframes (for details, see User's Manual 02.95 of the PEB 2091 Version 4.3, page 129).

Version 5.3 has been improved to allow almost free control of the conditions for Single Bits verification.
For compatibility, Version 5.3 can be configured to function either like Version 5.1 or alternatively like all other versions[2)].

Furthermore, verification of Single Bits changes can be chosen to be controlled by a triple last look processor. Choosing this filtering method will imply that a change in a Single Bit will be issued via MON-2 message only if an identical bit value has been received for three consecutive superframes. This setting for the M4 bits complies with ANSI T1.601 without need for further software efforts. Note that this is the default setting for the M4 bits in all non repeater modes (see Table 4). Note also that this filtering method setting can be combined with the CRC filtering method.

In addition, verification of the M4 bits is completely independent of verification of bits M51, M52 and M61. This allows using the M4 bits in compliance with ANSI T1.601 (Triple Last Look), and still retain the freedom to use bits M51, M52 an M61 for other purposes (i.e. control functions, or even very low rate data transmission).

Control of the Single Bits is mode independent. This allows more flexibility, e.g. in repeater applications.

Selection of the filtering method is controlled via MON-8 messages. It is therefore available in stand alone mode as well as in µP mode.

1 Upstream in the LT modes and downstream in the NT modes
2 Note however that the default setting of Version 5.3 is different than all previous versions. The default setting of Version 5.3 is given in Table 4, page 32 and Table 5, page 32.

Definitions

As selection of the verification method for Single Bits is done via MON-8 messages, it is convenient to recall the format of MON-8 messages, which is given in Table 2 below. For more details on MON-8 messages, refer to User's Manual 02.95 of the PEB 2091 Version 4.3, page 129 ff.

Table 2 Format of MON-8-Messages

1. Byte		2. Byte
1 0 0 0	r | 0 0 0	D7 D6 D5 D4 D3 D2 D1 D0
MON-8	Register | Addr.	Local Command (Message/Data)

r: Register address – 0 = local function register
– 1 = internal register

D0…7 Local command – 00 … FF_H = local function code
– 00 … FF_H = internal register address

The MON-8 commands used to control the verification method are all local functions. The Register bit "r" should therefore be set to "0" in this case.

The Single Bits in the U frame are defined to be bits M41 to M48 (eight bits) in addition to the three bits M51, M52 and M61 and the FEBE bit. These bits are highlighted in Table 3, which gives the general structure of the U frame. In the following section Bits M41 to M48 are referred to as *M4 Bits***.** Bits M51, M52 and M61 are referred to as *Additional Overhead Bits.*

Table 3 U-Frame Structure

		Framing	2B + D	Overhead Bits (M1 – M6)					
	Quat Positions	1 – 9	10 – 117	118	118	119	119	120	120
	Bit Positions	1 – 18	19 – 234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B + D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B + D	EOCa1	EOCa2	EOCa3	ACT/ ACT	1	1
	2	SW	2B + D	EOC d/m	EOCi1	EOCi2	DEA / PS1	1	FEBE
	3	SW	2B + D	EOCi3	EOCi4	EOCi5	1/ PS2	CRC1	CRC2
	4	SW	2B + D	EOCi6	EOCi7	EOCi8	1/ NTM	CRC3	CRC4
	5	SW	2B + D	EOCa1	EOCa2	EOCa3	1/ CSO	CRC5	CRC6
	6	SW	2B + D	EOC d/m	EOCi1	EOCi2	1	CRC7	CRC8
	7	SW	2B + D	EOCi3	EOCi4	EOCi5	UOA / SAI	CRC9	CRC10
	8	SW	2B + D	EOCi6	EOCi7	EOCi8	AIB / NIB	CRC11	CRC12
2,3…									
						LT- to NT dir. >	/	< NT- to LT dir.	

– ISW Inverted Synchronization Word (quad): – 3 – 3 + 3 + 3 + 3 – 3 + 3 – 3 – 3
– SW Synchronization Word (quad): + 3 + 3 – 3 – 3 – 3 + 3 – 3 + 3 + 3
– CRC Cyclic Redundancy Check
– EOC Embedded Operation Channel

a = address bit
d/m = data / message bit
i = information (data / message)

– ACT Activation bit — ACT = (1) –> Layer 2 ready for communication
– DEA Deactivation bit — DEA = (0) –> LT informs NT that it will turn off
– CSO Cold Start Only — CSO = (1) –> NT-activation with cold start only
– UOA U-Only Activation — UOA = (0) –> U-only activated
– SAI S-Activity Indicator — SAI = (0) –> S-interface is deactivated
– FEBE Far-end Block Error — FEBE = (0) –> Far-end block error occurred
– PS1 Power Status Primary Source — PS1 = (1) –> Primary power supply OK
– PS2 Power Status Secondary Source — PS2 = (1) –> Secondary power supply OK
– NTM NT-Test Mode — NTM = (0) –> NT busy in test mode
– AIB Alarm Indication Bit — AIB = (0) –> Interruption (according to ANSI)
– NIB Network Indication Bit — NIB = (1) –> no function (reserved for network use)

Verification Control for M4 Bits

Table 4 gives the available settings for M4 Bits filtering via MON-8 command.

Table 4 Setting Filtering Method for M4 Bits

Code D7-D0 (Bin)[1)]	Symbol	Function
1000 1110	TLL (Default, not RP)	A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look. This is the default setting after reset in all non repeater modes
1000 1101	CRC (Default, RP)	A change in at least one of the M4 Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one. This is the default setting after reset in the repeater modes
1000 1111	TLL, CRC	A change in at least one of the M4 Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
1000 1100	On Change	Every change in at least one of the M4 Bits will be passed via MON-2

1) see Table 2 for definition

Verification Control for Additional Overhead Bits

Table 5 gives the available settings for Additional Overhead Bits (M51, M52, M61) filtering via MON-8 command.

Table 5 Setting Filtering Method for Additional Overhead Bits

Code D7-D0 (Bin)[1)]	Symbol	Function
1000 1010	TLL (Default, not RP)	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look. This is the default setting after reset in all non repeater modes
1000 1001	CRC (Default, RP)	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only if the CRC is valid for the last two superframes, not including the current one. This is the default setting after reset in the repeater modes

Table 5 Setting Filtering Method for Additional Overhead Bits

Code D7-D0 (Bin)[1)]	Symbol	Function
1000 1011	TLL, CRC	A change in at least one of the Additional Overhead Bits will be passed via MON-2 only after valid triple last look, and if the CRC is valid for the last two superframes, not including the current one
1000 1000	On Change	Every change in at least one of the Additional Overhead Bits will be passed via MON-2

1) see Table 2 for definition

Reset behavior

MON-2 messages will be issued only if the receiver is synchronized. This is done to avoid meaningless MON-2 messages if data transmission is not synchronized.

In other words, MON-2 messages will be issued **only** in the following states (page numbers refer to User's Manual 02.95 of the PEB 2091 Version 4.3):

*In **LT Mode** (page 165):* "Line Active", "Pend. Transparent", "S/T Deactivated", "Pend. Deactivation" and "Transparent".

*In **NT Mode** (page 175):* "Synchronized 1", "Synchronized 2", "Wait for Act", "Transparent", "ERROR S/T", "Pend. Deact. S/T", "Pend. Deact. U" and "Analog Loop Back".

*In **LT-Repeater Mode** (page 185):* "Pend. Transparent", "Transparent", "Pend. Deactivation".

*In **NT-Repeater Mode** (page 186):* "Synchronized", "Transparent", "ERROR", "Pend. Deact." and "Analog Loop Back".

Mode setting via MON-8 will be reset only if the "Test" state is entered (see User's Manual 02.95 of the PEB 2091 Version 4.3, pages 165, 175, 185 and 186), e.g. after Hardware Reset, Software Reset or Power-On Reset.

2.2 Undervoltage Detection

Note: This feature is only available in the microprocessor mode (PMODE = "1").

The undervoltage detector is enabled by setting the ADF:UVD bit to "1", see "ADF-Register", page 51. Note that the default setting of this bit after power on will be "1", i.e. the undervoltage detection feature will be activated. It activates the reset signal if the supply voltage drops below the threshold U_L (typically 4.21 V, see Figure 5 below and "Undervoltage Detection Timing", page 59).

It also acts as power on reset by creating a reset pulse on pin $\overline{RST}$ if the supply voltage rises above U_H (typically 4.30 V). It then stays inactive until the supply voltage drops again below the threshold level U_L (see also "Power On Reset (POR)", page 34, for more information).

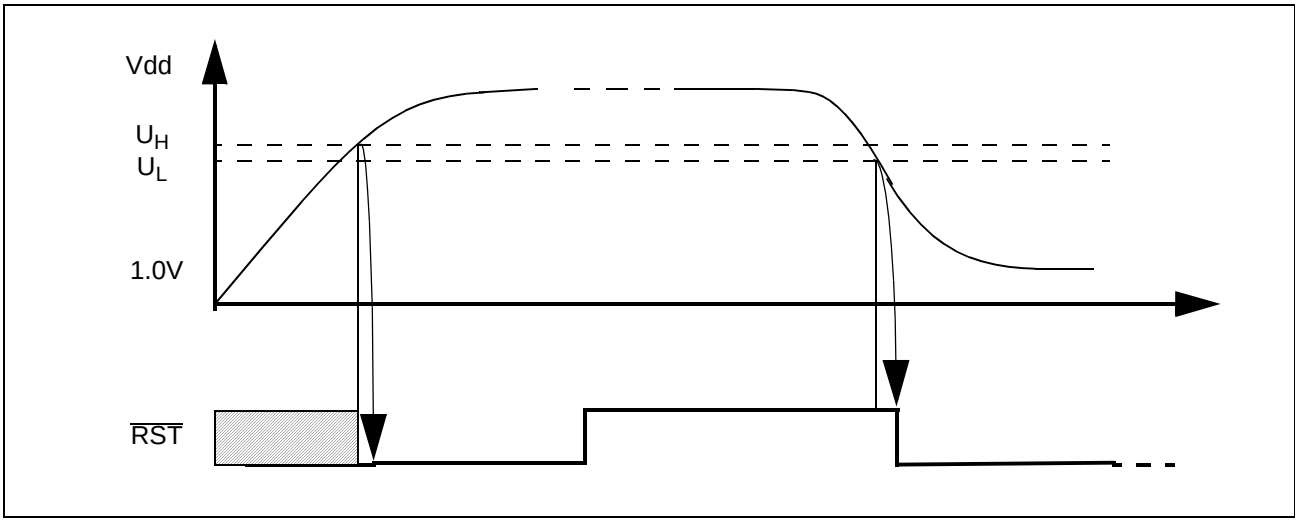


Figure 5 UVD Control of Pin $\overline{RST}$

While the supply voltage is below threshold U_L, the microcontroller clock MCLK is stopped and the MCLK output remains low[1)]. If the supply voltage falls below threshold U_L, the clock is stopped immediately which may result in one shorter high period of the clock signal. For dynamic properties, see "Undervoltage Detection Timing", page 59.

Important: For power saving reasons, this function is not available in power down. Still pin $\overline{RST}$ will not float in this state and the power on reset function is still available, see 2.3 below.

2.3 Power On Reset (POR)

Version 5.3 of the PEB/F 2091 is equipped with a POR feature. During power on or power off, an internal reset will be generated if the POR threshold (between 2.5 V and 4.5 V) is reached. This is independent of mode setting. However there is a difference in reset duration and indication between the stand alone mode and the microprocessor mode.
In stand alone mode this internal reset (POR) will be fully equivalent to the hardware reset generated by activating the pin RESQ. The duration of the reset pulse will be some value between 10 and 30 µs.

1 The behavior of the microcontroller clock MCLK is not specified below the supply voltage of 4.0 Volt.

The processor mode (PMODE="1") has two additional properties:
- The POR will be given on the pin $\overline{RST}$
- The POR will also reset the register STCR, as described in Delta Sheet of the PEB 2091 Vesion 5.1, page 21.

The duration of POR in this mode will be some value between 60 and 70 ms.

2.4 Upstream Wake-Up Indication in the LT Repeater Mode

In repeater applications the IOM®-2 clocks are usually delivered by the NT repeater (see User's Manual 02.95 of the PEB 2091 Version 4.3, page 43). In power down the IOM®-2 clock will be shut down. During power down the reception of a wake up tone from down stream will therefore not be indicated on C/I channel in up stream direction. In versions 5.1 and 5.2 of the IEC-Q the IOM®-2 interface should be held active or a special circuit should be implemented directly on the U interface to detect the wake up tone from down stream. The first solution will result in high power consumption of the repeater, the second one is not cost effective.

Version 5.3 of the IEC-Q is equipped with an internal wake up detection function which doesn't depend on IOM®-2[1)]. In the "Deactivated" state of the LT Repeater mode the pin DOUT will be clamped to "0" if a wake tone from down stream is detected and if no Monitor channel command is active or pending (in both up and down stream directions)[2)]. This allows connecting pin DOUT of the LT repeater directly to pin DIN of the NT repeater, and activation initiated by the TE will be carried out without restrictions, as Figure 6 below and the example thereafter show

1 Note that the 15.36 MHz master clock will still be required. Version 5.3 provides such a clock on pin CLS in the NT repeater mode. Refer to "Master Clock on Pin CLS in NT Repeater Mode", page 36.

2 To achieve this, all Monitor channel commands and indications of the LT Repeater should be completed before the NT Repeater enters the power down state.

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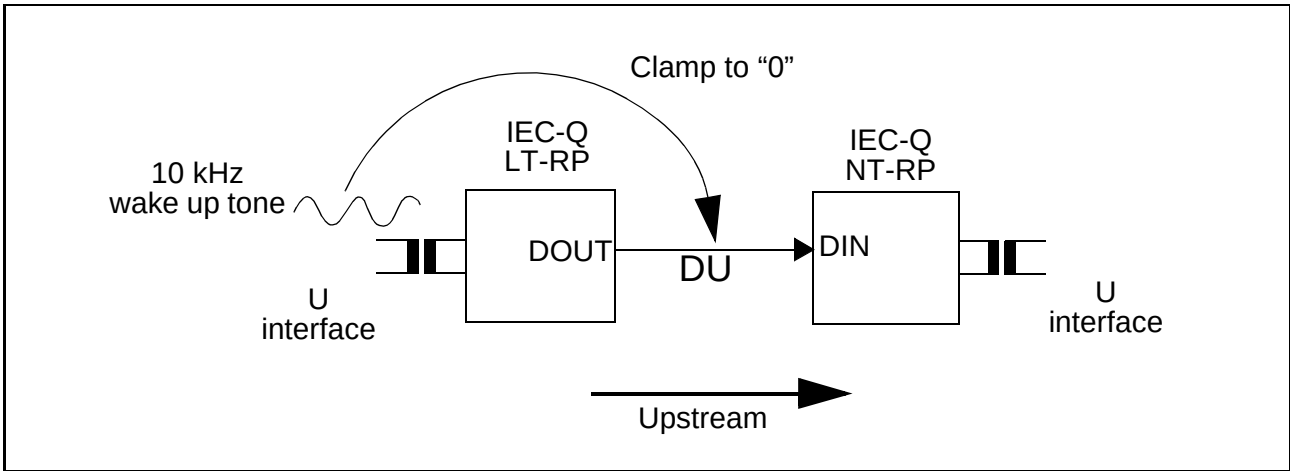


Figure 6 Wake Up Indication in Repeater Power Down

Example: Repeater activation initiated by the terminal

- NT and LT repeater are in power down. No Monitor Channel command is active or pending.
- A wake tone is received from down stream.
- The LT repeater pulls DOUT low which is detected by the NT repeater on DIN.
- The NT repeater activates the IOM®-2 interface (see User’s Manual 02.95 of the PEB 2091 Version 4.3, page 186).
- The LT repeater moves to the Awake state and DOUT will be released to indicate AR on the C/I Channel. Note that the C/I command DC must be given on DIN (see User’s Manual 02.95 of the PEB 2091 Version 4.3, page 185).
- Activation takes now place as described in User’s Manual 02.95 of the PEB 2091 Version 4.3, page 157.

2.5 Master Clock on Pin CLS in NT Repeater Mode

In repeater applications the device used as LT repeater is synchronized to the upstream unit through the device used as NT repeater. To achieve this, a PLL is required to provide a synchronized 15.36 MHz master clock to the LT repeater (see User’s Manual 02.95 of the PEB 2091 Version 4.3, page 53). If versions 5.1 or 5.2 of PEB/F 2091 are used the PLL will need a 15.36 MHz crystal or a special circuitry to generate this master clock. Moreover, in power down this PLL will be kept active to provide a 15.36 MHz master clock for the board.

Version 5.3 has been improved to provide an **un**sychronized 15.36 MHz master clock on pin CLS in NT-RP mode. This can be used by the PLL to generate a sychronized master

clock e.g. for the LT repeater. This clock on CLS will also be provided in power down, which makes it possible to switch the PLL off in power down to reduce power consumption of the repeater. Note that a 15.36 MHz master clock must be supplied to the LT repeater in power down in order to maintain its ability of detecting awake tones.

See also "Timing Properties of CLS in NT Repeater Mode", page 60.

2.6 IOM®-2 Clock Disable

Note This feature is only available in the master mode of the IEC-Q, i.e. modes in which the IOM®-2 clocks are delivered by the IEC-Q

Applications in which the IEC-Q is not the only potential IOM®-2 clock master on the board have to deal with IOM®-2 clock conflicts during and after reset. Among these applications are dual-mode S- or U-terminals and circuits (see "Dual Mode U and S Terminals and PC Cards", page 28). Typical applications would include the ISAC-S TE (PSB 2186) or the IPAC (PSB 2115) in TE mode. Both devices output FSC and DCL during and after reset.
The PEB/F 2091 V5.3 in the 64 pin packages (T-QFP-64 or M-QFP-64) has a pin (pin 64, ICE) which allows to enable or disable the IOM®-2-clocks and the data-lines. It is possible to change the status of pin ICE without the need of a reset signal being applied. In µP-mode the status of pin ICE can be overridden by bit ADF2:ICEC. The value of pin ICE and the bit-value are EXORed (see Table 6 below).

This function can also be controlled in the P-LCC-44 package in the microprocessor mode (PMODE = "1") by bit ADF2:ICEC, see "ADF2-Register", page 52.

The following table gives an overview of the control mechanisms of this function in different settings. The terms “Idle” and “active” of the IOM®-2 interface in Table 6 are defined as follows:

Idle means that no FSC and DCL clocks are output. Clocks may be applied to pins FSC and DCL. However, they are ignored by the IEC-Q. Data on pin DIN is ignored. However, the internal DIN signal will be clamped to “1”. Pin DOUT is ’floating’ (same as ’DOUT not in Slot Position’, in the User’s Manual 02.95 of the PEB 2091 Version 4.3, page 49).

Active means that the behavior is as in former versions of the IEC-Q. The IOM®-2 clocks FSC and DCL are output on the corresponding pins.
Due to the 100kOhm pull-up resistor this is the default configuration after reset if pin ICE is not connected.

Table 6 IOM®-2 Clock Disable Overview (Only in the IOM®-2 Master Modes)

Operation Mode	Package	ADF2:ICEC bit polarity	ICE pin polarity	IOM®-2 interface
Stand alone mode (PMODE= “0” or unconnected)	P-LCC-44	Not available	Not available	Active
	M-QFP-64 or T-QFP-64	Not available	“1” or not connected	Active
			“0”	Idle
µP mode (PMODE=”1”)	P-LCC-44	“0” (default)	Not available	Active
		“1”		Idle
	M-QFP-64 or T-QFP-64	“0” (default)	“1” or not connected	Active
			“0”	Idle
		“1”	“1” or not connected	Idle
			“0”	Active

2.7 Superframe Marker Enable in µP Mode

Note: This function is only available in the µP-LT Modes.

In LT modes the superframe marker can be indicated by a short frame synchronization signal (FSC) of the IOM®-2 interface. If the high phase of FSC lasts one DCL period or less, the U interface frame will be reset and the Inverted Synchronization Word (ISW) will be inserted at the beginning of the next available basic frame (see User’s Manual 02.95 of the PEB 2091 Version 4.3, page 112). Consequently, spikes on the FSC might be unintentionally recognized as superframe marker by the IEC-Q. In most cases (> 85%) such a spike will introduce permanent high bit error rate. It is therefore very important to make sure, that no spikes on pin FSC could occur. However, cases were reported where spikes on pin FSC couldn’t be avoided.

Version 5.3 of the PEB/F 2091 offers a way to overcome this problem. Setting bit SFEN of register ADF2 (see "ADF2-Register", page 52) to “0” will disable the superframe marker function. This prevents spikes on FSC to trigger superframes. Bit errors caused by the additional FSC pulses will not last longer than 3 IOM®-2 frames.

Note Setting ADF2:SFEN to “0” will introduce the same behavior as Version 5.2 (refer to the corresponding point in Delta Sheet of the PEB/F 2091 V5.2). However, the value of ADF2:SFEN after reset will be “1”, which means that the superframe marker function is enabled by default and therefore compatible to all PEB/F 2091 versions up to 5.1.

2.8 Activation in the µP-NT Mode

Note This function is only available if the NT mode (pin LT="0") in conjunction with the microprocessor mode (PMODE = "1") are used. Note also that if the IOM®-2 clock disable mode is set (see chapter 2.6, page 37) activation in µP NT mode without IOM®-2 will not be possible.

In some NT and TE applications in the µP mode, the IOM®-2 interface is functionally not needed (e.g. inband signaling, some PC card applications etc.). In such applications versions 5.1 and 5.2 of the PEB/F 2091 needed the IOM®-2 interface or at least some kind of work around to be able to activate the device from the power down state (see for example "Activation of the PEB/F 2091 Version 5.1 in NT Mode by µC" of Errata Sheet of the PEB/F 2091 V5.1). This is due to the fact that in the deactivated state no IOM®-2 clocks are issued. In this case C/I codes written to the CIWU register will not reach the kernel of these versions of PEB/F 2091.

Version 5.3 has been improved and this restriction does not apply anymore. It is now possible to control the internal state of the pin DIN via the MSB of the CIWU register (see "CIWU-Register", page 53). Setting the SPU (software power up) bit to "0" in the NT mode will cause the DIN signal to be set internally to "0", regardless of the value of the pin DIN. Setting the SPU bit to "1", which is the default value after reset, will set the pin DIN transparent to the internal circuit, see Figure 7 below.

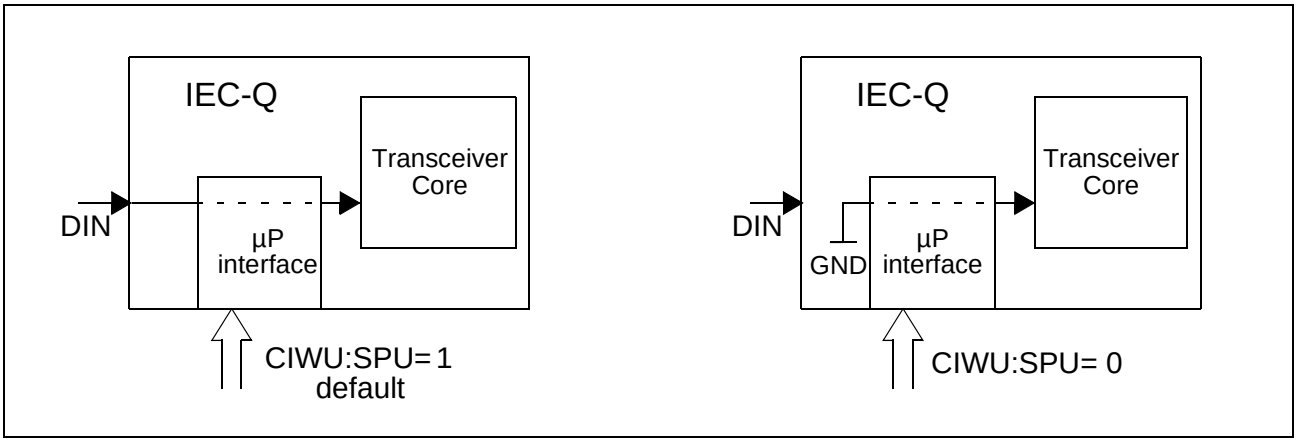


Figure 7 DIN Control via CIWU:SPU in NT µP Mode

Example for activation with µP

Assumption: The C/I-Channel is being controlled via µP (i.e., SWST:CI=1, see Delta Sheet of the PEB/F 2091 V5.1, page 51).

To activate the PEB/F 2091 V5.3 in NT-mode from power down without external control of the pin DIN the following procedure has to be used:

- Set the SPU bit to "0" in the CIWU-register (see "CIWU-Register", page 53)
- Write C/I-command "TIM" (0_H)

- Read the CIRU register after receiving the ISTA:CICU interrupt and verify that the CI code “PU” (7_H) has been indicated
- Write the C/I-command “AR” (8_H) in combination with setting the SPU bit to “1” in the CIWU register (see "CIWU-Register", page 53)

2.9 Selectable Polarity of S/G Bit

Note: This function is only available if the “Decentral HDLC-Processing via S/G Bit in NT-TE Mode” is used (refer to Delta Sheet of the PEB 2091 Vesion 5.1).

In µP Mode the Stop/Go bit on the IOM®-2 interface can be controlled by the register bits SWST:BS, SWST:SGL and ADF:CBAC (see Delta Sheet of the PEB 2091 Vesion 5.1, page 51-53). In versions 5.1 and 5.2, setting bit SWST:BS to “1” and SWST:SGL to “0” will set the S/G bit to “1” for a period of 4 IOM®-2 frames after receiving the EOC message 25_H. The S/G bit will then be automatically set back to “0” afterward.

However, in Wireless Local Loop applications the MBMC may need the S/G bit with inverse polarity, i.e. the S/G bit should be set to “0” for a period of 4 IOM®-2 frames if the EOC message 25_H is received. The S/G bit should be set automatically back to “1” afterwards.

In Version 5.3 the function of the S/G bit controller has been enhanced to fulfill the requirements of this application without the need for additional circuitry. The polarity of the S/G bits can now be controlled by the bit ADF:CBAC. Setting ADF:CBAC to “0”, which is the default value for this bit after reset, will cause Version 5.3 to behave like versions 5.1 and 5.2. Setting ADF:CBAC to “1” will cause the S/G bit to assume the inverse polarity, the way it is needed for Wireless Local Loop applications (for system architecture, see for example "Wireless Local Loop", page 27).

The following table and state machine give the detailed behavior of the complete Decentral HDLC-Processing function. Changes compared with versions 5.1 and 5.2 will be written in bold type style.

Table 7 Function of the Register Bits: SWST:BS, SWST:SGL and ADF:CBAC

SWST:BS	SWST:SGL	ADF:CBAC	Description (X is don’t care)
0	0	x	S/G bit always "0"
0	1	0	S/G bit always "1"
0	1	1	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit controls S/G-bit, upstream D-channel not affected

Table 7 Function of the Register Bits: SWST:BS, SWST:SGL and ADF:CBAC

SWST:BS	SWST:SGL	ADF:CBAC	Description (X is don't care)
1	**0**	**0**	**S/G bit set to "1" for 4 IOM®-2-frames with EOC 25_H received, automatically reset to "0" after that. This is the default setting of ADF:CBAC after reset.**
1	**0**	**1**	**S/G bit set to "0" for 4 IOM®-2-frames with EOC 25_H received, automatically reset to "1" after that**
1	1	0	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit not read by IEC-Q V 5.3
1	1	1	S/G bit set to "1" continuously with EOC 25_H received, reset to "0" with EOC 27_H received BAC bit controls upstream D-channel and S/G-bit

State Machine

The exact S/G Bit Control function is given in the following state diagrams.

The values in the state diagrams are to be interpreted as follows:

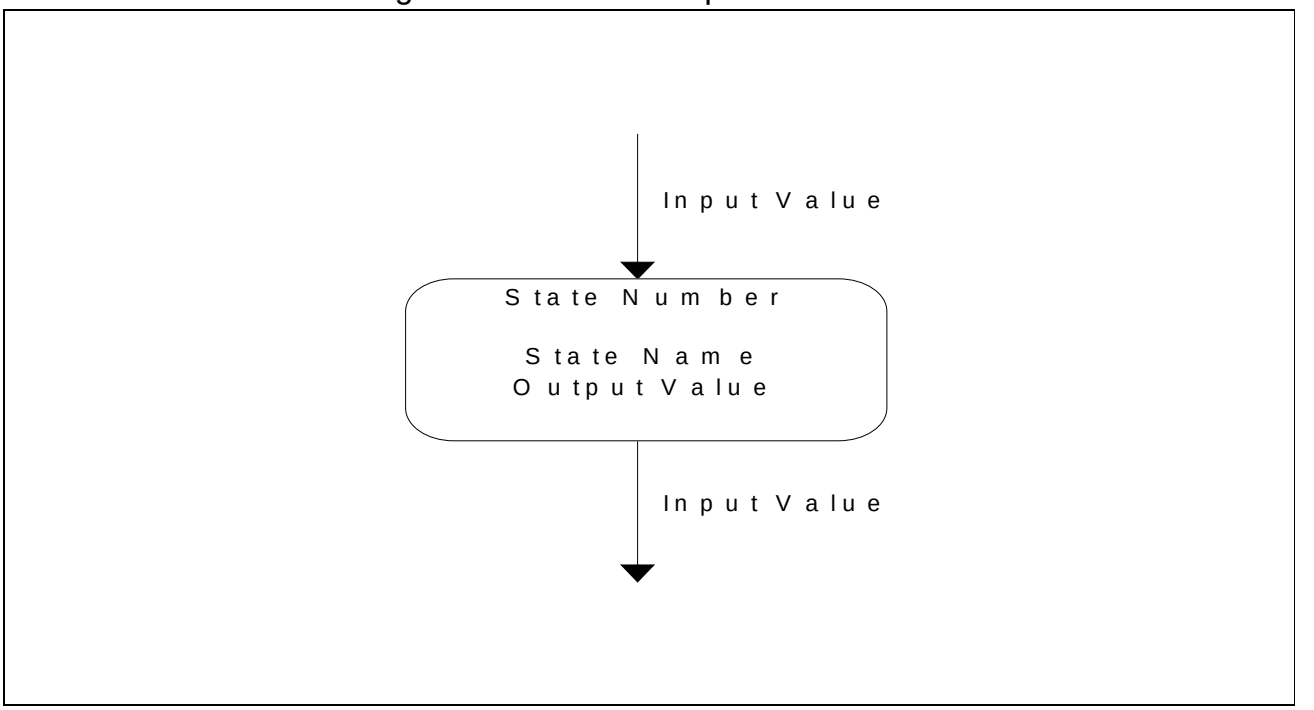
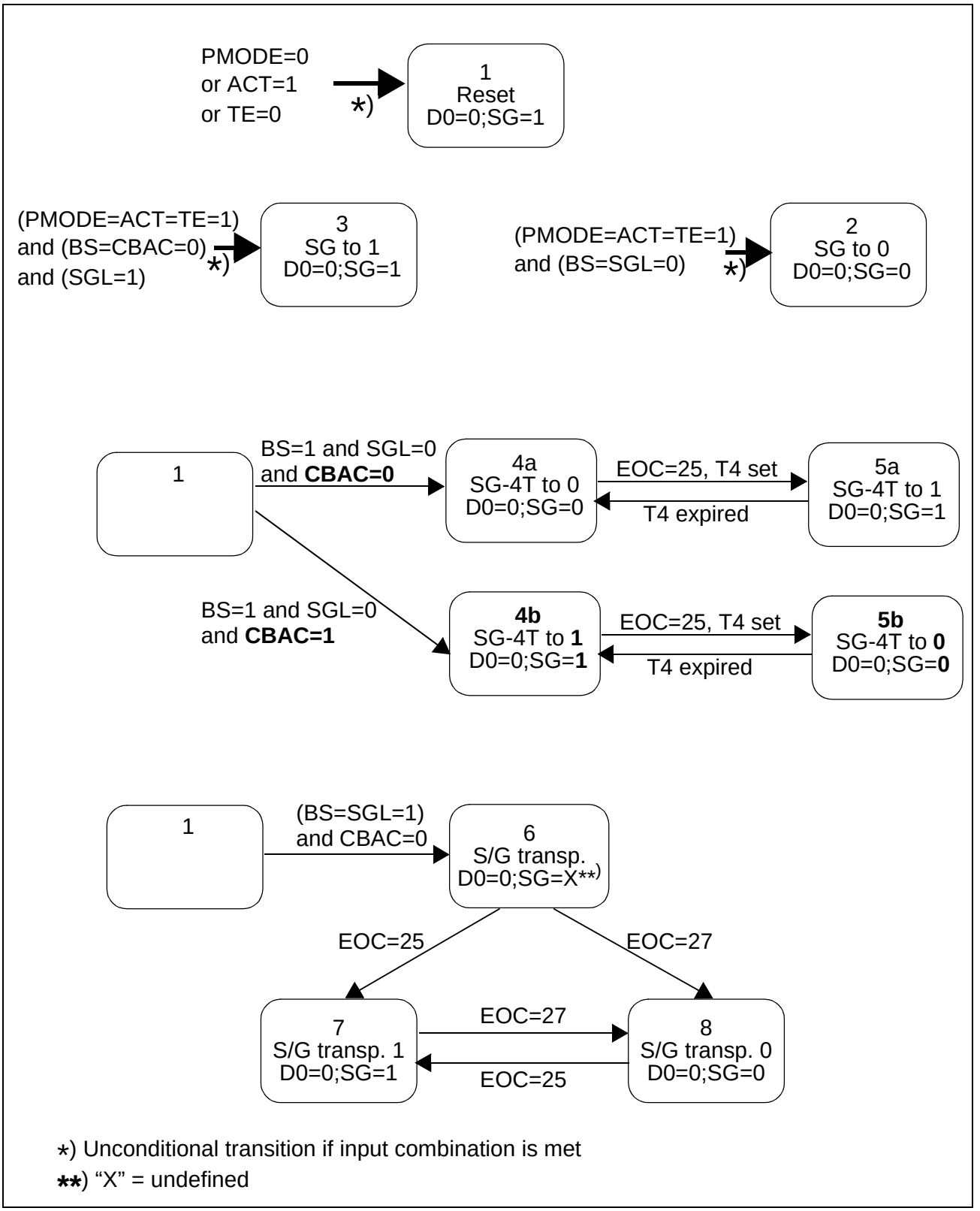


Figure 8 State Machine Notation for S/G Bit Control

State Machine:



*) Unconditional transition if input combination is met

**) "X" = undefined

Figure 9 State Machine for S/G Bit Control (part 1)

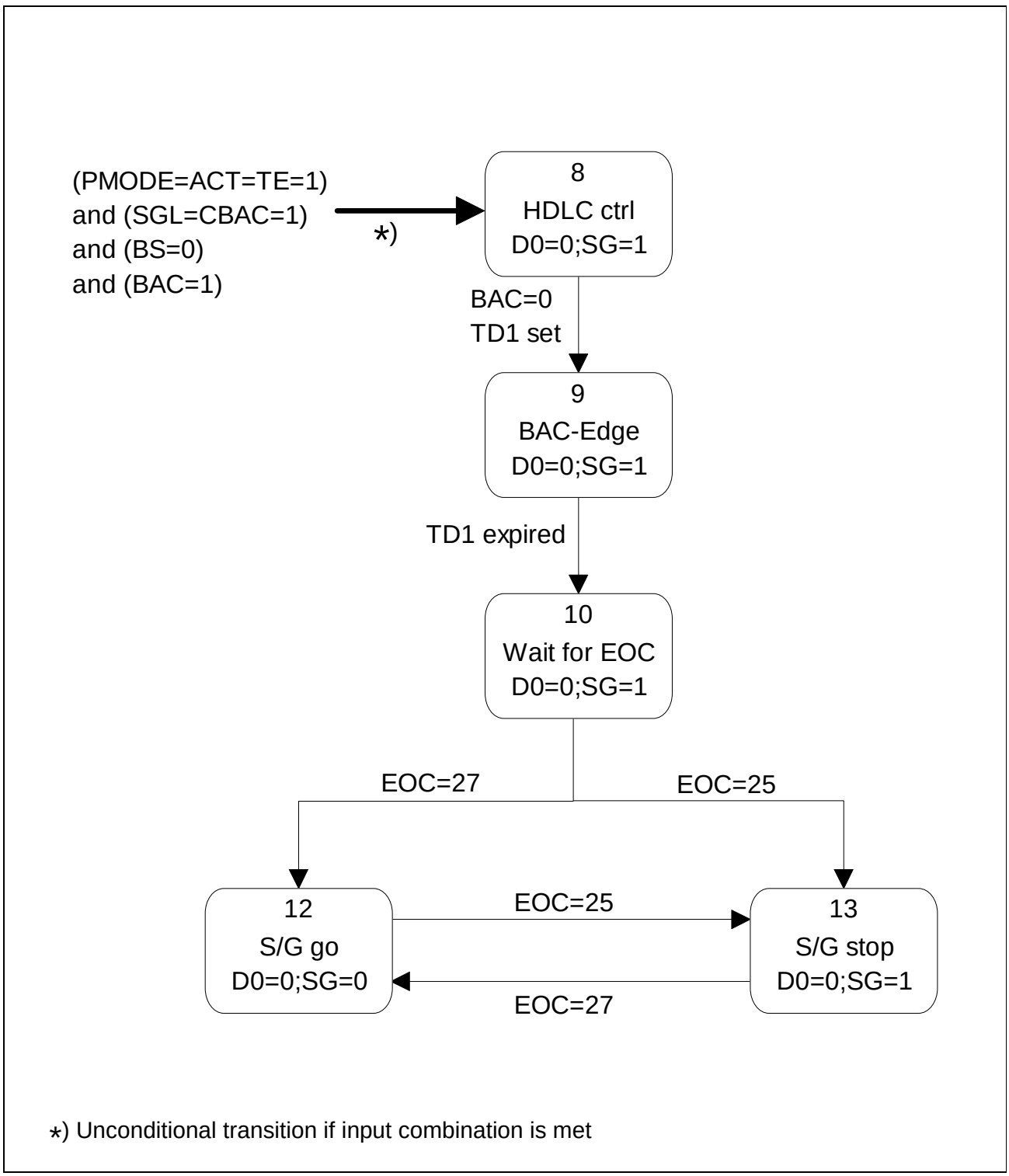


Figure 10 State Machine for S/G Bit Control (part 2)

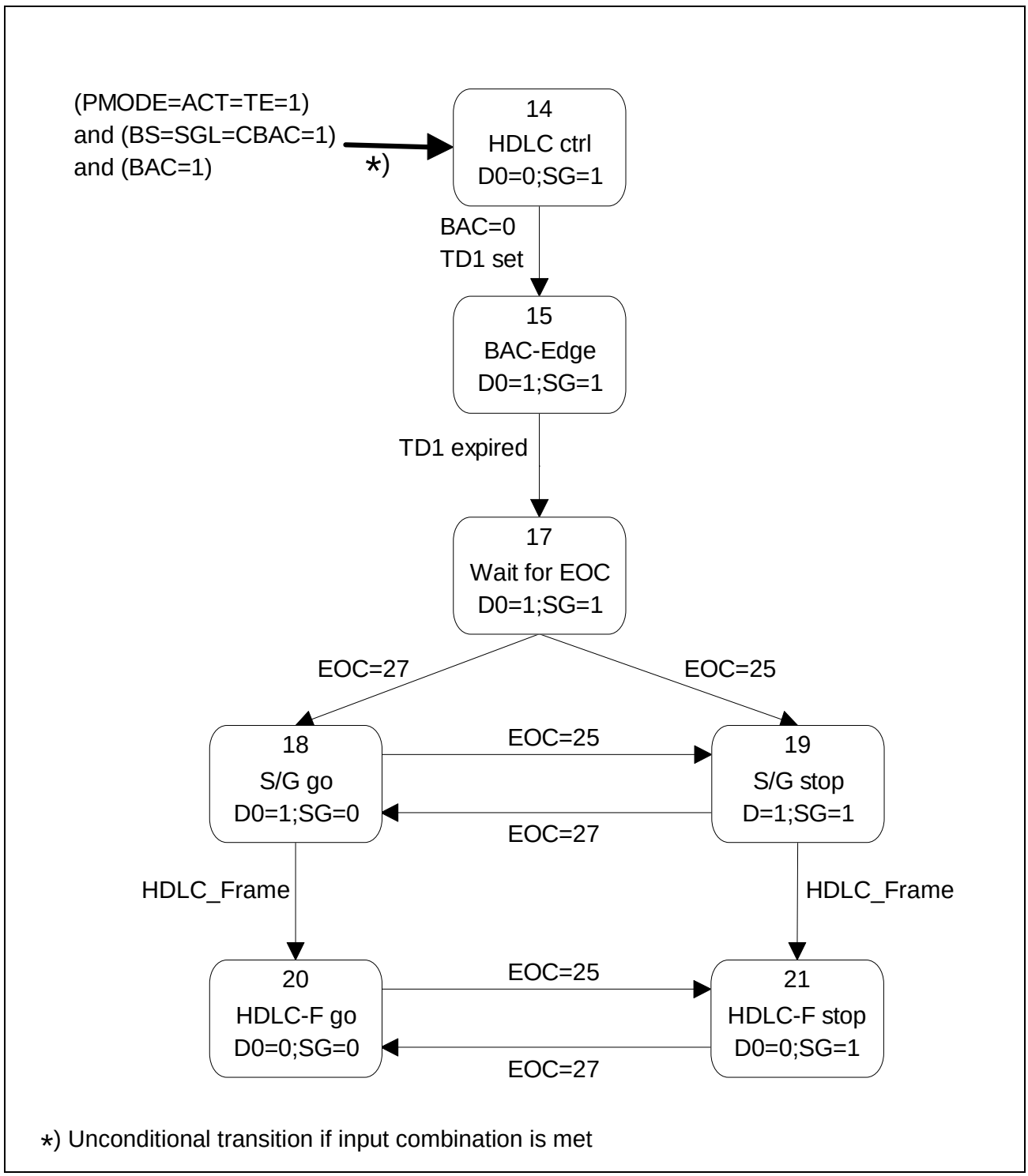


Figure 11 State Machine for S/G Bit Control (Part 3)

Inputs

No.	Signal name	Description
1	PMODE	Corresponds to the PMODE pin. Set to "1" (only) in the microprocessor mode
2	TE	This input is set to "1" (only) in the TE mode
3	ACT	"1" on this input indicates receiver synchronization (e.g. in the Transparent state, see User's Manual 02.95 of the PEB 2091 Version 4.3, page 175).
4	BS	SWST:BS bit.
5	SGL	SWST:SGL bit.
6	CBAC	ADF:CBAC bit.
7	EOC=25	This input indicates that the EOC code 25h (stop) was received from the U interface.
8	EOC=27	This input indicates that the EOC code 27h (go) was received from the U interface.
9	T1 set	An internal 500 micro seconds timer is enabled.
10	T1 expired	The 500 micro seconds timer (see 9) has expired.
11	TD1 set	An internal timer TD1 is enabled. The length of this timer depends on the position of the EOC frame in the currently received U data. It varies between 7.5 and 15 ms.
12	TD1 expired	The timer TD1 has expired, (see 11).
13	BAC	BAC bit on DIN. This is bit no. 27 positioned in the third IOM®-2 slot

Outputs

No.	Signal name	Description
1	SG	Value of the S/G bit on DOUT. The S/G bit is bit no. 27 in the third slot on DOUT.
2	D0	Sets the D channel upstream to "0" if active ("1")

2.10 Indication of S/G Bit Status on Pin SG

Note: This feature is only available if the following two conditions apply:

- The “Decentral HDLC-Processing via S/G Bit in NT-TE Mode” is being used (refer to Delta Sheet of the PEB 2091 Vesion 5.1, page 30 ff).
- One of the packages T-QFP-64 or M-QFP-64 is being used.
  This function is not available in the P-LCC-44 package.

Applications which use the S/G bit control functions (see also "Selectable Polarity of S/G Bit", page 40) may need to get the S/G information independently of the IOM®-2 interface. This may be the case, for example, if the IOM®-2 interface is not being used at all (full control via µP), or if other devices are used to communicate with the IEC-Q, which are not equipped with an IOM®-2 interface (e.g. in Wireless Local Loop applications if a burst mode controller other than PMB x727 is being used).

The following feature has been added in Version 5.3 to simplify the usage of the IEC-Q in such applications. The S/G bit status information will be additionally provided on pin SG, see "Pin Configuration", page 9 ff.

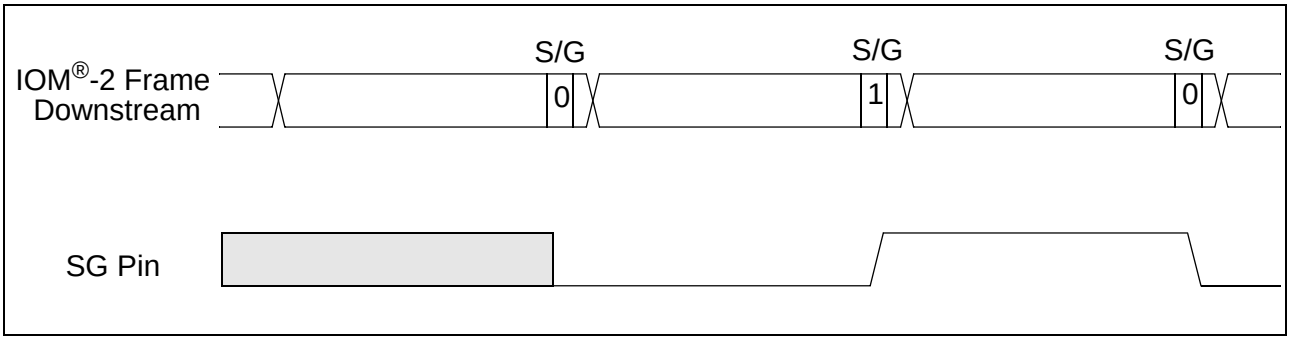


Figure 12 S/G Bit Status on Pin S/G

Note that in state number 6 of the S/G bit control state machine (see Figure 9, page 43) the S/G bit is not defined. In this case the polarity of pin SG may differ from the polarity of the S/G bit on IOM®-2.

For timing properties see "Timing Properties of Pin SG in TE Mode", page 61.

2.11 Activation Attempt Initiated by NT in NT-Auto Mode

According to the User’s Manual 02.95 of the PEB 2091 Version 4.3, page 90, the IEC-Q will start one single activation attempt after leaving the “TEST” state, i.e. after being reset in the NT-Auto mode. In Version 5.3 of the IEC-Q this applies only if the LT is available and ready for activation, e.g. if the LT is not in the reset or in any test state.
However, If the LT is not ready for activation, the NT will periodically start a new activation attempt every 15 seconds, till the LT side will be available and ready for activations initiated by the NT side.

Note Refer also to the corresponding erratum in Errata Sheets of the PEB/F 2091 Versions 5.1 and 5.2. This erratum will not be cleared. The behavior described above could be useful in this application.

2.12 Schmitt Trigger in Reset Path

To avoid unintentional device reset by very short spikes on pin RESQ (< 3 ns) a Schmitt Trigger has been implemented in the Reset path.

To guarantee a successful device reset, the minimum pulse length on pin RESQ has to be at least 30 ns.

Note Pulses below 30 ns could also cause a Hardware reset, but this can't be guaranteed. Note also that the reset will be executed only after IOM®-2 clocks are issued (valid only in NT-PBX and LT modes).

3 Cleared Errata

The following errata of IEC-Q versions 5.1 and 5.2 have been cleared.

3.1 Improved: Higher IOM Jitter in NT Mode Reduced

The IOM Jitter in NT Mode has been reduced in Version 5.3 compared with versions 4.4, 5.1 and 5.2. The IOM jitter will be the same as in Version 4.3 and older.

This addresses the corresponding remarks of Errata Sheet of the PEB/F 2091 Version 5.1 and Errata Sheet of the PEB/F 2091 Version 5.2.

3.2 Undervoltage Detection

Refer to "Undervoltage Detection", page 33 for details.

This clears the corresponding errata of Errata Sheet of the PEB/F 2091 Version 5.1 and Errata Sheet of the PEB/F 2091 Version 5.2.

3.3 Cleared: Bit Errors on the U-Interface in LT Burst Mode

The superframe marker can now be used as described in User’s Manual 02.95 of the PEB 2091 Version 4.3, page 112, without restrictions. Note that the superframe marker function can be disabled in µP mode (see "Superframe Marker Enable in µP Mode", page 38).

This clears the corresponding erratum of Errata Sheet of the PEB/F 2091 V5.1.

3.4 Dropped: Monitor Channel Receive Constraints

The Monitor channel handling can now be used as described in Delta Sheet of the PEB 2091 Vesion 5.1 without restrictions.

This clears the corresponding Errata of Errata Sheet of the PEB/F 2091 V5.1 and Errata Sheet of the PEB/F 2091 V5.2.

3.5 Data Propagation Time from the LT-IOM to the NT-IOM

The propagation time from the IOM interface on the LT side to the IOM interface on the NT side between any two activations will be constant if Version 5.3 is being used on both LT and NT sides.

This clears the corresponding Errata of Errata Sheets of the PEB 2091 Version 5.1 and 5.2.

Note It is recommended to use the DFE-Q/AFE (PEB 24911/PEB 24902) for the LT side and Version 5.3 for the NT side in Wireless Local Loop applications. Beside higher accuracy, this gives access to important features, e.g. concerning propagation delay measurements.

3.6 Cleared: Bit Errors and Corrupted Single Pulses in LT Modes

The corresponding erratum of Errata Sheet of the PEB/F 2091 V5.1 has been cleared.

3.7 Cleared: Warm Start Time Requirement not Met in LT Mode

The corresponding erratum of Errata Sheet of the PEB/F 2091 V5.1 has been cleared.

3.8 Constant Propagation Delay in Wireless Local Loop Applications

The constant propagation delay requirements needed for Wireless Local Loop applications, are fulfilled. This applies if PEB 24911 (QUAD IEC-DFE-Q) versions 1.2 or 1.3 are used in the Central Office and Version 5.3 of PEB/F 2091 is used for the Base Station. Refer to the corresponding Application Note.

This clears the corresponding errata of Errata Sheet of the PEB/F 2091 V5.1 and Errata Sheet of the PEB/F 2091 V5.2.

3.9 Activation in NT Mode by µC

Version 5.3 has been improved to provide this function. See "Activation in the µP-NT Mode", page 39 for details.

This addresses the corresponding remarks in Errata Sheet of the PEB/F 2091 V5.1 and Errata Sheet of the PEB/F 2091 V5.2.

4 Register Description

Important: This chapter applies only in µP mode.

This chapter gives a detailed description of the registers which were changed, compared with versions 5.1 and 5.2 of the PEB/F 2091. Changed bits will be written in bold type style.

4.1 ADF-Register

Additional Features Register (ADF). Write Address E_H.

Default: 14_H

7							0	
WTC2	WTC1	PCL1	PCL0		**UVD**	BCL	CBAC	E_H

WTC2, WTC1: Watchdog Controller

The bit patterns “10“ and “01“ has to be written in WTC1 and WTC2 by the enabled watchdog timer within 132ms. If it fails to do so, a reset signal of 5ms at pin $\overline{RST}$ is generated.

PCL1, PCL0: Prescaler

The clock frequency on MCLK is selected by setting the bits according to the table below:

PCL1	PCL0	Frequency at MCLK (MHz)
0	0	7.68
0	I	3.84
I	0	1.92
I	I	0.96

UVD: **Undervoltage Detector**

UVD = 1 enables the undervoltage detector. For details "Undervoltage Detection", page 33.

UVD = 0 disables the undervoltage detector.

BCL: Bit Clock

BCL = 1 changes the DCL-output into the bit-clock-mode.

BCL = 0 gives the doubled bit clock on the DCL-output.

CBAC: Control BAC

Operates in combination with SWST:SGL and SWST:BS bits to control the S/G bit and the BAC bit. For the functional description see Table 7, “Function of the Register Bits: SWST:BS, SWST:SGL and ADF:CBAC,” on page 40.

4.2 ADF2-Register

Additional Features Register 2 (ADF2).Write Address 4_H.

Default: 18_H

7							0	
TE1	MTO	DOD	**SFEN**	MIN		**ICEC**		4_H

TE1: Terminal Equipment Channel 1

TE1 = 1 enables the IEC-Q TE to write Monitor data on DOUT to the MON1 channel instead of the MON0 channel and to write 6-bit C/I indications on DOUT into the C/I-channel 1.

TE1 = 0 enables the normal TE operations where the IEC-Q TE addresses only IOM-2 channel 0.

MTO: Monitor Procedure Time-out

MTO = 1 disables the internal 6ms Monitor time-out.

MTO = 0 enables the internal 6ms Monitor time-out.

DOD: Dout Open Drain

DOD = 1 selects pin DOUT to be open drain.

DOD = 0 selects pin DOUT to be tristate.

SFEN: Superframe Enable

SFEN = 0 disables the superframe marker function.

SFEN = 1 enables the superframe marker function.

MIN: Monitor-In-Bit

MIN = 1 combined with the SWST:MON = “1“ and ADF2:TE1 = “0“ bits, enables the controller to access the core of the IEC-Q TE.

MIN = 0 combined with the SWST:MON = “1“ and ADF2:TE1 = “0“ bits, enables the controller to access the IOM-2 interface directed out of the IEC-Q TE.

ICEC: **IOM-2 Clocks Enable Control**
ICE= 0: The status of pin ICE is valid (default).

ICE= 1: Inverts meaning of pin ICE

Clocks are enabled if pin ICE=0.
Clocks are disabled if pin ICE=1.

4.3 CIWU-Register

The Write C/I-code to U Register (CIWU) writes the C/I-code to the U-transceiver.
Write Address C_H

Default: $C3_H$

7							0	
SPU	1	C/I	C/I	C/I	C/I	1	1	C_H

SPU: **Software Power-Up bit. Valid only in the NT mode.**
SPU= 1: Data on DIN will be transparently transmitted to the U-transceiver (default)
SPU= 0: Data on DIN will be ignored and binary “0” will be continuously transmitted to the U-transceiver if the NT mode is selected (pin LT=”0”).

6. bits: Set to “1“.

5.-2. bits: Contain the C/I-code going to the U-transceiver.

1., 0. bits: Set to “1“.

5 Electrical Characteristics

5.1 Power Consumption

The power consumption of Version 5.3 has been reduced, compared with Version 5.1. Version 5.3 will have the same power consumption values as Version 5.2.

All measurements with random 2B + D data in active states.

Mode	Test Conditions	Limit Values		Unit
		typ.	max.	
Power up	5.00 V, open outputs 98 Ω load at AOUT/BOUT Inputs at VDD/GND	53.0	59.0	mA
LT-Power down	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature ≥ 0°C Inputs at VDD/GND	6.7	11.0	mA
	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature < 0°C Inputs at VDD/GND	8.0	13.0	mA
NT-Power down	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature ≥ 0°C Inputs at VDD/GND	4.7	9.0	mA
	5.00 V, open outputs 98 Ω load at AOUT/BOUT Temperature < 0°C Inputs at VDD/GND	6.5	11.0	mA

5.2 DC Characteristics

VDD = 4.75 to 5.25 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
L-level input leakage current for pin ICE (internal pull-up resistor)	I_{ILPU}	– 100	100	µA	V_I = GND[1)]
H-level input leakage current for pin ICE (internal pull-up resistor)	I_{IHPU}	– 10	10	µA	V_I = VDD[1)]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
H-level output voltage for pin SG	V_{OH1}	2.4		V	I_{OH1} = 0.4 mA[1)]
L-level output voltage for pin SG	V_{OL1}		0.4	V	I_{OL1} = 2 mA[1)]

1) Inputs at VDD/GND

Pin Capacitances

T_A = 25 °C; V_{DD} = 5 V ± 5 %; V_{SS} = 0 V; f_C = 1 MHz

Pin	Parameter	Symbol	Limit Values		Unit
			min.	max.	
ICE	Pin capacitance	C_{IO}		7	pF

5.3 AC Characteristics

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output wave forms are shown in Figure 13 below.

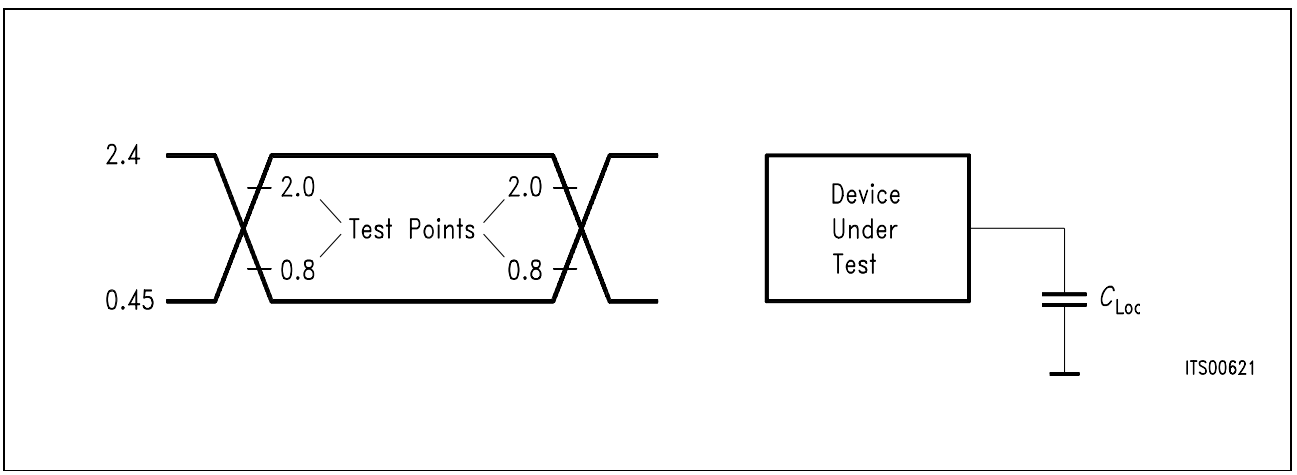


Figure 13 Input/Output Wave Form for AC Tests

5.3.1 Microprocessor Interface Timing in Parallel Mode

The microprocessor interface timing in the parallel mode has been accelerated. This allows using the IEC-Q in applications which demand high data transmission rates, e.g. PCM-4, 8, or in applications with high speed microcontroller.

5.3.1.1 Siemens/Intel Bus Mode

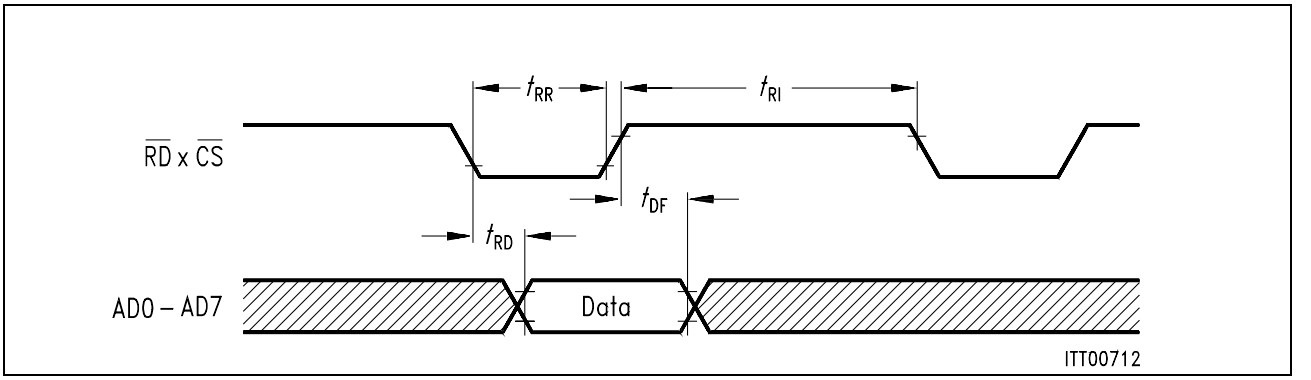


Figure 14 Siemens/Intel Read Cycle

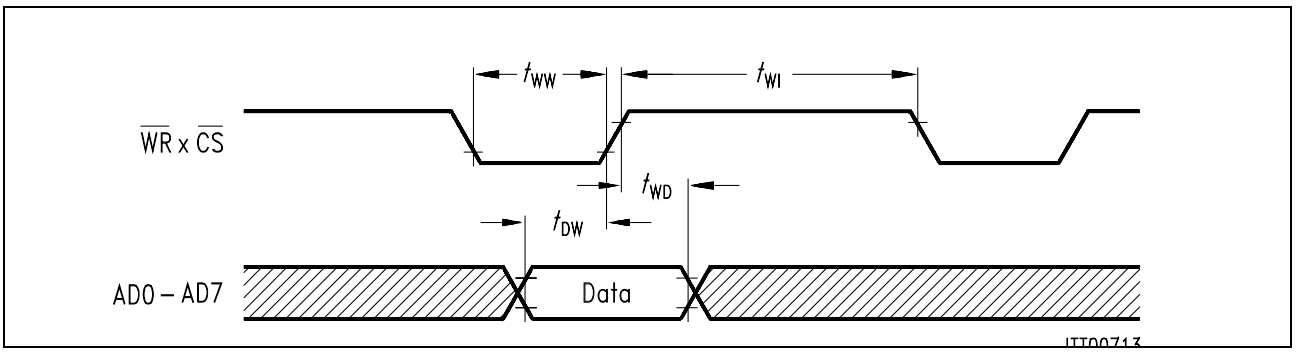


Figure 15 Siemens/Intel Write Cycle

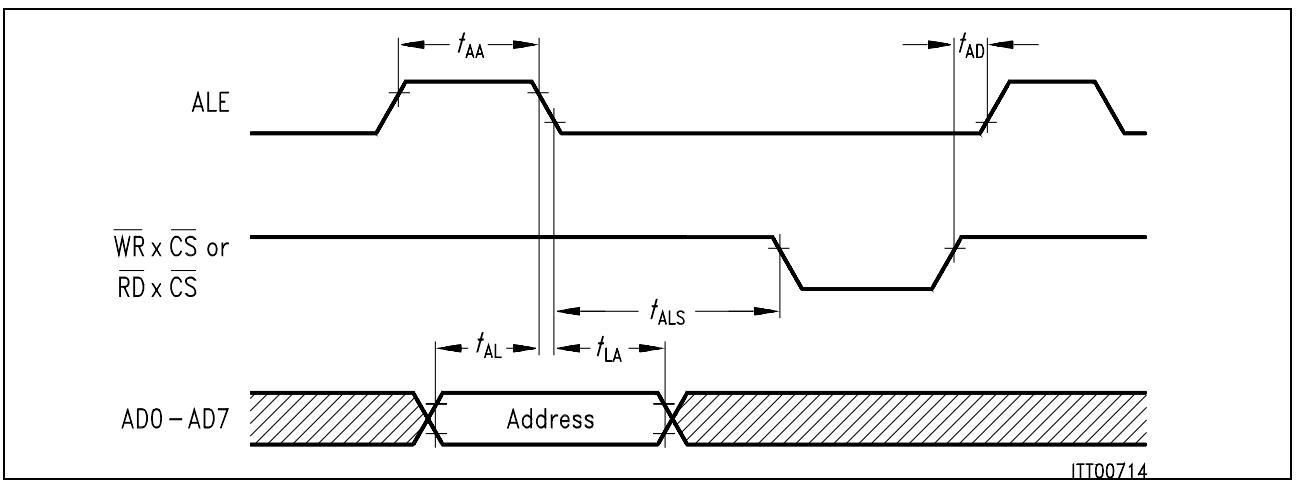


Figure 16 Siemens/Intel Multiplexed Address Timing

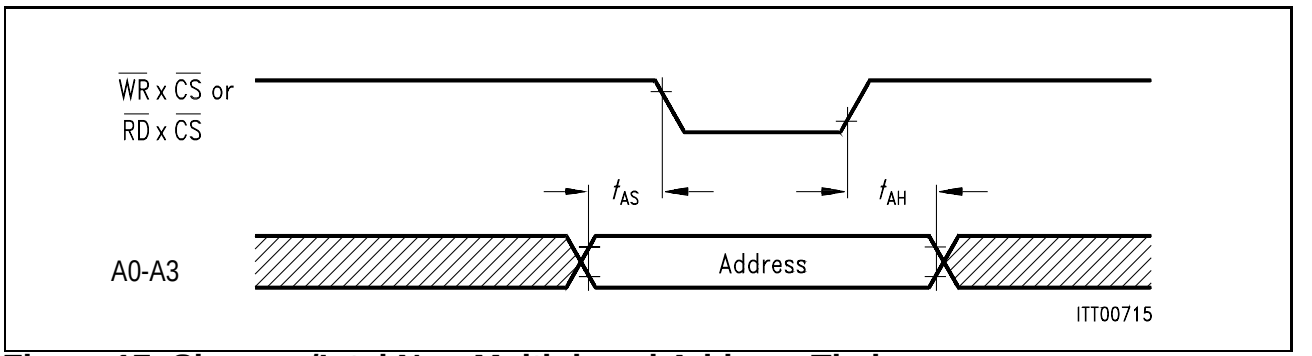


Figure 17 Siemens/Intel Non-Multiplexed Address Timing

5.3.1.2 Motorola Bus Mode

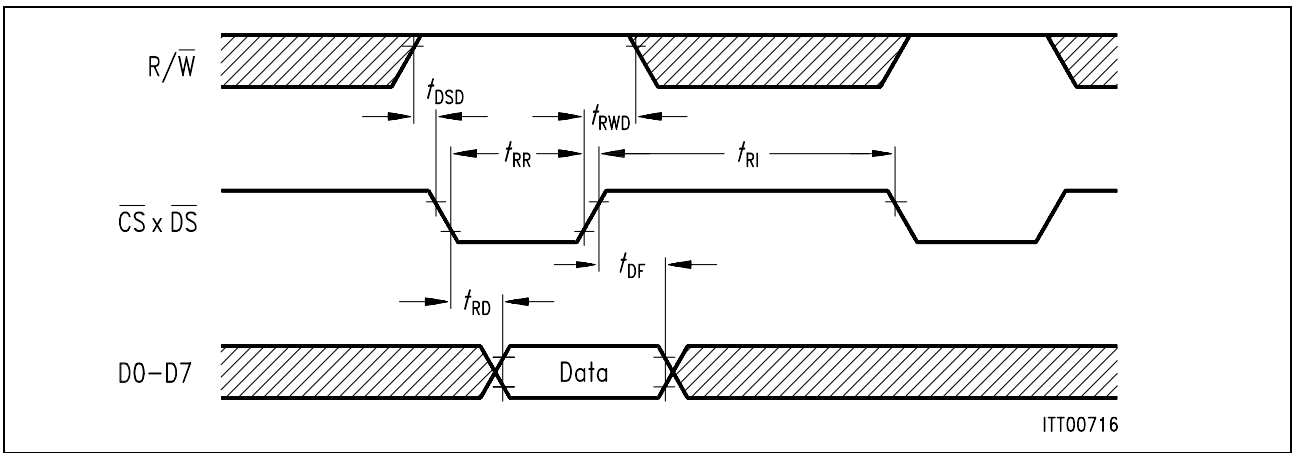


Figure 18 Motorola Read Timing

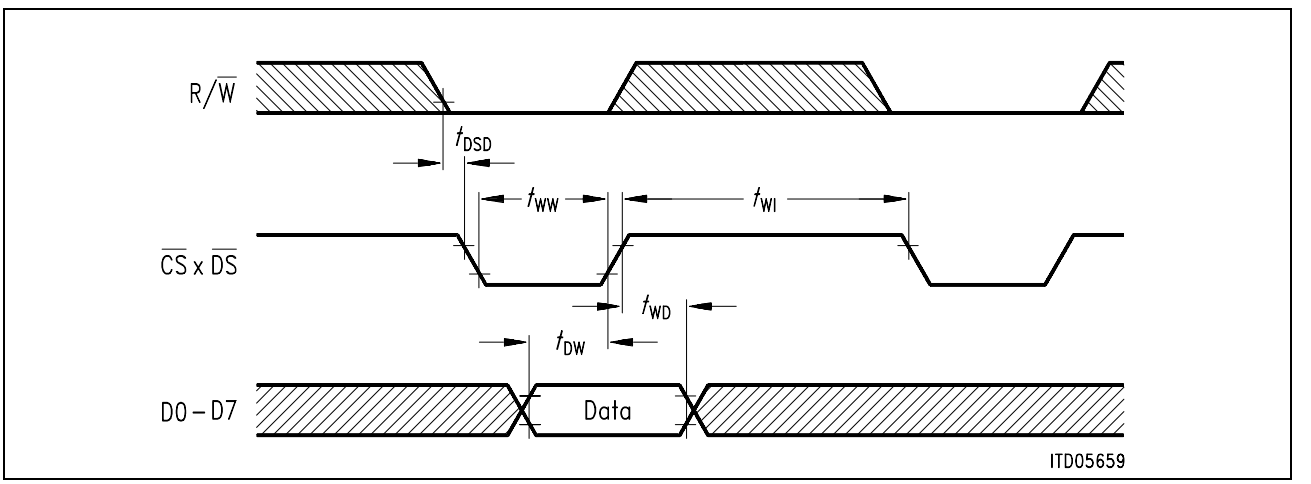


Figure 19 Motorola Write Cycle

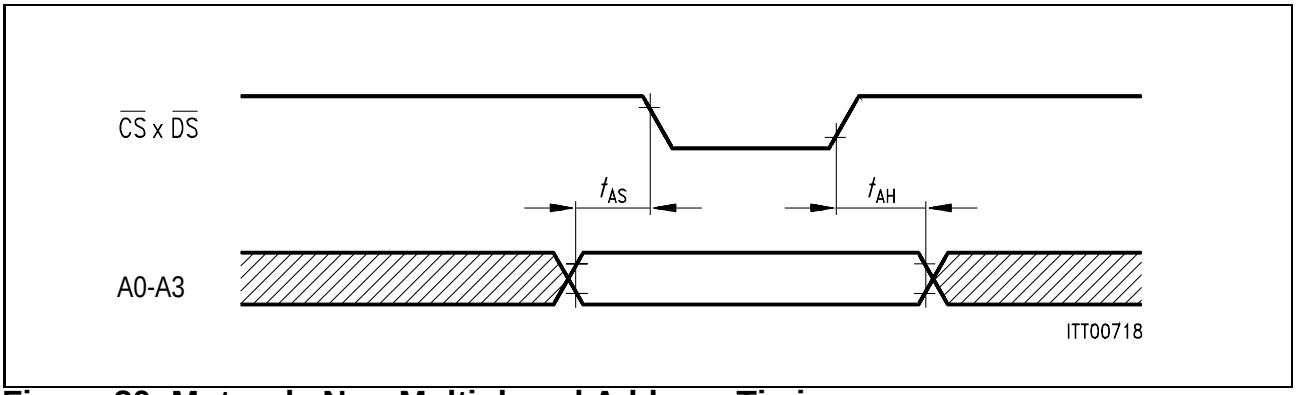


Figure 20 Motorola Non-Multiplexed Address Timing

5.3.1.3 Timing Values of the µP Interface in Parallel Mode

C_{Load} = 50pF

Parameter	Symbol	min.	max.	unit
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	15		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	25		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	0		ns
ALE pulse delay	t_{AD}	10		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ x $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$ x $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

5.3.2 Undervoltage Detection Timing

The timing of the undervoltage detection function (see "Undervoltage Detection", page 33) is given below.

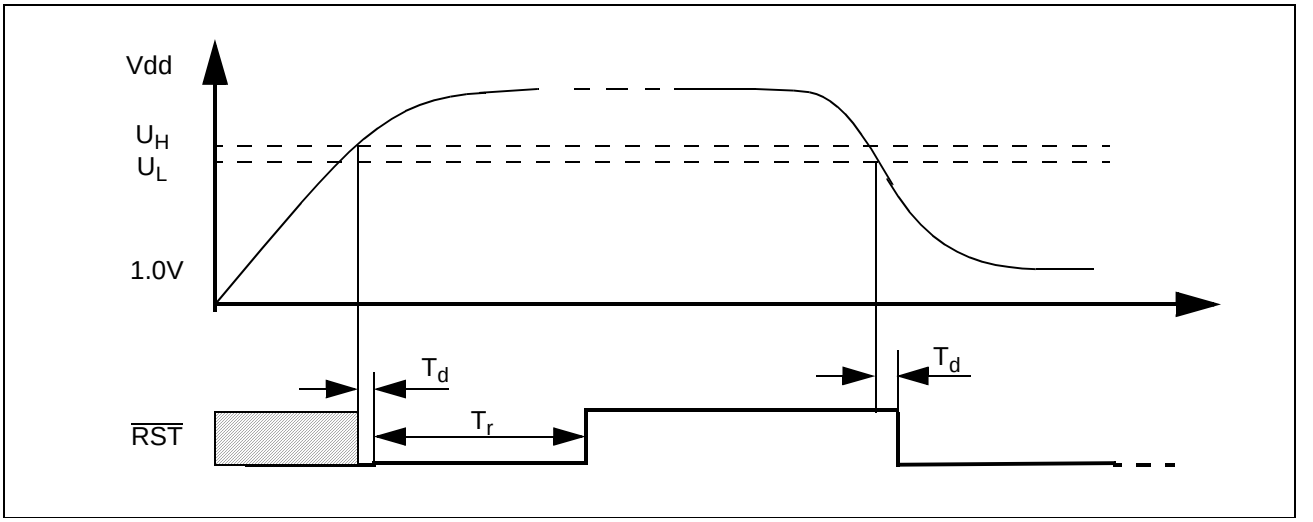


Figure 21 UVD Timing Characteristics

Table 8 Timing Parameters of UVD Function

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Upper threshold voltage	U_H	4.1	4.3	4.5	V
Lower threshold voltage	U_L	U_H -0.11	U_H -0.085	U_H -0.05	V
Length of reset pulse	T_r 1)	67			ms
Delay of the reset generation after the threshold voltage has been passed	T_d	0	10	20	µs
Slope of the rise and fall time of VDD at every point of time	dV/dt	0		10^4	V/s

1) Note that this specification holds only if stability of the 15.36 MHz clock is guaranteed. During power-up, the reset pulse may therefore vary slightly from the value mentioned above due to instability of the oscillator during start up.

5.3.3 Timing Properties of CLS in NT Repeater Mode

C_{Load} = 20pF

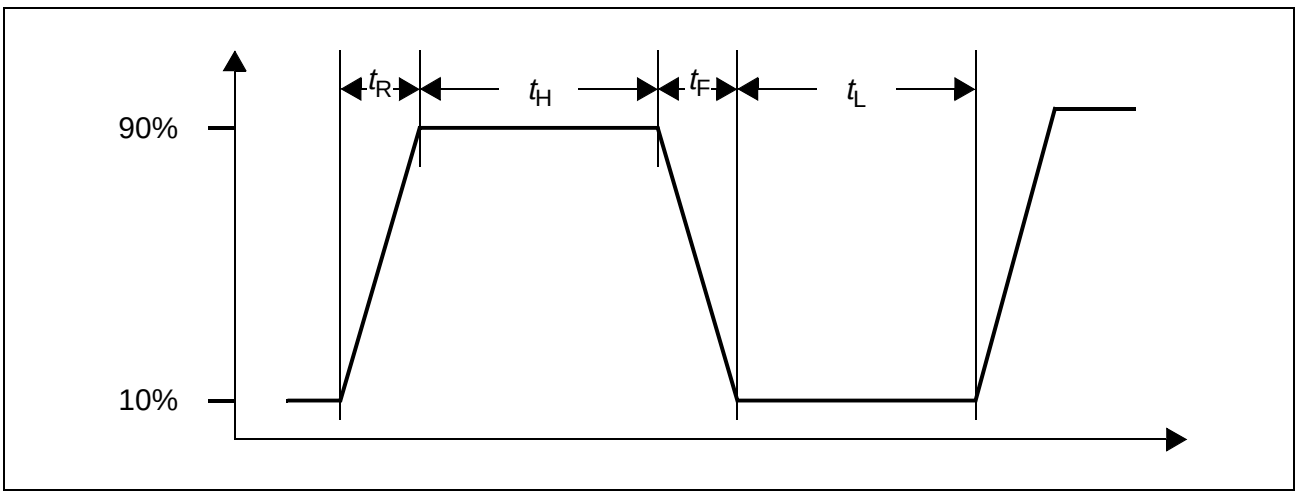


Figure 22 Dynamic Characteristics of CLS in NT-RP Mode

Table 9 Output Characteristics of CLS in NT-RP Mode

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Pulse width high, low	t_H, t_L	26	39	ns
Rise time, fall time	t_R, t_F	0	13	ns

5.3.4 Timing Properties of Pin SG in TE Mode

C_{Load} = 25pF

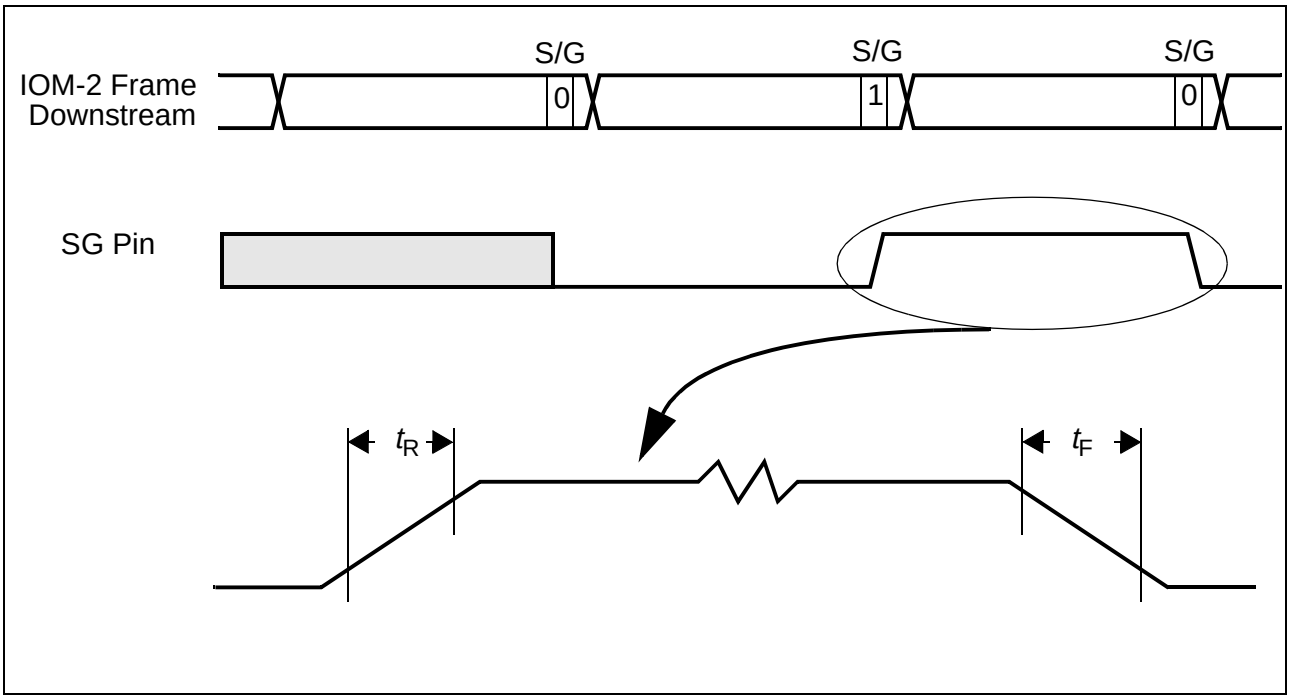


Figure 23 Dynamic Characteristics of Pin SG

Table 10 Output Characteristics of Pin S/G

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Rise time, fall time	t_R,t_F	0	30	ns

6 Package Outlines

Plastic Package, P-LCC-44
(Metric Quad Flat Package)

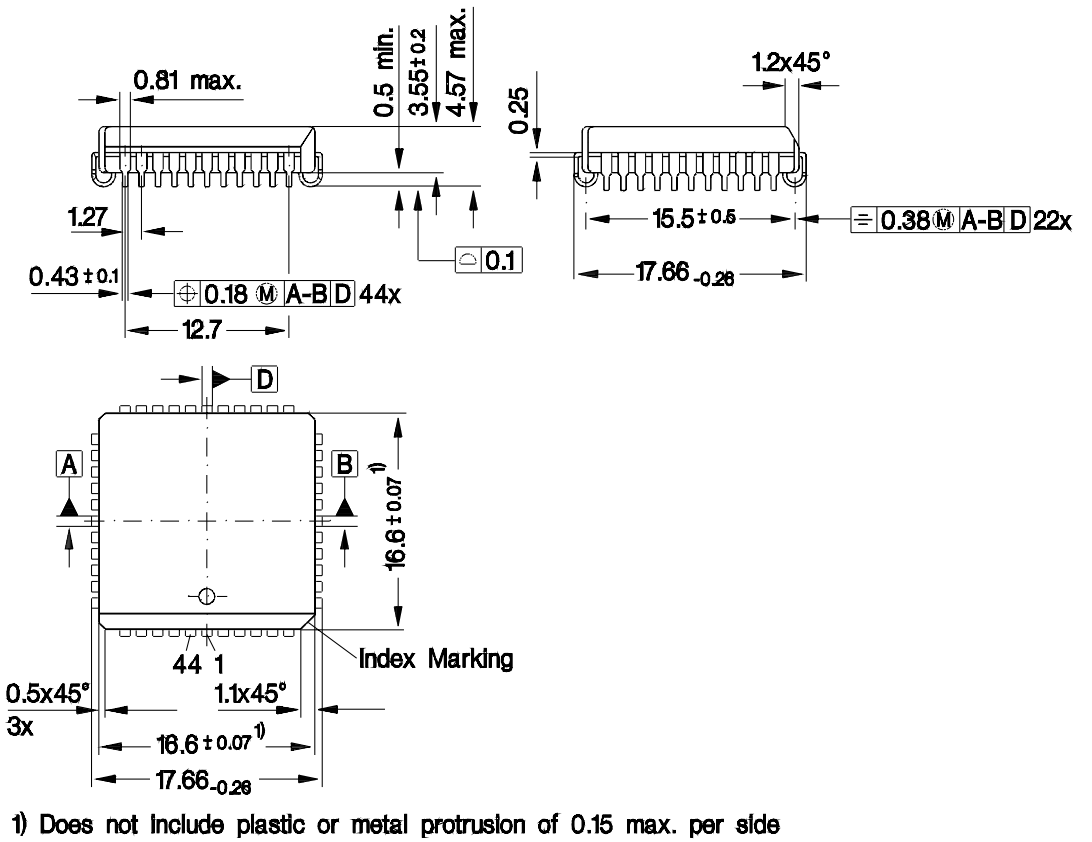


Figure 24 Package Outline for P-LCC-44

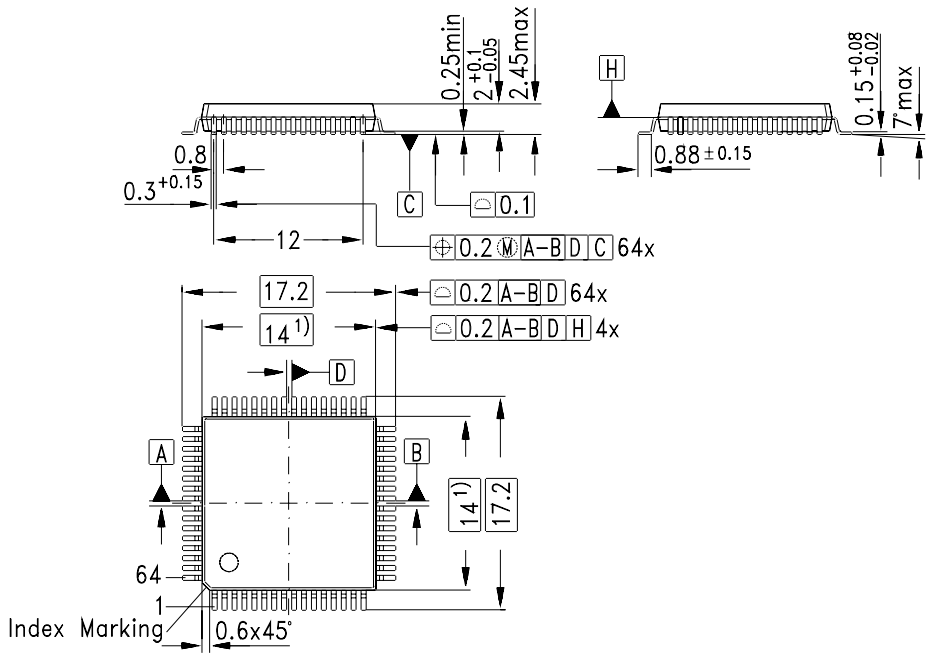
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, M-QFP-64
(Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

Figure 25 Package Outline for M-QFP-64

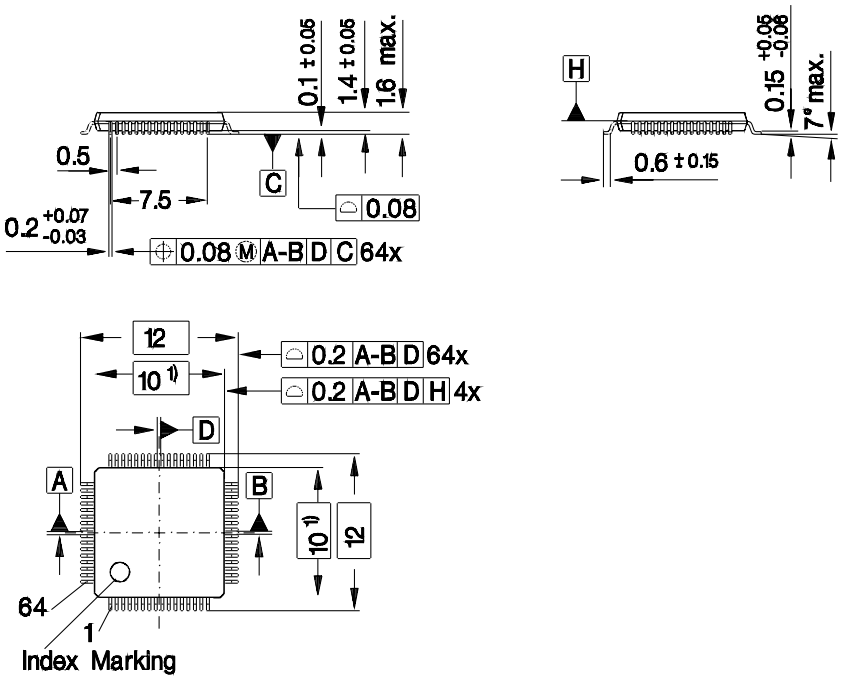
Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, T-QFP-64
(Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 26 Package Outline for T-QFP-64

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm