

R1LV0208BSA

2Mb Advanced LPSRAM (256k word x 8bit)

R10DS0272EJ0101
Rev.1.01
2020.2.20

Description

The R1LV0208BSA is a family of low voltage 2-Mbit static RAMs organized as 262,144-word by 8-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies. The R1LV0208BSA has realized higher density, higher performance and low power consumption. The R1LV0208BSA is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives. The R1LV0208BSA has been packaged in 32-pin sTSP.

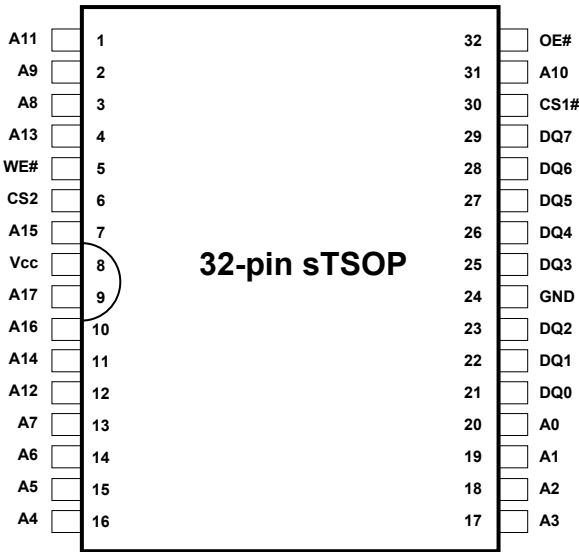
Features

- Single 2.7V~3.6V power supply
- Small stand-by current: 1μA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1# and CS2
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LV0208BSA-5SI#B1	55 ns	-40 ~ +85°C	8mm×13.4mm 32-pin plastic sTSP	Tray
R1LV0208BSA-5SI#S1				Embossed tape

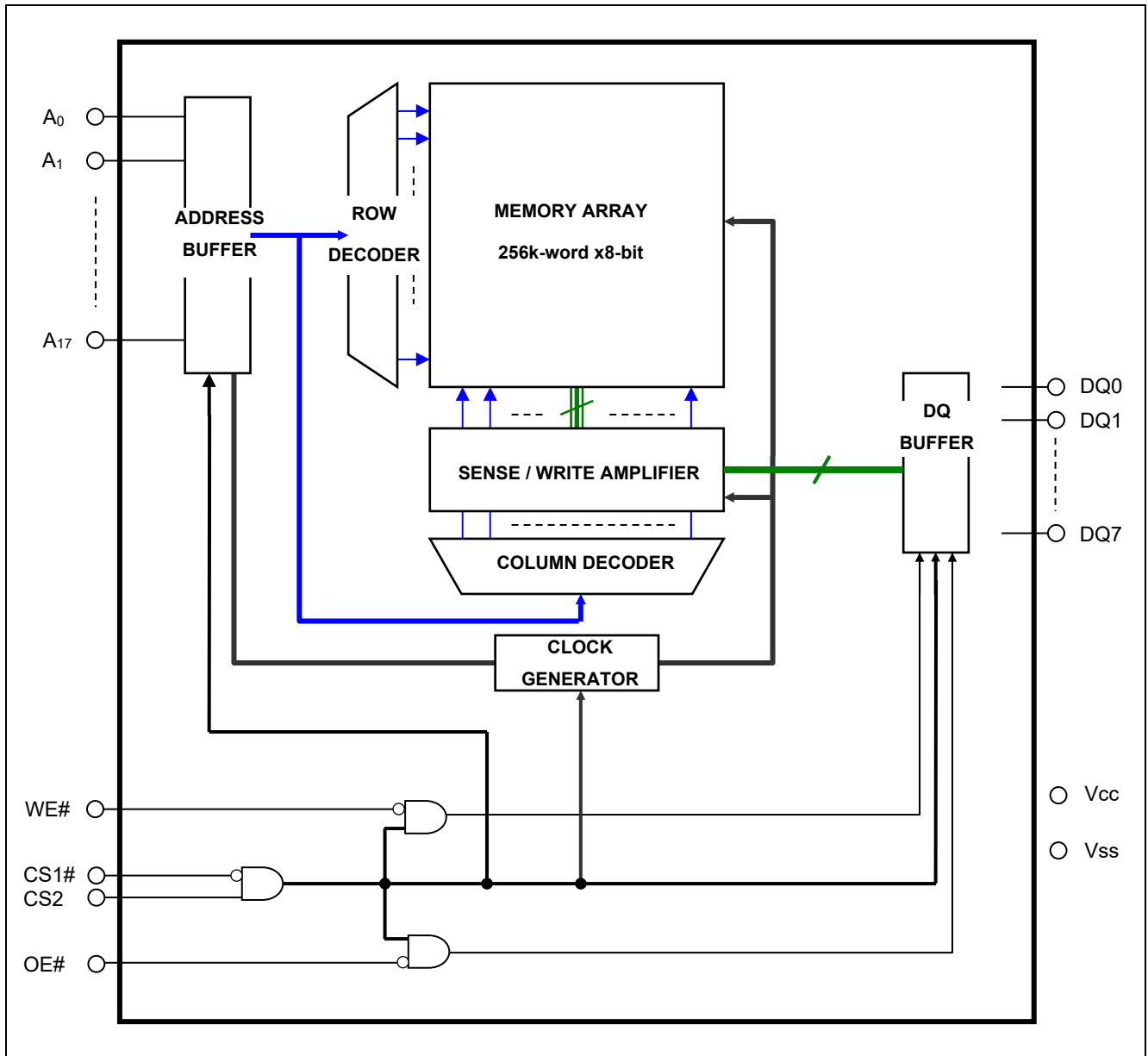
Pin Arrangement



Pin Description

Pin name	Function
Vcc	Power supply
Vss (GND)	Ground
A0 to A17	Address input
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
X	L	X	X	High-Z	Stand-by
H	X	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	V_T	-0.5 ¹ to Vcc+0.5 ²	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. -3.0V for pulse ≤ 30 ns (full width at half maximum)

2. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V _{CC}	2.7	3.0	3.6	V	
	V _{SS}	0	0	0	V	
Input high voltage	V _{IH}	2.0	-	V _{CC} +0.3	V	
Input low voltage	V _{IL}	-0.3	-	0.6	V	1
Ambient temperature range	T _a	-40	-	+85	°C	

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	I _{LI}	-	-	1	μA	Vin = Vss to Vcc	
Output leakage current	I _{LO}	-	-	1	μA	CS1# =V _{IH} or CS2 =V _{IL} or OE# =V _{IH} , VI/O =Vss to Vcc	
Average operating current	I _{CC1}	-	15	25	mA	Min. cycle, duty =100%, II/O = 0mA, CS1# =V _{IL} , CS2 =V _{IH} , Others = V _{IH} /V _{IL}	
	I _{CC2}	-	2	5	mA	Cycle =1μs, duty =100%, II/O = 0mA, CS1# ≤ 0.2V, CS2 ≥ Vcc-0.2V, V _{IH} ≥ Vcc-0.2V, V _{IL} ≤ 0.2V	
Standby current	I _{SB}	-	-	0.33	mA	(1) CS1# =V _{IH} , Others =V _{IH} /V _{IL} or (2) CS2 =V _{IL} , Others =V _{IH} /V _{IL}	
Standby current	I _{SB1}	-	1*1	2	μA	~+25°C	Vin = Vss to Vcc, (1) CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -0.5mA	
	V _{OH2}	Vcc - 0.5	-	-	V	I _{OH} = -0.05mA	
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

Capacitance

(V_{CC} = 2.7V ~ 3.6V, f = 1MHz, T_a = -40 ~ +85°C)

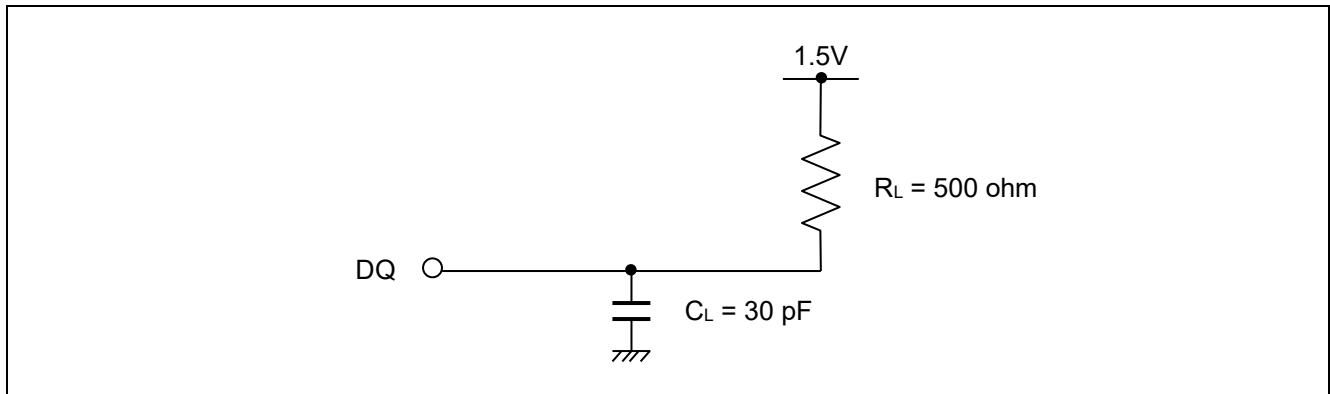
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C _{in}	-	-	8	pF	V _{in} = 0V	1
Input / output capacitance	C _{I/O}	-	-	10	pF	V _{I/O} = 0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels: $V_{IL} = 0.4V$, $V_{IH} = 2.2V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55	-	ns	
Address access time	t_{AA}	-	55	ns	
Chip select access time	t_{ACS1}	-	55	ns	
	t_{ACS2}	-	55	ns	
Output enable to output valid	t_{OE}	-	30	ns	
Output hold from address change	t_{OH}	10	-	ns	
Chip select to output in low-Z	t_{CLZ1}	10	-	ns	2,3
	t_{CLZ2}	10	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	ns	1,2,3
	t_{CHZ2}	0	20	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2,3

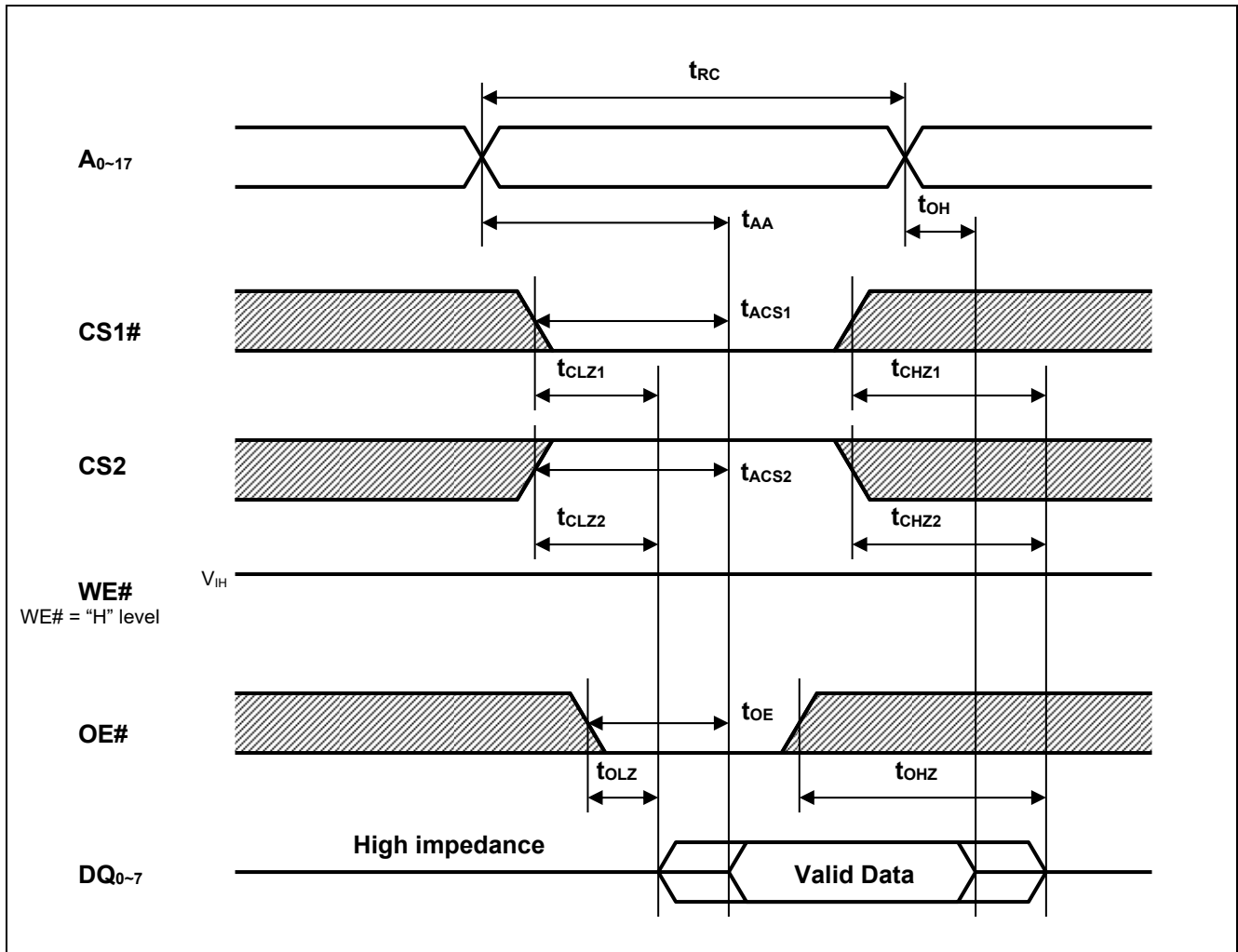
Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	-	ns	
Address valid to end of write	t_{AW}	50	-	ns	
Chip select to end of write	t_{CW}	50	-	ns	5
Write pulse width	t_{WP}	45	-	ns	4
Address setup time	t_{AS}	0	-	ns	6
Write recovery time	t_{WR}	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	ns	
Data hold from write time	t_{DH}	0	-	ns	
Output enable from end of write	t_{OW}	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	ns	1,2

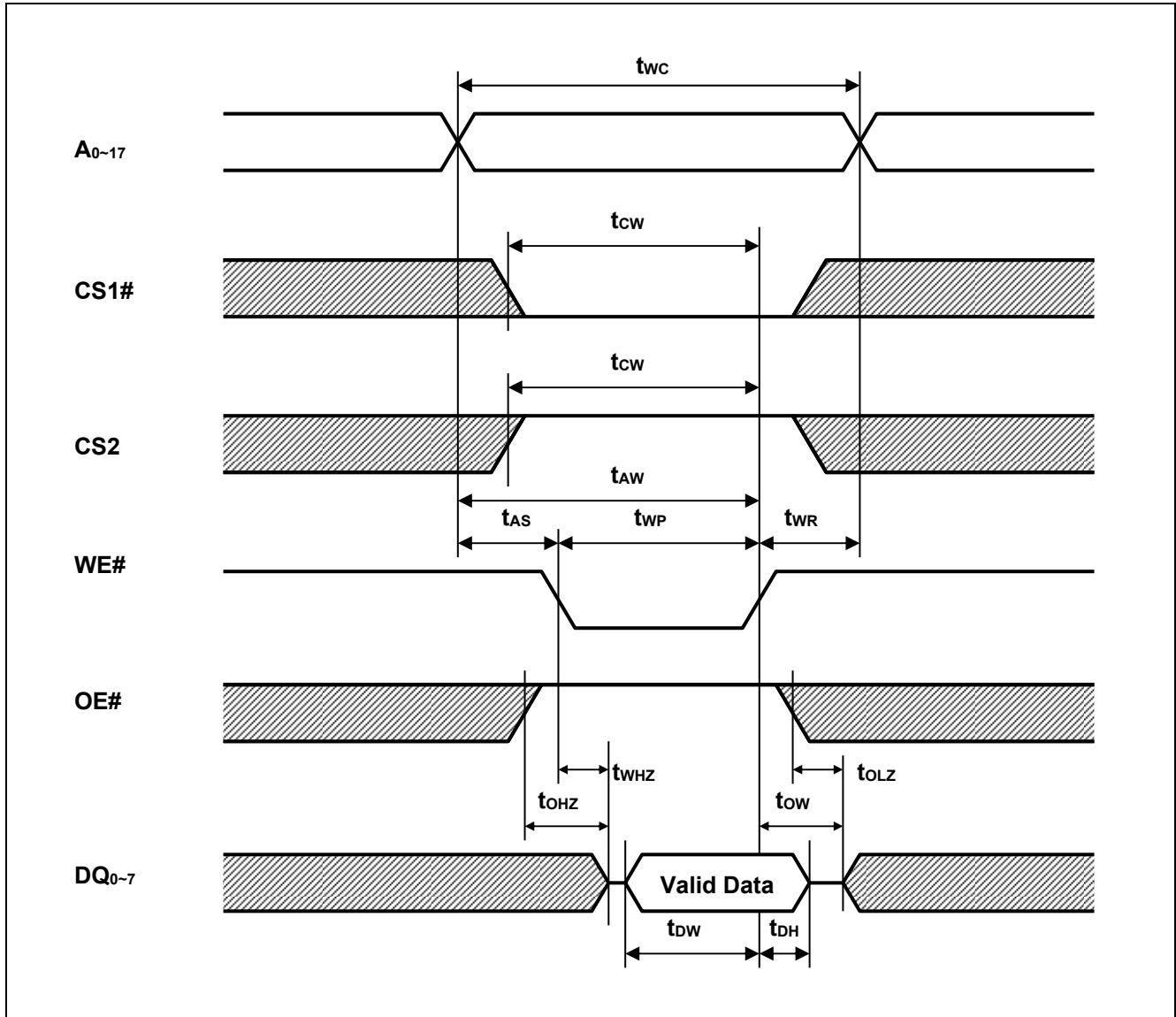
- Note
1. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE#.
A write begins at the latest transition among CS1# going low, CS2 going high and WE# going low.
A write ends at the earliest transition among CS1# going high, CS2 going low and WE# going high.
 t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.
 6. t_{AS} is measured the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.
 8. Don't apply inverted phase signal externally when DQ pin is output mode.

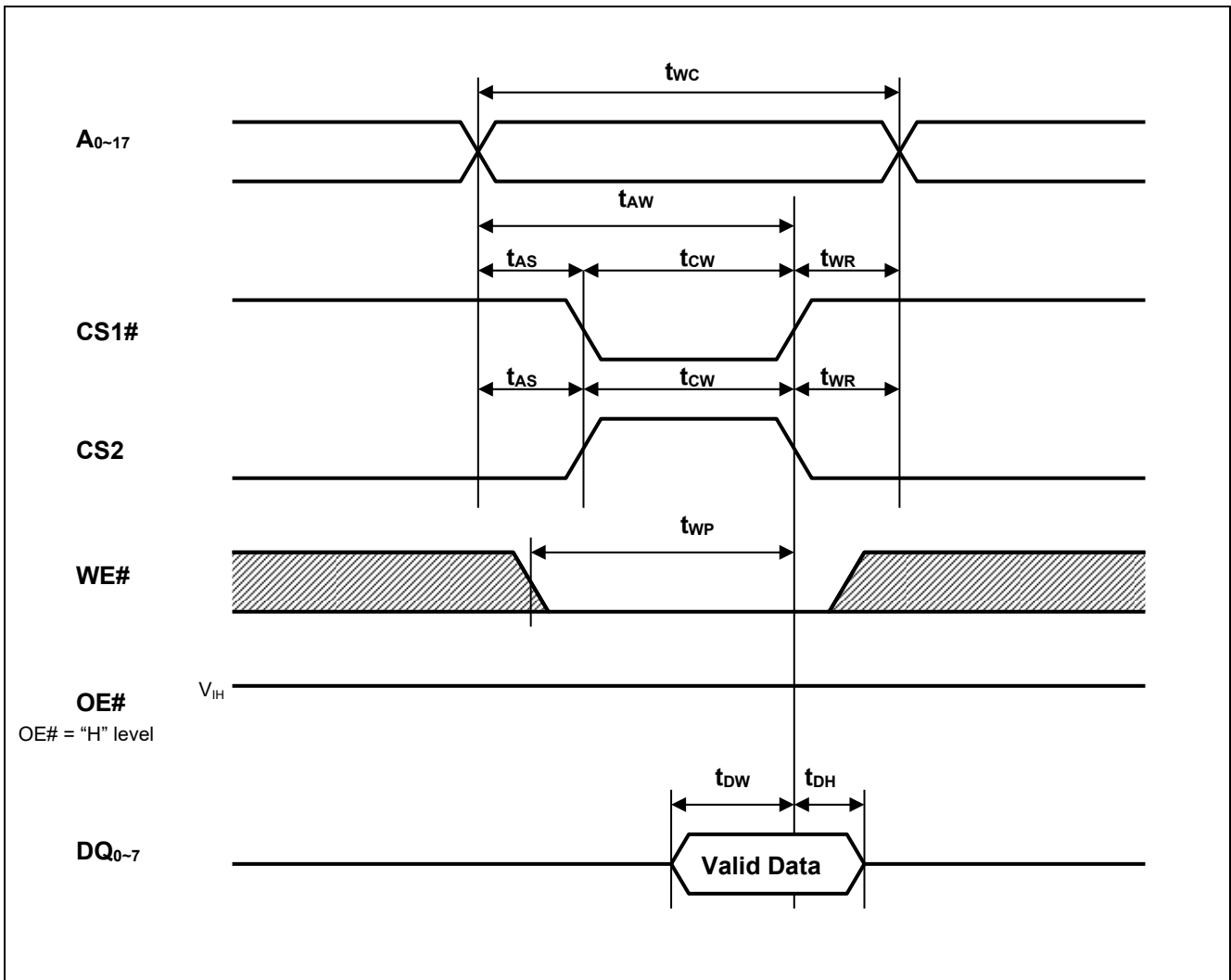
Timing Waveforms

Read Cycle



Write Cycle (1) (WE# CLOCK)



Write Cycle (2) (CS1#, CS2 CLOCK)

Low Vcc Data Retention Characteristics

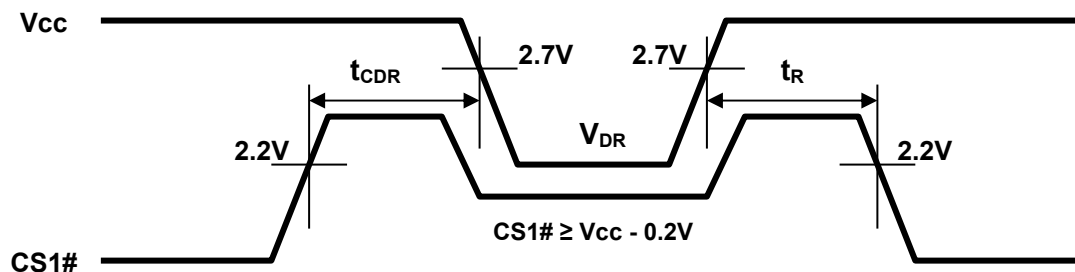
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*2}	
V _{CC} for data retention	V _{DR}	2.0	-	3.6	V	Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V	
Data retention current	I _{CCDR}	-	1 ^{*1}	2	μA	~+25°C	Vcc=3.0V, Vin ≥ 0V, (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ Vcc-0.2V, CS2 ≥ Vcc-0.2V
		-	-	3	μA	~+40°C	
		-	-	8	μA	~+70°C	
		-	-	10	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t _R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

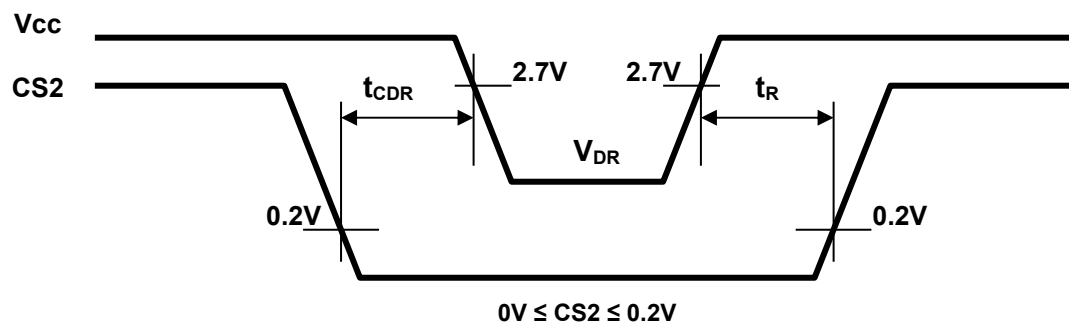
2. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE#, OE#, DQ) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms

(1) CS1# Controlled



(2) CS2 Controlled



Revision History	R1LV0208BSA Data Sheet
------------------	------------------------

Rev.	Date	Description	
		Page	Summary
1.00	2017.1.27	-	First Edition issued
1.01	2020.2.20	Last page	Updated the Notice to the latest version

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.