Silicon Carbide Schottky Diode

650 V, 20 A

FFSD2065B

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

Features

- Max Junction Temperature 175°C
- Avalanche Rated 94 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuit

ABSOLUTE MAXIMUM RATINGS

(T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
E_{AS}	Single Pulse Avalanche Energy (Note 1)		94	mJ
I_F	Continuous Rectified Forward Current @ T_C < 143°C		20	A
	Continuous Rectified Forward Current @ T_C < 135°C		23.4	
$I_{F, Max}$	Non−Repetitive Peak Forward Surge Current	T_C = 25°C, 10 μs	763	A
		T_C = 150°C, 10 μs	650	
$I_{F, SM}$	Non−Repetitive Forward Surge Current	Half−Sine Pulse, t_p = 8.3 ms	80	A
P_{tot}	Power Dissipation	T_C = 25°C	160	W
		T_C = 150°C	27	
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 94 mJ is based on starting T_J = 25°C, L = 0.5 mH, I_{AS} = 19.4 A, V = 50 V.

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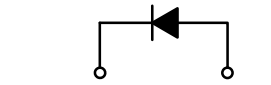
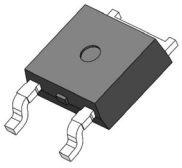
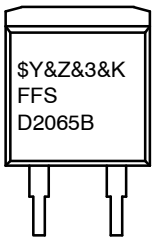


Schottky Diode



DPAK3 (TO−252, 3 LD)
CASE 369AS

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FFSD2065B	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.94	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping†
FFSD2065B	FFSD2065B	DPAK3 (Pb−Free / Halogen Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	I_F = 20 A, T_C = 25°C		1.38	1.7	V
		I_F = 20 A, T_C = 125°C		1.6	2.0	
		I_F = 20 A, T_C = 175°C		1.72	2.4	
I_R	Reverse Current	V_R = 650 V, T_C = 25°C		0.5	40	μA
		V_R = 650 V, T_C = 125°C		1	80	
		V_R = 650 V, T_C = 175°C		2	160	
Q_C	Total Capacitive Charge	V = 400 V		51		nC
C	Total Capacitance	V_R = 1 V, f = 100 kHz		866		pF
		V_R = 200 V, f = 100 kHz		80		
		V_R = 400 V, f = 100 kHz		70		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

(T_J = 25°C Unless Otherwise Noted)

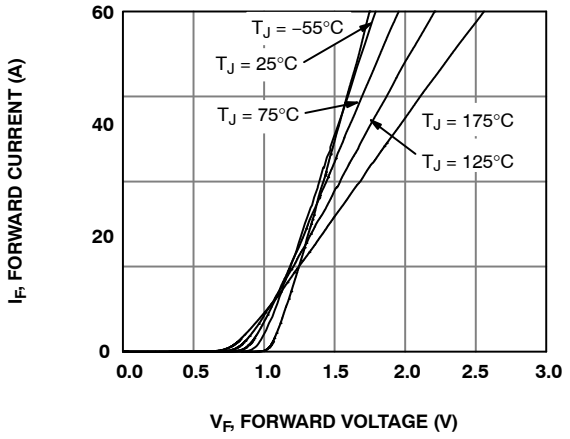


Figure 1. Forward Characteristics

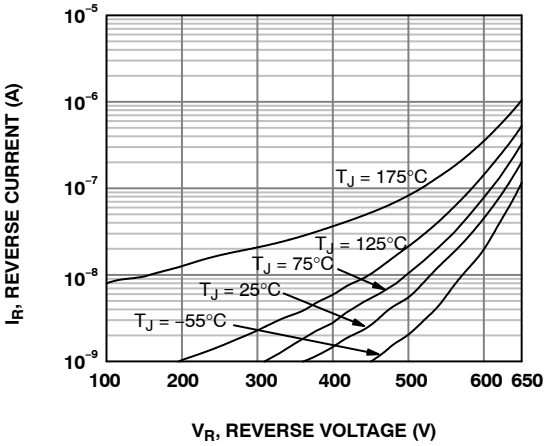


Figure 2. Reverse Characteristics

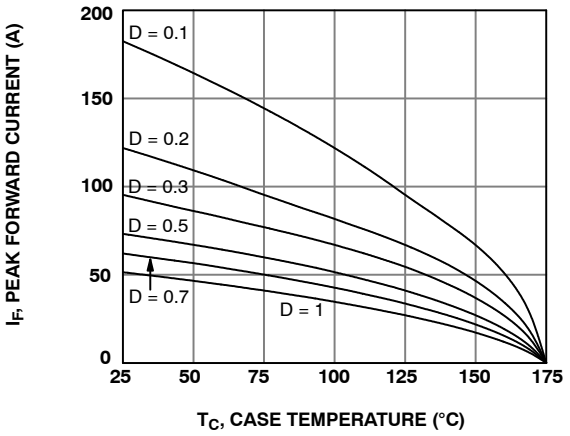


Figure 3. Current Derating

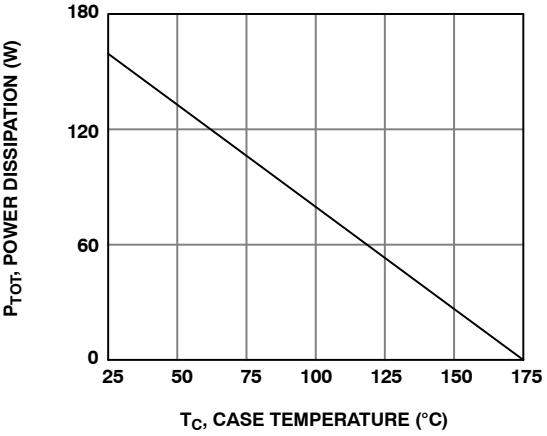


Figure 4. Power Dissipation

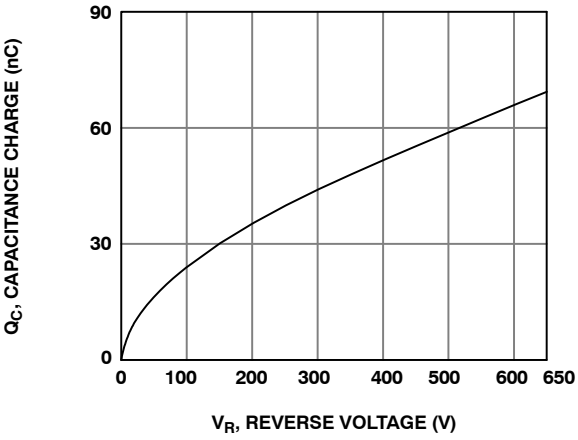


Figure 5. Capacitance Charge vs. Reverse Voltage

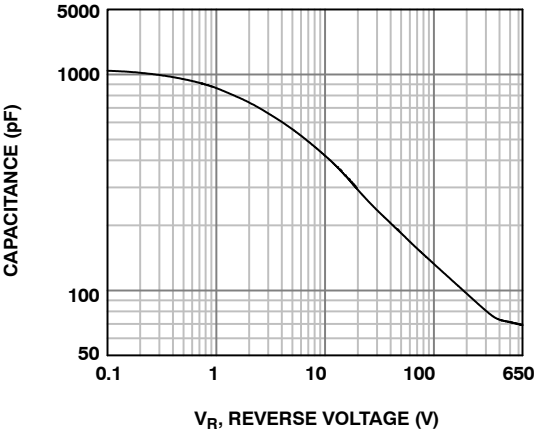


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C Unless Otherwise Noted)

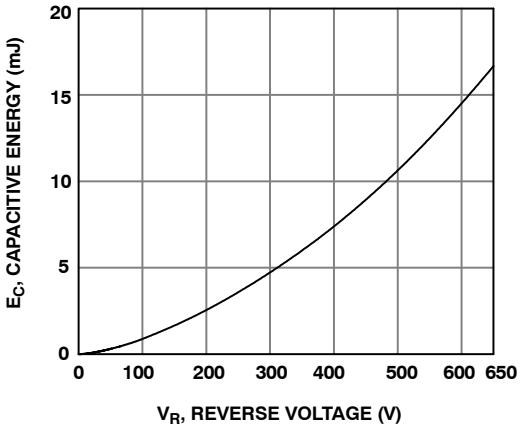


Figure 7. Capacitance Stored Energy

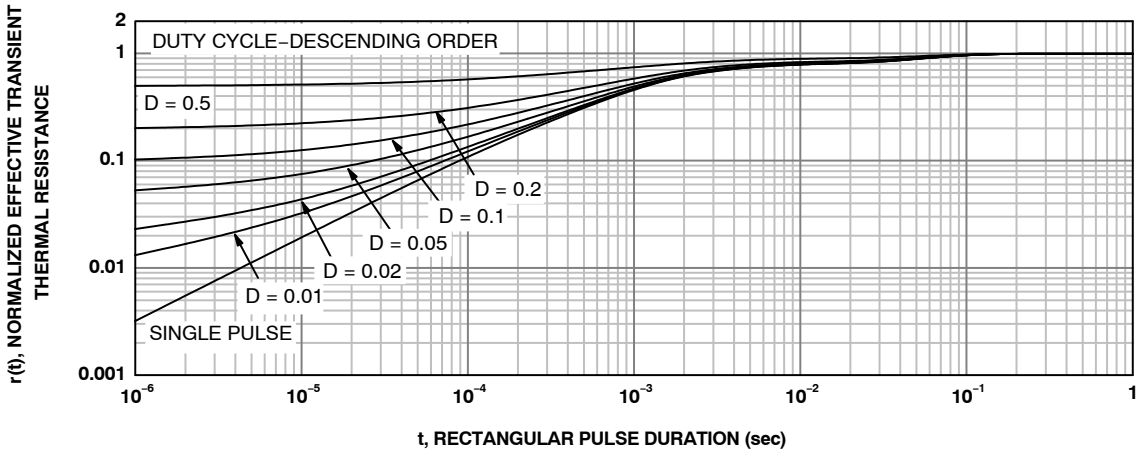


Figure 8. Junction−to−Case Transient Thermal Response Curve

TEST CIRCUIT AND WAVEFORMS

L = 0.5 mH
R < 0.1 Ω
V_{DD} = 50 V
EAVL = 1/2LI2 [$V_{R(AVL)}$ / ($V_{R(AVL)}$ − V_{DD})]
Q1 = IGBT (BV_{CES} > DUT $V_{R(AVL)}$)

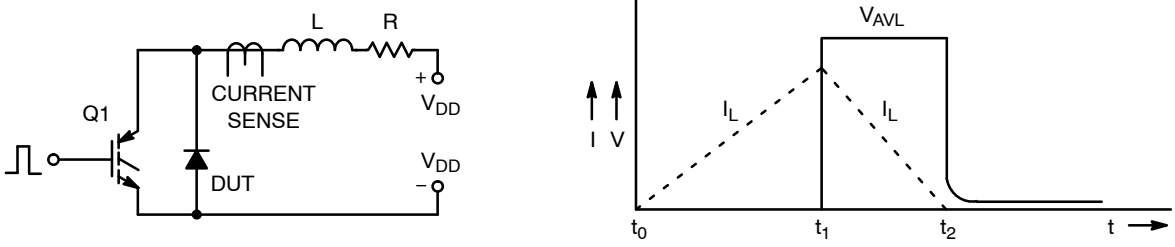


Figure 9. Unclamped Inductive Switching Test Circuit & Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DPAK3 (TO−252 3 LD)
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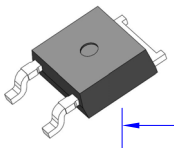
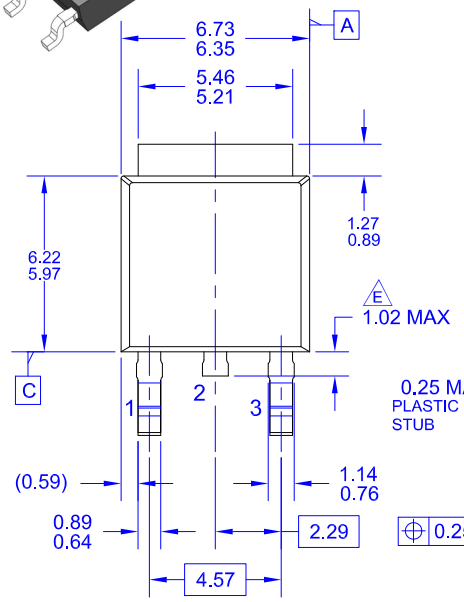
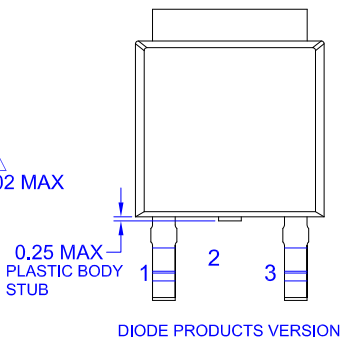
ISSUE O

DATE 30 SEP 2016



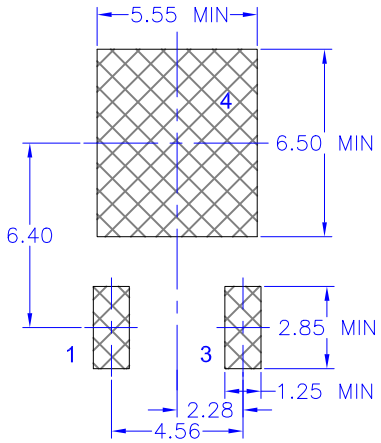


NON-DIODE PRODUCTS VERSION

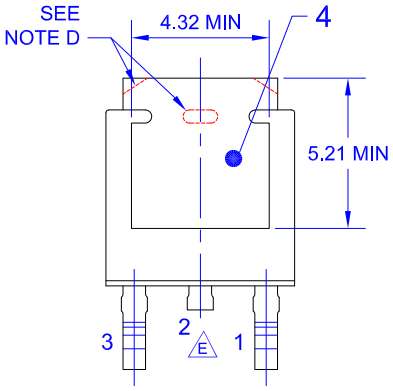


DIODE PRODUCTS VERSION

0.25 M A M C



LAND PATTERN RECOMMENDATION



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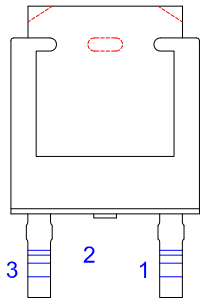
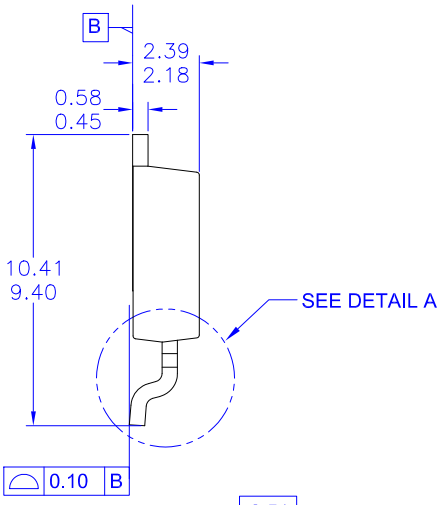
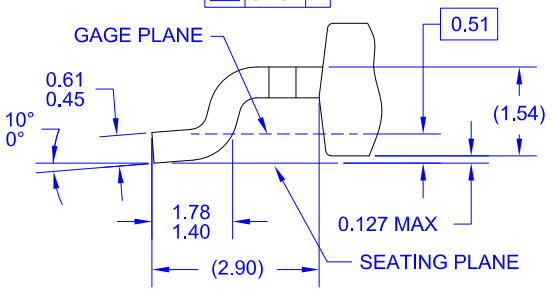


DIODE PRODUCTS VERSION



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

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DESCRIPTION:	**DPAK3 (TO−252 3 LD)**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

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