8 GHz to 16 GHz, 4-Channel, X Band and Ku Band Beamformer

Data Sheet **ADAR1000**

FEATURES

8 GHz to 16 GHz frequency range
Half-duplex for transmit and receive modes
Single-pin transmit and receive control
360° phase adjustment range
2.8° phase resolution
≥31 dB gain adjustment range
≤0.5 dB gain resolution
Bias and control for external transmit and receive modules
Memory for 121 prestored beam positions
Four −20 dBm to +10 dBm power detectors
Integrated temperature sensor
Integrated 8-bit ADC for power detectors and temperature sensor
Programmable bias modes
4-wire SPI interface

APPLICATIONS

Phased array radar
Satellite communications systems

GENERAL DESCRIPTION

The ADAR1000 is a 4-channel, X and Ku frequency band, beamforming core chip for phased arrays. This device operates in half-duplex between receive and transmit modes. In receive mode, input signals pass through four receive channels and are combined in a common RF_IO pin. In transmit mode, the RF_IO input signal is split and passes through the four transmit channels. In both modes, the ADAR1000 provides a ≥31 dB gain adjustment range and a full 360° phase adjustment range in the radio frequency (RF) path, with 6-bit resolution (less than ≤0.5 dB and 2.8°, respectively).

A simple 4-wire serial port interface (SPI) controls all of the on-chip registers. In addition, two address pins allow SPI control of up to four devices on the same serial lines. Dedicated transmit and receive load pins also provide synchronization of all core chips in the same array, and a single pin controls fast switching between the transmit and receive modes.

The ADAR1000 is available in a compact, 88-terminal, 7 mm × 7 mm, LGA package and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

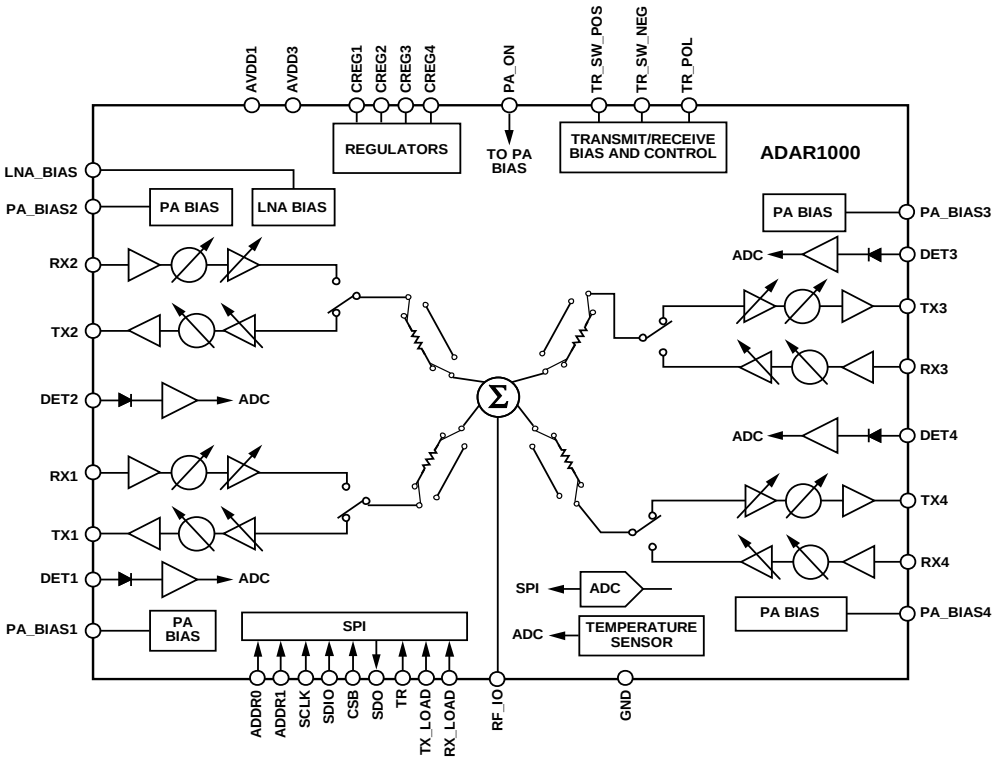

Figure 1.

Rev. A **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

3/2019—Rev. 0 to Rev. A

Change to Phase and Gain Switching Time Parameter, Table 1 ... 5
Added SPI Write All Mode Section and Figure 6; Renumbered Sequentially ... 7
Added Figure 8 ... 9
Changes to Table 5 ... 10
Reorganized Typical Performance Characteristics Section Layout ... 12
Changes to Figure 12 ... 12
Added Figure 21 ... 14
Changes to Figure 26 ... 14
Changes to Figure 31 ... 15
Changes to Figure 33 ... 16
Added Figure 40 ... 17
Added Figure 46 and Figure 49 ... 18
Changes to Figure 50 and Caption ... 18
Changes to Figure 54, Figure 55, and Figure 56 ... 19
Changes to Figure 60 and Figure 61 ... 20
Changes to Phase and Gain Control Section ... 24
Added Figure 86 ... 24
Changes to External Switch Control Section ... 25
Changes to Table 6 ... 26
Added Chip Addressing Section ... 27
Changes to Memory Access Section ... 27
Added Table 7, Table 8, and Table 9, and Table 10; Renumbered Sequentially ... 27
Added Phase Control Registers Section, Table 13, and Table 14 ... 34
Added Table 15 and Table 16 ... 35
Added Transmit/Receive Delay Control Section ... 37
Changes to Figure 92 ... 38
Changes to Table 20 ... 39
Added Table 21 ... 40
Added Powering the ADAR1000 Section, Figure 93 to Figure 97, and Table 22 ... 41

6/2018—Revision 0: Initial Version

SPECIFICATIONS

AVDD1 = −5 V, AVDD3 = +3.3 V, T_A = 25°C, and the device is programmed to the maximum channel gain and the nominal bias conditions, unless otherwise noted. Nominal bias register settings: Register 0x034 = 0x08, Register 0x035 = 0x55, Register 0x036 = 0x2D, and Register 0x37 = 0x06. Low power bias register settings: Register 0x034 = 0x05, Register 0x035 = 0x1A, Register 0x036 = 0x2A, and Register 0x37 = 0x03.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING CONDITIONS					
RF Range		8		16	GHz
Operating Temperature		−40		+85	°C
TRANSMIT SECTION	RF_IO, TX1, TX2, TX3, and TX4 pins				
Maximum Gain					
9.5 GHz			21		dB
11.5 GHz			19		dB
14 GHz			16		dB
Gain Flatness vs. Frequency	Across any 1 GHz bandwidth				dB
	From 9 GHz to 14 GHz		±1.0		dB
	From 8 GHz to 15 GHz		±1.7		dB
Gain Variation vs. Temperature	11.5 GHz		±2.5		dB
Output 1 dB Compression (P1dB)	Maximum gain setting				
Nominal Bias Setting					
9.5 GHz			10		dBm
11.5 GHz			10		dBm
14 GHz			10		dBm
Low Bias Setting					
9.5 GHz			6		dBm
11.5 GHz			8		dBm
14 GHz			7		dBm
Saturated Power (P_{SAT})	Maximum gain setting				
Nominal Bias Setting					
9.5 GHz			14		dBm
11.5 GHz			14		dBm
14 GHz			13		dBm
Low Bias Setting					
9.5 GHz			14		dBm
11.5 GHz			14		dBm
14 GHz			13		dBm
Gain Resolution			≤0.5		dB
Root Mean Square (RMS) Gain Error	Over phase settings and frequencies		0.2		dB
Phase Adjustment Range			360		Degrees
Phase Resolution			2.8		Degrees
RMS Phase Error	Over phase settings and frequencies		2		Degrees
Noise Figure	Maximum gain setting				
Nominal Bias Setting					
9.5 GHz			22		dB
11.5 GHz			23		dB
14 GHz			25		dB
Low Bias Setting					
9.5 GHz			22		dB
11.5 GHz			23		dB
14 GHz			25		dB
Channel to Channel Isolation[1]			−40		dB
Transmit Output to RF_IO	Maximum gain setting, 9.5 GHz		−60		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output Return Loss	TX1, TX2, TX3, or TX4 pin		−10		dB
Input Return Loss	RF_IO pin		−12		dB
Output Third-Order Intercept (IP3)	Maximum gain setting, 1 MHz carrier spacing				
Nominal Bias Setting					
9.5 GHz			20		dBm
11.5 GHz			21		dBm
14 GHz			22		dBm
Low Bias Setting					
9.5 GHz			15		dBm
11.5 GHz			16		dBm
14 GHz			16		dBm
RECEIVE SECTION					
Maximum Measured Gain[2]					
9.5 GHz	Nominal bias setting		10		dB
11.5 GHz			9		dB
14 GHz			7		dB
Maximum Channel Gain[3]					
9.5 GHz	Nominal bias setting		16		dB
11.5 GHz			15		dB
14 GHz			13		dB
Gain Flatness	Across any 1 GHz bandwidth				
	From 9 GHz to 14 GHz		±1.0		dB
	From 8 GHz to 15 GHz		±1.7		dB
Gain Variation vs. Temperature	11.5 GHz		±3		dB
Input P1dB					
Nominal Bias Setting					
9.5 GHz			−16		dBm
11.5 GHz			−16		dBm
14 GHz			−15		dBm
Low Bias Setting					
9.5 GHz			−13		dBm
11.5 GHz			−12		dBm
14 GHz			−10		dBm
Input IP3	Maximum gain setting, carrier spacing 1 MHz				
Nominal Bias Setting					
9.5 GHz			−7		dBm
11.5 GHz			−7		dBm
14 GHz			−6		dBm
Low Bias Setting					
9.5 GHz			−7		dBm
11.5 GHz			−6		dBm
14 GHz			−5		dBm
Gain Adjustment Range	Variable gain amplifier (VGA) and step attenuator		≥31		dB
Gain Resolution			≤0.5		dB
RMS Gain Error			0.2		dB
Phase Adjustment Range			360		Degrees
Phase Resolution			2.8		Degrees
RMS Phase Error			2		Degrees

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise Figure	Maximum gain setting				
Nominal Bias Setting					
9.5 GHz			8		dB
11.5 GHz			8		dB
14 GHz			9		dB
Low Bias Setting					
9.5 GHz			9		dB
11.5 GHz			10		dB
14 GHz			11		dB
Channel to Channel Isolation[4]			40		dB
RF_IO to Receive Isolation			60		dB
Input Return Loss			−10		dB
Output Return Loss	RF_IO pin		−12		dB
TEMPERATURE SENSOR					
Range		−40		+85	°C
Slope			0.8		LSB/°C
Nominal Analog-to-Digital Converter (ADC) Output	Power-on reset (POR) mode (transmit and receive not enabled), T_A = 25°C		145		Decimal
Resolution			8		Bits
TRANSMIT AND RECEIVE SWITCHING	TX_LOAD, RX_LOAD, and TR pins				
Transmit and Receive Switching Time	From TR at 50% to RF at 90%		180		ns
Phase and Gain Switching Time	From TX_LOAD or RX_LOAD at 50% to RF at 90%		20		ns
POWER DETECTOR	DET1, DET2, DET3, and DET4 pins				
RF Input Power Range	11.5 GHz	−20		+10	dBm
Input Return Loss			−10		dB
Nominal ADC Output Code	Input power (P_{IN}) = 0 dBm, 11.5 GHz		60		Decimal
Resolution			8		Bits
POWER AMPLIFIER (PA) DIGITAL-TO-ANALOG CONVERTER (DAC)	PA_BIAS1, PA_BIAS2, PA_BIAS3, and PA_BIAS4 pins				
Resolution			8		Bits
Voltage Range			−4.8 to 0		V
Source and Sink Current			−10 to +10		mA
Off to On Switching Time	From TR or CSB at 50% to V_{OUT} at 90%, V_{OUT} from −1 V to −2 V, 1 nF C_{LOAD}		60		ns
On to Off Switching Time	From TR or CSB at 50% to V_{OUT} at 10%, V_{OUT} from −1 V to −2 V, 1 nF C_{LOAD}		60		ns
LOW NOISE AMPLIFIER (LNA) DAC	LNA_BIAS pin				
Resolution			8		Bits
Voltage Range			−4.8 to 0		V
Source and Sink Current			−10 to+10		mA
Off to On Switching Time	From TR or CSB at 50% to V_{OUT} at 90%, V_{OUT} from −2 V to −1 V, 1 nF C_{LOAD}		60		ns
On to Off Switching Time	From TR or CSB at 50% to V_{OUT} at 10%, V_{OUT} from −1 V to −2 V, 1 nF C_{LOAD}		60		ns
TRANSMIT AND RECEIVE MODULE CONTROL	TR_SW_POS, TR_SW_NEG, TR_POL pins				
Voltage Range	TR_SW_NEG, TR_POL		−4.8 to 0		V
	TR_SW_POS		0 to 3.2		V
Off to On Switching Time	From TR or CSB at 50% to V_{OUT} at 90%		15		ns
On to Off Switching Time	From TR or CSB at 50% to V_{OUT} at 10%		15		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	TR, RX_LOAD, TX_LOAD, CSB, SCLK, and SDIO pins				
Input High Voltage (V_{IH})		1.0			V
Input Low Voltage (V_{IL})				0.3	V
High and Low Input Current, (I_{INH}, I_{INL})			±1		µA
Input Capacitance (C_{IN})			1		pF
LOGIC OUTPUTS	SDO and SDIO pins				
Output High Voltage, (V_{OH})	Output high current (I_{OH}) = −10 mA	1.4			V
Output Low Voltage, (V_{OL})	Output low current (I_{OL}) = 10 mA			0.4	V
POWER SUPPLIES					
AVDD1		−5.25	−5	−4.75	V
AVDD3		3.1	3.3	3.5	V
I_{AVDD1}	Quiescent (reset state)		−4		mA
I_{AVDD1}	PA bias outputs fully loaded		−50		mA
I_{AVDD3}					
Reset Mode (Standby)			23		mA
Transmit Mode	Four channels enabled, nominal bias		350		mA
	Four channels enabled, low bias setting		240		mA
Receive Mode	Four channels enabled, nominal bias		260		mA
	Four channels enabled, low bias setting		160		mA

[1] From one transmit channel port to another, both channels must be set to the maximum gain.
[2] Measured gain is the ratio of the output power at RF_IO to the input power applied to any single receive port, with the other three receive ports terminated in 50 Ω.
[3] Channel gain is the ratio of the output power at RF_IO to the input power applied to any single receive port, with the other three receive ports driven and phased for coherent combining, excluding the 6 dB combining gain. The channel gain is approximately 6 dB higher than the measured gain.
[4] From one receive channel port to another, both channels must be set to the maximum gain.

TIMING SPECIFICATIONS

AVDD1 = −5 V, AVDD3 = +3.3 V, T_A = 25°C, unless otherwise noted.

Table 2. SPI Timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Maximum Clock Rate (t_{SCLK})		25		MHz	
Minimum Pulse Width High (t_{PWH})		10		ns	
Minimum Pulse Width Low (t_{PWL})		10		ns	
Setup Time, SDIO to SCLK (t_{DS})		5		ns	
Hold Time, SDIO to SCLK (t_{DH})		5		ns	
Data Valid, SDO to SCLK (t_{DV})		5		ns	
Setup Time, CSB to SCLK (t_{DCS})		10		ns	
SDIO, SDO Rise Time (t_R)		20		ns	Outputs loaded with 80 pF, 10% to 90%
SDIO, SDO Fall Time (t_F)		20		ns	Outputs loaded with 80 pF, 10% to 90%

Timing Diagrams

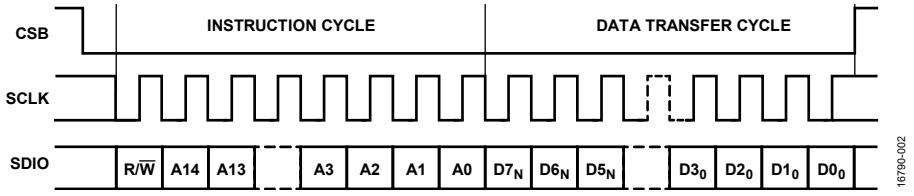


Figure 2. Serial Port Interface Register Timing (MSB First)

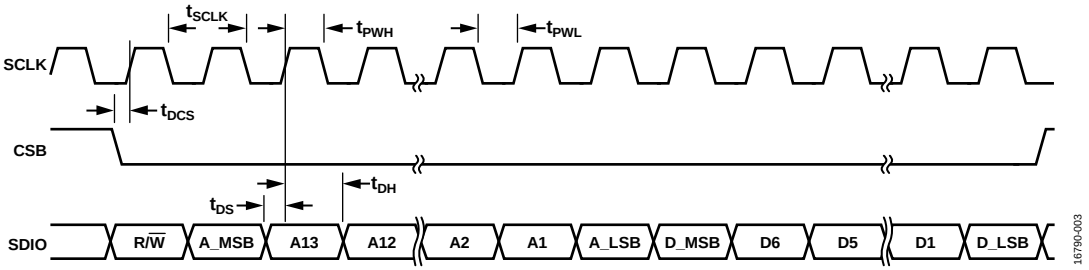


Figure 3. Timing Diagram for the Serial Port Interface Register Write

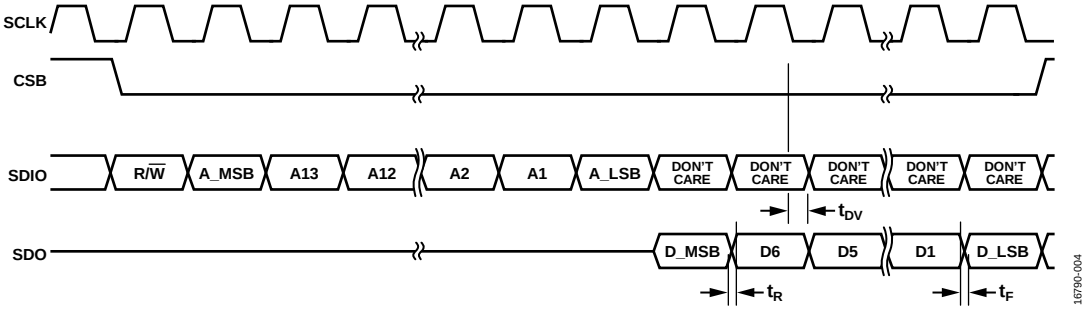


Figure 4. Timing Diagram for Serial Port Interface Register Read

SPI Block Write Mode

Data can be written to the SPI registers in a block write mode, where the register address automatically increments, and data for consecutive registers can be written without sending new address bits. Data writing can be continued indefinitely until CSB is raised again, ending the write process.

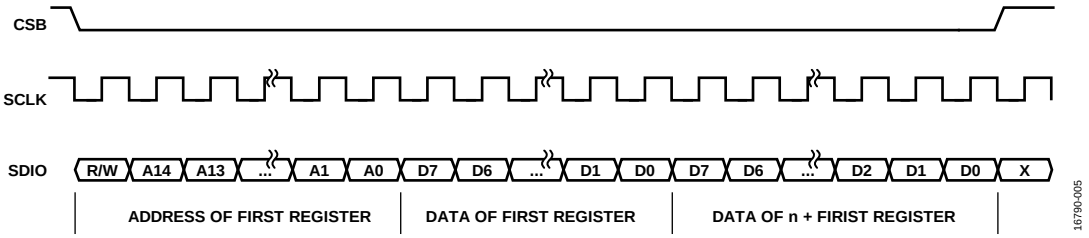


Figure 5. Timing Diagram for Block Write Mode

SPI Write All Mode

Data can be written to the SPI registers in a write all mode, where the data is written to all chips connected to the SPI bus with a single write command, regardless of the ADDR1 and ADDR0 values, by setting address Bits[A14:A11] = 0001. The write all mode allows the user to broadcast the same data, up to four ADAR1000 devices, with a single SPI write.

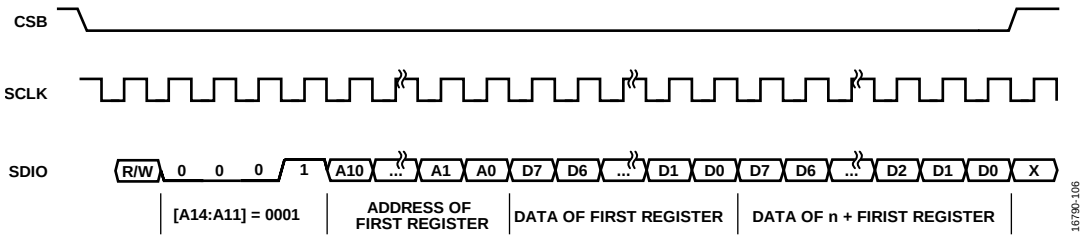


Figure 6. SPI Write All Instruction and Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
AVDD1 to GND	−5.5 V
AVDD3 to GND	3.6 V
Digital Input/Output Voltage to GND	2.0 V
Maximum RF Input Power	20 dBm
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Junction Temperature (T_J)	135°C
Electrostatic Discharge (ESD)	
Charged Device Model (CDM)	±500 V
Human Body Model (HBM)	±2500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. The PCB thermal design requires careful attention.

θ_{JA} is the junction to the ambient with the exposed pad soldered down, and θ_{JC} is the junction to the exposed pad.

Table 4. Thermal Resistance

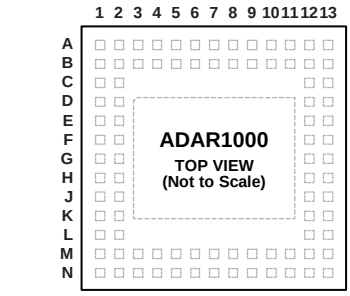
Package Type	θ_{JA}	θ_{JC}	Unit
CC-88-1[1]	18.7	10.1	°C/W

[1] Simulated based on PCB specified in JESD-51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. CONNECT THE EXPOSED PAD AND ALL GND CONNECTIONS TO A LOW IMPEDANCE GROUND PLANE ON THE PCB.

16790-006

Figure 7. Pin Configuration (Top View)

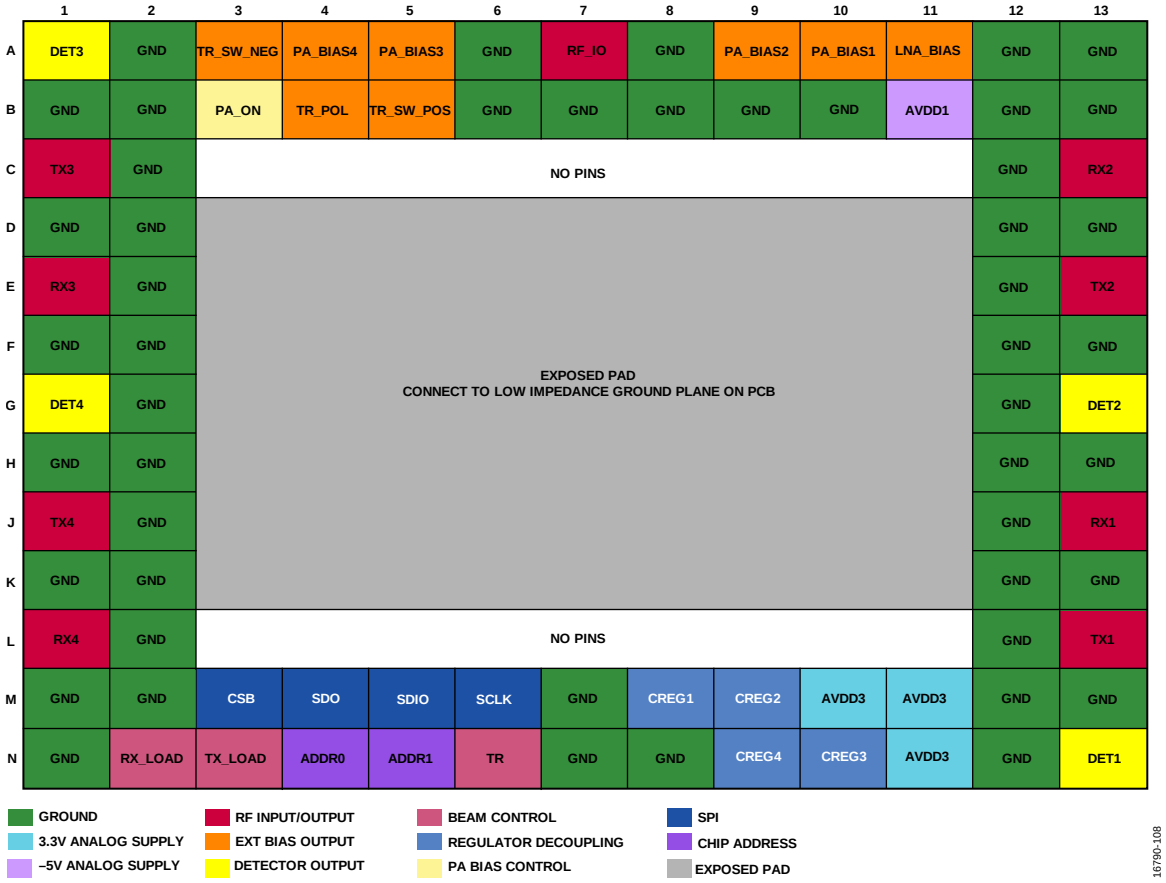


Figure 8. Pin Configuration, Color Coded (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	DET3	Channel 3 Power Detector Input. DET3 is internally ac-coupled and enabled by Register 0x030, Bit 1. The nominal operating input power range is −20 dBm to +10 dBm.
A2, A6, A8, A12, A13, B1, B2, B6 to B10, B12, B13, C2, C12, D1, D2, D12, D13, E2, E12, F1, F2, F12, F13, G2, G12, H1, H2, H12, H13, J2, J12, K1, K2, K12, K13, L2, L12, M1, M2, M7, M12, M13, N1, N7, N8, N12	GND	RF Ground. Tie all ground pins together to a low impedance plane on the PCB board.
A3	TR_SW_NEG	Gate Control Output for External Transmit and Receive Switch (0 V or −5 V).
A4	PA_BIAS4	Gate Bias Output for Channel 4 External PA. Output ranges from 0 to −4.8 V, controlled by a combination of the PA_ON pin, Register 0x02C (CH4_PA_BIAS_ON value), and Register 0x049 (CH4_PA_BIAS_OFF value). Output is set to the CH4_PA_BIAS_OFF value if the PA_ON pin is at logic low.
A5	PA_BIAS3	Gate Bias Output for Channel 3 External PA. Output ranges from 0 to −4.8 V, controlled by a combination of the PA_ON pin, Register 0x02B (CH3_PA_BIAS_ON value), and Register 0x048 (CH3_PA_BIAS_OFF value). Output is set to the CH3_PA_BIAS_OFF value if the PA_ON pin is at logic low.
A7	RF_IO	Common RF Pin for Input in Transmit Mode and Output in Receive Mode.
A9	PA_BIAS2	Gate Bias Output for Channel 2 External PA. Output ranges from 0 to −4.8 V, controlled by a combination of the PA_ON pin, Register 0x02A (CH2_PA_BIAS_ON value), and Register 0x047 (CH2_PA_BIAS_OFF value). Output is set to the CH2_PA_BIAS_OFF value if the PA_ON pin is at logic low.
A10	PA_BIAS1	Gate Bias Output for Channel 1 External PA. Output ranges from 0 to −4.8 V, controlled by a combination of the PA_ON pin, Register 0x029 (CH1_PA_BIAS_ON value), and Register 0x046 (CH1_PA_BIAS_OFF value). Output is set to the CH1_PA_BIAS_OFF value if the PA_ON pin is at logic low.
A11	LNA_BIAS	Gate Bias Output for External LNA. Output ranges from 0 to −4.8 V, controlled by a combination of Register 0x030 (Bit 4, LNA_BIAS_OUT_EN), Register 0x02D (LNA_BIAS_ON value), and Register 0x04A (LNA_BIAS_OFF value). Output floats if Register 0x030, Bit 4 is at logic low.
B3	PA_ON	PA Enable Input. Set this pin to logic high for PA bias voltages to assume the values set by the EXT_PAx_BIAS_ON and EXT_PAx_BIAS_OFF registers (x = 1 to 4). All PA_BIASx outputs take on the corresponding CHx_PA_BIAS_OFF value if the PA_ON pin is at logic low. This pin is internally pulled up to the 1.8 V low dropout (LDO) regulator bias voltage with a 100 kΩ resistor.
B4	TR_POL	Gate Control Output for External Polarization Switch (0 V or −5 V).
B5	TR_SW_POS	Gate Control Positive Output for External Transmit and Receive Switch (0 V or 3.3 V).
B11	AVDD1	−5 V Power Supply. AVDD1 provides the negative currents for sinking the PA_BIASx and LNA_BIAS outputs. If the PA_BIASx and LNA_BIAS pins are not used, the user can connect AVDD1 to ground to reduce power consumption and to use a single voltage supply.
C1	TX3	Channel 3 Output in Transmit Mode.
C13	RX2	Channel 2 Input in Receive Mode.
E1	RX3	Channel 3 Input in Receive Mode.
E13	TX2	Channel 2 Output in Transmit Mode.
G1	DET4	Channel 4 Power Detector Input. DET4 is internally ac-coupled and enabled by Register 0x030, Bit 0. The nominal operating input power range is −20 dBm to +10 dBm.
G13	DET2	Channel 2 Power Detector Input. DET2 is internally ac-coupled and enabled by Register 0x030, Bit 2. The nominal operating input power range is −20 dBm to +10 dBm.
J1	TX4	Channel 4 Output in Transmit Mode.
J13	RX1	Channel 1 Input in Receive Mode.
L1	RX4	Channel 4 Input in Receive Mode.
L13	TX1	Channel 1 Output in Transmit Mode.
M3	CSB	SPI Chip Select Input (1.8 V CMOS Logic). Serial communication is enabled when CSB goes low. When CSB goes high, serial data is loaded into the register corresponding to the address in the instruction cycle (see Figure 2) in write mode.

Pin No.	Mnemonic	Description
M4	SDO	SPI Serial Data Output (1.8 V CMOS Logic).
M5	SDIO	SPI Serial Data Input and Output (1.8 V CMOS Logic).
M6	SCLK	SPI Serial Clock Input (1.8 V CMOS Logic). In write mode, data is sampled on the rising edge of SCLK. During a read cycle, output data changes at the falling edge of SCLK.
M8	CREG1	Decoupling Pin for 1.8 V LDO Reference. Connect a 1 µF capacitor through a low impedance path from this pin to a ground plane.
M9	CREG2	Decoupling Pin for 2.8 V LDO Output. Connect a 1 µF capacitor through a low impedance path from this pin to a ground plane.
M10, M11, N11	AVDD3	3.3 V Voltage Power Supply Inputs.
N2	RX_LOAD	Load Receive Registers Input (1.8 V CMOS Logic). A rising edge causes contents in the receive channel holding registers to transfer to the working registers.
N3	TX_LOAD	Load Transmit Registers Input (1.8 V CMOS Logic). A rising edge causes contents in the transmit channel holding registers to transfer to the working registers.
N4	ADDR0	Chip Select Address 0 Input (1.8 V CMOS Logic). ADDR1 and ADDR0 together select one of four core chips to accept the serial instructions and data.
N5	ADDR1	Chip select Address 1 Input (1.8 V CMOS Logic). ADDR1 and ADDR0 together select one of four core chips to accept the serial instructions and data.
N6	TR	Transmit and Receive Mode Select Input (1.8 V CMOS Logic).
N9	CREG4	Decoupling Pin for 1.8 V LDO Output. Connect a 1 µF capacitor through a low impedance path from this pin to a ground plane.
N10	CREG3	Decoupling Pin for 2.8 V LDO Reference. Connect a 1 µF capacitor through a low impedance path from this pin to a ground plane.
N13	DET1	Channel 1 Power Detector Input. DET1 is internally ac-coupled and enabled by Register 0x030, Bit 3. The nominal operating input power range is −20 dBm to +10 dBm.
	EPAD	Exposed Pad. Connect the exposed pad and all GND connections to a low impedance ground plane on the PCB.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = −5 V, ADVDD3 = +3.3 V, T_A = 25°C, nominal bias settings and reported gain is measured gain, unless otherwise stated.

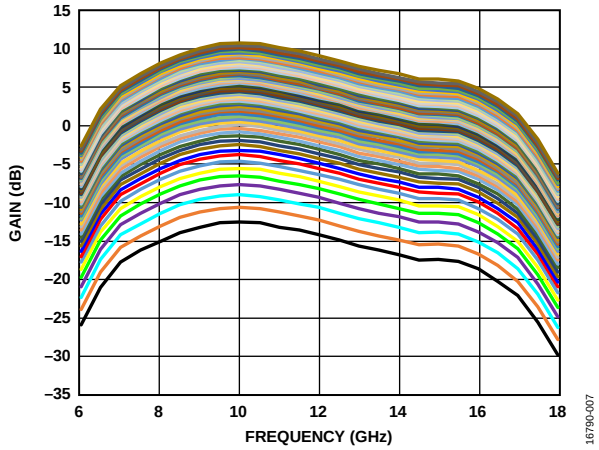


Figure 9. Gain vs. Frequency for Gain Settings from 0 to 127, Single Receive Channel

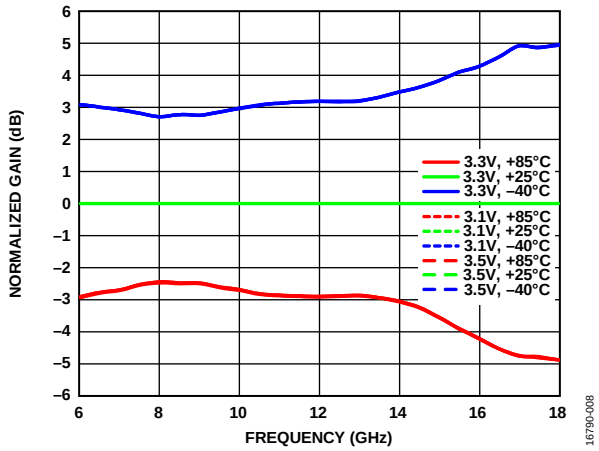


Figure 10. Normalized Gain vs. Frequency over AVDD3 Supply and Temperature, Receive Channel

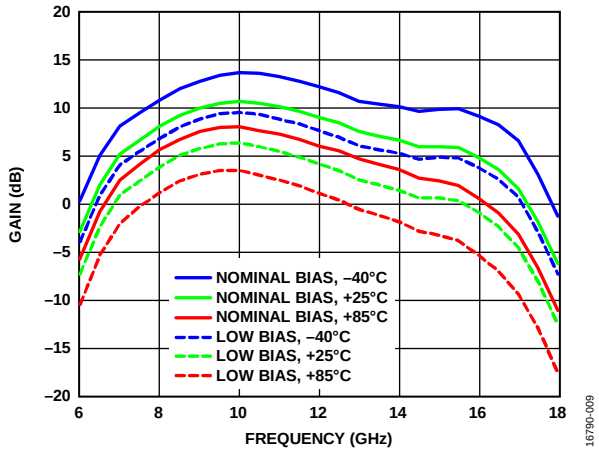


Figure 11. Gain vs. Frequency over Bias and Temperature, Receive Channel

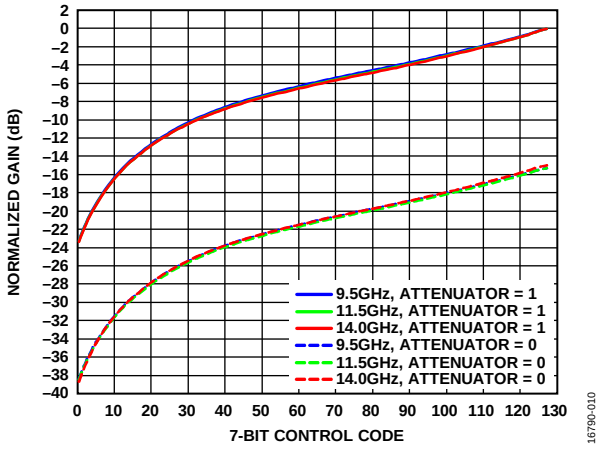


Figure 12. Normalized Gain vs. 7-Bit Gain Control Code, Single Receive Channel

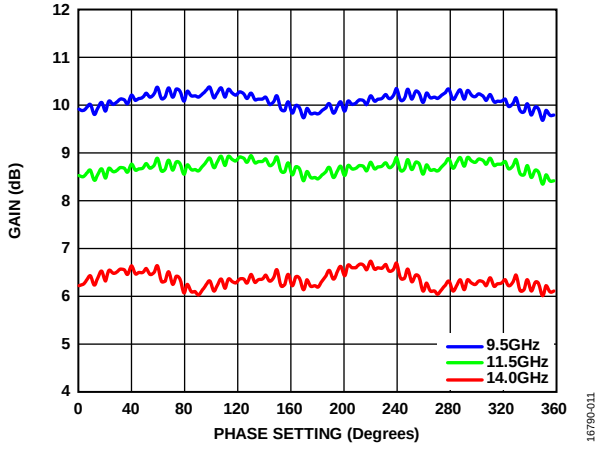


Figure 13. Gain vs. Phase Setting over Frequency, Receive Channel

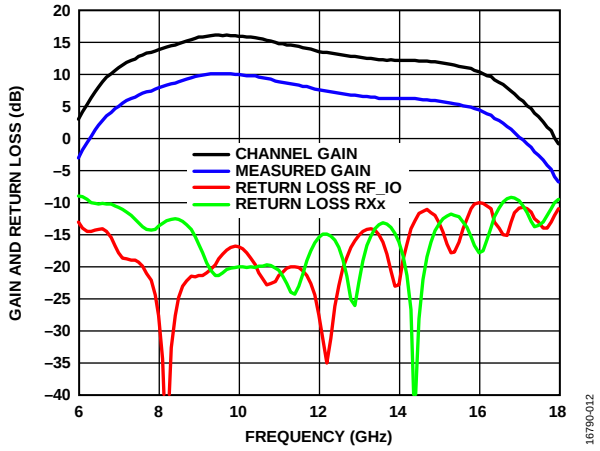


Figure 14. Gain and Return Loss vs. Frequency, at Maximum Gain, Receive Channel

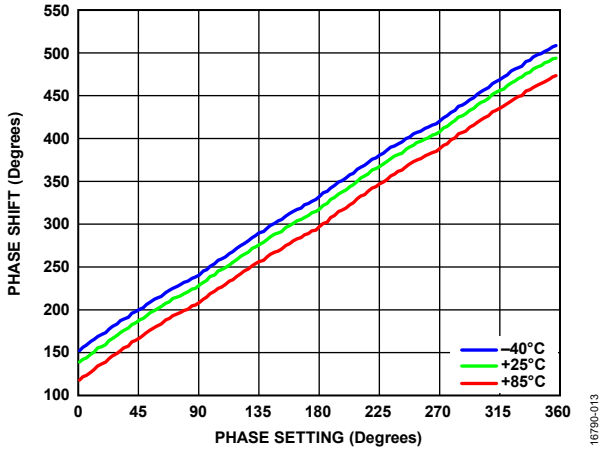


Figure 15. Phase Shift vs. Phase Setting over Temperature, Receive Channel

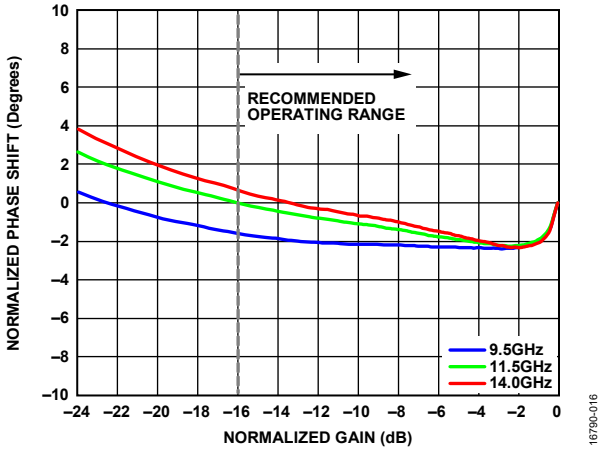


Figure 18. Normalized Phase Shift vs. Normalized Gain over Frequency, Receive Channel

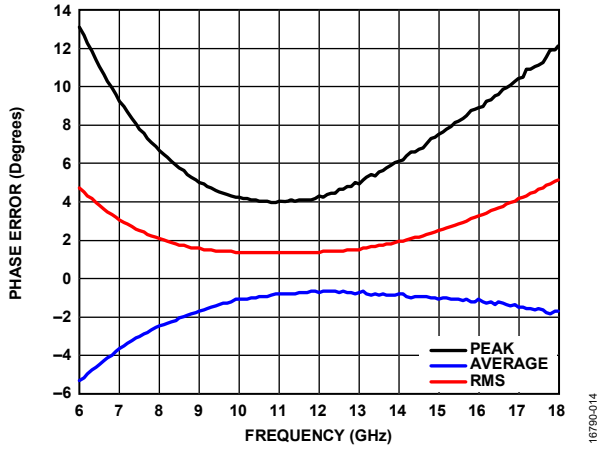


Figure 16. Phase Error vs. Frequency, Receive Channel

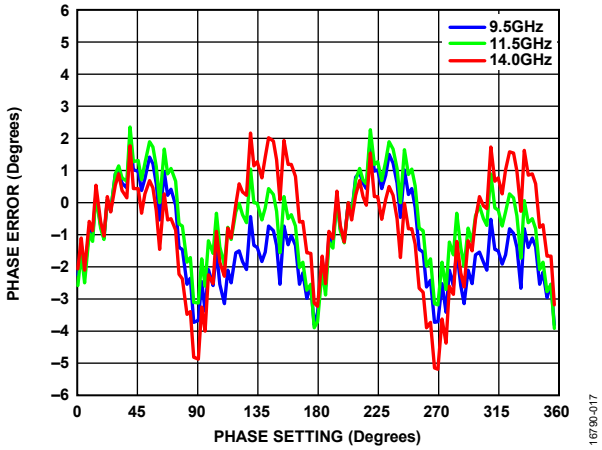


Figure 19. Phase Error vs. Phase Setting over Frequency, Receive Channel

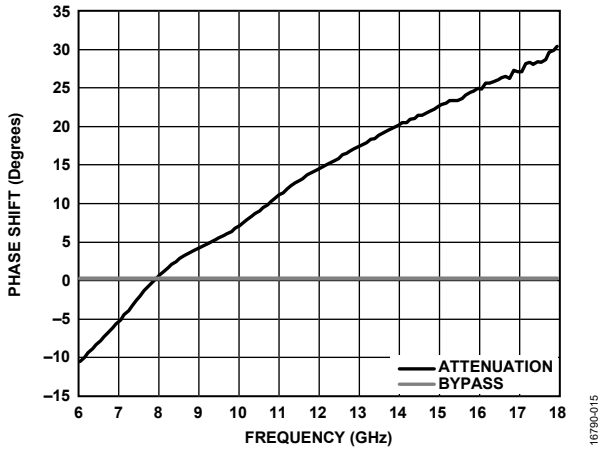


Figure 17. Phase Shift vs. Frequency for Step Attenuator in Attenuation Mode, Normalized to Bypass Mode, Receive Channel

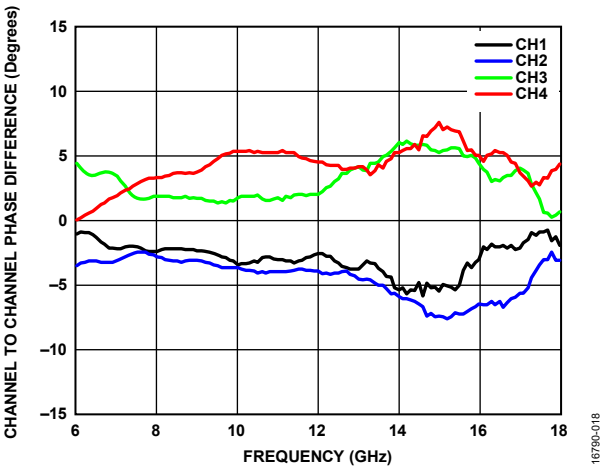


Figure 20. Channel to Channel Phase Difference vs. Frequency, Receive Channel

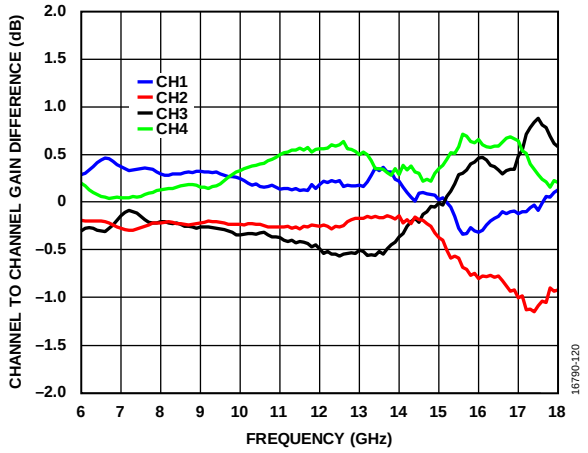


Figure 21. Channel to Channel Gain Difference vs. Frequency, Receive Channel

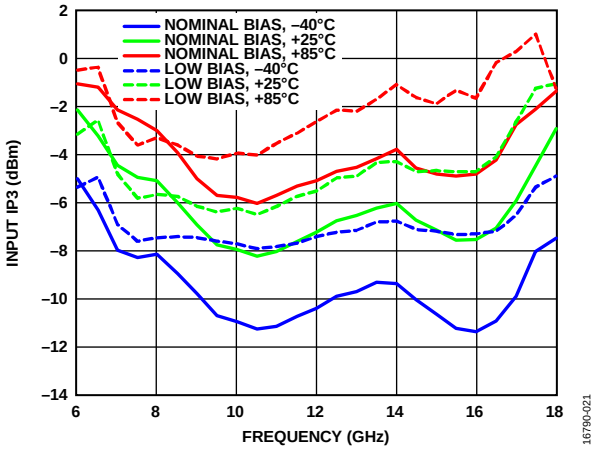


Figure 24. Input IP3 vs. Frequency over Bias and Temperature, Receive Channel

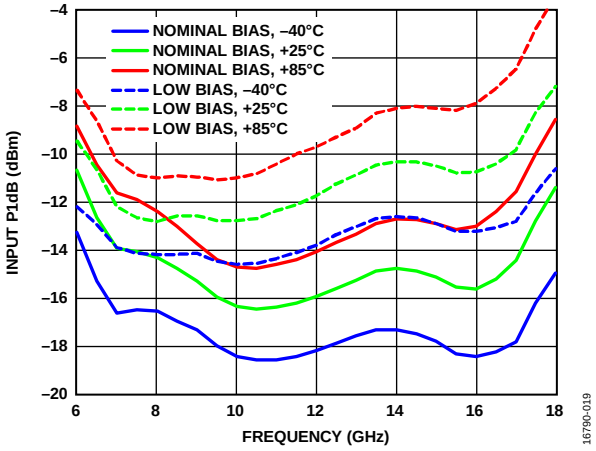


Figure 22. Input P1dB vs. Frequency over Bias and Temperature, Receive Channel

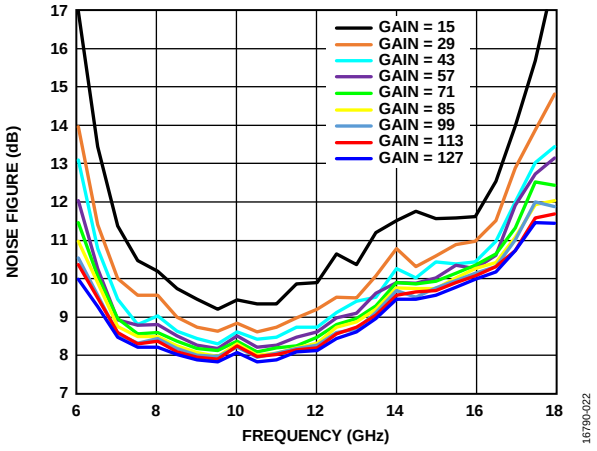


Figure 25. Noise Figure vs. Frequency over Gain, Receive Channel

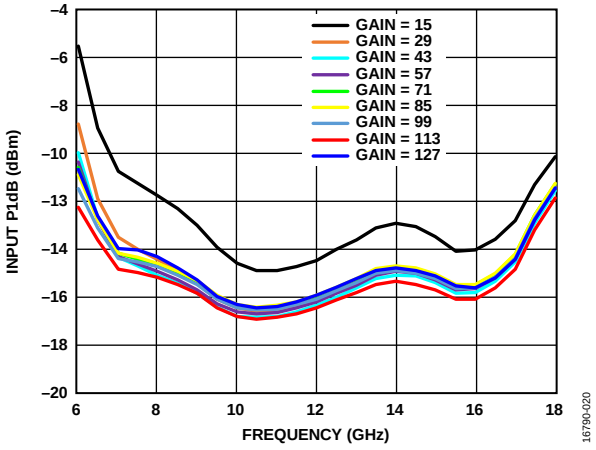


Figure 23. Input P1dB vs. Frequency over Gain, Receive Channel

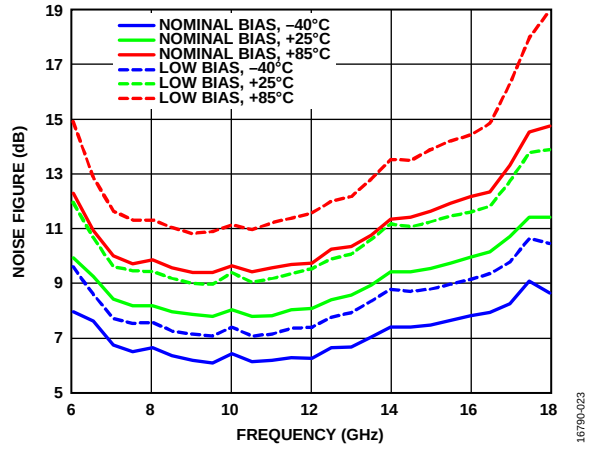


Figure 26. Noise Figure vs. Frequency over Bias and Temperature, Receive Channel

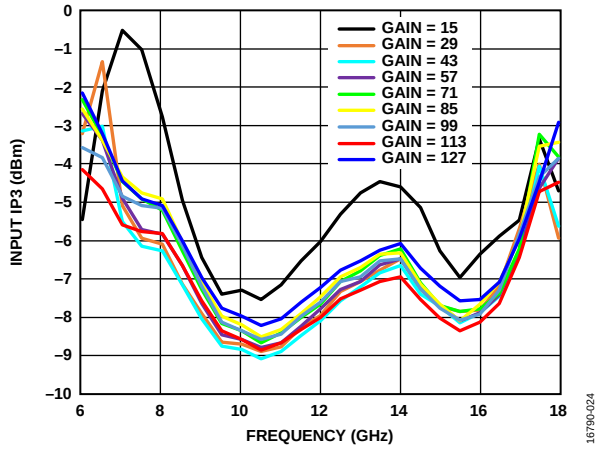


Figure 27. Input IP3 vs. Frequency over Gain, Receive Channel

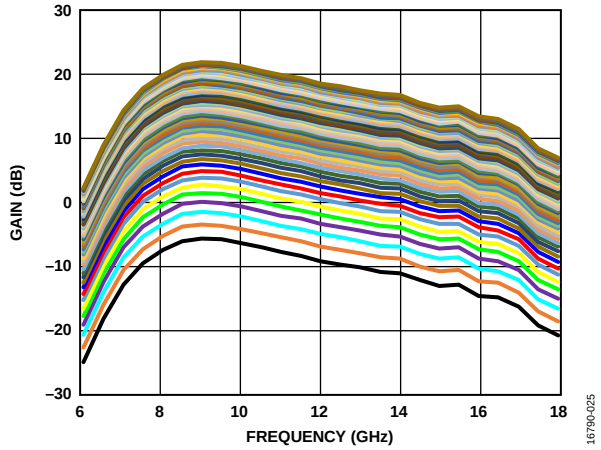


Figure 28. Gain vs. Frequency over Gain Settings from 0 to 127, Single Transmit Channel

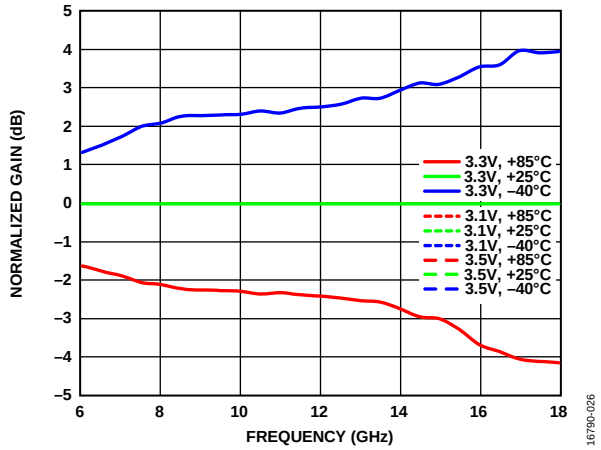


Figure 29. Normalized Gain vs. Frequency over AVDD3 Supply and Temperature, Transmit Channel

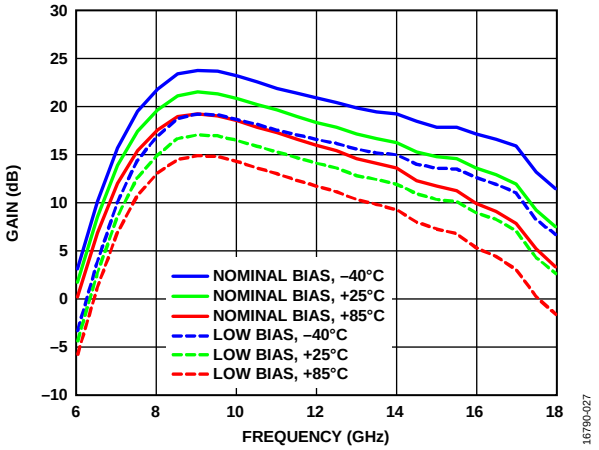


Figure 30. Gain vs. Frequency over Bias and Temperature, Single Transmit Channel

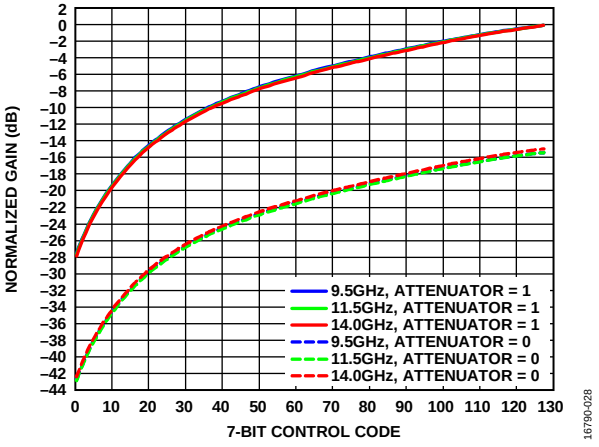


Figure 31. Normalized Gain vs. 7-Bit Gain Control Code, Transmit Channel

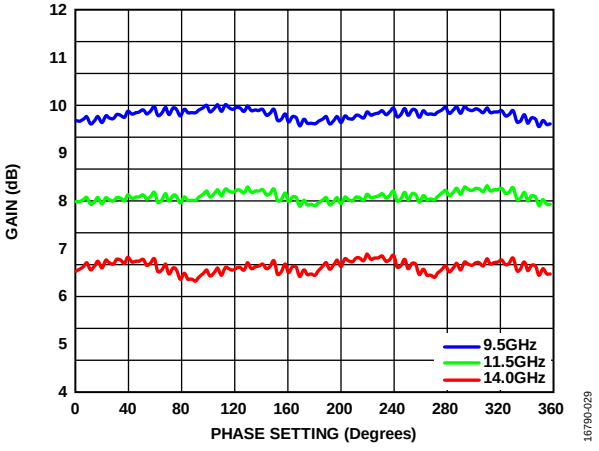


Figure 32. Gain vs. Phase Setting over Frequency, Single Transmit Channel

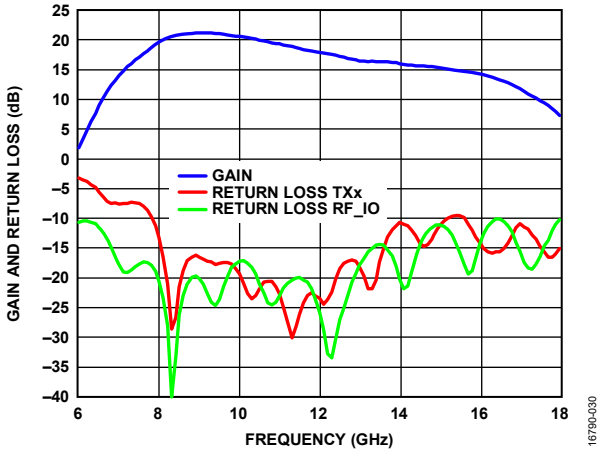


Figure 33. Gain and Return Loss vs. Frequency, Transmit Channel

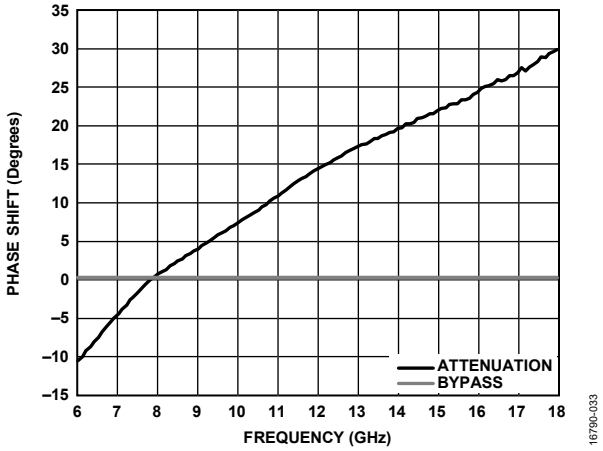


Figure 36. Phase Shift vs. Frequency for Step Attenuator in Attenuation Mode, Normalized to Bypass Mode, Transmit Channel

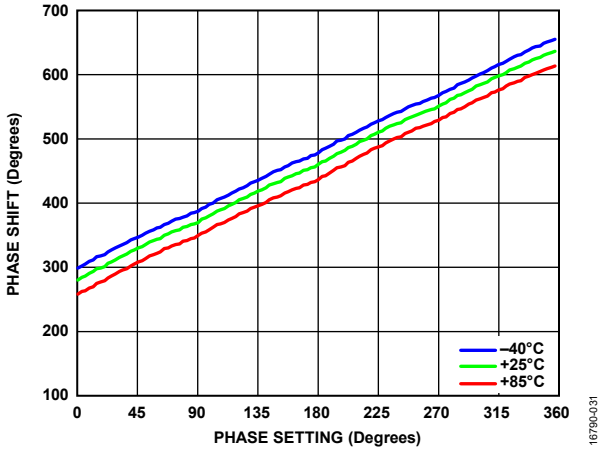


Figure 34. Phase Shift vs. Phase Setting over Temperature, Transmit Channel

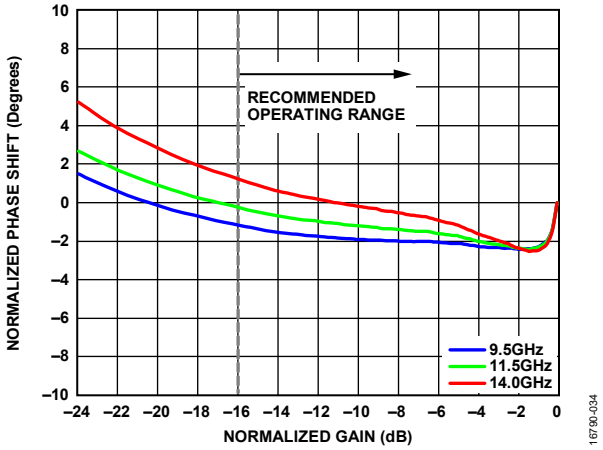


Figure 37. Normalized Phase Shift vs. Normalized Gain over Frequency, Transmit Channel

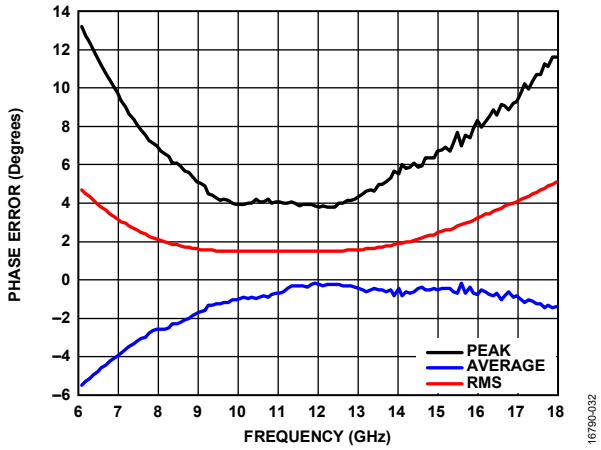


Figure 35. Phase Error vs. Frequency, Transmit Channel

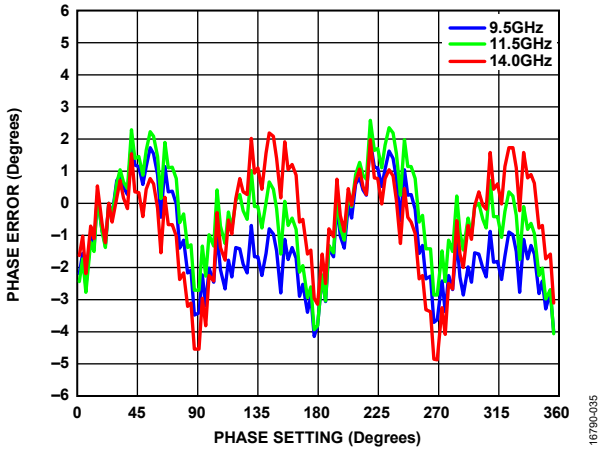


Figure 38. Phase Error vs. Phase Setting over Frequency, Transmit Channel

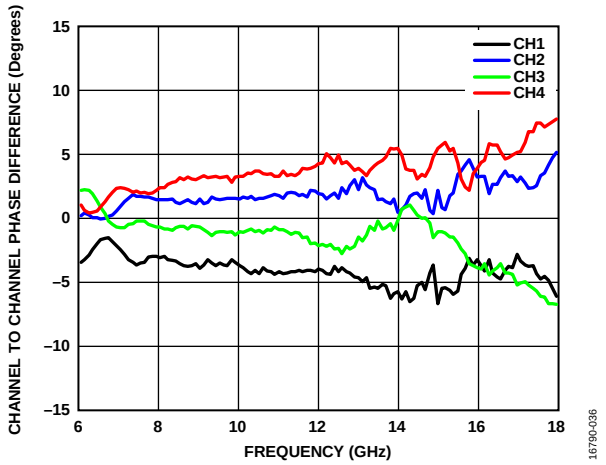


Figure 39. Channel to Channel Phase Difference vs. Frequency, Transmit Channel

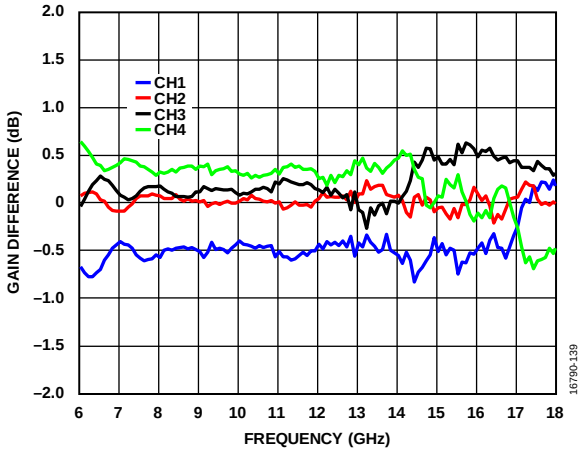


Figure 40. Channel to Channel Gain Difference vs. Frequency, Transmit Channel

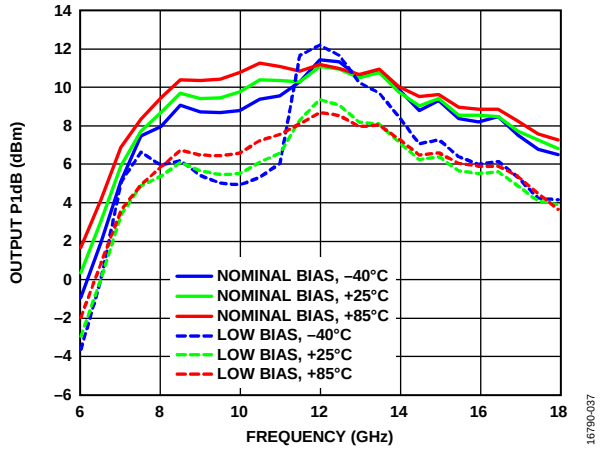


Figure 41. Output P1dB vs. Frequency over Bias and Temperature, Transmit Channel

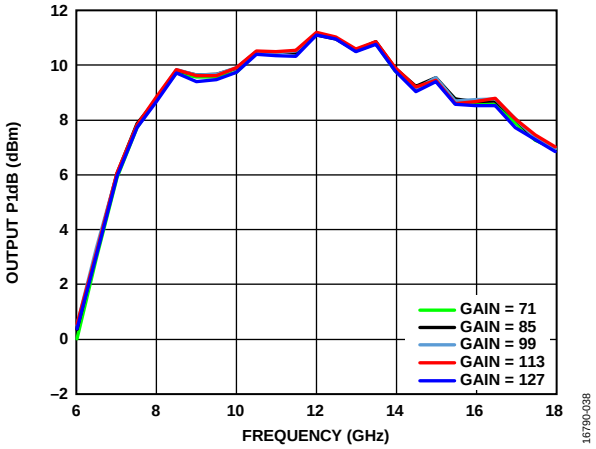


Figure 42. Output P1dB vs. Frequency over Gain, Transmit Channel

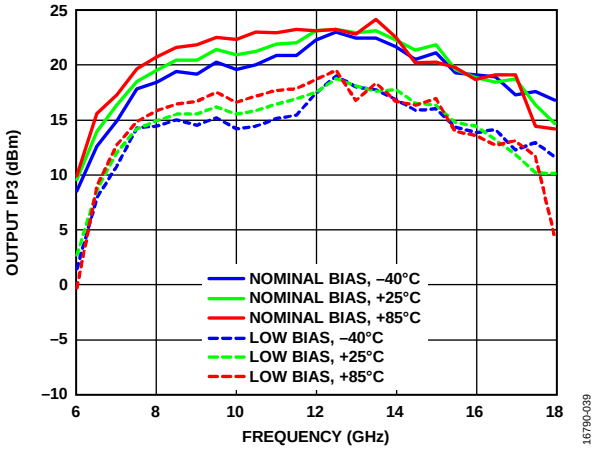


Figure 43. Output IP3 vs. Frequency over Bias and Temperature, Transmit Channel

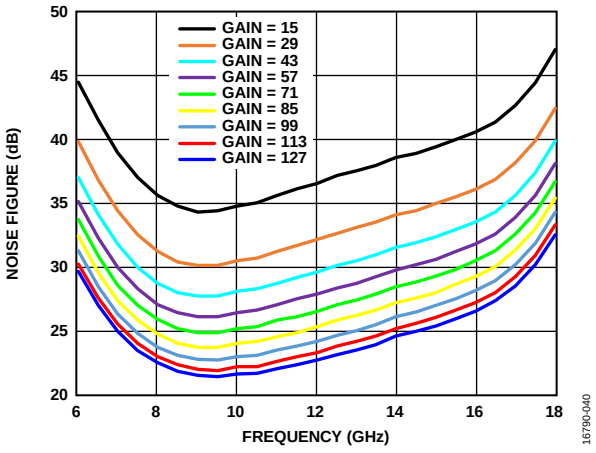


Figure 44. Noise Figure vs. Frequency over Gain, Transmit Channel

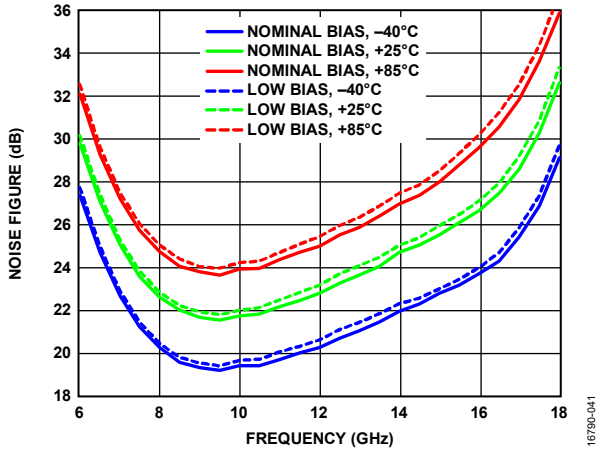


Figure 45. Noise Figure vs. Frequency over Bias and Temperature, Transmit Channel

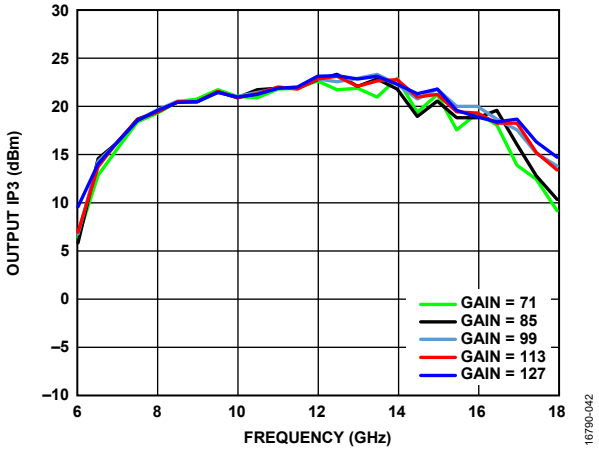


Figure 48. Output IP3 vs. Frequency over Gain, Transmit Channel

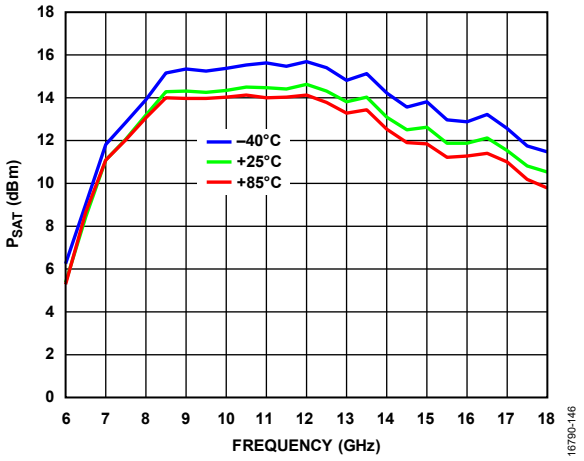


Figure 46. P_{SAT} vs. Frequency, Transmit Channel, Nominal Bias, Maximum Gain and Phase Set to 45°, All Channels Enabled

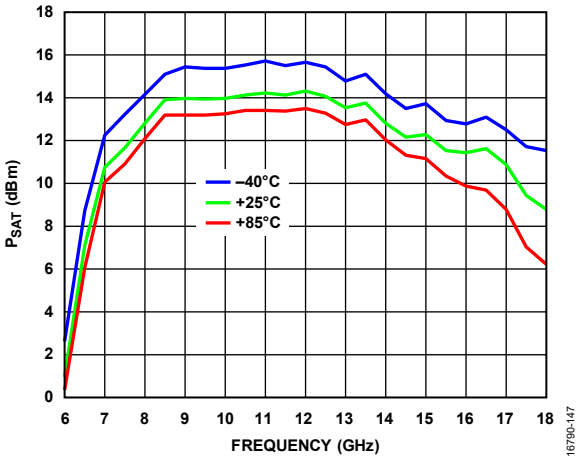


Figure 49. P_{SAT} vs. Frequency, Transmit Channel, Low Bias, Maximum Gain and Phase Set to 45°, All Channels Enabled

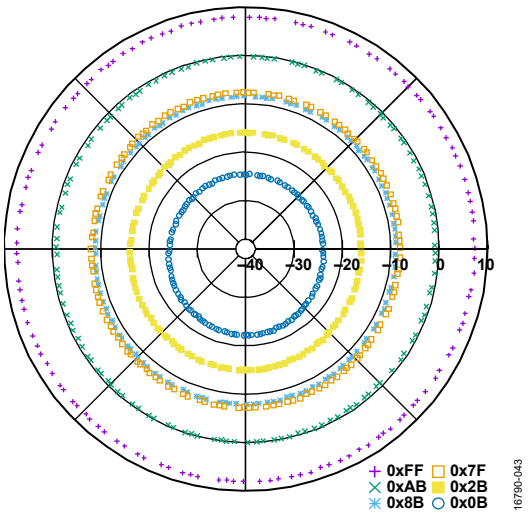


Figure 47. Gain Variation vs. Phase over Gain, 9.5 GHz, Receive Channel

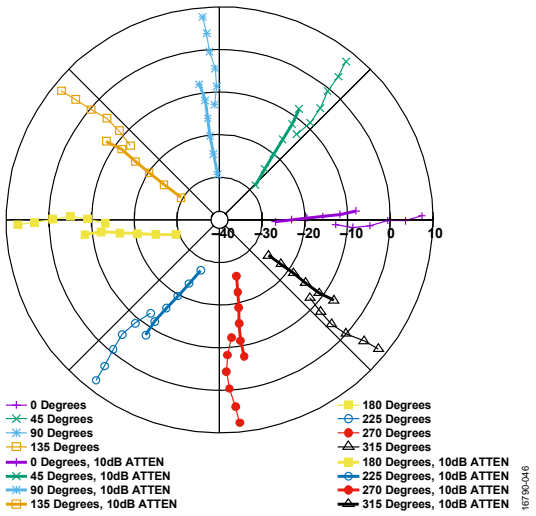


Figure 50. Phase Variation vs. Gain over Phase, 9.5 GHz, Receive Channel

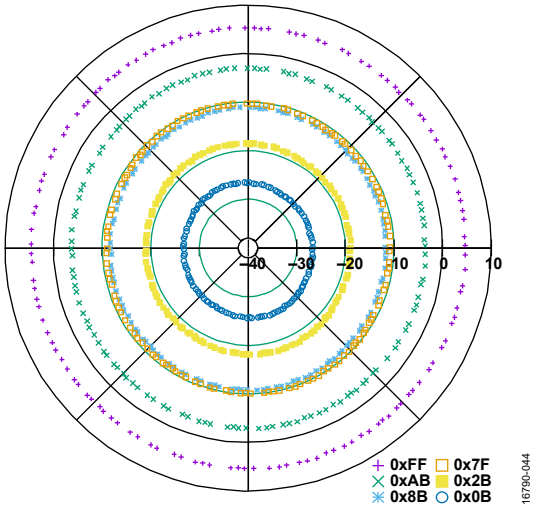


Figure 51. Gain Variation vs. Phase over Gain, 11.5 GHz, Receive Channel

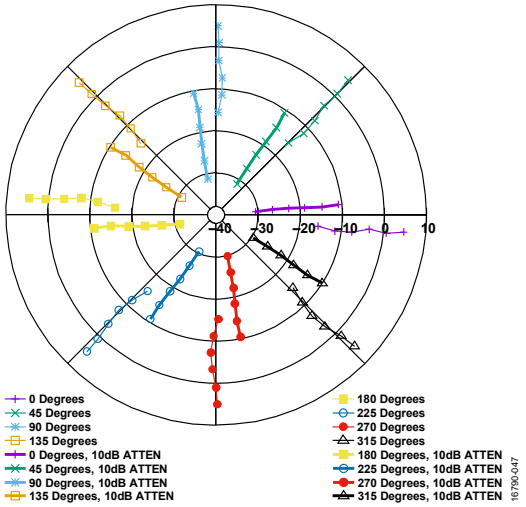


Figure 54. Phase Variation vs. Gain over Phase, 11.5 GHz, Receive Channel

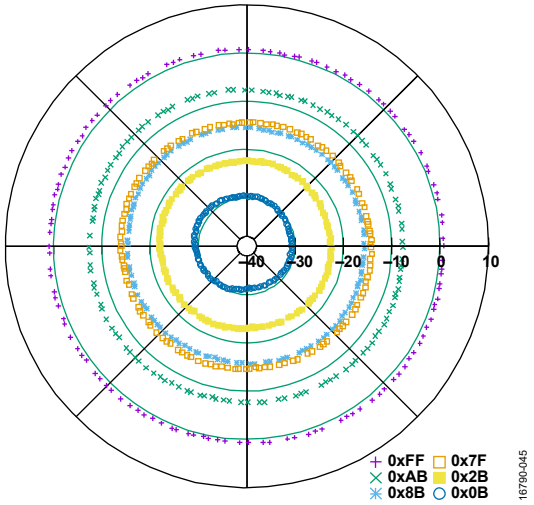


Figure 52. Gain Variation vs. Phase over Gain, 14 GHz, Receive Channel

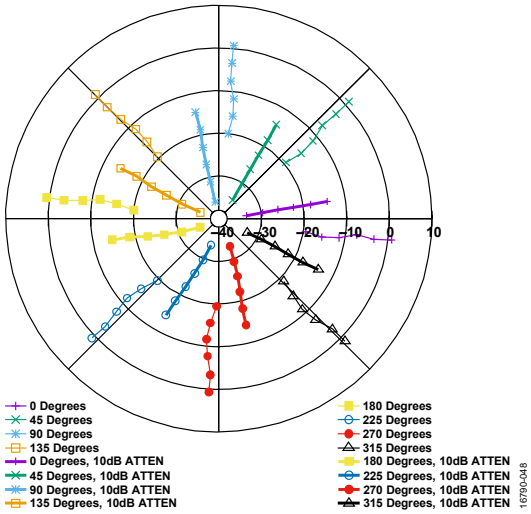


Figure 55. Phase Variation vs. Gain over Phase, 14 GHz, Receive Channel

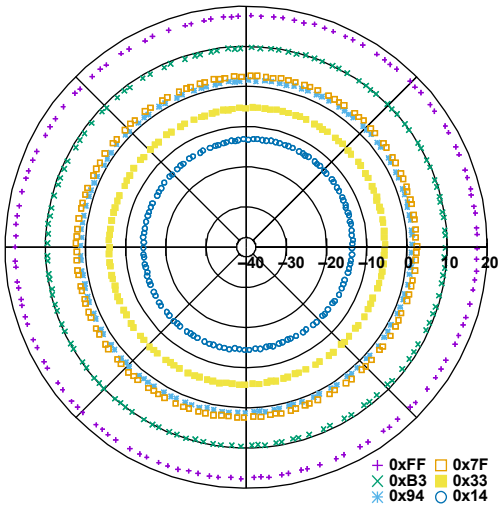


Figure 53. Gain Variation vs. Phase over Gain, 9.5 GHz, Transmit Channel

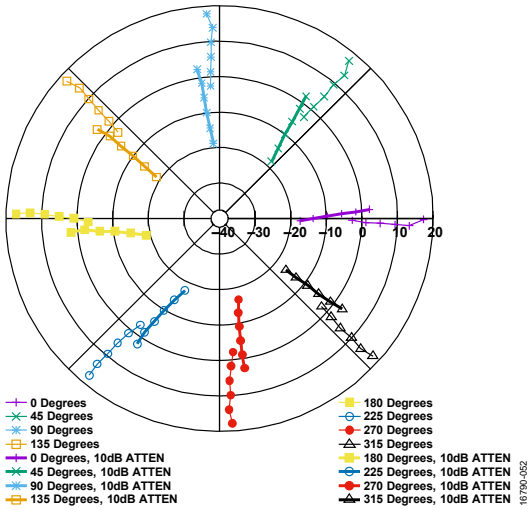


Figure 56. Phase Variation vs. Gain over Phase, 9.5 GHz, Transmit Channel

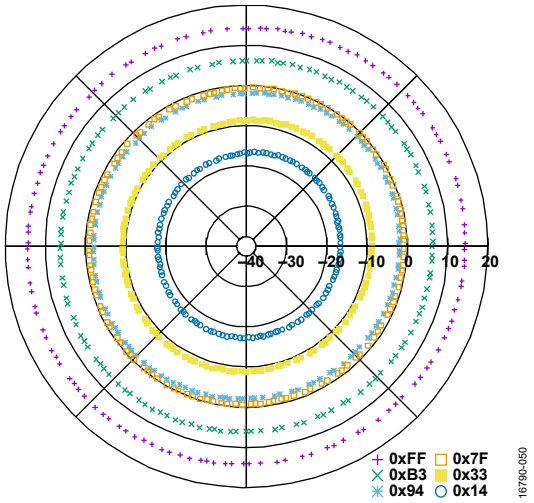


Figure 57. Gain Variation vs. Phase over Gain, 11.5 GHz, Transmit Channel

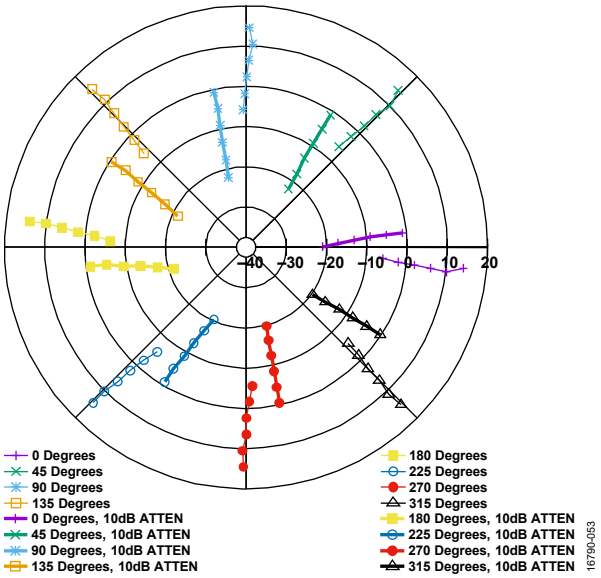


Figure 60. Phase Variation vs. Gain over Phase, 11.5 GHz, Transmit Channel

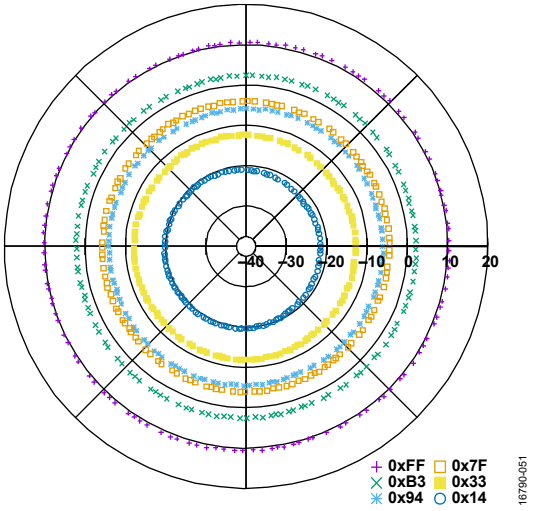


Figure 58. Gain Variation vs. Phase over Gain, 14 GHz, Transmit Channel

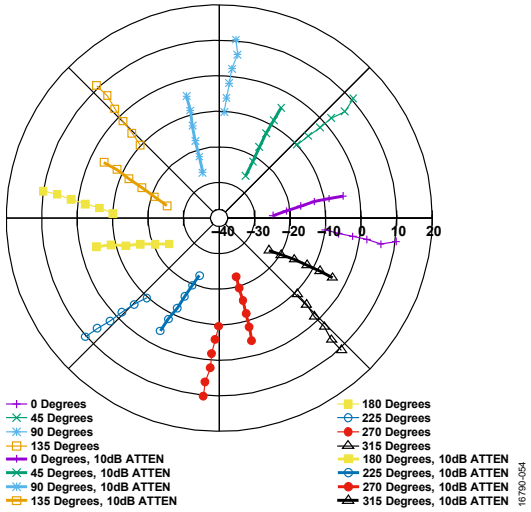


Figure 61. Phase Variation vs. Gain over Phase, 14 GHz, Transmit Channel

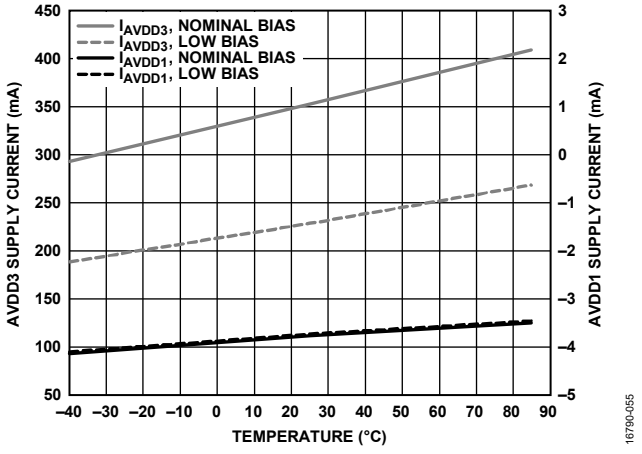


Figure 59. AVDD3 and AVDD1 Supply Current vs. Temperature, Four Transmit Channels Enabled, Normal Bias Mode and Low Bias Mode

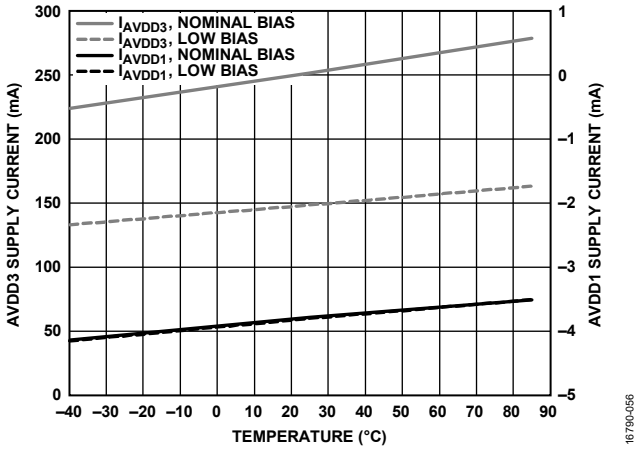


Figure 62. AVDD3 and AVDD1 Supply Current vs. Temperature, Four Receive Channels Enabled, Normal Bias Mode and Low Bias Mode

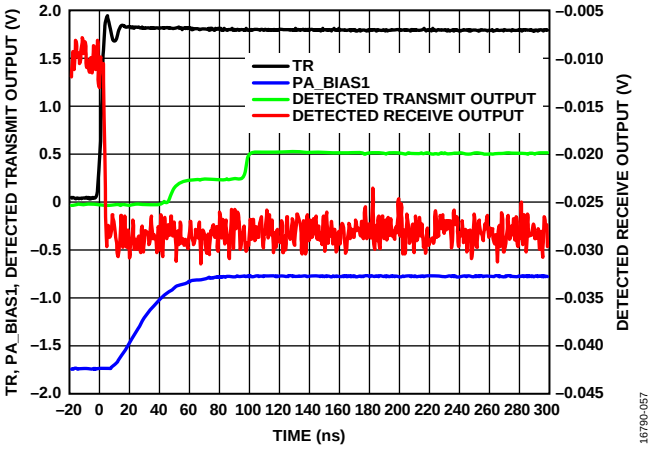


Figure 63. Receive to Transmit Switching Response to TR Rising Edge

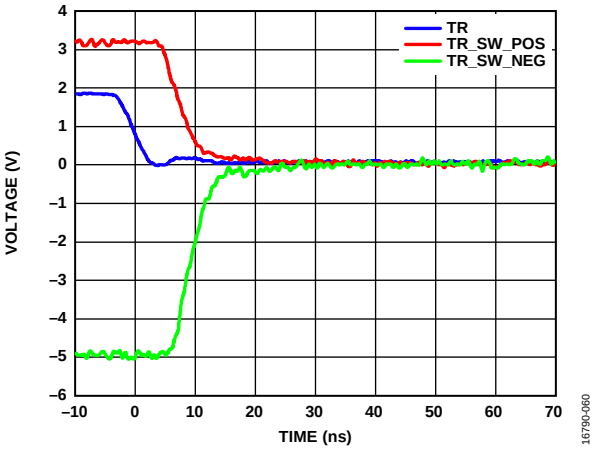


Figure 66. TR_SW_POS and TR_SW_NEG Response to TR Falling Edge

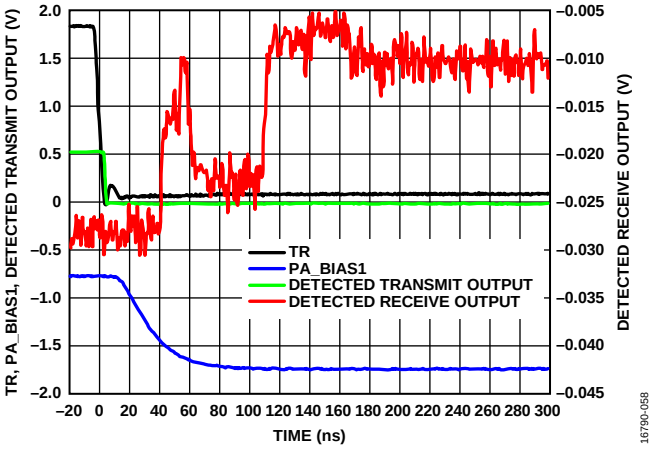


Figure 64. Transmit to Receive Switching Response to TR Falling Edge

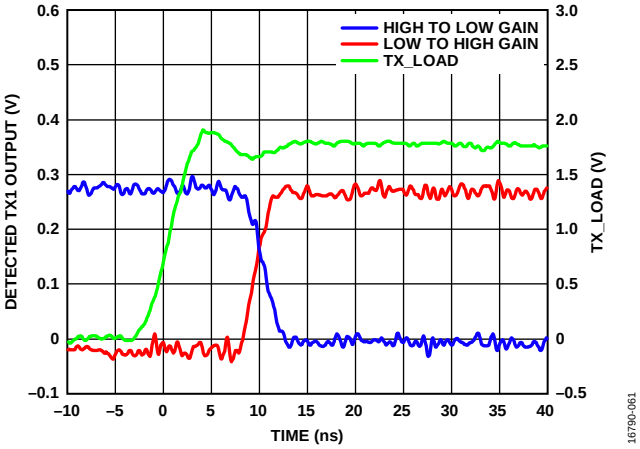


Figure 67. Gain Settling Response to TX_LOAD

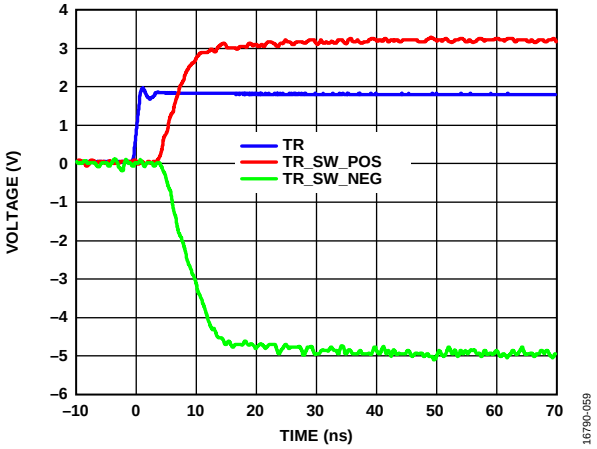


Figure 65. TR_SW_POS and TR_SW_NEG Response to TR Rising Edge

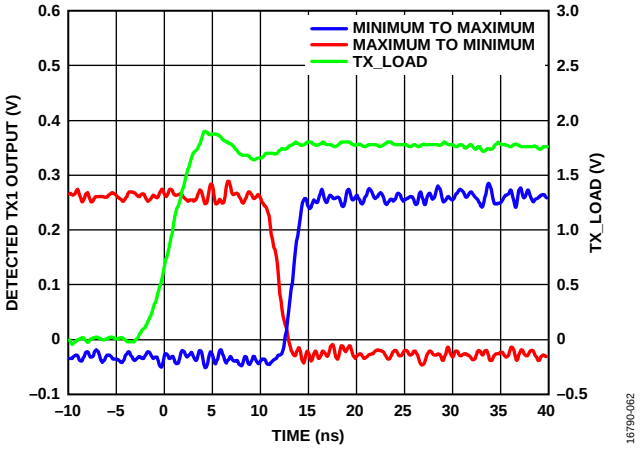


Figure 68. Phase Settling Response (as TX1 Vector Modulator Inphase-Channel Output) to TX_LOAD

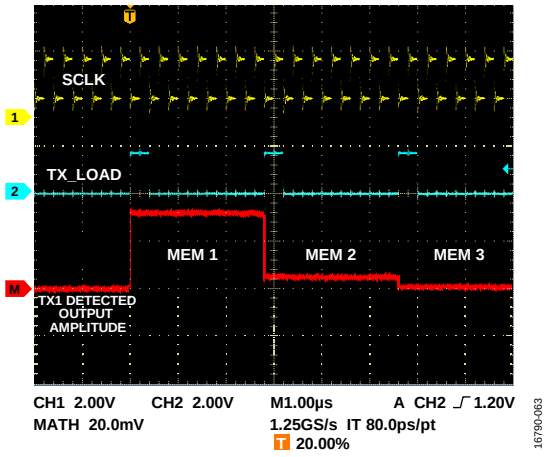


Figure 69. Beam Position Memory Advance vs. TX_LOAD

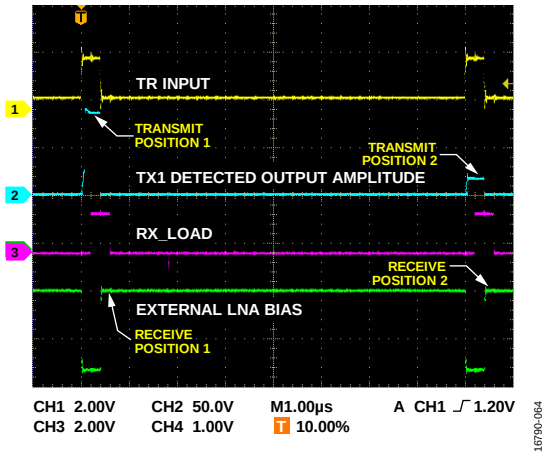


Figure 70. Beam Position Memory Advance vs. RX_LOAD with Transmit and Receive Switching

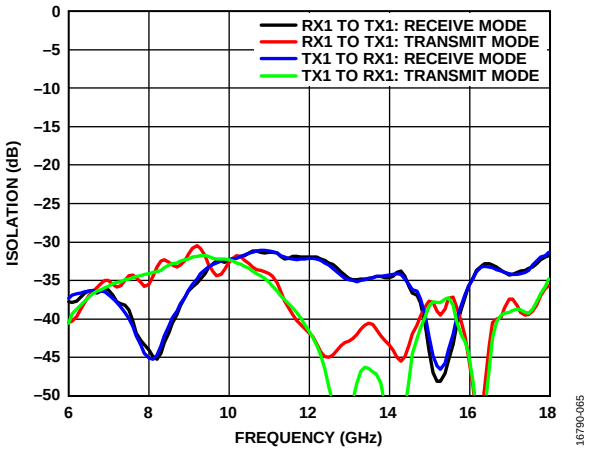


Figure 71. Isolation vs. Frequency, Transmit to Receive Channel

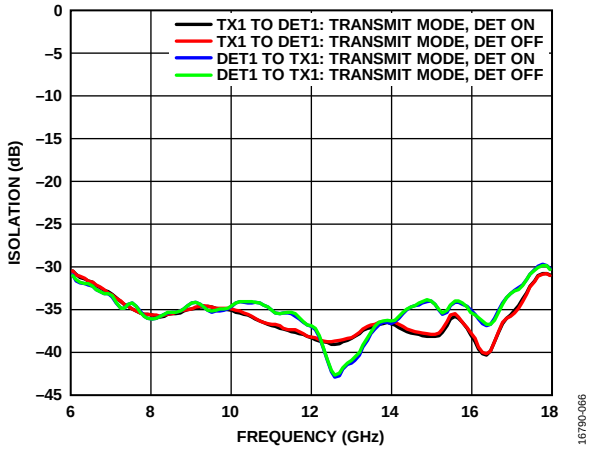


Figure 72. Isolation vs. Frequency, Transmit to Detector and Detector to Transmit

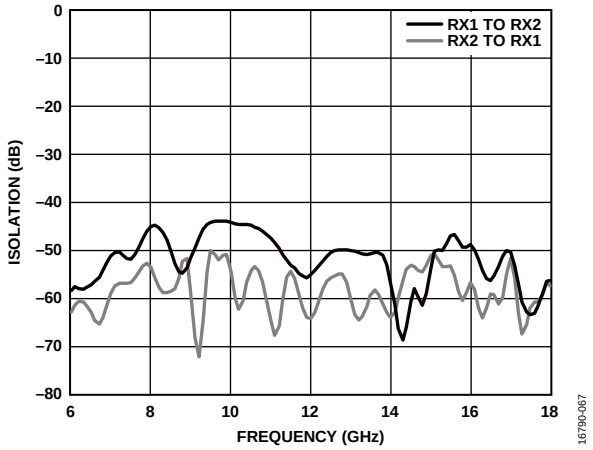


Figure 73. Isolation vs. Frequency, Receive Channel to Receive Channel

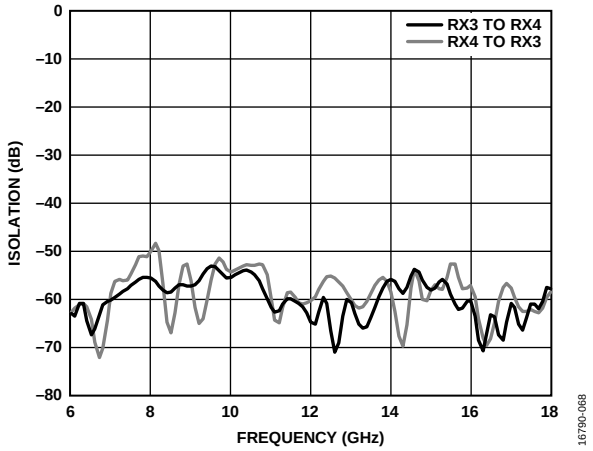


Figure 74. Isolation vs. Frequency, Receive Channel to Receive Channel

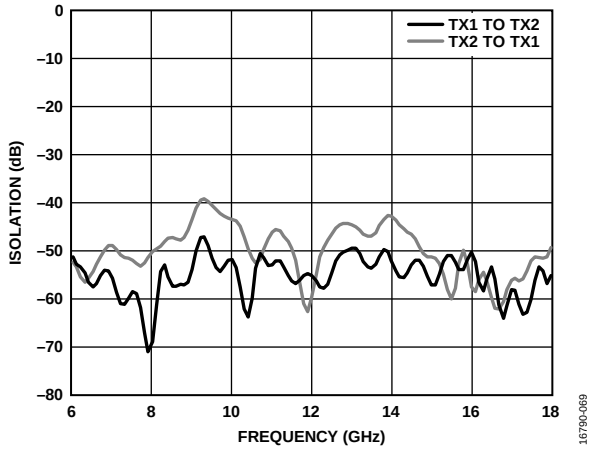


Figure 75. Isolation vs. Frequency, Transmit Channel to Transmit Channel

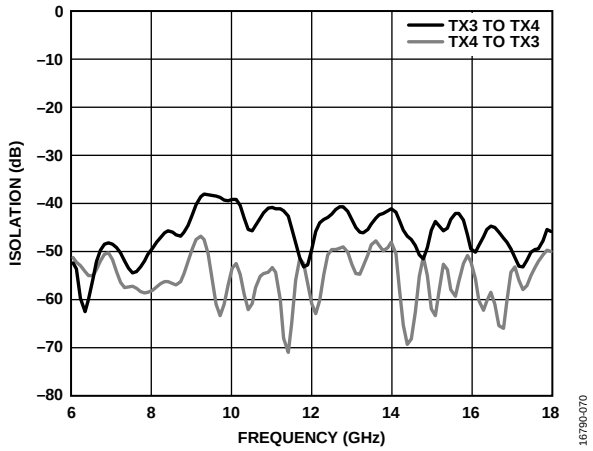


Figure 76. Isolation vs. Frequency, Transmit Channel to Transmit Channel

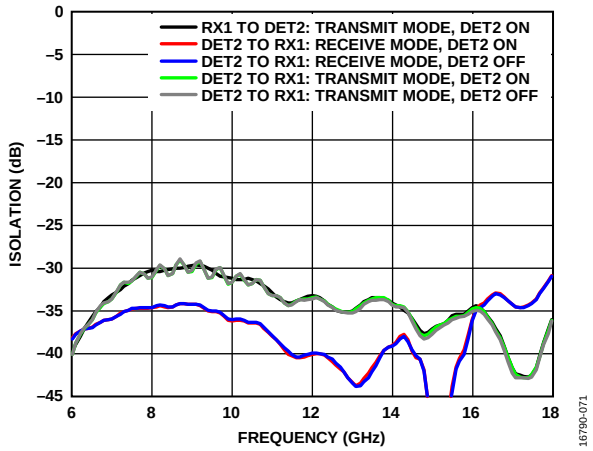


Figure 77. Input Isolation vs. Frequency, Receive to Detector and Detector to Receive

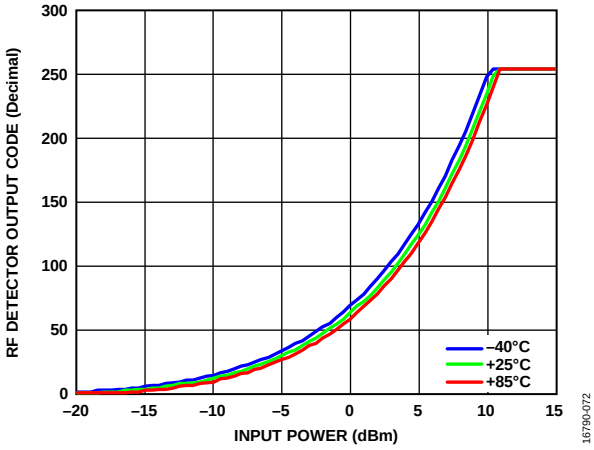


Figure 78. RF Detector Output Code vs. Input Power and Temperature, 11.5 GHz

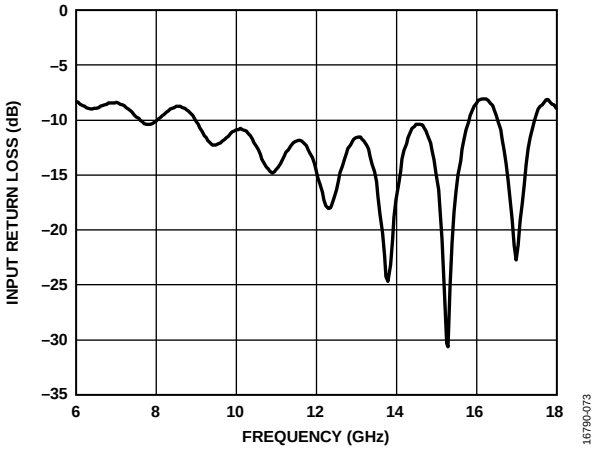


Figure 79. Input Return Loss vs. Frequency, RF Detector

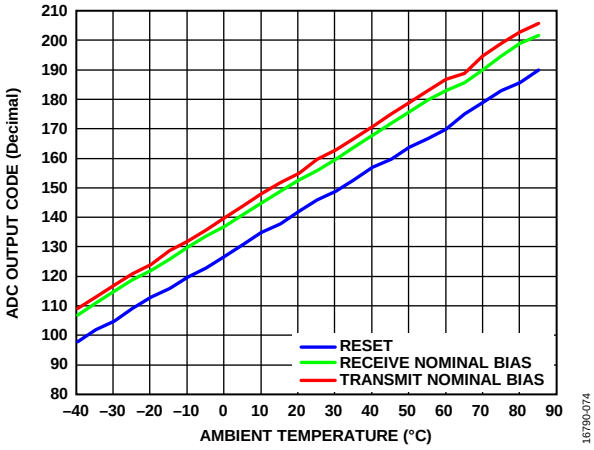


Figure 80. ADC Output Code vs. Ambient Temperature, Temperature Sensor

THEORY OF OPERATION

RF PATH

The ADAR1000 contains four identical transmit and receive channels for time division duplex (TDD) operation. As shown in Figure 81, each receive channel includes an LNA followed by a phase shifter and a VGA. Each transmit channel includes a VGA followed by a phase shifter and a driver amplifier. A control switch selects between the transmit and receive paths, and a step attenuator stage of 0 dB or 15 dB is included in the common path and shared between the transmit and receive modes before connecting to the passive 4:1 combining and splitting network. The primary function of the chip is to accurately set the relative phase and gain of each channel so that the signals coherently add in the desired direction. The individual element gain control compensates for temperature and process effects and provides tapering for the beam to achieve low-side lobe levels.

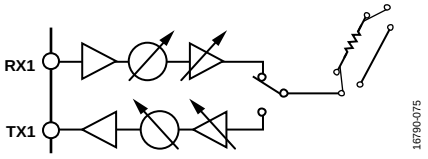


Figure 81. Transmit and Receive Channel Functional Diagram

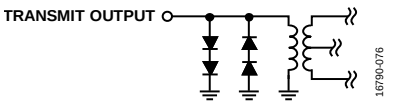


Figure 82. Transmit Channel Output Interface Schematic

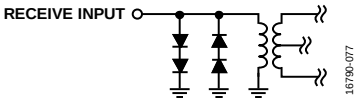


Figure 83. Receive Channel Input Interface Schematic

As shown in Figure 82 and Figure 83, the receive input and transmit output of each channel is connected to a balun, which converts the single-ended signal to the differential signal required for the active RF circuit blocks. The balun networks also match the input and outputs to 50 Ω over the operating bandwidth. Figure 84 shows the interface schematic for the common RF_IO port, which is single-ended, matched to 50 Ω over the operating bandwidth, and connected to dc ground through a shunt matching inductor.

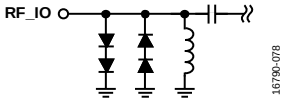


Figure 84. Common RF_IO Interface Schematic

PHASE AND GAIN CONTROL

Phase control is implemented using the active vector modulator architecture shown in Figure 85. The incoming signal is split into equal amplitude, inphase and quadrature (I and Q) signals that are amplified independently by two identical biphase VGAs and summed at the output to generate the required phase shift. Six bits control each VGA, five bits for amplitude control and one bit for polarity control, for a total of 12 bits per phase shifter. The vector modulator output voltage amplitude (V_{OUT}) and phase shift (Φ) are given by the following equations:

$$V_{OUT} = \sqrt{V_I^2 + V_Q^2}$$

$$\Phi = \arctan(V_Q/V_I)$$

where:
V_I is output voltage of the I channel VGA.
V_Q is the output voltage of the Q channel VGA.

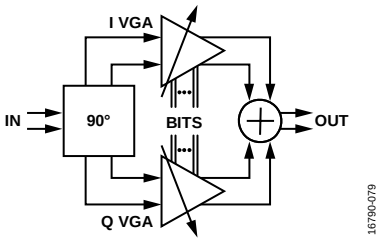


Figure 85. Active Vector Modulator Phase Shifter Block Diagram

Note that when evaluating the arctangent function, the proper phase quadrant must be selected. The signs of V_Q and V_I determine the phase quadrant according to the following:

- If V_Q and V_I are both positive, the phase shift is between 0° and 90°.
- If V_Q is positive and V_I is negative, the phase shift is between 90° and 180°.
- If V_Q and V_I are both negative, the phase shift is between 180° and 270°.
- If V_Q is negative and V_I is positive, the phase shift is between 270° and 360°.

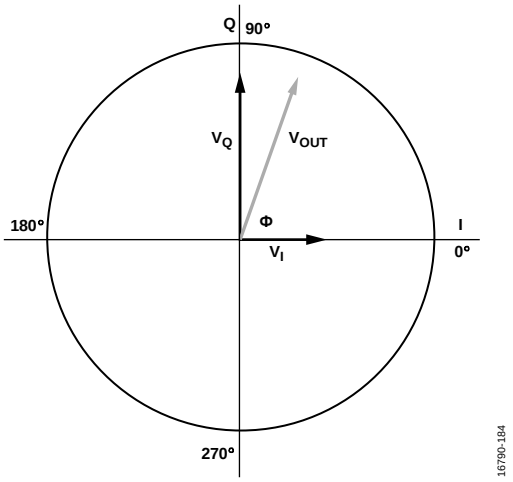


Figure 86. Vector Gain Representation

In general, select the V_Q and V_I values to give the desired phase shift while minimizing the variation in V_{OUT} (gain). However, allowing some amplitude variation can result in finer phase step resolution and/or lower phase errors.

Table 13 in the Phase Control Registers section details the values to set in Register 0x014 to Register 0x01B for the receiver and Register 0x020 to Register 0x027 for the transmitter, to sweep the phase while keeping the gain of the vector modulator constant. Keeping the vector modulator gain constant degrades the phase resolution to 2.8°.

If the values given Table 13 are used, the VGA exclusively executes the gain control in either the transmitter or receiver path. Register 0x010 to Register 0x013 and Register 0x01C to Register 0x01F control the receiver and transmitter VGAs, respectively. If using values not found in Table 13, be aware that both the vector modulator and the VGA affect the total gain.

The total gain (in dB) ($GAIN_{TOTAL}$) is calculated by the following equation:

$$GAIN_{TOTAL}\ (\text{dB}) = GAIN_{VM}\ (\text{dB}) + GAIN_{VGA}\ (\text{dB})$$

where:
$GAIN_{VM}$ is the vector modulator gain.
$GAIN_{VGA}$ is the VGA gain from any of the transmitter and receiver paths.

POWER DETECTORS

Four power detectors (one per channel) are provided to sample peak power coupled from the outputs of off chip power amplifiers for power monitoring. The on-chip ADC selects from the four detectors and converts the output to an 8-bit digital word that is read back over the SPI. Figure 87 shows a simplified power detector schematic. Each detector input (detector input in Figure 87) is ac-coupled to a diode-based detector, and then amplified and routed to the ADC. A reference diode (not shown) provides temperature compensation to minimize variation in the output voltage vs. the input power response over the operating temperature range.

The detector inputs are matched on chip to 50 Ω. Register 0x030 contains an enable bit (CHx_DET_EN) for each detector so that the detectors can be powered down when not in use.

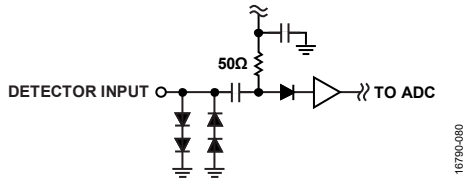


Figure 87. Simplified Power Detector Schematic

EXTERNAL AMPLIFIER BIAS DACs

Five on-chip DACs are provided for off chip biasing of gallium arsenide (GaAs) or gallium nitride (GaN) PAs. One DAC is intended for each of the four off chip Pas, and the fifth DAC is shared between the four off chip LNAs. Figure 88 shows a simplified schematic for the bias DACs. An 8-bit word from the SPI sets the DAC output, which is amplified and translated to a 0 V to −4.8 V range intended for the gate bias of the GaAs or GaN PAs. A push pull output stage allows sourcing or sinking of up to 10 mA for PAs that can draw significant gate current when pushed deep into compression. The LNA bias DAC also includes a disable mode with a high output impedance, which provides flexibility for self biased LNAs that also have an external gate voltage adjustment capability. The LNA_BIAS_ OUT_EN bit (Bit 4, Register 0x030) provides this control.

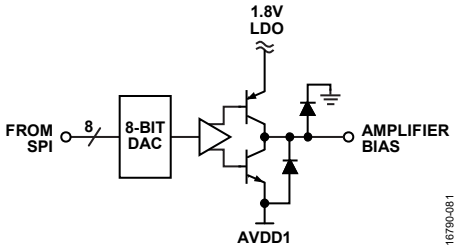


Figure 88. Simplified PA/LNA Bias DAC Schematic

Two SPI registers are associated with each bias DAC, an on register (Register 0x029 through Register 0x02D) for setting the bias voltage for the amplifier when active, and an off register (Register 0x046 through Register 0x04A) for setting the appropriate voltage for turning the amplifier bias off. The BIAS_CTRL bit (Bit 6, Register 0x030) determines whether the DAC outputs must be changed by loading the new settings over the SPI each time, whether the outputs switch between the on and off registers with the TX_EN or RX_EN signal (SPI transmit and receive mode) or with the state of the external transmit and receive pin. All 0s correspond to a 0 V output, and all 1s correspond to a −4.8 V output.

EXTERNAL SWITCH CONTROL

The chip provides two driver outputs for external GaAs switch control: one (TR_SW_NEG) for an external transmit and receive switch, and the other (TR_POL) for a polarization switch. Figure 89 shows a simplified schematic of the TR_SW_NEG and TR_POL switch driver. The switch driver outputs between 0 V and AVDD1 (nominally −5 V). A push pull output stage allows sourcing or sinking of up to 1 mA.

The chip also provides a third driver output, TR_SW_POS (see Figure 90), to drive a transmit/receive switch requiring a positive control voltage. TR_SW_POS outputs between 0 V and AVDD3 (nominally 3.3 V). The external transmit and receive switch driver outputs change state along with the on-chip transmit and receive switches via the transmit and receive control signal (either through the SPI or the TR pin). Register 0x031 (SW_CTRL) contains all the control bits required for both switch drivers. The polarity of the transmit and receive switch driver output with respect to the transmit and receive control signal is set via the SW_DRV_ TR_STATE bit (Bit 7, Register 0x031) to provide flexibility for different GaAs switches. The external polarization switch changes with the state of the POL bit (Bit 0, Register 0x031). Write a high to the SW_DRV_EN_TR and SW_DRV_EN_POL bits (Bits[4:3], Register 0x031) to enable the switch drivers.

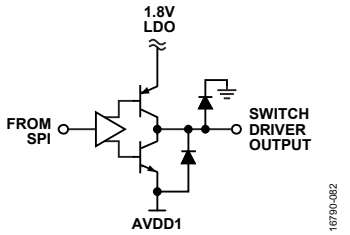


Figure 89. TR_SW_NEG and TR_POL Switch Driver

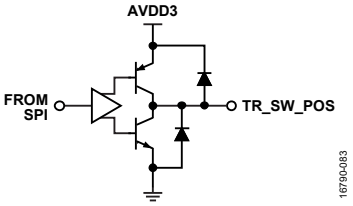


Figure 90. TR_SW_POS Switch Driver

TRANSMIT AND RECEIVE CONTROL

Properly transitioning from transmit mode to receive mode, and vice versa, is key to operating a TDD or radar phased array system. The ADAR1000 performs the transmitter to receiver and receiver to transmitter functionality based on a transmit and receive control signal input to the chip. Mode transition can be accomplished through either a SPI register write or via the digital transmit and receive input pin of the chip.

When using the SPI, all of the controls required to change the transmit and receive state are contained in Register 0x031, so that the transition is made using a single register write. First, the TR_SOURCE bit (Bit 2, Register 0x031) determines whether the SPI (low) or the TR pin (high) is used for transmit and receive control. When the SPI is used, the TR_SPI bit (Bit 1, Register 0x031) determines receive (low) or transmit (high) mode. The TX_EN and RX_EN bit (Bits[6:5], Register 0x031) must also be active to turn on the receive or transmit subcircuits for the applicable mode, as well as to turn on or off the gate bias for the external PAs and LNAs if the BIAS_CTRL bit (Bit 6, Register 0x030) is high. Register 0x031 also controls the external switch drivers as previously described in the External Switch Control section.

When the TR_SOURCE bit (Bit 2, Register 0x031) is high, the transmit and receive pin controls all operation necessary to switch from receive to transmit and vice versa. This operation includes setting the on-chip and off chip transmit and receive switches, enabling the receive or transmit subcircuits, as well as turning on and off the gate bias for the external PAs and LNAs if the BIAS_CTRL bit (Bit 6, Register 0x030) is high.

RF SUBCIRCUIT BIAS CONTROL AND ENABLES

Use Register 0x034 through Register 0x037 to adjust the bias current setting of each of the active RF subcircuits to trade RF performance for lower dc power. Table 6 provides the recommended settings for the nominal and low operating power modes. The nominal power mode provides the highest performance. When reducing dc power for power sensitive applications, this power reduction is at the expense of lower gain, higher noise figure, and lower linearity.

The RF subcircuits are powered down when not in use. When using the SPI for transmit and receive control, RF subcircuits and/or channels can be individually enabled via Register 0x02E (receive channel enables) and Register 0x02F (transmit channel enables). The TX_EN and RX_EN bits (Bits[6:5], Register 0x031) must also be at logic high to enable the transmit or receive subcircuits, respectively. The transmit and receive subcircuits cannot be turned on simultaneously, and if both TX_EN and RX_EN are high, both the transmit and receive subcircuits power down. If using the transmit and receive pin for transmit and receive control, the functions of the TX_EN and RX_EN automatically follow the state of the transmit and receive input, allowing fast switching between transmit and receive modes.

ADC OPERATION

The chip contains an 8-bit ADC for sampling the outputs of the four power detectors and the temperature sensor. Register 0x032 controls the ADC. The ADC_CLKFREQ_SEL (Bit 7, Register 0x032) selects between a 2 MHz or a 250 kHz clock frequency. The ADC_EN and CLK_EN bits (Bits[6:5], Register 0x032) allow the ADC to be powered down when not in use. The ST_CONV bit (Bit 4, Register 0x032) initiates a conversion, which requires 16 clock cycles for a minimum conversion time of 8 µs (2 MHz clock). The ADC_EOC (Bit 0, Register 0x032) read bit indicates when a conversion is complete and the 8-bit output is available for reading over the SPI. A mux selects between the five inputs based on the MUX_SEL bits (Bits[3:1], Register 0x032). The 8-bit output is read from Register 0x033 (ADC_OUTPUT).

Table 6. SPI Settings for Different Power Modes

				Bias Setting (Decimal)	
Subcircuit	**Register (Hexidecimal)**	**Bits**	**Bit Field**	**Nominal**	**Low Power**
Receive LNA	0x034	Bits[3:0]	LNA_BIAS	8	5
Receive Vector Modulator	0x035	Bits[2:0]	RX_VM_BIAS	5	2
Receive VGA	0x035	Bits[6:3]	RX_VGA_BIAS	10	3
Transmit Vector Modulator	0x036	Bits[2:0]	TX_VM_BIAS	5	2
Transmit VGA	0x036	Bits[6:3]	TX_VGA_BIAS	5	5
Transmit Driver	0x037	Bits[2:0]	TX_DRV_BIAS	6	3

CHIP ADDRESSING

Using the ADDR1 and ADDR0 pins to set the address of each individual chip, the user can connect the SCLK, CSB, SDIO, and SDO lines of up to four chips together. The ADDR1 and ADDR0 values correspond to the AD1 and AD0 bits (Bits[14:13] of the SPI address header) shown in Table 11, respectively.

An example write to Chip 2 has the following address bit settings. For a group of four chips, indexed 0 to 3, ADDR1 is set to high and ADDR0 is set to low with the address header set to Bits[14:13] = 10.

The user also has the option to write to all four chips with a single write by setting the address header Bits[14:11] = 0001.

MEMORY ACCESS

On-chip random access memory (RAM) is provided for storing phase and amplitude settings for up to 121 beam positions and seven bias settings for both transmit and receive modes, as shown in Table 11. A beam position consists of the gain, Vector Modulator I, and Vector Modulator Q settings for all four channels. Beam positions are stored in memory by writing to the 0x1000 through 0x1FFF locations. Beam positions are then loaded from memory by writing to Register 0x039 for the receive channels, and Register 0x03A for the transmit channels, which pulls the amplitude and phase setting for all four channels. Additionally, if the RX_CHX_RAM_BYPASS and TX_CHX_RAM_BYPASS bits (Bits[1:0], Register 0x038) are active, the amplitude and phase settings can be individually pulled for each receive or transmit channel, allowing even greater flexibility. In this case, the settings for each receive channel are loaded by writing to Register 0x03D through Register 0x040 and for each transmit channel by writing to Register 0x041 through Register 0x044. The BEAM_RAM_BYPASS bit in Register 0x038 determines where the amplitude and phase settings are pulled from the memory (low) or written to over the SPI (high).

Seven memory locations are also provided for storing bias settings for all the transmit and receive channel subcircuits, normally stored in Register 0x034 through Register 0x037. When the BIAS_RAM_BYPASS bit (Register 0x38, Bit 5) is at logic low, the bias setting can be recalled from memory instead of from the SPI.

Using Table 7, Table 8, Table 9, and Table 10 in conjunction with Table 11, the user can decode the receive beam position bits, transmit beam position bits, receive bias setting bits, and transmit receive bias setting bits that are located in the RAM.

An example of writing gain, phase, and bias values to the memory is provided in Table 21 in the SPI Programming Example section.

Additionally, the beam can be stepped sequentially through the positions stored in memory. To use this function, first load Register 0x04D through Register 0x04E with the transmit channel start and stop memory addresses, and Register 0x04F through Register 0x050 with the receive channel start and stop memory addresses. Then, apply six serial clock pulses followed by a pulse to the TX_LOAD or RX_LOAD input for recalling memory for the transmit or receive channels, respectively. Channel settings are loaded sequentially from memory by repeatedly applying the serial clock pulses plus TX_LOAD or RX_LOAD. This mode eliminates the need for a SPI register write to load the next beam position, resulting in faster beam transitions. An example of this operation is shown in Figure 69.

CALIBRATION

There is no built in calibration or factory calibration for the magnitude and phase of each gain and phase of the RF channel. The rms phase error resulting from using the I and Q settings is determined from the equations previously provided in the Phase and Gain Control section. The rms phase error can be improved by running a full over the air active electronically scanned array (AESA) calibration of each channel at the desired frequency operation.

Table 7. Beam Position Vector Modulator (VM) and VGA Decoding for Receiver and Transmitter Channel 1 to Channel 4

Bits[23:22]	Bit 21	Bits[20:16]	Bits[15:14]	Bit 13	Bits[12:8]	Bit 7	Bits[6:0]
Don't care	VM Q polarity	VM Q gain	Don't care	VM I polarity	VM I gain	Attenuator	VGA gain

Table 8. Receiver Bias Setting Decoding

Bits[31:28]	Bits[27:23]	Bits[22:20]	Bits[19:16]	Bits[15:8]	Bits[7:0]
Don't care	LNA bias	VM bias	VGA bias	External LNA bias on	External LNA bias off

Table 9. Transmitter Bias Setting Decoding for Bits[63:0]

Bits[63:56]	Bits[55:48]	Bits[47:40]	Bits[39:32]	Bits[31:24]	Bits[23:16]	Bits[15:8]	Bits[7:0]
External PA 4 bias On	External PA 4 bias off	External PA 3 bias on	External PA 2 bias on	External PA 1 bias on	External PA 3 bias off	External PA 2 bias off	External PA 1 bias off

Table 10. Transmitter Bias Setting Decoding for Bits[74:64]

Bits[79:75]	Bits[74:72]	Bits[70:68]	Bits[67:64]
Don't care	Driver bias	VM bias	VGA bias

Table 11. Control Register Address and SPI Beam Memory Address Map

SPI Address															
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Function
AD1	AD0	0	0	0	0	0	0	0	0	0	0	0	0	0	Addresses with Bit 12 equal to 0 point to the control registers described in the Register Map section
AD1	AD0	0	0	0	0	0	0	0	0	0	0	0	0	1	Control register locations
…	…	…	…	…	…	…	…	…	…	…	…	…	…	….	Range of addresses pointing to additional control register locations
AD1	AD0	0	1	1	1	1	1	1	1	1	1	1	1	1	Control register locations
															Addresses with Bit 12 equal to 1 point to the memory area for storing the beam settings at each location
AD1	AD0	1	0	0	0	0	0	0	0	0	0	0	0	0	Receive Channel 1 Beam Position 0, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	0	0	1	Receive Channel 1 Beam Position 0, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	0	1	0	Receive Channel 1 Beam Position 0, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	0	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	0	0	1	0	0	Receive Channel 2 Beam Position 0, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	1	0	1	Receive Channel 2 Beam Position 0, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	1	1	0	Receive Channel 2 Beam Position 0, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	0	0	1	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	0	1	0	0	0	Receive Channel 3 Beam Position 0, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	0	0	1	Receive Channel 3 Beam Position 0, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	0	1	0	Receive Channel 3 Beam Position 0, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	0	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	0	1	1	0	0	Receive Channel 4 Beam Position 0, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	1	0	1	Receive Channel 4 Beam Position 0, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	1	1	0	Receive Channel 4 Beam Position 0, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	0	1	1	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	1	0	0	0	0	Receive Channel 1 Beam Position 1, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	0	0	1	Receive Channel 1 Beam Position 1, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	0	1	0	Receive Channel 1 Beam Position 1, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	0	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	1	0	1	0	0	Receive Channel 2 Beam Position 1, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	1	0	1	Receive Channel 2 Beam Position 1, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	1	1	0	Receive Channel 2 Beam Position 1, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	1	0	1	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	0	1	1	0	0	0	Receive Channel 3 Beam Position 1, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	0	0	1	Receive Channel 3 Beam Position 1, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	0	1	0	Receive Channel 3 Beam Position 1, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	0	1	1	Not applicable

SPI Address														
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Function
AD1	AD0	1	0	0	0	0	0	0	0	1	1	1	0	0	Receive Channel 4 Beam Position 1, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	1	0	1	Receive Channel 4 Beam Position 1, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	1	1	0	Receive Channel 4 Beam Position 1, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	0	1	1	1	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	1	0	0	0	0	0	Receive Channel 1 Beam Position 2, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	0	0	1	Receive Channel 1 Beam Position 2, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	0	1	0	Receive Channel 1 Beam Position 2, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	0	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	1	0	0	1	0	0	Receive Channel 2 Beam Position 2, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	1	0	1	Receive Channel 2 Beam Position 2, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	1	1	0	Receive Channel 2 Beam Position 2, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	1	0	0	1	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	1	0	1	0	0	0	Receive Channel 3 Beam Position 2, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	0	0	1	Receive Channel 3 Beam Position 2, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	0	1	0	Receive Channel 3 Beam Position 2, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	0	1	1	Not applicable
AD1	AD0	1	0	0	0	0	0	0	1	0	1	1	0	0	Receive Channel 4 Beam Position 2, Bits[7:0]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	1	0	1	Receive Channel 4 Beam Position 2, Bits[15:8]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	1	1	0	Receive Channel 4 Beam Position 2, Bits[23:16]
AD1	AD0	1	0	0	0	0	0	0	1	0	1	1	1	1	Not applicable
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	Range of addresses pointing to additional receive beam positions
AD1	AD0	1	0	1	1	1	1	0	0	0	0	0	0	0	Receive Channel 1 Beam Position 121, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	0	0	1	Receive Channel 1 Beam Position 121, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	0	1	0	Receive Channel 1 Beam Position 121, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	0	0	1	0	0	Receive Channel 2 Beam Position 121, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	1	0	1	Receive Channel 2 Beam Position 121, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	1	1	0	Receive Channel 2 Beam Position 121, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	0	0	0	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	0	1	0	0	0	Receive Channel 3 Beam Position 121, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	0	0	1	Receive Channel 3 Beam Position 121, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	0	1	0	Receive Channel 3 Beam Position 121, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	0	1	1	0	0	Receive Channel 4 Beam Position 121, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	1	0	1	Receive Channel 4 Beam Position 121, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	1	1	0	Receive Channel 4 Beam Position 121, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	0	0	1	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	0	0	0	0	Receive Bias Setting 1, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	0	1	0	0	0	1	Receive Bias Setting 1, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	0	1	0	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	0	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	0	1	0	0	Receive Bias Setting 1, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	0	1	0	1	0	1	Receive Bias Setting 1, Bits[31:24]
AD1	AD0	1	0	1	1	1	1	0	0	1	0	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	0	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	0	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	0	0	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	1	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	1	0	1	Not applicable

SPI Address														
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Function
AD1	AD0	1	0	1	1	1	1	0	0	1	1	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	0	1	1	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	0	0	0	0	Receive Bias Setting 2, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	0	1	0	0	0	0	1	Receive Bias Setting 2, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	0	1	0	0	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	0	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	0	1	0	0	Receive Bias Setting 2, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	0	1	0	0	1	0	1	Receive Bias Setting 2, Bits[31:24]
AD1	AD0	1	0	1	1	1	1	0	1	0	0	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	0	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	0	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	0	0	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	1	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	1	0	1	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	0	1	0	1	1	1	1	Not applicable
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	Range of addresses pointing to additional receive bias settings
AD1	AD0	1	0	1	1	1	1	1	1	1	0	0	0	0	Receive Bias Setting 7, Bits[7:0]
AD1	AD0	1	0	1	1	1	1	1	1	1	0	0	0	1	Receive Bias Setting 7, Bits[15:8]
AD1	AD0	1	0	1	1	1	1	1	1	1	0	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	0	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	0	1	0	0	Receive Bias Setting 7, Bits[23:16]
AD1	AD0	1	0	1	1	1	1	1	1	1	0	1	0	1	Receive Bias Setting 7, Bits[31:24]
AD1	AD0	1	0	1	1	1	1	1	1	1	0	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	0	1	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	0	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	0	0	1	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	0	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	0	1	1	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	1	0	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	1	0	1	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	1	1	0	Not applicable
AD1	AD0	1	0	1	1	1	1	1	1	1	1	1	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	0	0	0	0	0	Transmit Channel 1 Beam Position 0, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	0	0	1	Transmit Channel 1 Beam Position 0, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	0	1	0	Transmit Channel 1 Beam Position 0, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	0	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	0	0	1	0	0	Transmit Channel 2 Beam Position 0, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	1	0	1	Transmit Channel 2 Beam Position 0, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	1	1	0	Transmit Channel 2 Beam Position 0, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	0	0	1	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	0	1	0	0	0	Transmit Channel 3 Beam Position 0, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	0	0	1	Transmit Channel 3 Beam Position 0, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	0	1	0	Transmit Channel 3 Beam Position 0, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	0	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	0	1	1	0	0	Transmit Channel 4 Beam Position 0, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	1	0	1	Transmit Channel 4 Beam Position 0, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	1	1	0	Transmit Channel 4 Beam Position 0, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	0	1	1	1	1	Not applicable

SPI Address															
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Function
AD1	AD0	1	1	0	0	0	0	0	0	1	0	0	0	0	Transmit Channel 1 Beam Position 1, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	0	0	1	Transmit Channel 1 Beam Position 1, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	0	1	0	Transmit Channel 1 Beam Position 1, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	0	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	1	0	1	0	0	Transmit Channel 2 Beam Position 1, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	1	0	1	Transmit Channel 2 Beam Position 1, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	1	1	0	Transmit Channel 2 Beam Position 1, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	1	0	1	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	1	1	0	0	0	Transmit Channel 3 Beam Position 1, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	0	0	1	Transmit Channel 3 Beam Position 1, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	0	1	0	Transmit Channel 3 Beam Position 1, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	0	1	1	Not applicable
AD1	AD0	1	1	0	0	0	0	0	0	1	1	1	0	0	Transmit Channel 4 Beam Position 1, Bits[7:0]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	1	0	1	Transmit Channel 4 Beam Position 1, Bits[15:8]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	1	1	0	Transmit Channel 4 Beam Position 1, Bits[23:16]
AD1	AD0	1	1	0	0	0	0	0	0	1	1	1	1	1	Not applicable
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	Range of addresses pointing to additional transmit beam positions
AD1	AD0	1	1	1	1	1	1	0	0	0	0	0	0	0	Transmit Channel 1 Beam Position 121, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	0	0	1	Transmit Channel 1 Beam Position 121, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	0	1	0	Transmit Channel 1 Beam Position 121, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	0	0	1	0	0	Transmit Channel 2 Beam Position 121, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	1	0	1	Transmit Channel 2 Beam Position 121, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	1	1	0	Transmit Channel 2 Beam Position 121, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	0	0	0	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	0	1	0	0	0	Transmit Channel 3 Beam Position 121, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	0	0	1	Transmit Channel 3 Beam Position 121, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	0	1	0	Transmit Channel 3 Beam Position 121, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	0	1	1	0	0	Transmit Channel 4 Beam Position 121, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	1	0	1	Transmit Channel 4 Beam Position 121, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	1	1	0	Transmit Channel 4 Beam Position 121, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	0	0	1	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	0	0	0	0	Transmit Bias Setting 1, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	0	0	1	Transmit Bias Setting 1, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	0	1	0	Transmit Bias Setting 1, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	0	1	0	0	Transmit Bias Setting 1, Bits[31:24]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	1	0	1	Transmit Bias Setting 1, Bits[39:32]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	1	1	0	Transmit Bias Setting 1, Bits[47:40]
AD1	AD0	1	1	1	1	1	1	0	0	1	0	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	1	0	0	0	Transmit Bias Setting 1, Bits[55:48]
AD1	AD0	1	1	1	1	1	1	0	0	1	1	0	0	1	Transmit Bias Setting 1, Bits[63:56]
AD1	AD0	1	1	1	1	1	1	0	0	1	1	0	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	1	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	1	1	0	0	Transmit Bias Setting 1, Bits[71:64]
AD1	AD0	1	1	1	1	1	1	0	0	1	1	1	0	1	Transmit Bias Setting 1, Bits[79:72]
AD1	AD0	1	1	1	1	1	1	0	0	1	1	1	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	0	0	1	1	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	0	0	0	0	Transmit Bias Setting 2, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	0	1	0	0	0	0	1	Transmit Bias Setting 2, Bits[15:8]

SPI Address														
14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Function
AD1	AD0	1	1	1	1	1	1	0	1	0	0	0	1	0	Transmit Bias Setting 2, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	0	1	0	0	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	0	1	0	0	Transmit Bias Setting 2, Bits[31:24]
AD1	AD0	1	1	1	1	1	1	0	1	0	0	1	0	1	Transmit Bias Setting 2, Bits[39:32]
AD1	AD0	1	1	1	1	1	1	0	1	0	0	1	1	0	Transmit Bias Setting 2, Bits[47:40]
AD1	AD0	1	1	1	1	1	1	0	1	0	0	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	1	0	0	0	Transmit Bias Setting 2, Bits[55:48]
AD1	AD0	1	1	1	1	1	1	0	1	0	1	0	0	1	Transmit Bias Setting 2, Bits[63:56]
AD1	AD0	1	1	1	1	1	1	0	1	0	1	0	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	1	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	1	1	0	0	Transmit Bias Setting 2, Bits[71:64]
AD1	AD0	1	1	1	1	1	1	0	1	0	1	1	0	1	Transmit Bias Setting 2, Bits[79:72]
AD1	AD0	1	1	1	1	1	1	0	1	0	1	1	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	0	1	0	1	1	1	1	Not applicable
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	Range of addresses pointing to additional receive bias settings
AD1	AD0	1	1	1	1	1	1	1	1	1	0	0	0	0	Transmit Bias Setting 7, Bits[7:0]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	0	0	1	Transmit Bias Setting 7, Bits[15:8]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	0	1	0	Transmit Bias Setting 7, Bits[23:16]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	1	1	1	0	1	0	0	Transmit Bias Setting 7, Bits[31:24]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	1	0	1	Transmit Bias Setting 7, Bits[39:32]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	1	1	0	Transmit Bias Setting 7, Bits[47:40]
AD1	AD0	1	1	1	1	1	1	1	1	1	0	1	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	1	1	1	1	0	0	0	Transmit Bias Setting 7, Bits[55:48]
AD1	AD0	1	1	1	1	1	1	1	1	1	1	0	0	1	Transmit Bias Setting 7, Bits[63:56]
AD1	AD0	1	1	1	1	1	1	1	1	1	1	0	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	1	1	1	1	0	1	1	Not applicable
AD1	AD0	1	1	1	1	1	1	1	1	1	1	1	0	0	Transmit Bias Setting 7, Bits[71:64]
AD1	AD0	1	1	1	1	1	1	1	1	1	1	1	0	1	Transmit Bias Setting 7, Bits[79:72]
AD1	AD0	1	1	1	1	1	1	1	1	1	1	1	1	0	Not applicable
AD1	AD0	1	1	1	1	1	1	1	1	1	1	1	1	1	Not applicable

APPLICATIONS INFORMATION

GAIN CONTROL REGISTERS

Gain control for each channel is provided through a combination of independent receive and transmit path VGAs, which provide over 16 dB of gain control range, and a switched 0 dB or 15 dB step attenuator that is shared between the transmit and receive channels. The resulting combined gain control range exceeds 31 dB. The gain of each receive or transmit channel is controlled by an 8-bit register. The VGAs require seven bits of control to ensure a 0.5 dB minimum step size with less than 0.25 dB error over all conditions, and the eighth bit controls the state of the switched attenuator.

To update the amplitude and phase settings, load the new settings over the SPI or from the on-chip memory. When updating the amplitude and phase setting over the SPI, write the new values to Register 0x010 through Register 0x01B to set the receive channel gains and phases, and to Register 0x01C through Register 0x027 to set the transmit channel gains and phases. These gain and phase settings are initially written to holding registers, and do not take effect until a positive pulse occurs on either the LDRX_OVERRIDE bit for the receive channel, or the LDTX_OVERRIDE bit for the transmit channel (Bit 0 and Bit 1, respectively, of Register 0x028). This positive pulse transfers the new settings from the holding registers to the working registers, causing the new settings to take effect in the RF subcircuits. This transfer can also be done by sending positive pulses to the RX_LOAD or TX_LOAD pin for the receive and transmit channels, respectively. This arrangement allows the chip to actively receive or transmit using one amplitude and phase setting while loading the next setting in the background.

The state of the switched attenuator also depends upon the transmit and receive control signal because the attenuator is shared between the transmit and the receive paths. Additionally, the BEAM_RAM_BYPASS bit (Bit 6 of Register 0x038) must be high for loading amplitude and phase settings over the SPI.

Alternatively, up to 121 gain and amplitude settings for both the receive and the transmit modes can be stored in the on-chip memory and then recalled by writing to Register 0x039 for the receive mode, and Register 0x03A for the transmit mode. When loading new settings over the SPI, the new settings loaded from memory do not take effect until the appropriate load command is sent.

The gain control registers for the receive channels are Register 0x010 through Register 0x013, and the gain control registers for the transmit channels are Register 0x01C through Register 0x01F. Bits[6:0] (RX_VGA_CHx and TX_VGA_CHx) of each register control the VGA gain approximately as shown in Figure 91. Limit the usage to the top 16 dB of the gain control range for optimal gain linearity and repeatability. Bit 7 (CHx_ATTN_RX and CHx_ATTN_TX) of each register controls the attenuator state (logic high means attenuator is bypassed).

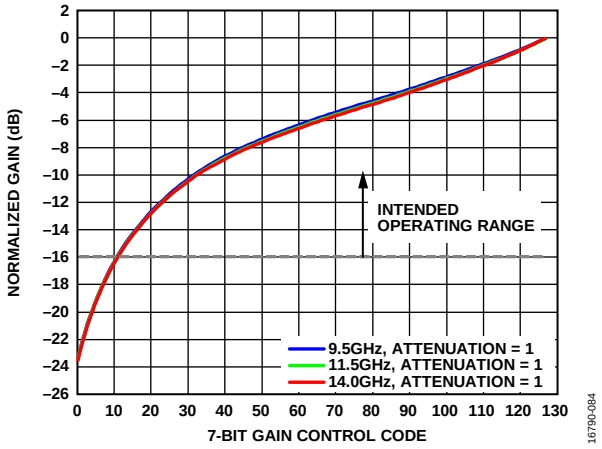


Figure 91. Normalized Gain vs. 7-Bit Gain Control Code

The TX_LOAD and RX_LOAD pins, or alternatively the LDTX_OVERRIDE and LDRX_OVERRIDE bits (Bits[1:0], Register 0x028, respectively), must be pulsed for new settings to take effect. New settings can be loaded in the background while transmitting and receiving using the current settings.

SWITCHED ATTENUATOR CONTROL

The CHx_ATTN_RX bit (Bit 7) of Register 0x010 through Register 0x013 control the receive step attenuators. The CHx_ATTN_TX bit (Bit 7) of Register 0x01C to Register 0x01F control the transmit step attenuators. A multiplexer (mux) determines whether the attenuator for each channel is set according to the receive or transmit working registers as shown in Table 12.

Table 12. Step Attenuator Control

Channel Transmit and Receive State	CHx_ATTN_RX[1]	CHx_ATTN_TX[1]	Channel x Attenuator State[1]
Receive	1	X[2]	Bypass
Receive	0	X[2]	Attenuation
Transmit	X[2]	1	Bypass
Transmit	X[2]	0	Attenuation

[1] From SPI, x = 1, 2, 3, or 4.
[2] X means don't care.

PHASE CONTROL REGISTERS

Phase is determined by setting the I and Q VGA gains of the vector modulator(s). The phase control registers for the receiver channels are Register 0x14 through Register 0x1B. The phase control registers for the transmitter channels are Register 0x020 through Register 0x027.

Each register controls the gain of I or Q VGA and the polarity bit to determine the quadrant of the resultant vector. See Figure 86 in the Phase and Gain Control section. Table 13 maps the user desired phase to data of several phase control registers. I Reg represents Register Bits[5:0], which includes the I polarity Bit 5 and the VM I Gain Bits[4:0]. Q Reg represents Bits[5:0], which includes the Q polarity Bit 5 and the VM Q Gain Bits[4:0].

Table 13. Quadrant 1 Phase Control—Mapping of I and Q VM VGA Register Settings to Phase Setting

Phase (Degrees)	I Reg (Hex)	Q Reg (Hex)
0	0x3F	20
2.8125	0x3F	21
5.625	0x3F	23
8.4375	0x3F	24
11.25	0x3F	26
14.0625	0x3E	27
16.875	0x3E	28
19.6875	0x3D	2A
22.5	0x3D	2B
25.3125	0x3C	2D
28.125	0x3C	2E
30.9375	0x3B	2F
33.75	0x3A	30
36.5625	0x39	31
39.375	0x38	33
42.1875	0x37	34
45	0x36	35
47.8125	0x35	36
50.625	0x34	37
53.4375	0x33	38
56.25	0x32	38
59.0625	0x30	39
61.875	0x2F	3A
64.6875	0x2E	3A
67.5	0x2C	3B
70.3125	0x2B	3C
73.125	0x2A	3C
75.9375	0x28	3C
78.75	0x27	3D
81.5625	0x25	3D
84.375	0x24	3D
87.1875	0x22	3D

Table 14. Quadrant 2 Phase Control—Mapping of I and Q VM VGA Register Settings to Phase Setting

Phase (Degrees)	I Reg (Hex)	Q Reg (Hex)
90	21	3D
92.8125	01	3D
95.625	03	3D
98.4375	04	3D
101.25	06	3D
104.0625	07	3C
106.875	08	3C
109.6875	0A	3C
112.5	0B	3B
115.3125	0D	3A
118.125	0E	3A
120.9375	0F	39
123.75	11	38
126.5625	12	38
129.375	13	37
132.1875	14	36
135	16	35
137.8125	17	34
140.625	18	33
143.4375	19	31
146.25	19	30
149.0625	1A	2F
151.875	1B	2E
154.6875	1C	2D
157.5	1C	2B
160.3125	1D	2A
163.125	1E	28
165.9375	1E	27
168.75	1E	26
171.5625	1F	24
174.375	1F	23
177.1875	1F	21

Table 15. Quadrant 3 Phase Control—Mapping of I and Q VM VGA Register Settings to Phase Setting

Phase (Degrees)	I Reg (Hex)	Q Reg (Hex)
180	1F	20
182.8125	1F	01
185.625	1F	03
188.4375	1F	04
191.25	1F	06
194.0625	1E	07
196.875	1E	08
199.6875	1D	0A
202.5	1D	0B
205.3125	1C	0D
208.125	1C	0E
210.9375	1B	0F
213.75	1A	10
216.5625	19	11
219.375	18	13
222.1875	17	14
225	16	15
227.8125	15	16
230.625	14	17
233.4375	13	18
236.25	12	18
239.0625	10	19
241.875	0F	1A
244.6875	0E	1A
247.5	0C	1B
250.3125	0B	1C
253.125	0A	1C
255.9375	08	1C
258.75	07	1D
261.5625	05	1D
264.375	04	1D
267.1875	02	1D

Table 16. Quadrant 4 Phase Control—Mapping of I and Q VM VGA Register Settings to Phase Setting

Phase (Degrees)	I Reg (Hex)	Q Reg (Hex)
270	01	1D
272.8125	21	1D
275.625	23	1D
278.4375	24	1D
281.25	26	1D
284.0625	27	1C
286.875	28	1C
289.6875	2A	1C
292.5	2B	1B
295.3125	2D	1A
298.125	2E	1A
300.9375	2F	19
303.75	31	18
306.5625	32	18
309.375	33	17
312.1875	34	16
315	36	15
317.8125	37	14
320.625	38	13
323.4375	39	11
326.25	39	10
329.0625	3A	0F
331.875	3B	0E
334.6875	3C	0D
337.5	3C	0B
340.3125	3D	0A
343.125	3E	08
345.9375	3E	07
348.75	3E	06
351.5625	3F	04
354.375	3F	03
357.1875	3F	01

TRANSMIT AND RECEIVE SUBCIRCUIT CONTROL

The TR_SOURCE bit (Bit 2, Register 0x031) determines whether a dedicated input pin (TR pin) or the SPI registers controls the switching between transmit or receive modes for the ADAR1000. If the TR input is selected, the transmit and receive subcircuit enables are also controlled by the transmit and receive input. Any combination of receive subcircuits or transmit subcircuits can be turned on at a given time. Transmit and receive subcircuits cannot be turned on simultaneously.

TR_SOURCE = 1 (TR Pin Control)

When TR_SOURCE = 1, if the TR input is at logic low, the device goes into receive mode and all receive subcircuits are turned on. If the TR input is at logic high, the device goes into transmit mode, and all transmit subcircuits turn on. As a result, all transmit and receive switching functionality are completely controlled by a single pin.

TR_SOURCE = 0 (SPI Control)

Register 0x02E, Register 0x02F, and Register 0x031 of the SPI registers turn the transmit and receive subcircuits on and off together. Typical operating mode is to set all channel and subcircuit enables active (that is, set Register 0x02E to 0x7F and Register 0x02F to 0x7F), and then use TX_EN and RX_EN (Bits[6:5] of Register 0x31, respectively) to turn on either the transmit subcircuits or receive subcircuits.

TRANSMIT AND RECEIVE SWITCH DRIVER CONTROL

The TR_SW_NEG and TR_SW_POS pins are the output pins that control the external switches that determine the signal flow direction between the transmit and receive modes that the ADAR1000 operates in. Several register bits and the TR pin work together to provide different ways to control the state of the TR_SW_NEG and TR_SW_POS pins.

To enable the switch drivers, set the SW_DRV_EN_TR bit (Bit 4, Register 0x031) to logic high.

The TR_SOURCE bit (Bit 2, Register 0x031) determines whether transmit and receive control is done through the TR_SPI bit (Bit 1, Register 0x031) an SPI or the dedicated transmit, and receive input pin to the chip (if TR_SOURCE = 0, the TR_SPI bit is in control).

The SW_DRV_TR_STATE bit (Bit 7, Register 0x031) determines the polarity of these switch driver outputs (TR_SW_POS and TR_SW_NEG) with respect to transmit and receive mode. Allowing the polarity to be programmable provides additional flexibility when using different transmit and receive switch control configurations (see Table 17).

Table 17. Controlling TR_SW_POS and TR_SW_NEG Output

SW_DRV_EN_TR (Register 0x031, Bit 4)	TR_SOURCE (Register 0x031, Bit 2)[1]	TR (Chip Input)[1]	TR_SPI (Register 0x031, Bit 1)[1]	SW_DRV_TR_MODE_SEL (Register 0x030, Bit 7)[1]	Device Transmit or Receive State[1]	SW_DRV_TR_STATE (Register 0x031, Bit 7)[1]	TR_SW_POS (Chip Output)	TR_SW_NEG (Chip Output)
0	X	X	X	X	X	X	Floating	Floating
1	0	X	0	0	Receive	0	Floating	0 V
1	0	X	0	0	Receive	1	Floating	−5 V
1	0	X	1	0	Transmit	0	Floating	−5 V
1	0	X	1	0	Transmit	1	Floating	0 V
1	1	0	X	0	Receive	0	Floating	0 V
1	1	0	X	0	Receive	1	Floating	−5 V
1	1	1	X	0	Transmit	0	Floating	−5 V
1	1	1	X	0	Transmit	1	Floating	0 V
1	0	X	0	1	Receive	0	0 V	Floating
1	0	X	0	1	Receive	1	3.3 V	Floating
1	0	X	1	1	Transmit	0	3.3 V	Floating
1	0	X	1	1	Transmit	1	0 V	Floating
1	1	0	X	1	Receive	0	0 V	Floating
1	1	0	X	1	Receive	1	3.3 V	Floating
1	1	1	X	1	Transmit	0	3.3 V	Floating
1	1	1	X	1	Transmit	1	0 V	Floating

[1] X means don't care.

PA BIAS OUTPUT CONTROL

The four PA bias output voltages are controlled by four separate DACs, which in turn are controlled by a combination of three bits from the SPI registers (BIAS_CTRL, TR_SOURCE, TX_EN), two input pins (TR and PA_ON), and the EXT_PAx_BIAS_ON (Register 0x029 to Register 0x02C) and EXT_PAx_BIAS_OFF (Register 0x046 to Register 0x049) bits (see Table 18). BIAS_CTRL determines if the bias DACs always use the CHx_PA_BIAS_ON value for each channel. TR_SOURCE determines whether switching between transmit and receive mode is controlled by the SPI register or the TR input. The PA_ON input determines whether to use the CHx_PA_BIAS_ON or CHx_PA_BIAS_OFF value when the ADAR1000 is in transmit mode and BIAS_CTRL is set to 1.

LNA BIAS OUTPUT CONTROL

The LNA_BIAS output voltage is controlled by a DAC which in turn is controlled by a combination of four bits in the SPI registers (LNA_BIAS_OUT_EN, BIAS_CTRL, TR_SOURCE, and RX_EN), the TR input pin, and the LNA_BIAS_ON and LNA_BIAS_OFF registers (Register 0x02D and Register 0x04A, respectively), as shown in Table 19. The LNA_BIAS output is only enabled if LNA_BIAS_OUT_EN = 1. Otherwise, the output is open. The output is set by the LNA_BIAS_ON register when the ADAR1000 is in receive mode and BIAS_CTRL is set to 1.

TRANSMIT/RECEIVE DELAY CONTROL

The delays between switching from transmitter-to-receiver and receiver-to-transmitter, Delay 1 and Delay 2, are controlled via Register 0x4B and Register 0x4C, respectively. The delay time is proportional to the SPI clock period. With a 50 ns clock period (20 MHz), the maximum value for either Delay 1 or Delay 2 is 750 ns. This delay value corresponds to a delay code of 15 or 0xF in either the top and/or bottom nibbles of Register 0x4B and Register 0x4C. A delay value of 0 corresponds to 0 ns delay, a delay value of 1 corresponds to 50 ns, a delay value of 2 corresponds to 100 ns, and so on.

Table 18. Control of PA Bias Outputs

BIAS_CTRL (Register 0x030, Bit 6)	TR_SOURCE (Register 0x031, Bit 2)	TX_EN (Register 0x031, Bit 6)	TR (Input to Chip)	PA_ON (Input to Chip)	PA Bias Bits Used (x = 1, 2, 3, or 4)
0	X[1]	X[1]	X[1]	X[1]	EXT_PAx_BIAS_ON
1	0	0	X[1]	X[1]	EXT_PAx_BIAS_OFF
1	0	1	X[1]	X[1]	EXT_PAx_BIAS_ON
1	1	0	0	X[1]	EXT_PAx_BIAS_OFF
1	1	0	1	0	EXT_PAx_BIAS_OFF
1	1	0	1	1	EXT_PAx_BIAS_ON

[1] X means don't care.

Table 19. Control of LNA_BIAS Output

LNA_BIAS_OUT_EN (Register 0x030, Bit 4)	BIAS_CTRL (Register 0x030, Bit 6)	TR_SOURCE (Register 0x031, Bit 2)	RX_EN (Register 0x031, Bit 5)	TR (Input to Chip)	LNA Bias Bits Used
0	X[1]	X[1]	X[1]	X[1]	Open circuit (floating)
1	0	0	0	X[1]	EXT_LNA_BIAS_ON
1	0	0	1	X[1]	EXT_LNA_BIAS_ON
1	1	0	0	X[1]	EXT_LNA_BIAS_OFF
1	1	0	1	X[1]	EXT_LNA_BIAS_ON
1	0	1	0	0	EXT_LNA_BIAS_ON
1	0	1	0	1	EXT_LNA_BIAS_ON
1	1	1	0	0	EXT_LNA_BIAS_OFF
1	1	1	0	1	EXT_LNA_BIAS_ON

[1] X means don't care.

Transmit and Receive Mode Switching

Figure 92 shows the timing for transmit and receive mode switching.

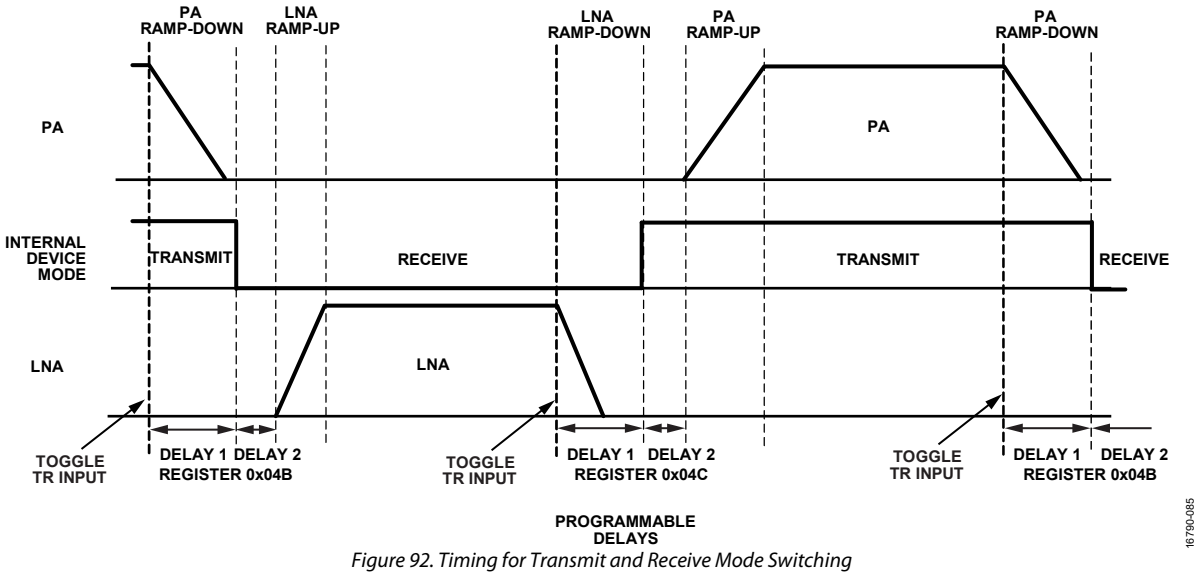


Figure 92. Timing for Transmit and Receive Mode Switching

SPI PROGRAMMING EXAMPLE

The SPI programming example in Table 20 sets up the bias of the different subcircuits, as well as the gain and phase settings of all channels. The device stays in the receive mode until the TR input is raised high, and the device switches into transmit mode. All the external amplifier bias and switches also change state accordingly.

Table 20. Register Programing to Set Up the ADAR1000

Register Address	Content (Hexadecimal)	Description
0x000	BD	Reset whole chip, use SDO line for readback, address auto incrementing in block write mode.
0x401	10	Allow LDO adjustments from user settings.
0x400	55	Adjust LDOs.
0x046	60	Set PA_BIAS1 output to approximately −1.8 V in receive mode.
0x047	60	Set PA_BIAS2 output to approximately −1.8 V in receive mode.
0x048	60	Set PA_BIAS3 output to approximately −1.8 V in receive mode.
0x049	60	Set PA_BIAS4 output to approximately −1.8 V in receive mode.
0x029	28	Set PA_BIAS1 output to approximately −0.8 V in transmit mode.
0x02A	28	Set PA_BIAS2 output to approximately −0.8 V in transmit mode.
0x02B	28	Set PA_BIAS3 output to approximately −0.8 V in transmit mode.
0x02C	28	Set PA_BIAS4 output to approximately −0.8 V in transmit mode.
0x02D	28	Set LNA_BIAS to approximately −0.8 V.
0x030	1F	Enable LNA_BIAS, select fixed output.
0x038	60	Select SPI instead of internal RAM for channel settings.
0x031	1C	Select TR input for transmit and receive switching control, enables switch outputs.
0x02F	7F	Select all four transmit channel and enable transmit driver, vector modulator, and VGA.
0x036	16	Set transmit VGA bias to 2, vector modulator bias to 6.
0x037	06	Set transmit driver bias to 6.
0x01C	FF	Set Channel 1 attenuator to 0 dB, VGA gain to maximum.
0x020	36	Set Channel 1 vector modulator I input to positive, Magnitude 16.
0x021	35	Set Channel 1 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°
0x01D	FF	Set Channel 2 attenuator to 0 dB, VGA gain to maximum.
0x020	36	Set Channel 2 vector modulator I input to positive, Magnitude 16.
0x 021	35	Set Channel 2 vector modulator Q input to positive, magnitude 15; these two together set phase to 45°.
0x 01E	FF	Set Channel 3 attenuator to 0 dB, VGA gain to maximum.
0x 020	36	Set Channel 3 vector modulator I input to positive, Magnitude 16.
0x 021	35	Set Channel 3 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 01F	FF	Set Channel 4 attenuator to 0 dB, VGA gain to maximum.
0x 020	36	Set Channel 4 vector modulator I input to positive, Magnitude 16.
0x 021	35	Set Channel 4 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 02E	7F	Select all four receive channel, enable receive LNA, vector modulator and VGA.
0x 034	08	Set receive LNA bias to 8.
0x 035	16	Set receive VGA bias to 2, vector modulator bias to 6.
0x 010	FF	Set Channel 1 attenuator to 0 dB, VGA gain to maximum.
0x 014	36	Set Channel 1 vector modulator I input to positive, Magnitude 16.
0x 015	35	Set Channel 1 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 011	FF	Set Channel 2 attenuator to 0 dB, VGA gain to maximum.
0x 016	36	Set Channel 2 vector modulator I input to positive, Magnitude 16.
0x 017	35	Set Channel 2 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 012	FF	Set Channel 3 attenuator to 0 dB; VGA gain to maximum.
0x 018	36	Set Channel 3 vector modulator I input to positive, Magnitude 16.
0x 019	35	Set Channel 3 vector modulator Q input to positive, Magnitude 15; these two together set phase to 45°.
0x 013	FF	Set Channel 4 attenuator to 0 dB, VGA gain to maximum.
0x 01A	36	Set Channel 4 vector modulator I input to positive, Magnitude 16.
0x 01B	35	Set Channel 4 vector modulator Q input to positive, Magnitude 15. These two together set phase to 45°.

Table 21. ADAR1000 Memory Register Programming Example for Beam Position 0 and Bias Setting 1

Register[1]	Content	Description
0x038	00	Set beam ram bypass and bias ram bypass bits to load working registers from memory
0x1000	FF	Set receiver VGA gain and attenuator values for Channel 1; VGA gain maximum, attenuator = 0 dB
0x1001	36	Set receiver I vector and polarity values for Channel 1; positive polarity, Magnitude = 16
0x1002	35	Set receiver Q vector and polarity values for Channel 1; positive polarity, Magnitude = 15
0x1004	FF	Set receiver VGA gain and attenuator values for Channel 2; VGA gain maximum, attenuator = 0 dB
0x1005	36	Set receiver I vector and polarity values for Channel 2; positive polarity, Magnitude = 16
0x1006	35	Set receiver Q vector and polarity values for Channel 2; positive polarity, Magnitude = 15
0x1008	FF	Set receiver VGA gain and attenuator values for Channel 3; VGA gain maximum, attenuator = 0 dB
0x1009	36	Set receiver I vector and polarity values for Channel 3; positive polarity, Magnitude = 16
0x100A	35	Set receiver Q vector and polarity values for Channel 3; positive polarity, Magnitude = 15
0x100C	FF	Set receiver VGA gain and attenuator values for Channel 4; VGA gain maximum, attenuator = 0 dB
0x100D	36	Set receiver I vector and polarity values for Channel 4; positive polarity, Magnitude = 16
0x100E	35	Set receiver Q vector and polarity values for Channel 4; positive polarity, Magnitude = 15
0x1790	60	Set receiver EXT_LNA_BIAS_OFF value for receiver Bias Setting 1; −1.8 V output
0x1791	28	Set receiver EXT_LNA_BIAS_ON value for receiver Bias Setting 1; −0.8 V output
0x1794	16	Set receiver vector modulator and VGA bias values for receiver; VGA = 2, vector modulator = 6
0x1795	08	Set receiver LNA bias value for receiver; LNA = 8
0x1800	FF	Set transmitter VGA gain and attenuator values for Channel 1
0x1801	36	Set transmitter I vector and polarity values for Channel 1
0x1802	35	Set transmitter Q vector and polarity values for Channel 1
0x1804	FF	Set transmitter VGA gain and attenuator values for Channel 2
0x1805	36	Set transmitter I vector and polarity values for Channel 2
0x1806	35	Set transmitter Q vector and polarity values for Channel 2
0x1808	FF	Set transmitter VGA gain and attenuator values for Channel 3
0x1809	36	Set transmitter I vector and polarity values for Channel 3
0x180A	35	Set transmitter Q vector and polarity values for Channel 3
0x180C	FF	Set transmitter VGA gain and attenuator values for Channel 4
0x180D	36	Set transmitter I vector and polarity values for Channel 4
0x180E	35	Set transmitter Q vector and polarity values for Channel 4
0x1F90	60	Set transmitter EXT_PA1_BIAS_OFF value for transmitter; −1.8 V output
0x1F91	60	Set transmitter EXT_PA2_BIAS_OFF value for transmitter; −1.8 V output
0x1F92	60	Set transmitter EXT_PA3_BIAS_OFF value for transmitter; −1.8 V output
0x1F94	28	Set transmitter EXT_PA1_BIAS_ON value for transmitter; −0.8 V output
0x1F95	28	Set transmitter EXT_PA2_BIAS_ON value for transmitter; −0.8 V output
0x1F96	28	Set transmitter EXT_PA3_BIAS_ON value for transmitter; −0.8 V output
0x1F98	60	Set transmitter EXT_PA4_BIAS_OFF value for transmitter; −1.8 V output
0x1F99	28	Set transmitter EXT_PA4_BIAS_ON value for transmitter; −0.8 V output
0x1F9C	16	Set transmitter vector modulator and VGA bias values for transmitter; VGA bias = 2, vector modulator = 6
0x1F9D	06	Set transmitter driver bias value for transmitter; driver = 6
0x39	80	Set all receiver channels to Beam Position 0 and set the fetch bit; the user can individually set the receiver channels using Register 0x03D through Register 0x040
0x3A	80	Set all transmitter channels to Beam Position 0 and set the fetch bit; the user can individually set the transmitter channels using Register 0x041 through Register 0x044
0x51	08	Set receiver bias to Bias Setting 1 and set the fetch bit
0x52	08	Set receiver bias to Bias Setting 1 and set the fetch bit

[1] Transmitter and receiver gain are set to maximum and the phase value is 45° for all channels. Refer to Table 7 through Table 11 for bit decoding and memory address values.

POWERING THE ADAR1000

The ADAR1000 has two power supply domains, +3.3V and −5 V. These power supplies can be driven with the synchronous step down regulator LT8609S and the inverting dc to dc converter LT3462, respectively. With a single 5.5 V supply driving both the LT8609S and LT3462, the LT8609S generates the +3.3 V supply, while the LT3462 generates the −5 V supply.

A single ADAR1000 is tested using the LT8609S and LT3462. Figure 93 and Figure 94 show the rise and fall times of the LNA_BIAS pin under a maximum load condition of −10 mA. Figure 95 and Figure 96 show the rise and fall times of all four PA_BIASx pins, each with a maximum load condition of −10 mA. A simplified block diagram of the test setup for the LT8609S and LT3462 is shown in Figure 97.

If more than two ADAR1000 devices must be powered, and if the user does not want multiple LT8609S and LT3462 devices, there are several solutions that power from four to 64 ADAR1000 devices by using a single chip per voltage supply. Table 22 shows these solutions by providing the quantity of ADAR1000 devices and the corresponding chips required to power multiple ADAR1000 devices.

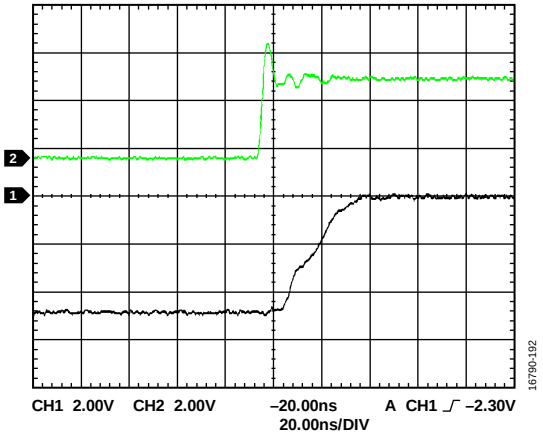


Figure 93. LNA_BIAS Rise Time; −10 mA Load

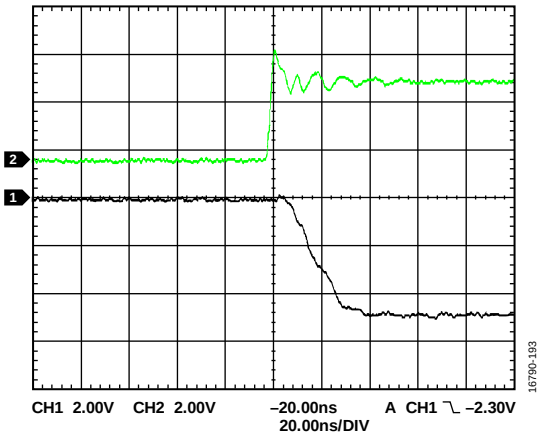


Figure 94. LNA_BIAS Fall Time; −10 mA load

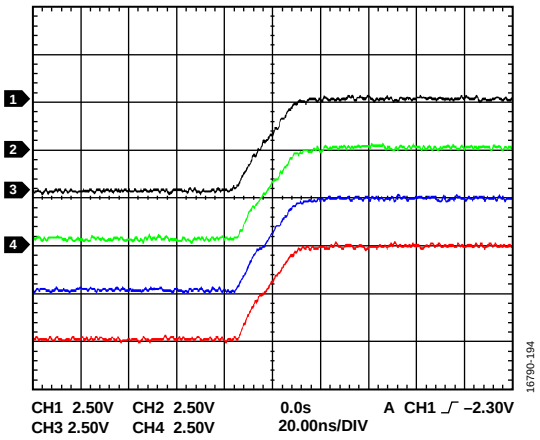


Figure 95. PA_BIAS1, PA_BIAS2, PA_BIAS3, or PA_BIAS 4 Rise Time; −10 mA load

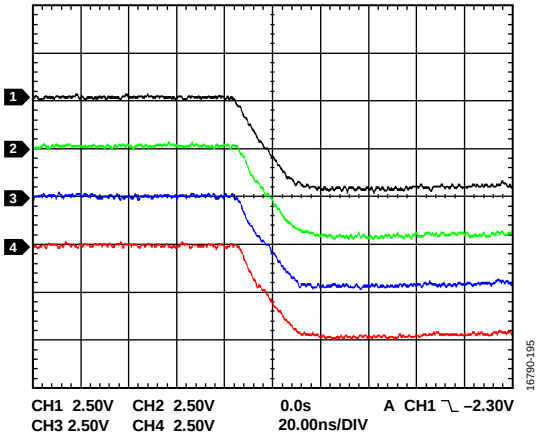


Figure 96. PA_BIAS1, PA_BIAS2, PA_BIAS3, or PA_BIAS4 Fall Time; −10 mA Load

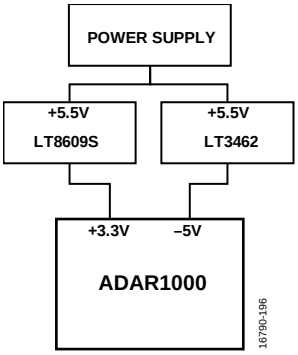


Figure 97. Block Diagram of the LT8609S and the LT3462 Powering the ADAR1000

Table 22. Power Solutions for Multiple ADAR1000 Devices

ADAR1000 Quantity	Supplying +3.3 V	Supplying −5 V
4	LT8609S	LT1931
16	LT8642S	LT3580
32	LTC7151S	LT3957A
64	LTM4636	LT3757

REGISTER MAP

Table 23. Control Registers Summary

Reg. (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
000	INTERFACE_ CONFIG_A	[7:0]	SOFTRESET	LSB_ FIRST	ADDR_ ASCN	SDO ACTIVE	SDO ACTIVE_	ADDR_ ASCN_	LSB_FIRST_	SOFTRESET_	0x00	R/W
001	INTERFACE_ CONFIG_B	[7:0]	SINGLE_ INSTRUCTION	CSB_ STALL	MASTER_ SLAVE_RB	SLOW_ INTER FACE_ CTRL	RESERVED	SOFT_RESET		RESERVED	0x00	R/W
002	DEV_CONFIG	[7:0]	DEV_STATUS				CUST_OPERATING_ MODE		NORM_ OPERATING_MODE		0x10	R/W
003	CHIP_TYPE	[7:0]	CHIP_TYPE								0x00	R
004	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
005	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
00A	SCRATCH_PAD	[7:0]	SCRATCHPAD								0x00	R/W
00B	SPI_REV	[7:0]	SPI_REV								0x00	R
00C	VENDOR_ID_H	[7:0]	VENDOR_ID[15:8]								0x00	R
00D	VENDOR_ID_L	[7:0]	VENDOR_ID[7:0]								0x00	R
00F	TRANSFER_REG	[7:0]	RESERVED							MASTER_ SLAVE_XFER	0x00	R/W
010	CH1_RX_GAIN	[7:0]	CH1_ATTN_RX	RX_VGA_CH1							0x00	R/W
011	CH2_RX_GAIN	[7:0]	CH2_ATTN_RX	RX_VGA_CH2							0x00	R/W
012	CH3_RX_GAIN	[7:0]	CH3_ATTN_RX	RX_VGA_CH3							0x00	R/W
013	CH4_RX_GAIN	[7:0]	CH4_ATTN_RX	RX_VGA_CH4							0x00	R/W
014	CH1_RX_PHASE_I	[7:0]	RESERVED		RX_VM_ CH1_POL_I	RX_VM_CH1_GAIN_I					0x00	R/W
015	CH1_RX_PHASE_Q	[7:0]	RESERVED		RX_VM_ CH1_ POL_Q	RX_VM_CH1_GAIN_Q					0x00	R/W
016	CH2_RX_PHASE_I	[7:0]	RESERVED		RX_VM_ CH2_ POL_I	RX_VM_CH2_GAIN_I					0x00	R/W
017	CH2_RX_PHASE_Q	[7:0]	RESERVED		RX_VM_ CH2_ POL_Q	RX_VM_CH2_GAIN_Q					0x00	R/W
018	CH3_RX_PHASE_I	[7:0]	RESERVED		RX_VM_ CH3_ POL_I	RX_VM_CH3_GAIN_I					0x00	R/W
019	CH3_RX_PHASE_Q	[7:0]	RESERVED		RX_VM_ CH3_ POL_Q	RX_VM_CH3_GAIN_Q					0x00	R/W
01A	CH4_RX_PHASE_I	[7:0]	RESERVED		RX_VM_ CH4_ POL_I	RX_VM_CH4_GAIN_I					0x00	R/W
01B	CH4_RX_PHASE_Q	[7:0]	RESERVED		RX_VM_ CH4_ POL_Q	RX_VM_CH4_GAIN_Q					0x00	R/W
01C	CH1_TX_GAIN	[7:0]	CH1_ATTN_TX	TX_VGA_CH1							0x00	R/W
01D	CH2_TX_GAIN	[7:0]	CH2_ATTN_TX	TX_VGA_CH2							0x00	R/W
01E	CH3_TX_GAIN	[7:0]	CH3_ATTN_TX	TX_VGA_CH3							0x00	R/W
01F	CH4_TX_GAIN	[7:0]	CH4_ATTN_TX	TX_VGA_CH4							0x00	R/W
020	CH1_TX_PHASE_I	[7:0]	RESERVED		TX_VM_ CH1_POL_I	TX_VM_CH1_GAIN_I					0x00	R/W
021	CH1_TX_PHASE_Q	[7:0]	RESERVED		TX_VM_ CH1_ POL_Q	TX_VM_CH1_GAIN_Q					0x00	R/W
022	CH2_TX_PHASE_I	[7:0]	RESERVED		TX_VM_ CH2_ POL_I	TX_VM_CH2_GAIN_I					0x00	R/W

Reg. (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
023	CH2_TX_PHASE_Q	[7:0]	RESERVED		TX_VM_CH2_POL_Q	TX_VM_CH2_GAIN_Q					0x00	R/W
024	CH3_TX_PHASE_I	[7:0]	RESERVED		TX_VM_CH3_POL_I	TX_VM_CH3_GAIN_I					0x00	R/W
025	CH3_TX_PHASE_Q	[7:0]	RESERVED		TX_VM_CH3_POL_Q	TX_VM_CH3_GAIN_Q					0x00	R/W
026	CH4_TX_PHASE_I	[7:0]	RESERVED		TX_VM_CH4_POL_I	TX_VM_CH4_GAIN_I					0x00	R/W
027	CH4_TX_PHASE_Q	[7:0]	RESERVED		TX_VM_CH4_POL_Q	TX_VM_CH4_GAIN_Q					0x00	R/W
028	LD_WRK_REGS	[7:0]	RESERVED						LDTX_OVERRIDE	LDRX_OVERRIDE	0x00	W
029	CH1_PA_BIAS_ON	[7:0]	EXT_PA1_BIAS_ON								0x00	R/W
02A	CH2_PA_BIAS_ON	[7:0]	EXT_PA2_BIAS_ON								0x00	R/W
02B	CH3_PA_BIAS_ON	[7:0]	EXT_PA3_BIAS_ON								0x00	R/W
02C	CH4_PA_BIAS_ON	[7:0]	EXT_PA4_BIAS_ON								0x00	R/W
02D	LNA_BIAS_ON	[7:0]	EXT_LNA_BIAS_ON								0x00	R/W
02E	RX_ENABLES	[7:0]	RESERVED	CH1_RX_EN	CH2_RX_EN	CH3_RX_EN	CH4_RX_EN	RX_LNA_EN	RX_VM_EN	RX_VGA_EN	0x00	R/W
02F	TX_ENABLES	[7:0]	RESERVED	CH1_TX_EN	CH2_TX_EN	CH3_TX_EN	CH4_TX_EN	TX_DRV_EN	TX_VM_EN	TX_VGA_EN	0x00	R/W
030	MISC_ENABLES	[7:0]	SW_DRV_TR_MODE_SEL	BIAS_CTRL	BIAS_EN	LNA_BIAS_OUT_EN	CH1_DET_EN	CH2_DET_EN	CH3_DET_EN	CH4_DET_EN	0x00	R/W
031	SW_CTRL	[7:0]	SW_DRV_TR_STATE	TX_EN	RX_EN	SW_DRV_EN_TR	SW_DRV_EN_POL	TR_SOURCE	TR_SPI	POL	0x00	R/W
032	ADC_CTRL	[7:0]	ADC_CLKFREQ_SEL	ADC_EN	CLK_EN	ST_CONV	MUX_SEL			ADC_EOC	0x00	R/W
033	ADC_OUTPUT	[7:0]	ADC								0x00	R
034	BIAS_CURRENT_RX_LNA	[7:0]	RESERVED				LNA_BIAS				0x00	R/W
035	BIAS_CURRENT_RX	[7:0]	RESERVED	RX_VGA_BIAS				RX_VM_BIAS			0x00	R/W
036	BIAS_CURRENT_TX	[7:0]	RESERVED	TX_VGA_BIAS				TX_VM_BIAS			0x00	R/W
037	BIAS_CURRENT_TX_DRV	[7:0]	RESERVED					TX_DRV_BIAS			0x00	R/W
038	MEM_CTRL	[7:0]	SCAN_MODE_EN	BEAM_RAM_BYPASS	BIAS_RAM_BYPASS	RESERVED	TX_BEAM_STEP_EN	RX_BEAM_STEP_EN	TX_CHX_RAM_BYPASS	RX_CHX_RAM_BYPASS	0x00	R/W
039	RX_CHX_MEM	[7:0]	RX_CHX_RAM_FETCH	RX_CHX_RAM_INDEX							0x00	R/W
03A	TX_CHX_MEM	[7:0]	TX_CHX_RAM_FETCH	TX_CHX_RAM_INDEX							0x00	R/W
03D	RX_CH1_MEM	[7:0]	RX_CH1_RAM_FETCH	RX_CH1_RAM_INDEX							0x00	R/W
03E	RX_CH2_MEM	[7:0]	RX_CH2_RAM_FETCH	RX_CH2_RAM_INDEX							0x00	R/W
03F	RX_CH3_MEM	[7:0]	RX_CH3_RAM_FETCH	RX_CH3_RAM_INDEX							0x00	R/W
040	RX_CH4_MEM	[7:0]	RX_CH4_RAM_FETCH	RX_CH4_RAM_INDEX							0x00	R/W
041	TX_CH1_MEM	[7:0]	TX_CH1_RAM_FETCH	TX_CH1_RAM_INDEX							0x00	R/W
042	TX_CH2_MEM	[7:0]	TX_CH2_RAM_FETCH	TX_CH2_RAM_INDEX							0x00	R/W

Reg. (Hex)	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
043	TX_CH3_MEM	[7:0]	TX_CH3_ RAM_FETCH	TX_CH3_RAM_INDEX							0x00	R/W
044	TX_CH4_MEM	[7:0]	TX_CH4_ RAM_FETCH	TX_CH4_RAM_INDEX							0x00	R/W
045	REV_ID	[7:0]	REV_ID								0x00	R
046	CH1_PA_BIAS_OFF	[7:0]	EXT_PA1_BIAS_OFF								0x00	R/W
047	CH2_PA_BIAS_OFF	[7:0]	EXT_PA2_BIAS_OFF								0x00	R/W
048	CH3_PA_BIAS_OFF	[7:0]	EXT_PA3_BIAS_OFF								0x00	R/W
049	CH4_PA_BIAS_OFF	[7:0]	EXT_PA4_BIAS_OFF								0x00	R/W
04A	LNA_BIAS_OFF	[7:0]	EXT_LNA_BIAS_OFF								0x00	R/W
04B	TX_TO_RX_ DELAY_CTRL	[7:0]	TX_TO_RX_DELAY_1				TX_TO_RX_DELAY_2				0x00	R/W
04C	RX_TO_ TX_DELAY_CTRL	[7:0]	RX_TO_TX_DELAY_1				RX_TO_TX_DELAY_2				0x00	R/W
04D	TX_BEAM_ STEP_START	[7:0]	TX_BEAM_STEP_START								0x00	R/W
04E	TX_BEAM_ STEP_STOP	[7:0]	TX_BEAM_STEP_STOP								0x00	R/W
04F	RX_BEAM_ STEP_START	[7:0]	RX_BEAM_STEP_START								0x00	R/W
050	RX_BEAM_ STEP_STOP	[7:0]	RX_BEAM_STEP_STOP								0x00	R/W
051	RX_BIAS_RAM_CTL	[7:0]	RESERVED				RX_BIAS_ RAM_FETCH	RX_BIAS_RAM_INDEX			0x00	R/W
052	TX_BIAS_RAM_CTL	[7:0]	RESERVED				TX_BIAS_ RAM_FETCH	TX_BIAS_RAM_INDEX			0x00	R/W
400	LDO_TRIM_CTL_0	[7:0]	LDO_TRIM_REG								0x00	R/W
401	LDO_TRIM_CTL_1	[7:0]	RESERVED						LDO_TRIM_SEL		0x00	R/W

REGISTER DESCRIPTIONS

Address: 0x000, Reset: 0x00, Name: INTERFACE_CONFIG_A

Functions of the last four bits in this register are intentionally replicated from the first four bits in a reverse manner so that the bit pattern is the same, whether sent LSB first or MSB first.

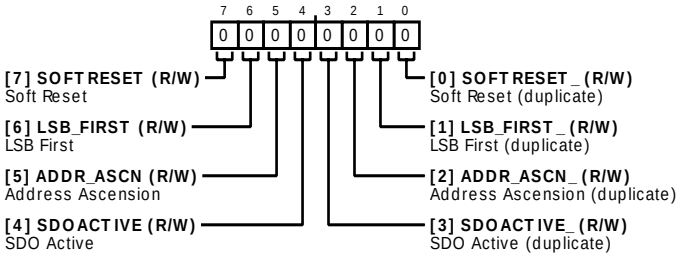


Table 24. Bit Descriptions for INTERFACE_CONFIG_A

Bit	Bit Name	Settings	Description	Reset	Access
7	SOFTRESET		Soft Reset	0x0	R/W
6	LSB_FIRST		LSB First	0x0	R/W
5	ADDR_ASCN		Address Ascension	0x0	R/W
4	SDOACTIVE		SDO Active	0x0	R/W
3	SDOACTIVE_		SDO Active (duplicate)	0x0	R/W
2	ADDR_ASCN_		Address Ascension (duplicate)	0x0	R/W
1	LSB_FIRST_		LSB First (duplicate)	0x0	R/W
0	SOFTRESET_		Soft Reset (duplicate)	0x0	R/W

Address: 0x001, Reset: 0x00, Name: INTERFACE_CONFIG_B

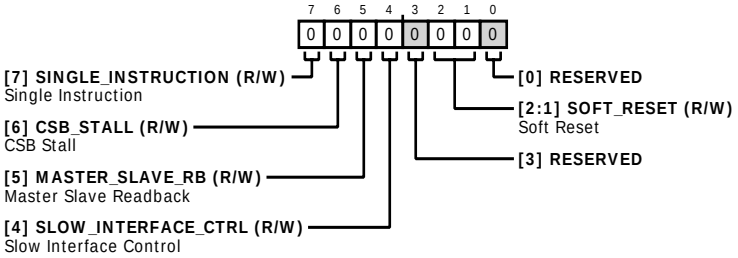


Table 25. Bit Descriptions for INTERFACE_CONFIG_B

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INSTRUCTION		Single Instruction	0x0	R/W
6	CSB_STALL		CSB Stall	0x0	R/W
5	MASTER_SLAVE_RB		Master Slave Readback	0x0	R/W
4	SLOW_INTERFACE_CTRL		Slow Interface Control	0x0	R/W
3	RESERVED		Reserved	0x0	R
[2:1]	SOFT_RESET		Soft Reset	0x0	R/W
0	RESERVED		Reserved	0x0	R

Address: 0x002, Reset: 0x10, Name: DEV_CONFIG

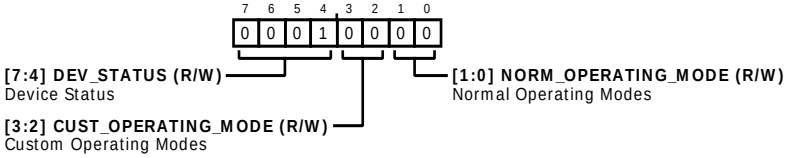


Table 26. Bit Descriptions for DEV_CONFIG

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	DEV_STATUS		Device Status	0x1	R/W
[3:2]	CUST_OPERATING_MODE		Custom Operating Modes	0x0	R/W
[1:0]	NORM_OPERATING_MODE		Normal Operating Modes	0x0	R/W

Address: 0x003, Reset: 0x00, Name: CHIP_TYPE

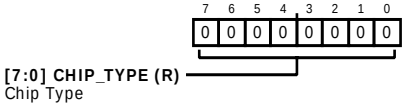


Table 27. Bit Descriptions for CHIP_TYPE

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	CHIP_TYPE		Chip Type	0x0	R

Address: 0x004, Reset: 0x00, Name: PRODUCT_ID_H

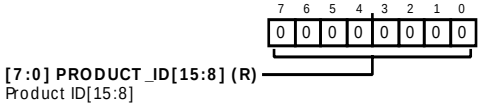


Table 28. Bit Descriptions for PRODUCT_ID_H

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]		Product ID[15:8]	0x0	R

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_L

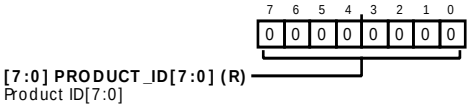


Table 29. Bit Descriptions for PRODUCT_ID_L

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]		Product ID[7:0]	0x0	R

Address: 0x00A, Reset: 0x00, Name: SCRATCH_PAD

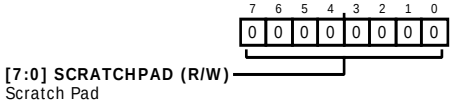


Table 30. Bit Descriptions for SCRATCH_PAD

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	SCRATCHPAD		Scratch Pad	0x0	R/W

Address: 0x00B, Reset: 0x00, Name: SPI_REV

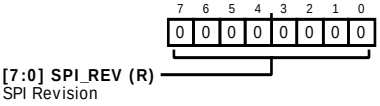


Table 31. Bit Descriptions for SPI_REV

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	SPI_REV		SPI Revision	0x0	R

Address: 0x00C, Reset: 0x00, Name: VENDOR_ID_H

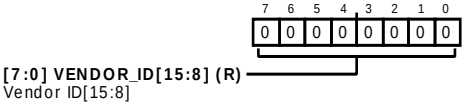


Table 32. Bit Descriptions for VENDOR_ID_H

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]		Vendor ID[15:8]	0x0	R

Address: 0x00D, Reset: 0x00, Name: VENDOR_ID_L

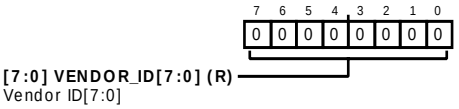


Table 33. Bit Descriptions for VENDOR_ID_L

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]		Vendor ID[7:0]	0x0	R

Address: 0x00F, Reset: 0x00, Name: TRANSFER_REG

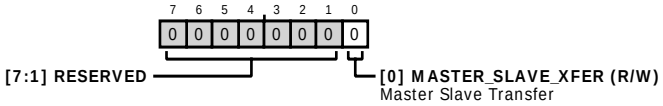


Table 34. Bit Descriptions for TRANSFER_REG

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved	0x0	R
0	MASTER_SLAVE_XFER		Master Slave Transfer	0x0	R/W

Address: 0x010, Reset: 0x00, Name: CH1_RX_GAIN

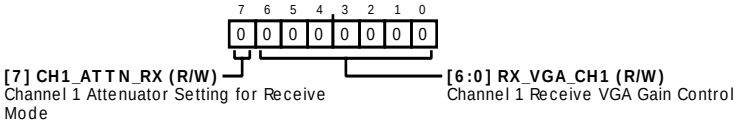


Table 35. Bit Descriptions for CH1_RX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH1_ATTN_RX		Channel 1 Attenuator Setting for Receive Mode	0x0	R/W
[6:0]	RX_VGA_CH1		Channel 1 Receive VGA Gain Control	0x0	R/W

Address: 0x011, Reset: 0x00, Name: CH2_RX_GAIN

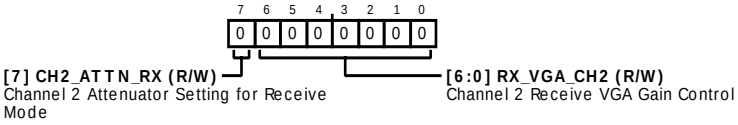


Table 36. Bit Descriptions for CH2_RX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH2_ATTN_RX		Channel 2 Attenuator Setting for Receive Mode	0x0	R/W
[6:0]	RX_VGA_CH2		Channel 2 Receive VGA Gain Control	0x0	R/W

Address: 0x012, Reset: 0x00, Name: CH3_RX_GAIN

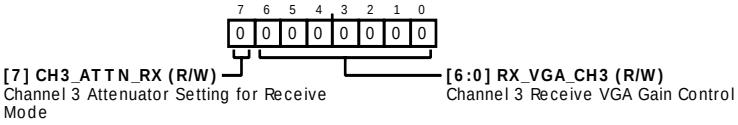


Table 37. Bit Descriptions for CH3_RX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH3_ATTN_RX		Channel 3 Attenuator Setting for Receive Mode	0x0	R/W
[6:0]	RX_VGA_CH3		Channel 3 Receive VGA Gain Control	0x0	R/W

Address: 0x013, Reset: 0x00, Name: CH4_RX_GAIN

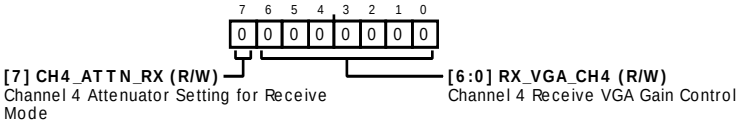


Table 38. Bit Descriptions for CH4_RX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH4_ATTN_RX		Channel 4 Attenuator Setting for Receive Mode	0x0	R/W
[6:0]	RX_VGA_CH4		Channel 4 Receive VGA Gain Control	0x0	R/W

Address: 0x014, Reset: 0x00, Name: CH1_RX_PHASE_I

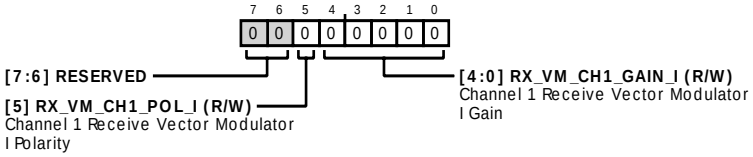


Table 39. Bit Descriptions for CH1_RX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH1_POL_I		Channel 1 Receive Vector Modulator I Polarity	0x0	R/W
[4:0]	RX_VM_CH1_GAIN_I		Channel 1 Receive Vector Modulator I Gain	0x0	R/W

Address: 0x015, Reset: 0x00, Name: CH1_RX_PHASE_Q

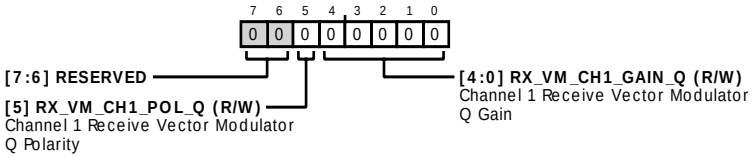


Table 40. Bit Descriptions for CH1_RX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH1_POL_Q		Channel 1 Receive Vector Modulator Q Polarity	0x0	R/W
[4:0]	RX_VM_CH1_GAIN_Q		Channel 1 Receive Vector Modulator Q Gain	0x0	R/W

Address: 0x016, Reset: 0x00, Name: CH2_RX_PHASE_I

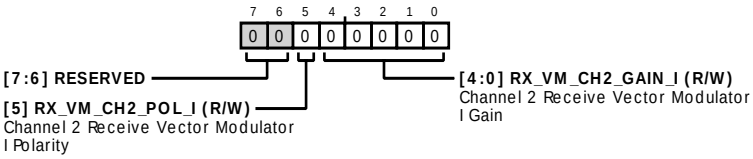


Table 41. Bit Descriptions for CH2_RX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH2_POL_I		Channel 2 Receive Vector Modulator I Polarity	0x0	R/W
[4:0]	RX_VM_CH2_GAIN_I		Channel 2 Receive Vector Modulator I Gain	0x0	R/W

Address: 0x017, Reset: 0x00, Name: CH2_RX_PHASE_Q

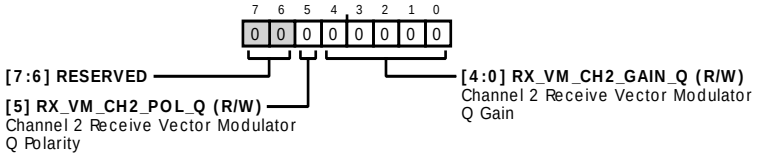


Table 42. Bit Descriptions for CH2_RX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH2_POL_Q		Channel 2 Receive Vector Modulator Q Polarity	0x0	R/W
[4:0]	RX_VM_CH2_GAIN_Q		Channel 2 Receive Vector Modulator Q Gain	0x0	R/W

Address: 0x018, Reset: 0x00, Name: CH3_RX_PHASE_I

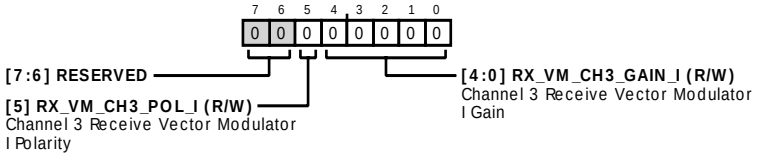


Table 43. Bit Descriptions for CH3_RX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
5	RX_VM_CH3_POL_I		Channel 3 Receive Vector Modulator I Polarity	0x0	R/W
[4:0]	RX_VM_CH3_GAIN_I		Channel 3 Receive Vector Modulator I Gain	0x0	R/W

Address: 0x019, Reset: 0x00, Name: CH3_RX_PHASE_Q

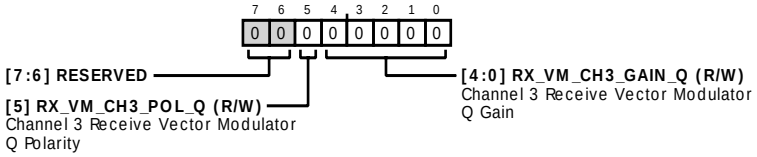


Table 44. Bit Descriptions for CH3_RX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH3_POL_Q		Channel 3 Receive Vector Modulator Q Polarity	0x0	R/W
[4:0]	RX_VM_CH3_GAIN_Q		Channel 3 Receive Vector Modulator Q Gain	0x0	R/W

Address: 0x01A, Reset: 0x00, Name: CH4_RX_PHASE_I

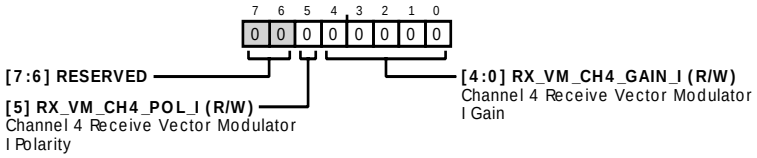


Table 45. Bit Descriptions for CH4_RX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH4_POL_I		Channel 4 Receive Vector Modulator I Polarity	0x0	R/W
[4:0]	RX_VM_CH4_GAIN_I		Channel 4 Receive Vector Modulator I Gain	0x0	R/W

Address: 0x01B, Reset: 0x00, Name: CH4_RX_PHASE_Q

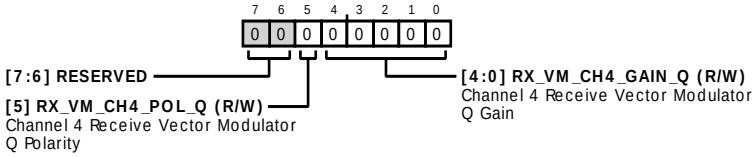


Table 46. Bit Descriptions for CH4_RX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	RX_VM_CH4_POL_Q		Channel 4 Receive Vector Modulator Q Polarity	0x0	R/W
[4:0]	RX_VM_CH4_GAIN_Q		Channel 4 Receive Vector Modulator Q Gain	0x0	R/W

Address: 0x01C, Reset: 0x00, Name: CH1_TX_GAIN

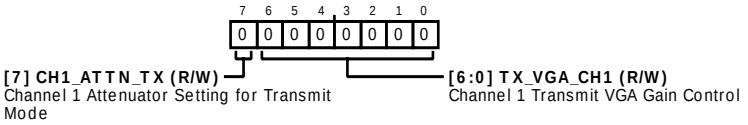


Table 47. Bit Descriptions for CH1_TX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH1_ATTN_TX		Channel 1 Attenuator Setting for Transmit Mode	0x0	R/W
[6:0]	TX_VGA_CH1		Channel 1 Transmit VGA Gain Control	0x0	R/W

Address: 0x01D, Reset: 0x00, Name: CH2_TX_GAIN

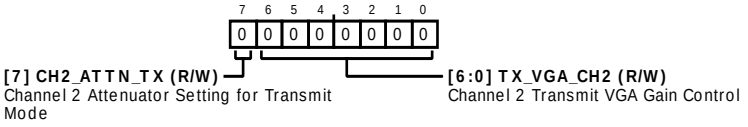


Table 48. Bit Descriptions for CH2_TX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH2_ATTN_TX		Channel 2 Attenuator Setting for Transmit Mode	0x0	R/W
[6:0]	TX_VGA_CH2		Channel 2 Transmit VGA Gain Control	0x0	R/W

Address: 0x01E, Reset: 0x00, Name: CH3_TX_GAIN

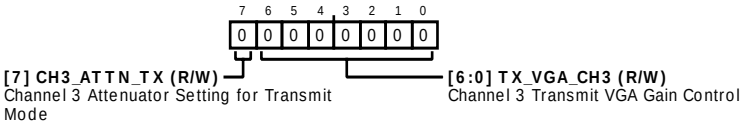


Table 49. Bit Descriptions for CH3_TX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH3_ATTN_TX		Channel 3 Attenuator Setting for Transmit Mode	0x0	R/W
[6:0]	TX_VGA_CH3		Channel 3 Transmit VGA Gain Control	0x0	R/W

Address: 0x01F, Reset: 0x00, Name: CH4_TX_GAIN

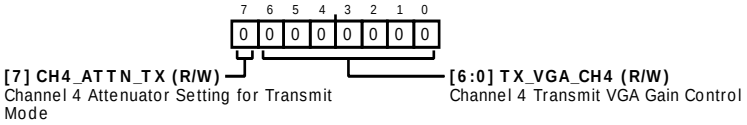


Table 50. Bit Descriptions for CH4_TX_GAIN

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	CH4_ATTN_TX		Channel 4 Attenuator Setting for Transmit Mode	0x0	R/W
[6:0]	TX_VGA_CH4		Channel 4 Transmit VGA Gain Control	0x0	R/W

Address: 0x020, Reset: 0x00, Name: CH1_TX_PHASE_I

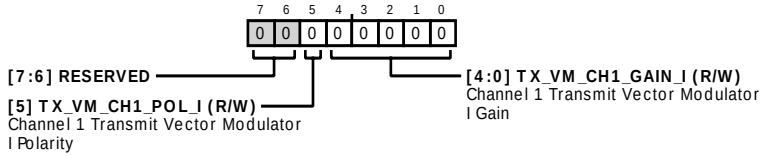


Table 51. Bit Descriptions for CH1_TX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH1_POL_I		Channel 1 Transmit Vector Modulator I Polarity	0x0	R/W
[4:0]	TX_VM_CH1_GAIN_I		Channel 1 Transmit Vector Modulator I Gain	0x0	R/W

Address: 0x021, Reset: 0x00, Name: CH1_TX_PHASE_Q

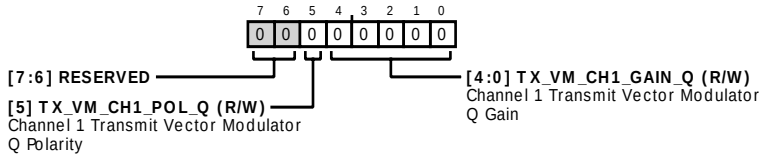


Table 52. Bit Descriptions for CH1_TX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH1_POL_Q		Channel 1 Transmit Vector Modulator Q Polarity	0x0	R/W
[4:0]	TX_VM_CH1_GAIN_Q		Channel 1 Transmit Vector Modulator Q Gain	0x0	R/W

Address: 0x022, Reset: 0x00, Name: CH2_TX_PHASE_I

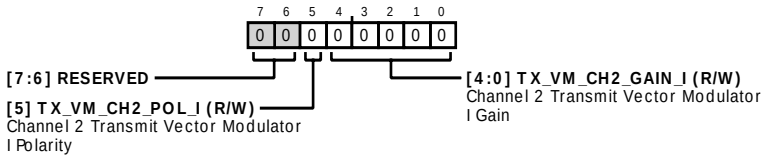


Table 53. Bit Descriptions for CH2_TX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH2_POL_I		Channel 2 Transmit Vector Modulator I Polarity	0x0	R/W
[4:0]	TX_VM_CH2_GAIN_I		Channel 2 Transmit Vector Modulator I Gain	0x0	R/W

Address: 0x023, Reset: 0x00, Name: CH2_TX_PHASE_Q

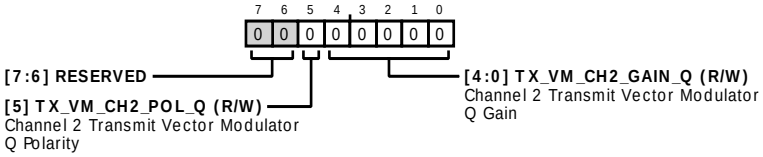


Table 54. Bit Descriptions for CH2_TX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH2_POL_Q		Channel 2 Transmit Vector Modulator Q Polarity	0x0	R/W
[4:0]	TX_VM_CH2_GAIN_Q		Channel 2 Transmit Vector Modulator Q Gain	0x0	R/W

Address: 0x024, Reset: 0x00, Name: CH3_TX_PHASE_I

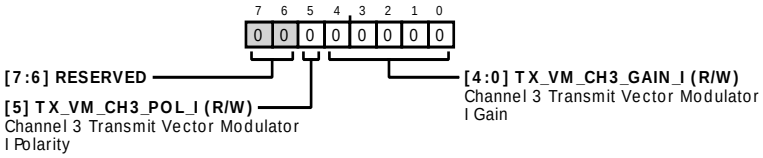


Table 55. Bit Descriptions for CH3_TX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH3_POL_I		Channel 3 Transmit Vector Modulator I Polarity	0x0	R/W
[4:0]	TX_VM_CH3_GAIN_I		Channel 3 Transmit Vector Modulator I Gain	0x0	R/W

Address: 0x025, Reset: 0x00, Name: CH3_TX_PHASE_Q

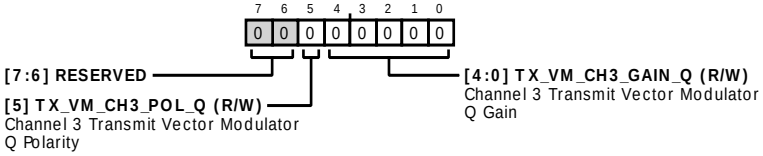


Table 56. Bit Descriptions for CH3_TX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH3_POL_Q		Channel 3 Transmit Vector Modulator Q Polarity	0x0	R/W
[4:0]	TX_VM_CH3_GAIN_Q		Channel 3 Transmit Vector Modulator Q Gain	0x0	R/W

Address: 0x026, Reset: 0x00, Name: CH4_TX_PHASE_I

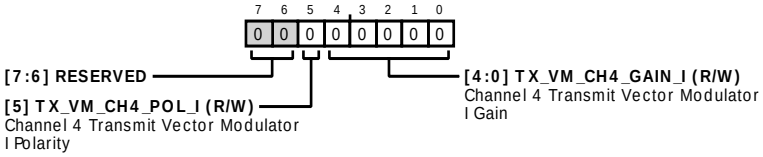


Table 57. Bit Descriptions for CH4_TX_PHASE_I

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH4_POL_I		Channel 4 Transmit Vector Modulator I Polarity	0x0	R/W
[4:0]	TX_VM_CH4_GAIN_I		Channel 4 Transmit Vector Modulator I Gain	0x0	R/W

Address: 0x027, Reset: 0x00, Name: CH4_TX_PHASE_Q

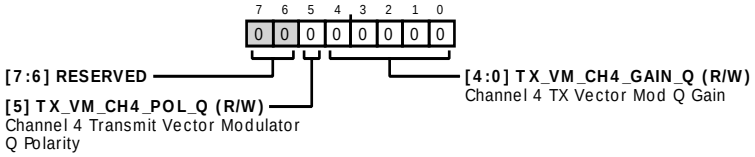


Table 58. Bit Descriptions for CH4_TX_PHASE_Q

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved	0x0	R
5	TX_VM_CH4_POL_Q		Channel 4 Transmit Vector Modulator Q Polarity	0x0	R/W
[4:0]	TX_VM_CH4_GAIN_Q		Channel 4 Transmit Vector Modulator Q Gain	0x0	R/W

Address: 0x028, Reset: 0x00, Name: LD_WRK_REGS

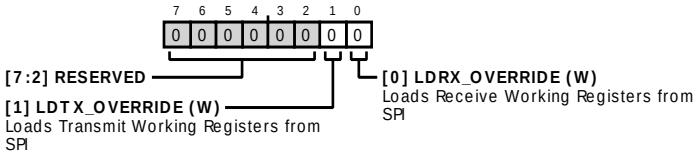


Table 59. Bit Descriptions for LD_WRK_REGS

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved	0x0	R
1	LDTX_OVERRIDE		Loads Transmit Working Registers from SPI	0x0	W
0	LDRX_OVERRIDE		Loads Receive Working Registers from SPI	0x0	W

Address: 0x029, Reset: 0x00, Name: CH1_PA_BIAS_ON

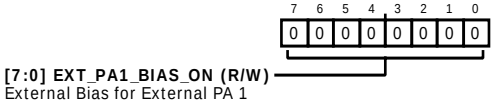


Table 60. Bit Descriptions for CH1_PA_BIAS_ON

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA1_BIAS_ON		External Bias for External PA 1	0x0	R/W

Address: 0x02A, Reset: 0x00, Name: CH2_PA_BIAS_ON

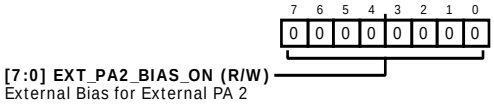


Table 61. Bit Descriptions for CH2_PA_BIAS_ON

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA2_BIAS_ON		External Bias for External PA 2	0x0	R/W

Address: 0x02B, Reset: 0x00, Name: CH3_PA_BIAS_ON

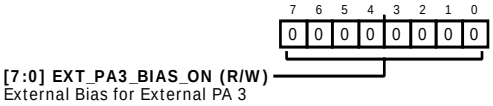


Table 62. Bit Descriptions for CH3_PA_BIAS_ON

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA3_BIAS_ON		External Bias for External PA 3	0x0	R/W

Address: 0x02C, Reset: 0x00, Name: CH4_PA_BIAS_ON

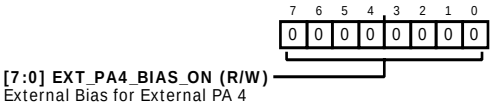


Table 63. Bit Descriptions for CH4_PA_BIAS_ON

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA4_BIAS_ON		External Bias for External PA 4	0x0	R/W

Address: 0x02D, Reset: 0x00, Name: LNA_BIAS_ON

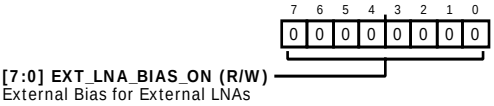


Table 64. Bit Descriptions for LNA_BIAS_ON

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_LNA_BIAS_ON		External Bias for External LNAs	0x0	R/W

Address: 0x02E, Reset: 0x00, Name: RX_ENABLES

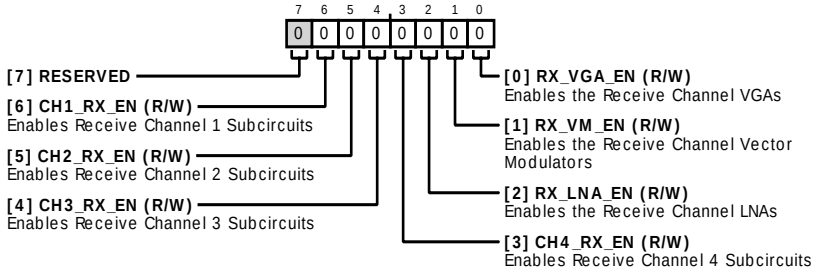


Table 65. Bit Descriptions for RX_ENABLES

Bit	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
6	CH1_RX_EN		Enables Receive Channel 1 Subcircuits	0x0	R/W
5	CH2_RX_EN		Enables Receive Channel 2 Subcircuits	0x0	R/W
4	CH3_RX_EN		Enables Receive Channel 3 Subcircuits	0x0	R/W
3	CH4_RX_EN		Enables Receive Channel 4 Subcircuits	0x0	R/W
2	RX_LNA_EN		Enables the Receive Channel LNAs	0x0	R/W
1	RX_VM_EN		Enables the Receive Channel Vector Modulators	0x0	R/W
0	RX_VGA_EN		Enables the Receive Channel VGAs	0x0	R/W

Address: 0x02F, Reset: 0x00, Name: TX_ENABLES

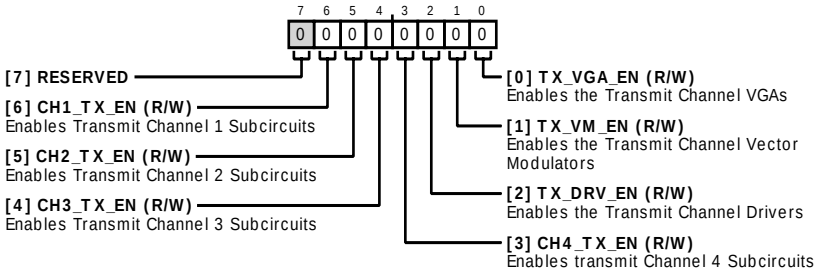


Table 66. Bit Descriptions for TX_ENABLES

Bit	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
6	CH1_TX_EN		Enables Transmit Channel 1 Subcircuits	0x0	R/W
5	CH2_TX_EN		Enables Transmit Channel 2 Subcircuits	0x0	R/W
4	CH3_TX_EN		Enables Transmit Channel 3 Subcircuits	0x0	R/W
3	CH4_TX_EN		Enables Transmit Channel 4 Subcircuits	0x0	R/W
2	TX_DRV_EN		Enables the Transmit Channel Drivers	0x0	R/W
1	TX_VM_EN		Enables the Transmit Channel Vector Modulators	0x0	R/W
0	TX_VGA_EN		Enables the Transmit Channel VGAs	0x0	R/W

Address: 0x030, Reset: 0x00, Name: MISC_ENABLES

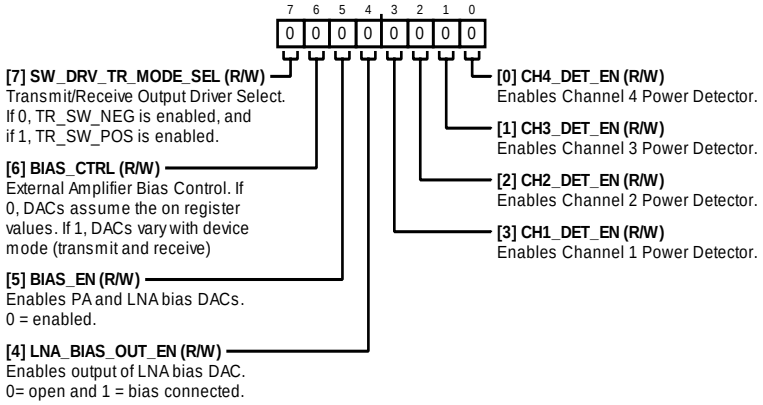


Table 67. Bit Descriptions for MISC_ENABLES

Bit	Bit Name	Settings	Description	Reset	Access
7	SW_DRV_TR_MODE_SEL		Transmit/Receive Output Driver Select. If 0, TR_SW_NEG is enabled, and if 1, TR_SW_POS is enabled.	0x0	R/W
6	BIAS_CTRL		External Amplifier Bias Control. If 0, DACs assume the on register values. If 1, DACs vary with device mode (transmit and receive).	0x0	R/W
5	BIAS_EN		Enables PA and LNA Bias DACs. 0 = enabled.	0x0	R/W
4	LNA_BIAS_OUT_EN		Enables Output of LNA Bias DAC. 0 = open and 1 = bias connected.	0x0	R/W
3	CH1_DET_EN		Enables Channel 1 Power Detector.	0x0	R/W
2	CH2_DET_EN		Enables Channel 2 Power Detector.	0x0	R/W
1	CH3_DET_EN		Enables Channel 3 Power Detector.	0x0	R/W
0	CH4_DET_EN		Enables Channel 4 Power Detector.	0x0	R/W

Address: 0x031, Reset: 0x00, Name: SW_CTRL

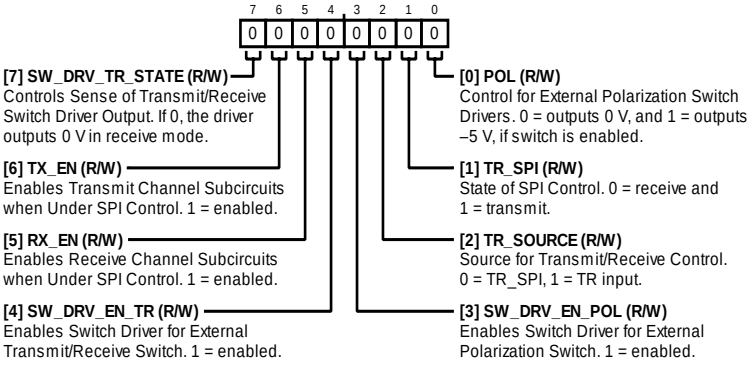


Table 68. Bit Descriptions for SW_CTRL

Bit	Bit Name	Settings	Description	Reset	Access
7	SW_DRV_TR_STATE		Controls Sense of Transmit/Receive Switch Driver Output. If 0, the driver outputs 0 V in receive mode.	0x0	R/W
6	TX_EN		Enables Transmit Channel Subcircuits when Under SPI Control. 1 = enabled.	0x0	R/W
5	RX_EN		Enables Receive Channel Subcircuits when Under SPI Control. 1 = enabled.	0x0	R/W
4	SW_DRV_EN_TR		Enables Switch Driver for External Transmit/Receive Switch. 1 = enabled.	0x0	R/W
3	SW_DRV_EN_POL		Enables Switch Driver for External Polarization Switch. 1 = enabled.	0x0	R/W
2	TR_SOURCE		Source for Transmit/Receive Control. 0 = TR_SPI, 1 = TR input.	0x0	R/W
1	TR_SPI		State of SPI Control. 0 = receive and 1 = transmit.	0x0	R/W
0	POL		Control for External Polarity Switch Drivers. 0 = outputs 0 V, and 1 = outputs −5 V, if switch is enabled.	0x0	R/W

Address: 0x032, Reset: 0x00, Name: ADC_CTRL

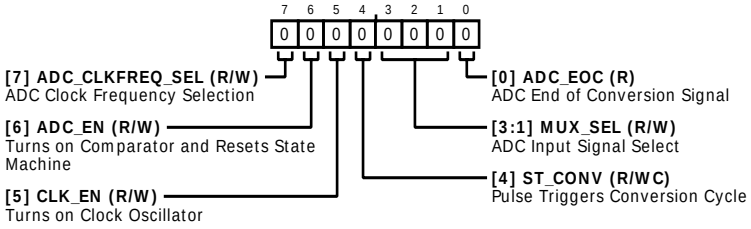


Table 69. Bit Descriptions for ADC_CTRL

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	ADC_CLKFREQ_SEL		ADC Clock Frequency Selection	0x0	R/W
6	ADC_EN		Turns on Comparator and Resets State Machine	0x0	R/W
5	CLK_EN		Turns on Clock Oscillator	0x0	R/W
4	ST_CONV		Pulse Triggers Conversion Cycle	0x0	R/WC
[3:1]	MUX_SEL		ADC Input Signal Select	0x0	R/W
0	ADC_EOC		ADC End of Conversion Signal	0x0	R

Address: 0x033, Reset: 0x00, Name: ADC_OUTPUT

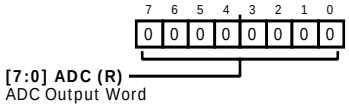


Table 70. Bit Descriptions for ADC_OUTPUT

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	ADC		ADC Output Word	0x0	R

Address: 0x034, Reset: 0x00, Name: BIAS_CURRENT_RX_LNA

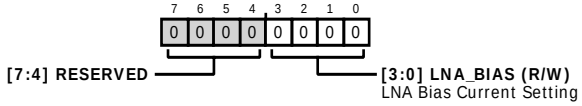


Table 71. Bit Descriptions for BIAS_CURRENT_RX_LNA

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
[3:0]	LNA_BIAS		LNA Bias Current Setting	0x0	R/W

Address: 0x035, Reset: 0x00, Name: BIAS_CURRENT_RX

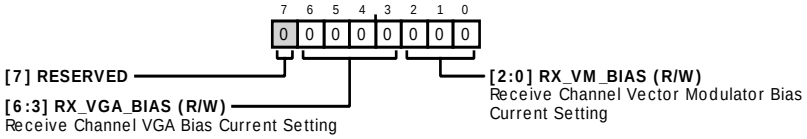


Table 72. Bit Descriptions for BIAS_CURRENT_RX

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
[6:3]	RX_VGA_BIAS		Receive Channel VGA Bias Current Setting	0x0	R/W
[2:0]	RX_VM_BIAS		Receive Channel Vector Modulator Bias Current Setting	0x0	R/W

Address: 0x036, Reset: 0x00, Name: BIAS_CURRENT_TX

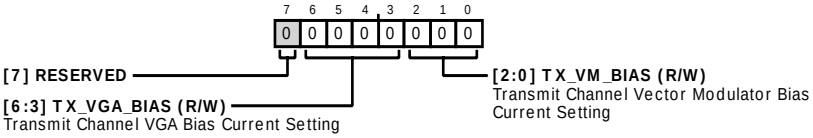


Table 73. Bit Descriptions for BIAS_CURRENT_TX

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Reserved	0x0	R
[6:3]	TX_VGA_BIAS		Transmit Channel VGA Bias Current Setting	0x0	R/W
[2:0]	TX_VM_BIAS		Transmit Channel Vector Modulator Bias Current Setting	0x0	R/W

Address: 0x037, Reset: 0x00, Name: BIAS_CURRENT_TX_DRV

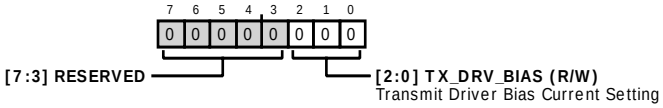


Table 74. Bit Descriptions for BIAS_CURRENT_TX_DRV

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:3]	RESERVED		Reserved	0x0	R
[2:0]	TX_DRV_BIAS		Transmit Driver Bias Current Setting	0x0	R/W

Address: 0x038, Reset: 0x00, Name: MEM_CTRL

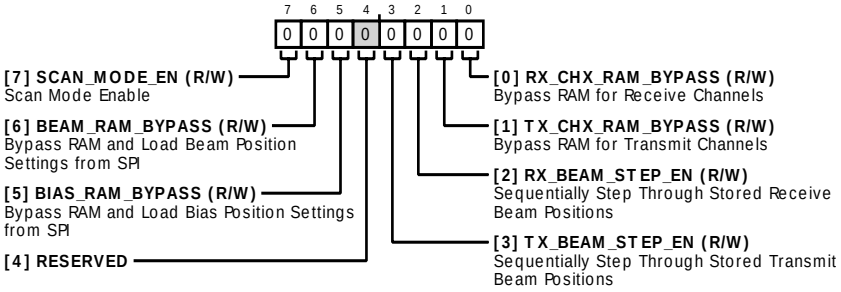


Table 75. Bit Descriptions for MEM_CTRL

Bit	Bit Name	Settings	Description	Reset	Access
7	SCAN_MODE_EN		Scan Mode Enable	0x0	R/W
6	BEAM_RAM_BYPASS		Bypass RAM and Load Beam Position Settings from SPI	0x0	R/W
5	BIAS_RAM_BYPASS		Bypass RAM and Load Bias Position Settings from SPI	0x0	R/W
4	RESERVED		Reserved	0x0	R
3	TX_BEAM_STEP_EN		Sequentially Step Through Stored Transmit Beam Positions	0x0	R/W
2	RX_BEAM_STEP_EN		Sequentially Step Through Stored Receive Beam Positions	0x0	R/W
1	TX_CHX_RAM_BYPASS		Bypass RAM for Transmit Channels	0x0	R/W
0	RX_CHX_RAM_BYPASS		Bypass RAM for Receive Channels	0x0	R/W

Address: 0x039, Reset: 0x00, Name: RX_CHX_MEM

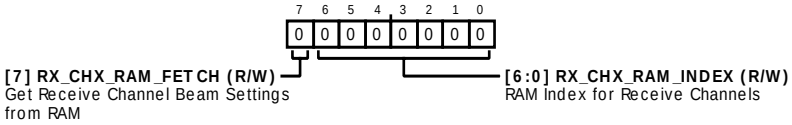


Table 76. Bit Descriptions for RX_CHX_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RX_CHX_RAM_FETCH		Get Receive Channel Beam Settings from RAM	0x0	R/W
[6:0]	RX_CHX_RAM_INDEX		RAM Index for Receive Channels	0x0	R/W

Address: 0x03A, Reset: 0x00, Name: TX_CHX_MEM

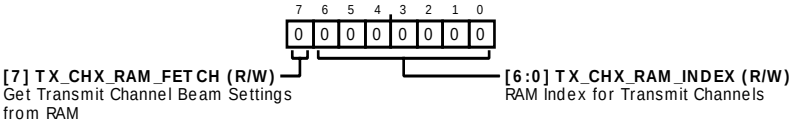


Table 77. Bit Descriptions for TX_CHX_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	TX_CHX_RAM_FETCH		Get Transmit Channel Beam Settings from RAM	0x0	R/W
[6:0]	TX_CHX_RAM_INDEX		RAM Index for Transmit Channels	0x0	R/W

Address: 0x03D, Reset: 0x00, Name: RX_CH1_MEM

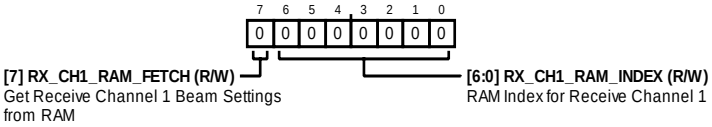


Table 78. Bit Descriptions for RX_CH1_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RX_CH1_RAM_FETCH		Get Receive Channel 1 Beam Settings from RAM	0x0	R/W
[6:0]	RX_CH1_RAM_INDEX		RAM Index for Receive Channel 1	0x0	R/W

Address: 0x03E, Reset: 0x00, Name: RX_CH2_MEM

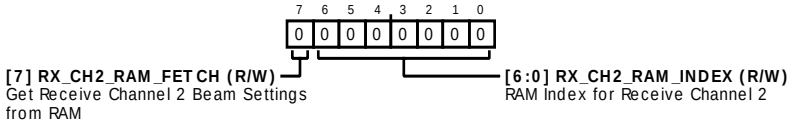


Table 79. Bit Descriptions for RX_CH2_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RX_CH2_RAM_FETCH		Get Receive Channel 2 Beam Settings from RAM	0x0	R/W
[6:0]	RX_CH2_RAM_INDEX		RAM Index for Receive Channel 2	0x0	R/W

Address: 0x03F, Reset: 0x00, Name: RX_CH3_MEM

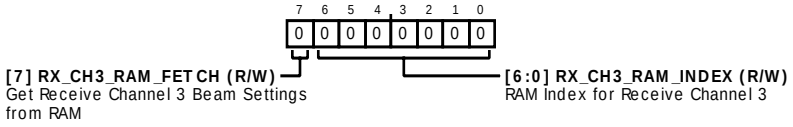


Table 80. Bit Descriptions for RX_CH3_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RX_CH3_RAM_FETCH		Get Receive Channel 3 Beam Settings from RAM	0x0	R/W
[6:0]	RX_CH3_RAM_INDEX		RAM Index for Receive Channel 3	0x0	R/W

Address: 0x040, Reset: 0x00, Name: RX_CH4_MEM

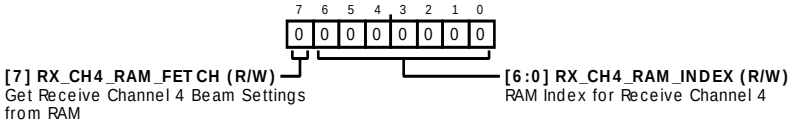


Table 81. Bit Descriptions for RX_CH4_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	RX_CH4_RAM_FETCH		Get Receive Channel 4 Beam Settings from RAM	0x0	R/W
[6:0]	RX_CH4_RAM_INDEX		RAM Index for Receive Channel 4	0x0	R/W

Address: 0x041, Reset: 0x00, Name: TX_CH1_MEM

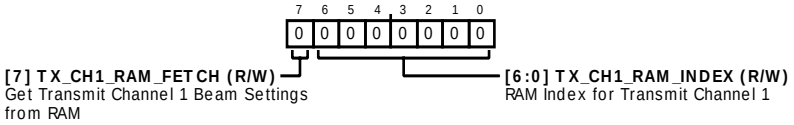


Table 82. Bit Descriptions for TX_CH1_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	TX_CH1_RAM_FETCH		Get Transmit Channel 1 Beam Settings from RAM	0x0	R/W
[6:0]	TX_CH1_RAM_INDEX		RAM Index for Transmit Channel 1	0x0	R/W

Address: 0x042, Reset: 0x00, Name: TX_CH2_MEM

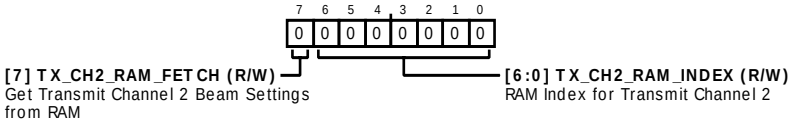


Table 83. Bit Descriptions for TX_CH2_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	TX_CH2_RAM_FETCH		Get Transmit Channel 2 Beam Settings from RAM	0x0	R/W
[6:0]	TX_CH2_RAM_INDEX		RAM Index for Transmit Channel 2	0x0	R/W

Address: 0x043, Reset: 0x00, Name: TX_CH3_MEM

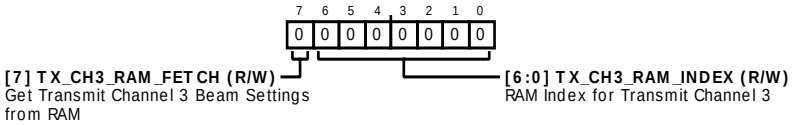


Table 84. Bit Descriptions for TX_CH3_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	TX_CH3_RAM_FETCH		Get Transmit Channel 3 Beam Settings from RAM	0x0	R/W
[6:0]	TX_CH3_RAM_INDEX		RAM Index for Transmit Channel 3	0x0	R/W

Address: 0x044, Reset: 0x00, Name: TX_CH4_MEM

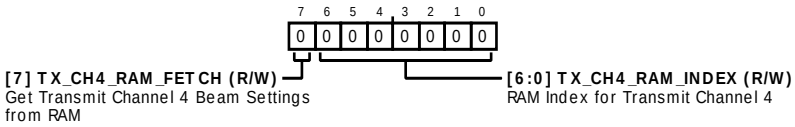


Table 85. Bit Descriptions for TX_CH4_MEM

Bit(s)	Bit Name	Settings	Description	Reset	Access
7	TX_CH4_RAM_FETCH		Get Transmit Channel 4 Beam Settings from RAM	0x0	R/W
[6:0]	TX_CH4_RAM_INDEX		RAM Index for Transmit Channel 4	0x0	R/W

Address: 0x045, Reset: 0x00, Name: REV_ID

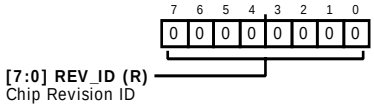


Table 86. Bit Descriptions for REV_ID

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	REV_ID		Chip Revision ID	0x0	R

Address: 0x046, Reset: 0x00, Name: CH1_PA_BIAS_OFF

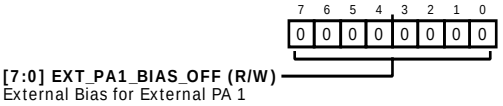


Table 87. Bit Descriptions for CH1_PA_BIAS_OFF

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA1_BIAS_OFF		External Bias for External PA 1	0x0	R/W

Address: 0x047, Reset: 0x00, Name: CH2_PA_BIAS_OFF

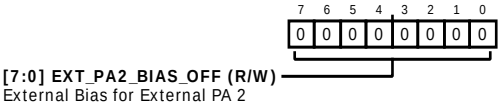


Table 88. Bit Descriptions for CH2_PA_BIAS_OFF

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA2_BIAS_OFF		External Bias for External PA 2	0x0	R/W

Address: 0x048, Reset: 0x00, Name: CH3_PA_BIAS_OFF

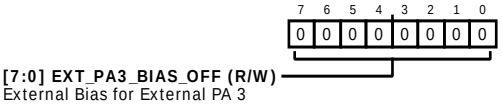


Table 89. Bit Descriptions for CH3_PA_BIAS_OFF

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA3_BIAS_OFF		External Bias for External PA 3	0x0	R/W

Address: 0x049, Reset: 0x00, Name: CH4_PA_BIAS_OFF

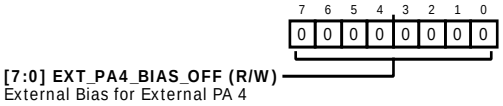


Table 90. Bit Descriptions for CH4_PA_BIAS_OFF

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_PA4_BIAS_OFF		External Bias for External PA 4	0x0	R/W

Address: 0x04A, Reset: 0x00, Name: LNA_BIAS_OFF

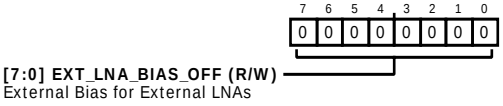


Table 91. Bit Descriptions for LNA_BIAS_OFF

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	EXT_LNA_BIAS_OFF		External Bias for External LNAs	0x0	R/W

Address: 0x04B, Reset: 0x00, Name: TX_TO_RX_DELAY_CTRL

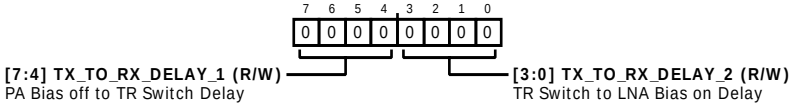


Table 92. Bit Descriptions for TX_TO_RX_DELAY_CTRL

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	TX_TO_RX_DELAY_1		PA Bias off to TR Switch Delay	0x0	R/W
[3:0]	TX_TO_RX_DELAY_2		TR Switch to LNA Bias on Delay	0x0	R/W

Address: 0x04C, Reset: 0x00, Name: RX_TO_TX_DELAY_CTRL

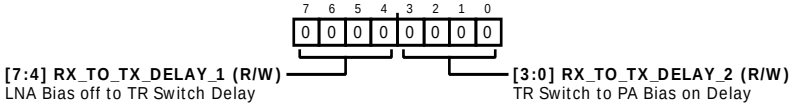


Table 93. Bit Descriptions for RX_TO_TX_DELAY_CTRL

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	RX_TO_TX_DELAY_1		LNA Bias off to TR Switch Delay	0x0	R/W
[3:0]	RX_TO_TX_DELAY_2		TR Switch to PA Bias on Delay	0x0	R/W

Address: 0x04D, Reset: 0x00, Name: TX_BEAM_STEP_START

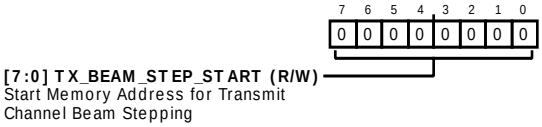


Table 94. Bit Descriptions for TX_BEAM_STEP_START

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	TX_BEAM_STEP_START		Start Memory Address for Transmit Channel Beam Stepping	0x0	R/W

Address: 0x04E, Reset: 0x00, Name: TX_BEAM_STEP_STOP

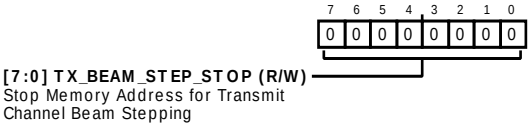


Table 95. Bit Descriptions for TX_BEAM_STEP_STOP

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	TX_BEAM_STEP_STOP		Stop Memory Address for Transmit Channel Beam Stepping	0x0	R/W

Address: 0x04F, Reset: 0x00, Name: RX_BEAM_STEP_START

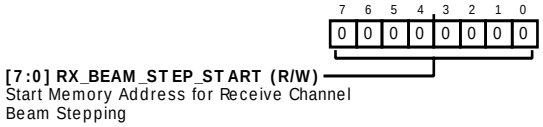


Table 96. Bit Descriptions for RX_BEAM_STEP_START

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	RX_BEAM_STEP_START		Start Memory Address for Receive Channel Beam Stepping	0x0	R/W

Address: 0x050, Reset: 0x00, Name: RX_BEAM_STEP_STOP

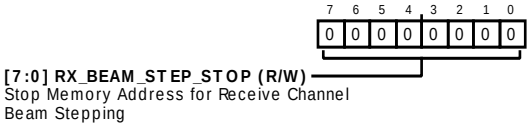


Table 97. Bit Descriptions for RX_BEAM_STEP_STOP

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:0]	RX_BEAM_STEP_STOP		Stop Memory Address for Receive Channel Beam Stepping	0x0	R/W

Address: 0x051, Reset: 0x00, Name: RX_BIAS_RAM_CTL

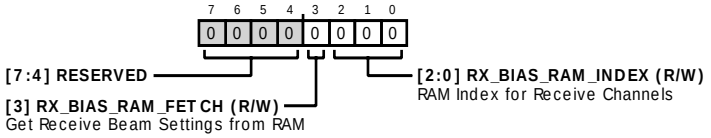


Table 98. Bit Descriptions for RX_BIAS_RAM_CTL

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
3	RX_BIAS_RAM_FETCH		Get Receive Beam Settings from RAM	0x0	R/W
[2:0]	RX_BIAS_RAM_INDEX		RAM Index for Receive Channels	0x0	R/W

Address: 0x052, Reset: 0x00, Name: TX_BIAS_RAM_CTL

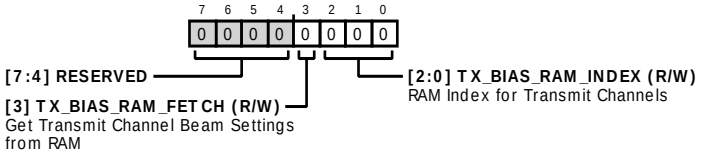


Table 99. Bit Descriptions for TX_BIAS_RAM_CTL

Bit(s)	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	R
3	TX_BIAS_RAM_FETCH		Get Transmit Channel Beam Settings from RAM	0x0	R/W
[2:0]	TX_BIAS_RAM_INDEX		RAM Index for Transmit Channels	0x0	R/W

Address: 0x400, Reset: 0x00, Name: LDO_TRIM_CTL_0

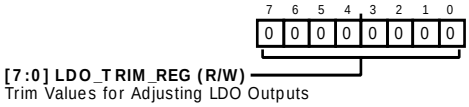


Table 100. Bit Descriptions for LDO_TRIM_CTL_0

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	LDO_TRIM_REG		Trim Values for Adjusting LDO Outputs	0x0	R/W

Address: 0x401, Reset: 0x00, Name: LDO_TRIM_CTL_1

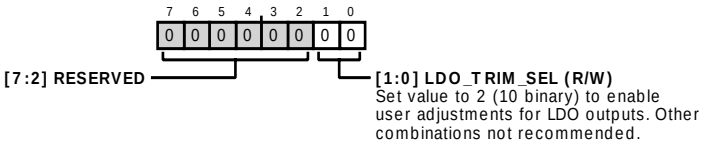


Table 101. Bit Descriptions for LDO_TRIM_CTL_1

Bits	Bit Name	Settings	Description	Reset	Access
[7:2]	RESERVED		Reserved.	0x0	R
[1:0]	LDO_TRIM_SEL		Set value to 2 (10 binary) to enable user adjustments for LDO outputs. Other combinations not recommended.	0x0	R/W

OUTLINE DIMENSIONS

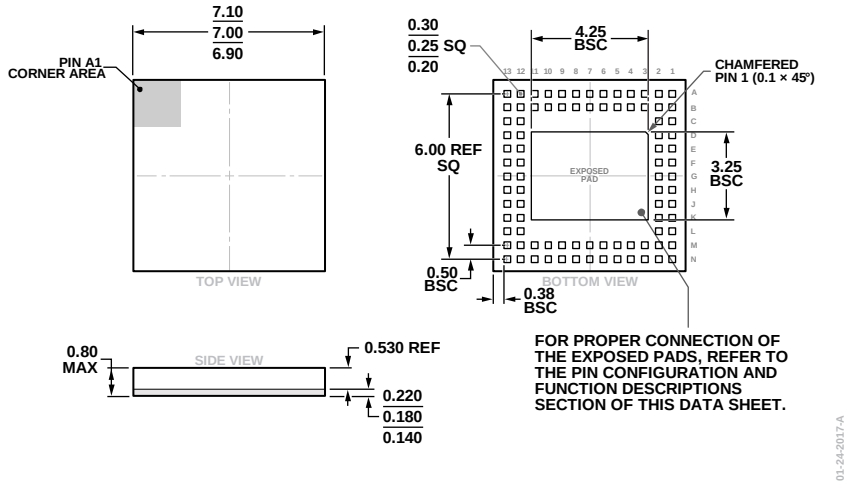


Figure 98. 88-Terminal Land Grid Array [LGA]
(CC-88-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADAR1000ACCZN	−40°C to +85°C	88-Terminal Land Grid Array [LGA]	CC-88-1
ADAR1000ACCZN-R7	−40°C to +85°C	88-Terminal Land Grid Array [LGA], 7″ Reel	CC-88-1
ADAR1000-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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